MITSUBISHI ELECTRIC
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for a greener tomorrow

iQ Platform-compatible PAC
Flexible High-speed I/O Control Module

MELSEC iQ-R series

Brief

MELSEC iQ-R Series Broadcast

Ultrahigh-speed response asynchronous from the CPU and control bus

The MELSEC iQ-R Series is equipped with a customizable high-speed digital field programmable gate array (FPGA) I/O module. Features include the ability to program control logic and microsecond-fast asynchronous I/O response times to the programmable controller CPU and control bus, realizing stable machine performance minimizing processing speed fluctuation.

Enhanced I/O flexibility

The flexibility in I/O capabilities has been increased by providing 12 input points (5/24 V DC, and differential) for connecting sensors and encoders, and 14 output points (5...24 V DC: 8 outputs, and differential: 6 outputs). Wide-range of control functions including speed measurement, adjusted pulse output, ratio setting/distributed output, PWM control, and cam switch control are all possible using FPGA.

Improvements

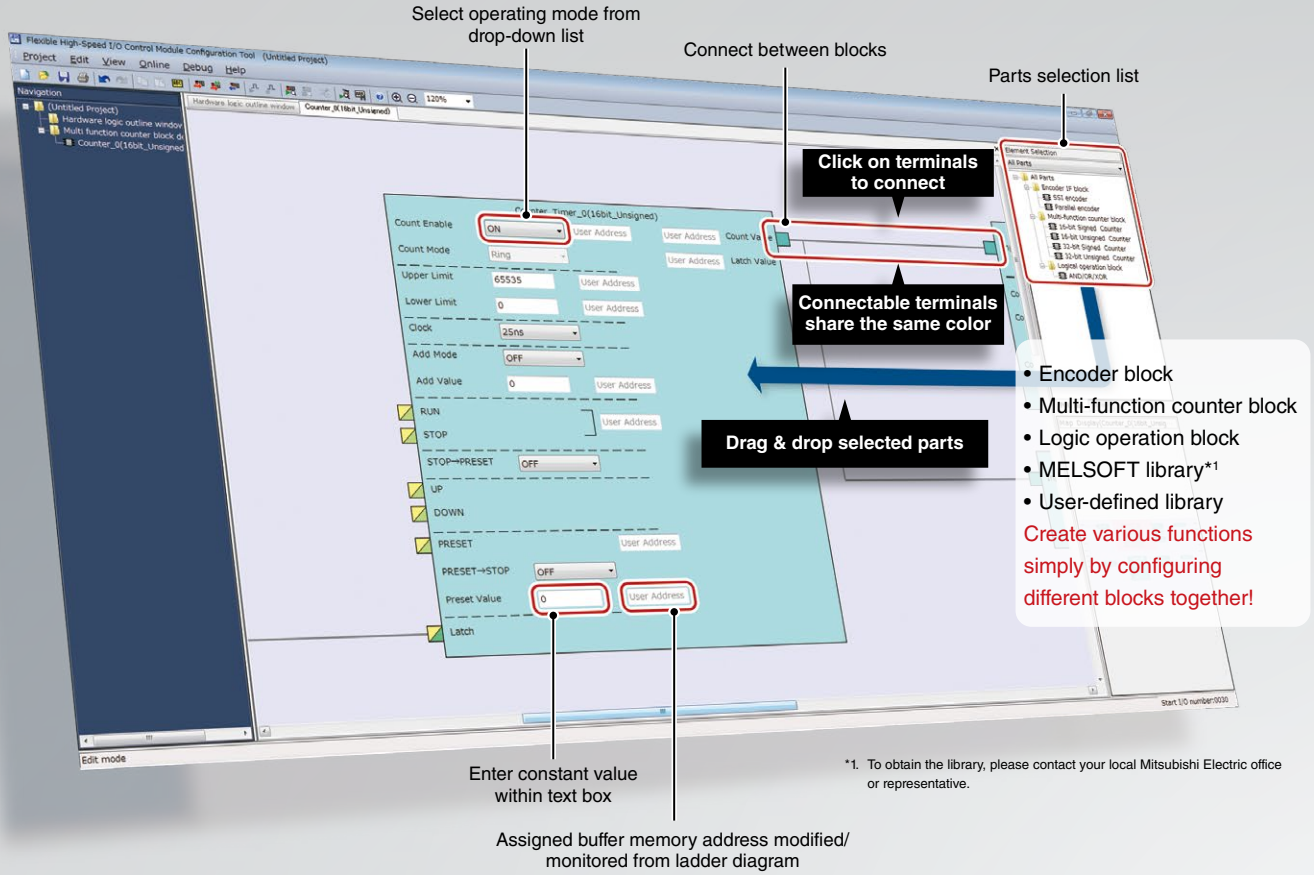
- Performance asynchronous to CPU realizing microsecond-level response times
- Lower development cost when creating complex applications
- Replacing a microcomputer/FPGA board

FPGA logic design enables more freedom in customization

Equipped with a FPGA, control logic can be programmed easily using GX Works3. This low-cost alternative to HDL programming, logic synthesis and timing analysis reduces the design process, which is a common feature of general FPGA logic design.

Hardware logic development cost minimized

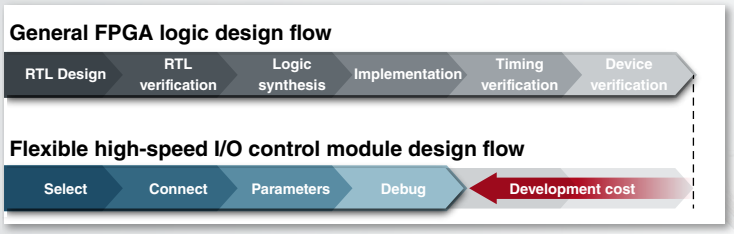
Used together with the dedicated configuration tool (integrated in GX Works3), the essential design processes associated with FPGA (HDL programming, logic synthesis and timing analysis) are no longer required, thereby reducing overall development cost.



*1. To obtain the library, please contact your local Mitsubishi Electric office or representative.

Graphic-based logic configuration

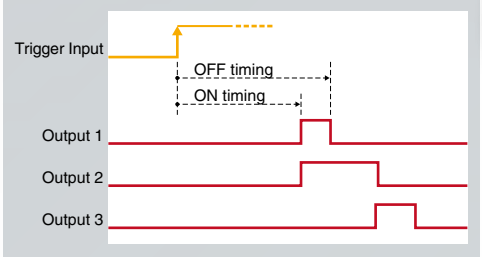
- Easy hardware logic design without the need for detailed knowledge of FPGA
- Intuitive configuration software
- Simple to verify logic as connection between various logic is immediately reflected

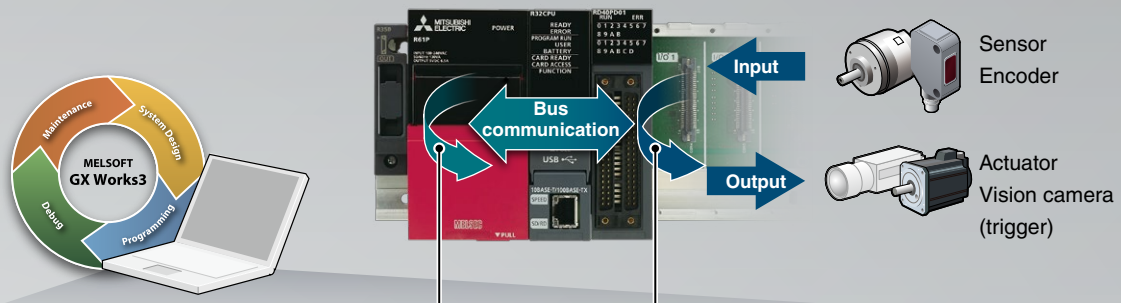


❶ High-speed, stable I/O response

The flexible high-speed I/O control module provides highly accurate control of I/O timing owing to the asynchronous execution of internal control logic to the CPU and control bus. Variation in processing time is reduced to nanoseconds, thereby enabling sensors such as proximity lasers to trigger vision cameras accurately, which is required in product testing equipment in order to capture products moving at high-speed.

- Trigger input timing is adjustable to a minimum of 25 ns resolution
- Variations in processing time can be reduced to nanoseconds, enabling highly accurate control





GX Works3
One Software, Many Possibilities

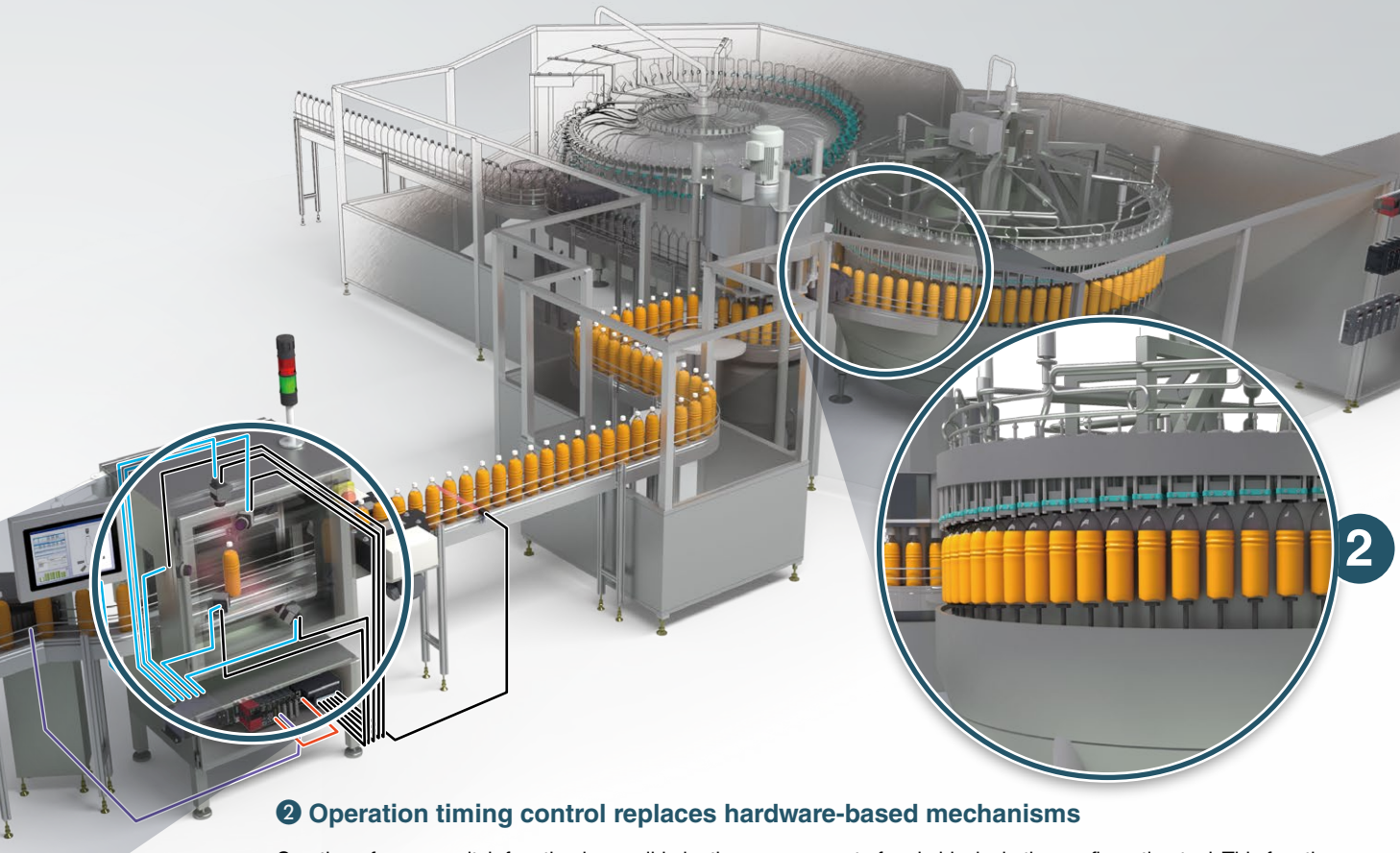
- Overall system control
- Module parameter registration
- Interrupt program management

RUN/STOP/Parameters

Status/Interrupt

Flexible high-speed I/O control module configuration software

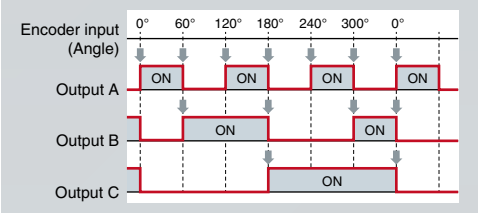
- Hardware logic-driven control
- Trigger interrupt programs in CPU
- Data communication with CPU buffer memory



❷ Operation timing control replaces hardware-based mechanisms

Creation of a cam switch function is possible by the arrangement of main blocks in the configuration tool. This function can operate as a low-maintenance, high-speed alternative to mechanical camshaft control, lowering asset cost as hardware and maintenance requirements are reduced. An encoder pulse can be used for high-precision timing, such as for filling applications that require valve timing on a rotating drum.

- High-precision timing control relative to each count of the encoder



Flexible High-speed I/O Control Module

- Further advanced inherited functions of I/O modules and high-speed counter module
- Extensive I/O and function combinations extend the application range
- I/O response times reduced to less than 1µs
- Hardware operation processing speed fluctuation reduced to nanoseconds
- Create hardware logic without FPGA knowledge
- Intuitive setting tool allows simple setting and connection of logic blocks
- Verify product operation from within the configuration tool

Specifications

Item	RD40PD01	
	DC	Differential
Number of input points (point)	12 (5/24 V DC/differential)	
Number of output points (point)	8 (5...24 V DC, 0.1 A/point)	6
Number of interrupts	8	
Input response time	≤ 1 µs	
Output response time	≤ 1 µs	
Max. pulse input speed (pulse/s)	200 k (200 kHz)	8 M (2 MHz)
Max. pulse output speed (pulse/s)	200 k (200 kHz)	8 M (2 MHz)
Main functions executable using main block combinations	Pulse count, coincidence detection, cam switch, highly-accurate pulse output, PWM output, ratio setting, pulse measurement, electrical interface conversion	
Main hardware logic processing time	Logic operation: Min. 87.5 ns, Coincidence output: Min. 137.5 ns, Cam switch: Min. 262.5 ns	
External interface		
40-pin connector	● (2x)	

Main blocks*1

Item		RD40PD01	
		DC	Differential
External input block			
Logic select		Inverted, not inverted	
Filter time (general input)		0 µs, 10 µs, 50 µs, 0.1 ms, 0.2 ms, 0.4 ms, 0.6 ms, 1 ms, 5 ms	
Filter time (pulse input) (pulse/s)		10 k, 100 k, 200 k, 500 k, 1 M, 2 M, 4 M, 8 M	
Parallel encoder block			
Input data type		Pure binary, gray code, BCD	
Data length		1 bit...12 bits	
SSI encoder block			
Input data type		Pure binary, gray code	
Data length		1 bit...32 bits	
Transmission speed		100 kHz, 200 kHz, 300 kHz, 400 kHz, 500 kHz, 1.0 MHz, 1.5 MHz, 2.0 MHz	
Multi function counter block			
Counter timer block	Type	Addition, subtraction, linear counter mode, ring counter mode, addition mode, preset counter function, latch counter function, internal clock function	
	Internal clock	25 ns, 50 ns, 0.1 µs, 1 µs, 10 µs, 100 µs, 1 ms	
	Counting range	32-bit signed binary (-2147483648...2147483647), 32-bit unsigned binary (0...4294967295) 16-bit signed binary (-32768...32767), 16-bit unsigned binary (0...65535)	
Compare block	Compare value	Same as the counting range	
	Compare mode	=, >, <, ≥, ≤, <>	
Cam switch block (steps)		16	
Set/Reset block		Uses signal input to Set terminal as a trigger to output High fixed signal Uses signal input to Reset terminal as a trigger to output Low fixed signal	
Logic operation block			
Logic operation type		AND, OR, XOR	
External output block			
Logic select		Inverted, not inverted	
Delay time*2		None,12.5 ns, 25 ns, 50 ns, 0.1 µs, 1 µs, 10 µs, 100 µs, 1 ms, inter-module synchronization	

*1. Included in the configuration tool.

*2. Can be set up to 64 multiples (not applicable when set to none or inter-module synchronization).

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⚠ For safe use

• To use the products listed in this publication properly, always read the relevant manuals before use.

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