MITSUBISHI

Ladder Logic Test Function software for Windows

SW3D5C-LLT-E(V)
SW3D5F-LLT-E(V)

Operating Manual

MELSEC

Mitsubishi Programmable Logic Controller

• SAFETY PRECAUTIONS •

(Read these precautions before using.)

When using Mitsubishi equipment, thoroughly read this manual and the associated manuals introduced in this manual. Also pay careful attention to safety and handle the module properly.
These precautions apply only to Mitsubishi equipment. Refer to the CPU module user's manual for a description of the PLC system safety precautions.
These • SAFETY PRECAUTIONS • classify the safety precautions into two categories: "DANGER" and "CAUTION".

⚠ DANGER	Procedures which may lead to a dangerous condition and cause death or serious injury if not carried out properly.
⚠ CAUTION	Procedures which may lead to a dangerous condition and cause superficial to medium injury, or physical damage only, if not carriedout properly.

Depending on circumstances, procedures indicated by ⚠CAUTION may also be linked to serious results.
In any case, it is important to follow the directions for usage.

[Cautions Regarding Test Operation]

⚠ DANGER

- The ladder logic test tool (LLT) simulate an actual PLC to debug sequence programs. However, the execution of a debugged sequence program cannot be guaranteed.
  After debugging using the ladder logic test tool (LLT), connect an actual PLC and debug the sequence program normally before starting actual operation.
  Failure to correctly debug a sequence program may result in accidents due to incorrect outputs of operations.
- The simulated result may differ from actual operation because the ladder logic test tool (LLT) cannot access I/O units or special function units and do not support some instructions or device memory.
  After debugging using the ladder logic test tool (LLT), connect an actual PLC and debug the sequence program normally before starting actual operation.
  Failure to correctly debug a sequence program may result in accidents due to incorrect outputs of operations.

REVISIONS

* The manual number is given on the bottom left of the back cover.

Print Date	* Manual Number	Revision
Apr., 1999	IB-0800001-A	First edition

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INTRODUCTION

Thank you for purchasing the Mitsubishi general-purpose MELSEC series sequencer.
Read this manual and make sure you understand the functions and performance of MELSEC series sequencer thoroughly in advance to ensure correct use.

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About Manuals

The following manuals are also related to this product.
In necessary, order them by quoting the details in the tables below.

Related Manuals

Manual Name	Manual Number (Model Code)
GPP Function software for Windows SW3D5C-GPPW-E SW3D5F-GPPW-E SW3D5C-LLT-E SW3D5F-LLT-E Operating Manual (Start up) Describes the system configuration, installation procedure, and start-up procedure of the SW3D5□-GPPW-E and SW3D5□-LLT-E software packages. (Packed with the product)	IB-0800000-A (13J950)
GPP Function software for Windows SW3D5C-GPPW-E SW3D5F-GPPW-E Operating Manual Describes the online functions of SW3D5□-GPPW-E including the programming procedure, printing out procedure, monitoring procedure, and debugging procedure. (Packed with the product)	IB-0800002-A (13J951)

About the Generic Terms and Abbreviations

Unless otherwise specified, the table below defines the abbreviations and terminology of the ladder logic test tool software package of model SW3D5C-LLT-E/SW3D5F-LLT-E used in this manual.

Generic Term/Abbreviation	Description
Ladder logic test tool (LLT)	Abbreviation for "SW3D5C-LLT-E/SW3D5F-LLT-E ladder logic test tool functions software package"
GPPW	Abbreviation for "SW□D5C-GPPW-E/SW□D5F-GPPW-E GPP function software package"
Windows 95	Abbreviation for "Microsoft Window 95 (English version)"
Windows 98	Abbreviation for "Microsoft Window 98 (English version)"
Windows NT 4.0	Abbreviation for "Microsoft Windows NT Workstation 4.0 (English version)"
Debug	Locating and correcting errors in a sequence program to create a correct program.
Device memory	Areas to store device data in the ladder logic test tool (LLT), including inputs (X), outputs (Y), relays (M), timers (T), data registers (D), etc.
Monitor	Monitoring to determine the ON/OFF status of bit devices or the PV of word devices.
Simulations	Test execution of a program on a personal computer with the ladder logic test tool (LLT) installed, instead of execution in an actual PLC.
Timing chart	Functions to visually confirm ON/OFF status of a bit device or the change in value of a word device.
WDT error	An error issued when a sequence program is written in such a way that it runs an infinite loop.
A Series CPU	A0J2H, A1FX, A1S, A1SJ, A1SH, A1SJH, A1N, A2C, A2CJ, A2N (S1), A2S, A2SH, A3N, A2A (S1), A3A, A2U (S1), A2US (S1), A2USH-S1, A3U, A4U, CPU board (A80BD-A2USH-S1)
QnA Series CPU	Q2A, Q2AS (H), Q2AS1, Q2AS (H) S1, Q3A, Q4A, Q4AR
FX series CPU	FX0 (S), FX0N, FX1N, FX2 (C), FX2N (C)
Motion controller CPU	A171SH, A172SH, A273UH (S3)

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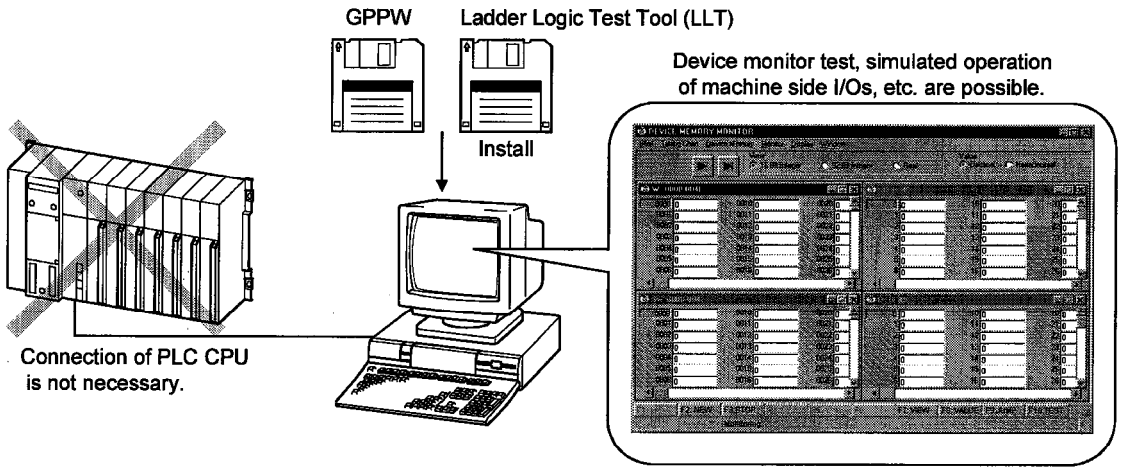
1. OUTLINE OF LADDER LOGIC TEST TOOL (LLT)

This operating manual describes the functions and operation of the SW3D5C-LLT-E/SW3D5F -LLT-E ladder logic test tool functions software package.

The SW3D5C-LLT-E/SW3D5F-LLT-E ladder logic test tool functions software package (hereafter "ladder logic test tool (LLT)") is a software package which runs under Windows95/98/NT4.0.
Offline debugging is possible by adding the ladder logic test tool (LLT) to a computer in which the SW□D5C-GPPW-E/SW□D5F-GPPW-E GPP function software package (hereafter "GPPW") is installed. The offline debugging functions include the device monitor test and simulated operation of external device I/Os.
As the ladder logic test tool (LLT) allow sequence programs to be developed and debugged on a single computer, checking a modified program is quick and easy.
GPPW must be installed before these functions can be used.



A sequence program created with GPPW can be debugged by writing it to the ladder logic test tool (LLT).
The sequence program is automatically written to the ladder logic test tool (LLT) when the ladder logic test tool (LLT) are started up.
See the following manuals for information on operations not covered in this manual:

- GPP Function software for Windows
  SW3D5C-GPPW-E SW3D5F-GPPW-E
  SW3D5C-LLT-E SW3D5F-LLT-E
  Operating Manual (Start-up).....IB-0800000-A
- GPP Function software for Windows
  SW3D5C-GPPW-E SW3D5F-GPPW-E
  Operating Manual.....IB-0800002-A

1.1 Features of the Ladder Logic Test Tool (LLT)

The features of the ladder logic test tool (LLT) are described below.

(1) Program Debugging Tool

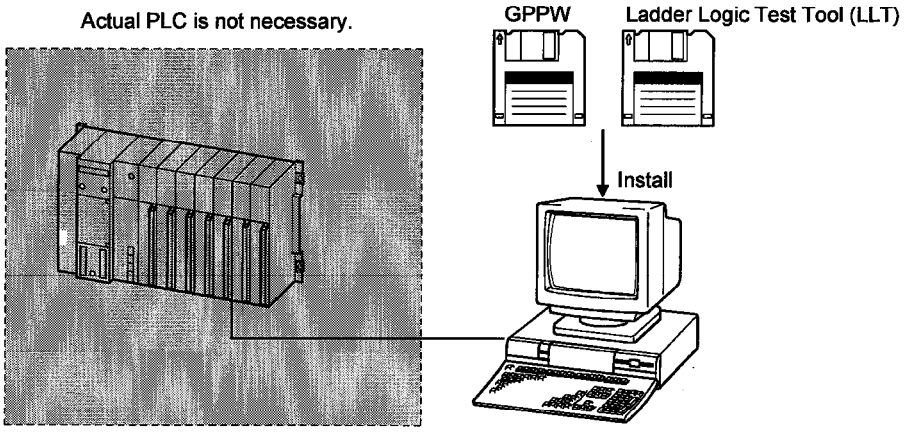
(a) No actual PLC Required

The program runs in the personal computer when the ladder logic test tool (LLT) are used, allowing program operation to be checked if no actual PLC is available.

Therefore, debugging is possible wherever a personal computer is available.

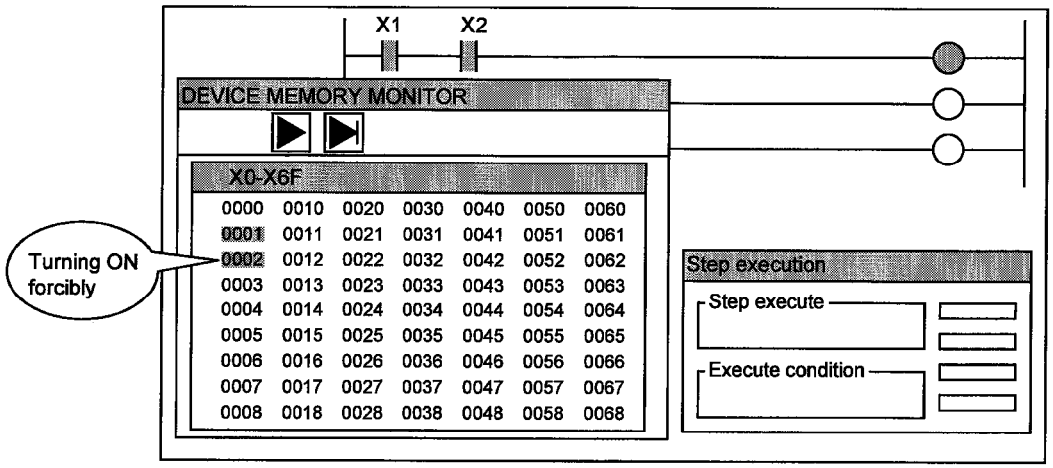
Also, as the ladder is created and debugged simultaneously on a single personal computer, program operation can be checked while ladders are being created.

The debugging environment is safe as no actual devices are connected to the actual PLC and no accident can result should an abnormal output arise due to a program bug.



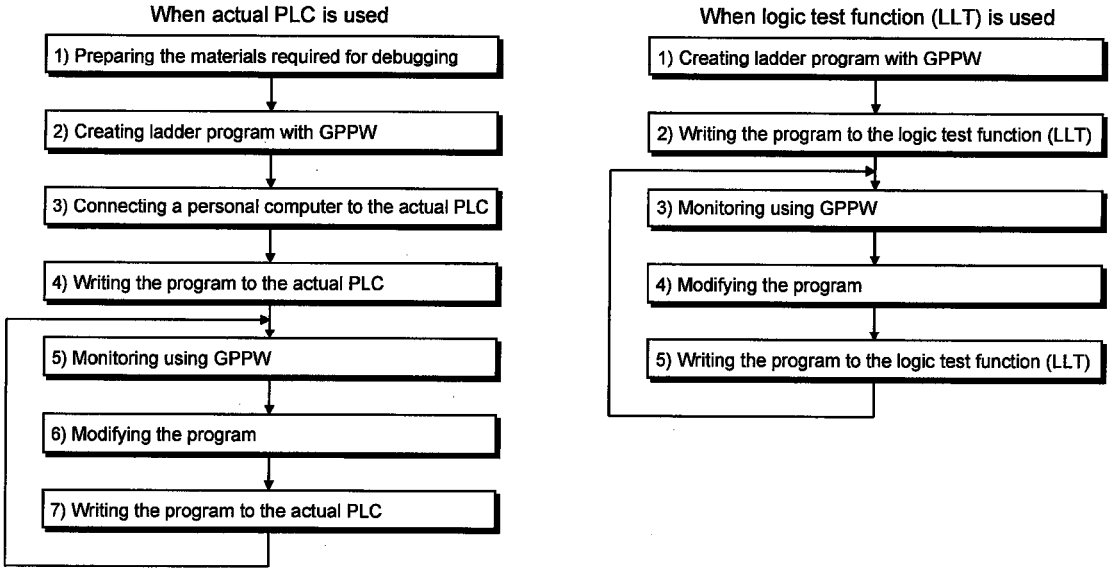
(b) Device Values Easy To Change

A device value can be easily changed on the ladder logic test tool (LLT) device memory monitor window by inputting a device value.
During GPPW step execution, device values can be changed in the ladder logic test tool (LLT) device memory monitor window for more efficient debugging operation.



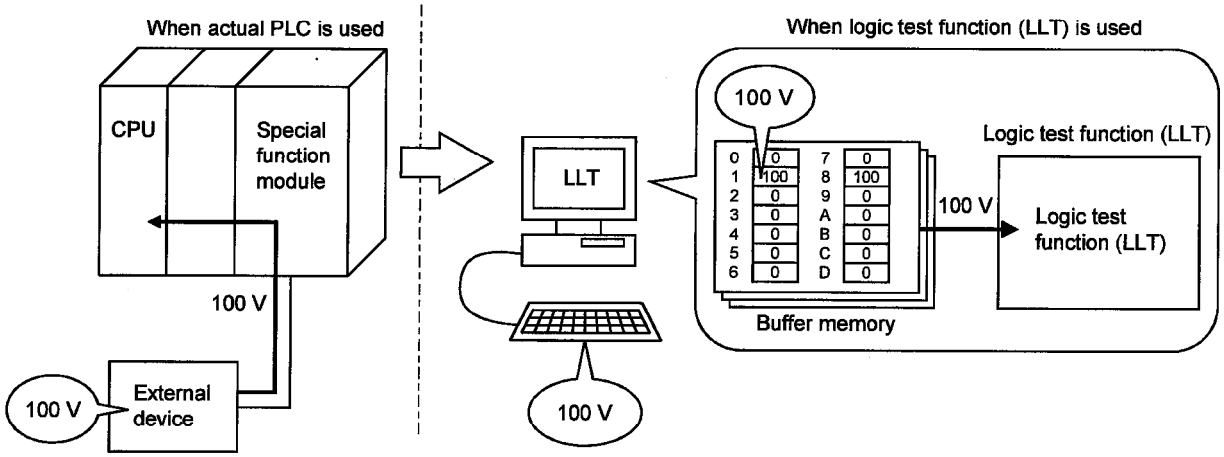
(c) Simplified Program Debugging Procedure.

As shown in the lower-left diagram, the conventional program debugging procedure was:
1) prepare the actual PLC and other materials required for debugging → 2) create ladder program with GPPW → 3) connect the personal computer to the actual PLC → 4) write program to the actual PLC → 5) monitor using GPPW → 6) modify program → 7) write program to the actual PLC
However, the procedure is simplified as shown in the lower-right diagram when the ladder logic test tool (LLT) are used, as no debugging materials or connections are required.



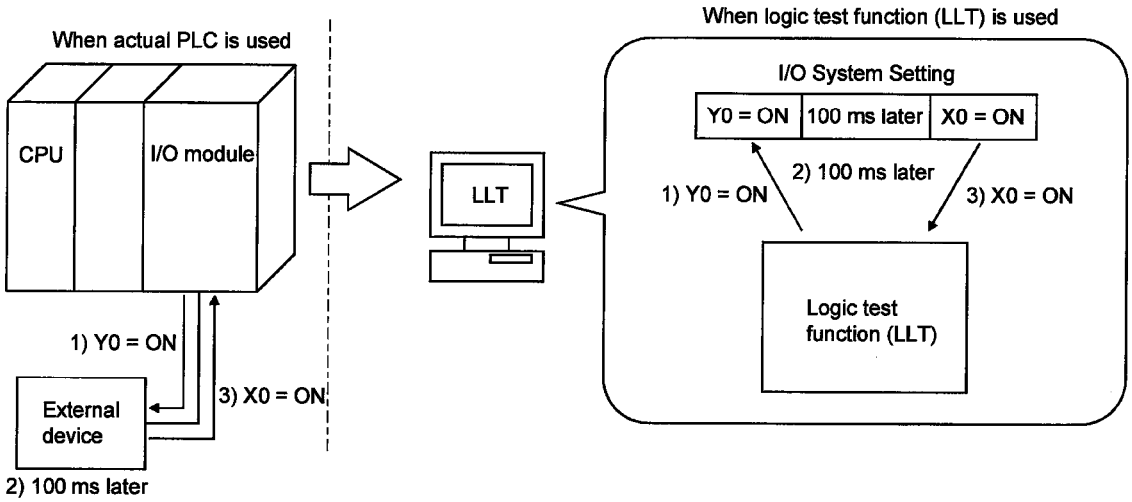
(2) Easy Debugging of FROM/TO Instructions for Special Function Modules

Simplifies the previously time-consuming debugging of programs whichprocess special function module I/Os (FROM/TO instructions).
By presetting values in the special function module buffer memory provided by the ladder logic test tool (LLT), the program can be debugged using simulated inputs from the special function modules.
Conversely, outputs to the special function modules can be monitored by monitoring the contents of the buffer memory.



(3) Simulation of External Device using I/O System Settings

In addition to the main program, a debugging program can be created by the system settings to model the external devices.



Conventional debugging involved creating a debugging sequence program to simulate inputs to external devices.
As an input (X) could be turned ON/OFF only in an external device connected to the I/O module, the program had to be modified by changing X0 → M0,X1 → M1, etc. to conduct debugging with no external device connected.
The I/O system settings function allows simulation of the external devices from the setting window, without creating a debugging sequence program.
As the main program is not modified, no adverse effects can result from additions or changes to the program for debugging.

(4) GPPW Online Functions Can be Used

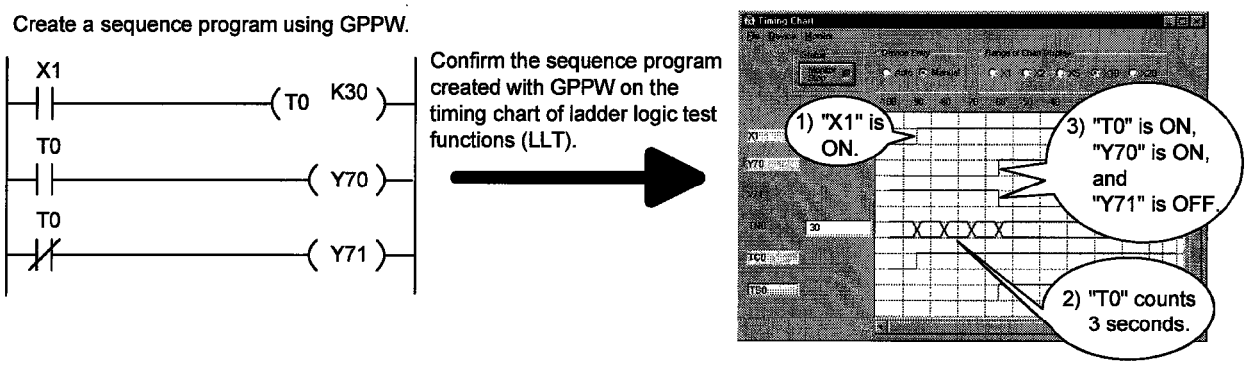
The combination of GPPW and ladder logic test tool (LLT) permits online functions such as the GPPW monitor test function and step execution to be used offline (see section 2.1).
For example, program step execution identical to when an actual PLC is connected is possible when offline.
This allows modifications in each line of data to be check during ladder monitoring.

(5) Tools Functions Save Buffer Memory Contents

The tool functions allow the contents of the device memory and special function unit buffer memory to be temporarily saved to the ladder logic test tool (LLT) and allow saved data to be read to the ladder logic test tool (LLT).
Temporarily saving the contents of the device memory and special function unit buffer memory during debugging and then reading this saved data to the ladder logic test tool (LLT) during the next debugging operation allows debugging to be restarted from the status when the data was saved.

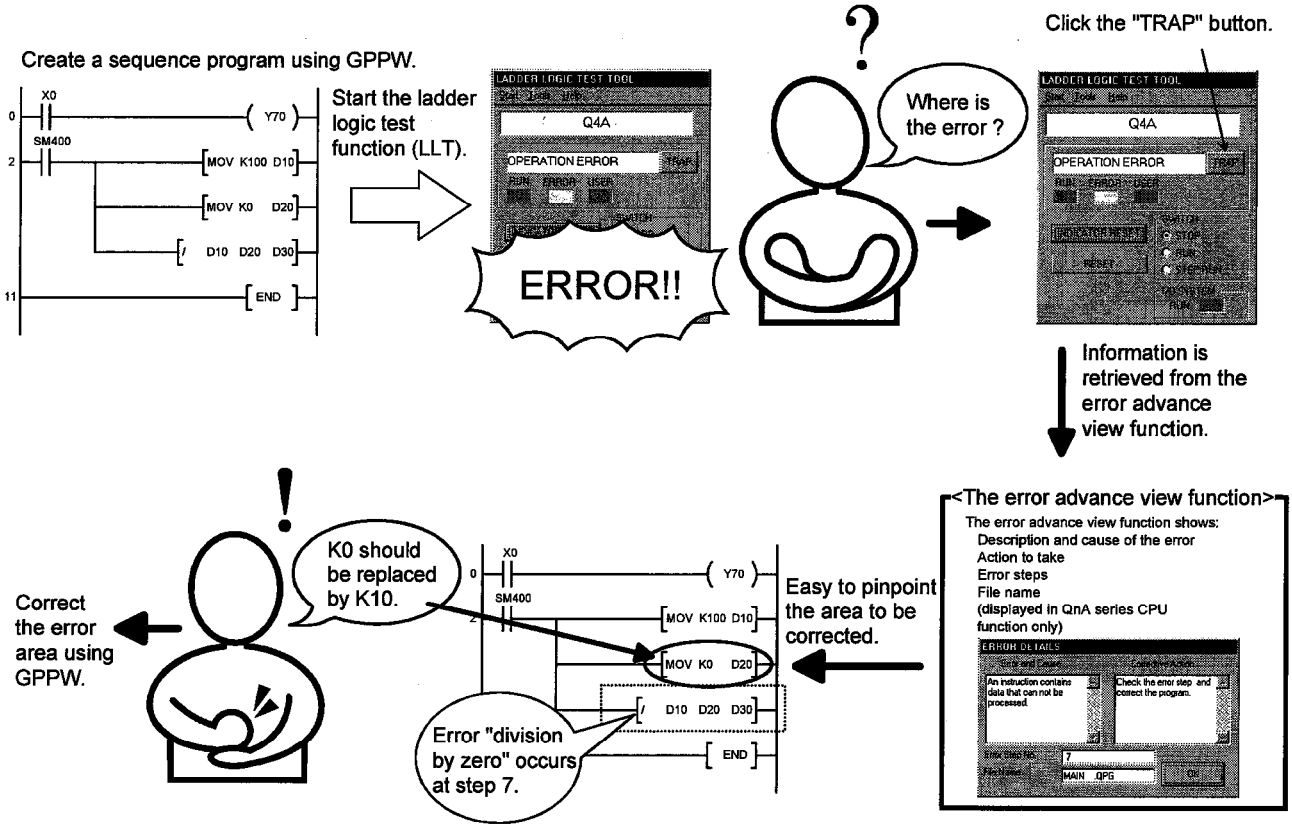
(6) Timing chart can be displayed

The timing chart shows the ON/OFF status of a bit device or the change in value of a word device at each scan.
It also makes debug tasks related to timing easier by providing a visual confirmation means of the ladder program.



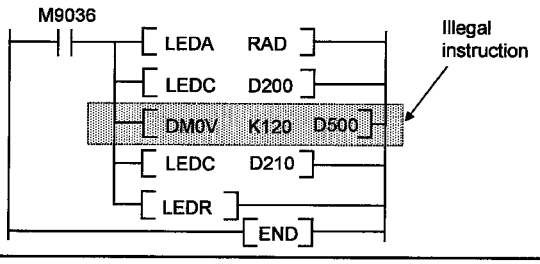
(7) Error advance view function

A detailed description is displayed in addition to the conventional LED display when an error such as an arithmetic error occurs during the simulation of the logistic test function.
This function saves time spent on referring to operation manuals and makes the search for the cause of the error easy as well.



1.2 Differences To Debugging with an actual PLC Connected

The specifications for debugging using the ladder logic test tool (LLT) differ from those for debugging with an actual PLC connected.
The main differences between debugging using the ladder logic test tool (LLT) and debugging with an actual PLC connected are shown below.
See Section 2.4 for details.

Item Name	Debugging with an Actual PLC Connected	Debugging with Ladder Logic Test Tool (LLT)	Applicable CPU
Step execution, skip execution, partial execution	Not supported by FX Series CPU functions	Debugging using step execution, skip execution, and partial execution makes debugging opera-tion more efficient.	• FXCPU
Device range check	Operation continues even if the indirect designation by the index register exceeds the device range.	"OPERATION ERROR" occurs when the device range determined by CPU type or parameters is exceeded. (For the device range for a specific CPU type, refer to Appendix 1.)	• ACPU • QnACPU • FXCPU • Motion controller CPU
Real number range check	Dedicated instructions to handle real numbers allow operation to continue when an illegal value occurs which cannot be evaluated as a real number.	Real number range checks are conducted rigorously. "OPERATION ERROR" is displayed if a value cannot be evaluated as a real number.	• ACPU • QnACPU • Motion controller CPU
Number range check	The result 0 is output when the A Series PLC DIV dedicated instruction (real number fixed decimal point division) is used to execute 0 ÷ 0. No error occurs.	The rigorous number range check can detect an illegal 0 denominator and "OPERATION ERROR" is generated if 0 ÷ 0 is executed.	• ACPU • Motion controller CPU
Illegal instruction in a dedicated instruction	The illegal instruction is ignored and operation continues.	The illegal instruction is checked and "INSTRCT CODE ERR." is displayed. Dedicated instructions must be described as blocks. (Example of illegal ladder) 	• ACPU • Motion controller CPU
Time concept	Actual time	Processing time considered as 100 ms per scan. Consequently, 5 scans are considered to take 500 ms.	• ACPU • QnACPU • FXCPU • Motion controller CPU

Item Name	Debugging with an Actual PLC Connected	Debugging with Ladder Logic Test Tool (LLT)	Applicable CPU
Supported instructions	All instructions can be used.	Data refresh instructions and PID control instructions (QnA Series, FX Series CPUs) cannot be used. These instructions are NOP. (For supported instructions, refer to Appendix 2.)	• ACPU • QnACPU • FXCPU • Motion controller CPU
Operating CPU type	According to CPU type used.	Operates as A4UCPU when an A Series CPU is selected, Q4ACPU when QnA Series CPU is selected, FXCPU when FX Series CPU is selected, or A4UCPU when motion controller CPU is selected.	• ACPU • QnACPU • FXCPU • Motion controller CPU
Special function module (special block)	Supported	Not supported. Only the buffer memory area of a special function module (special block) is supported.	• ACPU • QnACPU • FXCPU • Motion controller CPU
I/O module	Supported	Not supported	• ACPU • QnACPU • FXCPU • Motion controller CPU
Network	Supported	Not supported	• ACPU • QnACPU • FXCPU • Motion controller CPU
Memory cassette capacity	An error occurs in GPPW if data exceeding the memory cassette capacity is written to the PLC.	No error occurs and normal operation continues if data exceeding the memory cassette capacity is written to the PLC.	• ACPU • QnACPU • Motion controller CPU

2. SPECIFICATIONS

2.1 Table of Functions

The functions supported by the ladder logic test tool (LLT) are shown below.
The functions supported by the ladder logic test tool (LLT) include functions executed from the ladder logic test tool (LLT) menu and functions executed from the GPPW menu.
The Ladder Logic Test Tool simulates the function of the CPU selected at the time of execution of the LLT from the GPPW menu: it supports CPU's of type A, QnA, and FX. Also, when the CPU of the motion controller is selected, the corresponding function of the A Series CPU operates.
See the SW3D5C-GPPW-E/SW3D5F-GPPW-E Operating Manual for details about the operation of functions executed from the GPPW menu.

Table 2.1 Functions Supported by Ladder Logic Test Tool (LLT)

Function		Description	Reference
Functions executed from the GPPW menu	Ladder monitor Device monitor	• Monitors the processing status of the ladder logic test tool (LLT)	See the SW3D5C-GPPW-E /SW3D5F-GPPW-E Operating Manual
	Device test	• Forcibly write device values to the ladder logic test tool (LLT) during monitoring.	
	Write to PLC	• Writes parameter file and program file to ladder logic test tool (LLT).	
	PLC diagnostics	• Checks the ladder logic test tool (LLT) status and errors.	
	Skip execution	• Skips program execution in the range between two designated steps.	
	Partial execution	• Executes the part of the program in a designated step or pointer range.	
	Step execution	• Executes the sequence program one step at a time.	
	Remote operation	• Operates the ladder logic test tool (LLT) execution status.	
	Program monitor list	• Monitors the program execution status and number of executions as a table, starts and stops the program execution in the table.	
Functions executed from the ladder logic test tool (LLT) menu	I/O system settings	• Simulates the operation of external devices by simple settings.	See Chapter 4.
	Monitor test	• Conducts testing by monitoring the device memory status, displaying the ON/OFF chart of the devices, forcing the devices ON/OFF, and changing present values.	See Chapter 5.
	Tools	• Saves and reads the device memory and buffer memory.	See Chapter 6.
	Function equivalent to WDT	• Issues a WDT error if a sequence program is written in such a way that it runs an infinite loop.	—

2.2 Devices and Instructions Supported by the Ladder Logic Test Tool (LLT)

The ladder logic test tool (LLT) for the A Series, QnA Series, FX Series, and Motion controller CPU functions operate in the following ranges of devices and instructions.

Function Name	CPU Type	Device	Instruction
A Series CPU functions	A0J2H, A1FX, A1S(S1), A1SJ, A1SH, A1SJH, A1N, A2C, A2CJ, A2N(S1), A2S(S1), A2SH(S1), A3N, A2A(S1), A3A, A2U(S1), A2US(S1), A2AS(S1), A2AS-S30, A2AS-S60, A2USH-S1*1, A3U, A4U	Operates in the device range of the selected CPU type. (See Appendix 1 (1).)	Operates with the instructions supported by the ACPU. (See Appendix 2 (1).)
QnA Series CPU functions	Q2A, Q2AS(H), Q2AS1, Q2AS(H)S1, Q3A, Q4A, Q4AR	Operates in the device range of the selected CPU type. (See Appendix 1 (2).)	Operates with the instructions supported by the QnACPU. (See Appendix 2 (2).)
FX Series CPU functions	FX0(S), FX0N, FX1, FX2(C), FX2N(C)	Operates in the device range of the selected CPU type. (See Appendix 1 (3).)	Operates with the instructions supported by the FXCPU. (See Appendix 2 (3).)
Motion controller CPU functions	A171SH (equivalent to A2SH), A172SH (equivalent to A2SH (S1)), A273UH (S3) (equivalent to A3U)	Operates in the device range of the corresponding ACPU. (See Appendix 1 (1).)	Operates with the instructions supported by the ACPU. (See Appendix 2 (1).) However, motion dedicated instructions (SVST, CHGA, CHGV, CHGT, SFCS, ITP) are not supported. They are not processed.

*1: Select CPU type of A2USH-S1 when CPU board A80BD-A2USH-S1 is used.

However, some devices and instructions are restricted or are not supported. Unsupported devices and instructions are not processed (NOP). These NOP instructions are shown on the initial screen of the ladder logic test tool (LLT) as unsupported information. (See Section 3.3.)
See Appendix 1 List of Supported Devices and Appendix 2 List of Supported Instructions for details about the devices and instructions supported by the ladder logic test tool (LLT).

POINT

In this manual, the PLC portion of the motion controller is described as a function of the motion controller CPU.
In addition, the A171SH, A172SH, and A273UH(S3) are included in the device/instruction support range of the A2SH, A2SH(S1), and A3U respectively.

2.3 Ladder Logic Test Tool (LLT) Safety and Handling Precautions

The safety and handling precautions for the ladder logic test tool (LLT) are described below.

(1) The ladder logic test tool (LLT) simulates the actual PLC to debug sequence programs. However, the correct operation of a debugged sequence program cannot be guaranteed.
After debugging with the ladder logic test tool (LLT), before running the program in an actual application, connect a actual PLC and conduct a normal debugging operation.

(2) The calculated results may differ from actual operation because the ladder logic test tool (LLT) does not access the I/O modules or special function modules and do not support some instructions and devices.
After debugging with the ladder logic test tool (LLT), before running the program in an actual application, connect an actual PLC and conduct a normal debugging operation.

2.4 Ladder Logic Test Tool (LLT) Restrictions and Cautions

The restrictions and cautions when debugging with the ladder logic test tool (LLT) are described below.

2.4.1 Restrictions and cautions common to each type of CPU.

(1) Ladder logic test tool (LLT) Processing Time

The ladder logic test tool (LLT) processing time is calculated using 100 ms per scan. The length of each scan becomes the set constant scan time (default = 100 ms).
This is intended to eliminate changes due to computer performance and user-created sequence programs.
The scan time can be set to a value other than 100 ms by changing the constant scan time setting.
(For A4UCPU functions the time is changed in D9020, for Q4ACPU functions the time is changed using parameters, for FXCPU functions the time is changed in D8039.)

(2) Restarting the ladder logic test tool (LLT)

When restarting the ladder logic test tool (LLT) immediately after ending it, it may take longer than the usual restarting time.

(3) Device Range Checks using I/O System Settings

Appendix 3 shows a table of devices supported by I/O system settings.
The range of usable devices is the ladder logic test tool (LLT) device range, regardless of the parameter setting range.

(4) Interrupt Programs

Interrupt programs are not supported. Any sequence program created is not executed.

(5) Floating Decimal Point

Rounding errors can occur in the results of instructions using the floating decimal point. Therefore, the results may differ from calculations when a CPU is connected.

(6) Read from PLC, Compare with PLC

Not supported by the ladder logic test tool (LLT).

(7) Comments

Not supported by the ladder logic test tool (LLT).

(8) LED Reset Button

The LED display is cleared when the LED reset button on the initial window is clicked. However, the display immediately reappears if the cause of the error has not been removed, so it appears that the LED display is not reset when the button is clicked.

(9) Automatic Writing of the Ladder Logic Test Tool (LLT)

Parameters and sequence programs are written when the ladder logic test tool (LLT) is started up.
As the file register and device initial values are not automatically written, write them to the ladder logic test tool (LLT) using Write to PLC.

(10) Restrictions applied to Combinations with GPPW

The following table shows the restrictions that are applied when the LLT is used in combination with the GPPW.

		GPPW	
		SW2D5C/F-GPPW-E	SW3D5C/F-GPPW-E
Ladder Logic Test Tool (LLT)	SW2D5C/F -LLT-E	○	△*1
	SW3D5C/F -LLT-E	△*2	○

○ : No restrictions
△ : Partial restrictions

*1: Buffer memory monitor for the ladder logic test tool (LLT) can not be executed from GPPW, when A Series CPU is selected.
*2: Can not select buffer memory monitor from GPPW, when the ladder logic test tool (LLT) for A Series CPU is running.

Note

It is not possible to install an English version of the ladder logic test tool (LLT) when a Japanese version GPPW is already installed.

(11) Task Bar Settings

If Auto Hide is set in the Windows95/98 task bar settings, the task bar is hidden and not displayed at the bottom of the screen if the GPPW window is displayed at its maximum size and the ladder logic test tool (LLT) initial window is active. The task bar is displayed when the GPPW window is reduced or the GPPW window is set active.

2.4.2 Restrictions and cautions for the A Series CPU functions

(1) Special function module Compatibility

The ladder logic test tool (LLT) does not support the special function modules. The special function module buffer memory area capacity is 16 k points × 64 units. It is possible to save to and read from this area but any other access results in an error.

(2) Saving To and Reading From Buffer Memory

Make I/O assignments with GPPW before saving or reading the special function module buffer memory. (See the SW3D5C-GPPW-E/SW3D5F-GPPW-E Operating Manual.)
It is not possible to save to and read from the buffer area unless I/O assignments are made.

(3) Enabling and Disabling the Parameter Setting Items

Some GPPW parameter settings are disabled by the ladder logic test tool (LLT) even if data is set for them.
The settings disabled by the ladder logic test tool (LLT) are shown below.

Parameter		Setting
PLC parameter	Memory capacity	Disabled other than Sequence and "File register" of "program capacity".
	PLC system	"Output modes except for STOP→RUN" are disabled.
	PLC RAS	• "Annunciator display mode" is disabled. • Only Computation error and Special Unit access in the "operating mode when there is an error" are enabled.
	I/O assignment	All valid.
	Device	"Latch Start" is disabled.
Network Parameter		All disabled.

(4) Device Memory Monitor Device Range Check

T2048 to T3071 are used by the system and are unavailable for monitoring or testing.

(5) Microcomputer Programs

Not supported by the ladder logic test tool (LLT).

(6) PLC Memory Clear

Execute to clear all user data written to the ladder logic test tool (LLT) and initialize.
Also execute this function when unstable logic test function (LLT) operation occurs.

(7) A1FXCPU Built-in Functions

If the A1FXCPU type CPU is selected, the A1FXCPU I/O signals become general I/O signals during debugging with the ladder logic test tool (LLT). Consequently, the A1FX functions are identical to the I/O module functions.

2.4.3 Restrictions and cautions for the QnA Series CPU functions

(1) Special Function Module Compatibility

The ladder logic test tool (LLT) does not support the special function modules. The special function module buffer memory area capacity is 16 k points × 64 modules. It is possible to save to and read from this area but any other access results in an error.

(2) Saving To and Reading From Buffer Memory

Make I/O assignments with GPPW before saving or reading the special function module buffer memory. (See the SW3D5C-GPPW-E/SW3D5F-GPPW-E Operating Manual.)
It is not possible to save to and read from the buffer area unless I/O assignments are made.

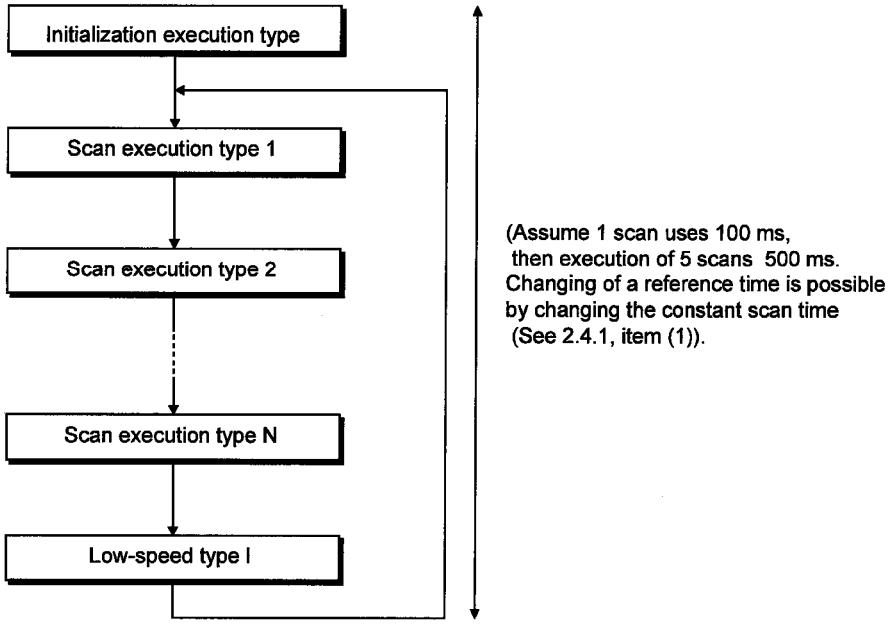
(3) Enabling and Disabling the Parameter Setting Items

Some GPPW parameter settings are disabled by the ladder logic test tool (LLT) even if data is set for them.
The settings disabled by the ladder logic test tool (LLT) are shown below.

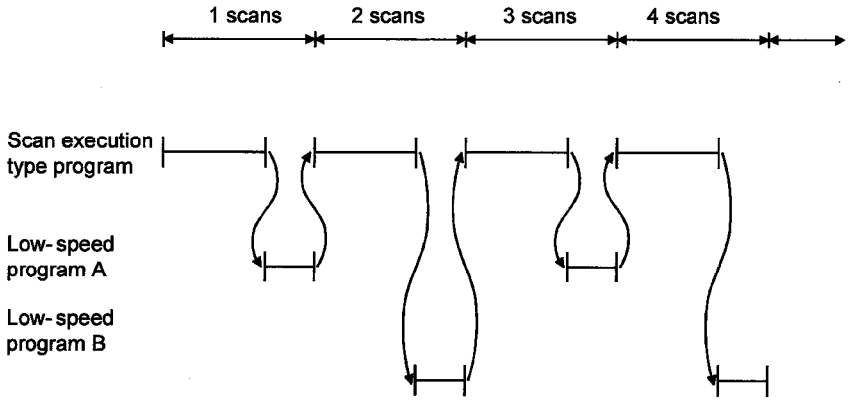
Parameter		Setting
PLC parameter	PLC name	All disabled.
	PLC system	Disabled, except for "Output mode at STOP to RUN" and "Common pointer No."
	PLC file	• The corresponding memory for the "file register" is disabled. • The "comment file used in a command" is disabled. • The corresponding memory for the "device initial value" is disabled. • The corresponding memory for the "file for local device" is disabled.
	PLC RAS	• "Error Check" is disabled. • Only Computation error and Special unit access error in the "operating mode when there is an error" are enabled. • "Annunciator display mode" is disabled. • "Break down history" and "Lowspeed program execution time" is disabled.
	I/O assignment	"Standard settings" (base, Power supply unit, Increase cable) are all disabled.
	Device	"Device point" and "Latch Start" are disabled.
	Program	All valid.
	Boot file	All disabled.
	SFC	All disabled.
Network Parameter		All disabled.

(4) Execution of Low-speed Programs

Regardless of the constant scan setting or setting of the low-speed program execution time, the ladder logic test tool (LLT) always executes the low-speed programs after the scan execution programs.
The program execution sequence is show below. (This sequence is identical during step operation.)



During each scan, all scan programs are executed before one low-speed type program is executed. Consequently, if N low-speed programs are set, N scans are required to execute them all.



POINT

Since a low-speed program is always completed within one scan, the monitor value of SM510 is always OFF.

(5) Device Memory Monitor Device Range Check

T31744 to T32767, SB800 to SB7FFF, and SW800 to SW7FFF are used by the system and are unavailable for monitoring or testing.

(6) Function Register (FD) Monitor

The function register (FD) monitor cannot be executed from the ladder logic test tool (LLT) menu. Execute it from the GPPW menu.

(7) TTMR Instruction Restrictions

A present value cannot be changed during TTMR instruction execution.

(8) I/O System Setting Device Range Check

SB800 to SB7FFF and SW800 to SW7FFFare used by the system and cannot be assigned.

(9) SFC Programs

Not supported by the ladder logic test tool (LLT).

(10) PLC Memory Format

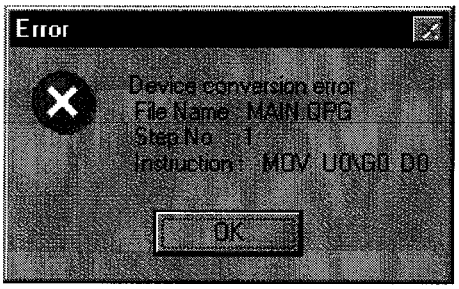
Execute to clear all user data written to the ladder logic test tool (LLT) and initialize.

Also execute this function when unstable logic test function (LLT) operation occurs.

(11) "MISSING END INS" Errors

If a buffer register (Un\G) with no I/O assignment is used for a program or status setting, "MISSING END INS" is displayed on the LED display.

After correctly setting the I/O assignments, write the parameters to the ladder logic test tool (LLT).



2.4.4 Restrictions and cautions for the FX Series CPU functions

(1) CPU Type Selection and FX CPU Operation

The ladder logic test tool (LLT) for the FX Series CPU functions operate according to the CPU functions and device range of the selected CPU.
Application instructions not supported by the selected CPU operate with the ladder logic test tool (LLT).
In cases where the sequence program may contain instructions not supported by the actual PLC due to conversion of a program for a higher model to a program for a lower model or due to input in the list mode, a program error occurs when the sequence program is written to the actual PLC, even if the program runs with the ladder logic test tool (LLT).
For example, the FX_0, FX_{0S} and FX_{0N} PLCs do not support pulse-execution application instructions, but these instructions run with the ladder logic test tool (LLT). Even so, a program error occurs when this program is written to the actual PLC because it contains non-supported instructions.

(2) STOP → RUN Program Check

A program error is detected by the STOP → RUN program check only if MC/MCR exists in the STL instruction or if no RET instruction is input for a STL instruction.
No other items are detected by the STOP → RUN program check. Therefore, use the GPPW program check functions in advance to check for these other errors.

(3) Program Memory Capacity

The maximum step capacity for each model is set.

(4) Watchdog Timer

The watchdog timer (D8000) operates every 200 ms for all CPUs. It can be rewritten but the written value has no effect on its operation.

(5) Debugging

The skip execution, partial execution, and step execution functions are only valid when using the ladder logic test tool (LLT). They cannot be used when an actual PLC is connected.

(6) Buffer Memory Monitor

The special extension device buffer memory in the ladder logic test tool (LLT) operates as general registers which allow reading and writing using FROM/TO instructions. This memory does not posses any special functions from the special extension devices.

(7) Analog Volume

The data registers (D8013, D8030, and D8031) storing the analog volume values for the FX_0, FX_{0S} and FX_{0N} PLCs operate as normal data registers. Use the GPPW device test functions to write values between 0 and 255 to these registers for testing.

(8) SORT Instruction

The SORT instruction is executed in the actual PLC over multiple scans. However, it is executed completely in a single scan in the ladder logic test tool (LLT) and M8029 (complete flag) operates immediately.

(9) SFC Programs

Testing of SFC programs for the FX PLC is possible because they are displayed as a ladder or list by the step ladder instructions (STL, RET) supported by the ladder logic test tool (LLT).

(10) Handling Keep Devices

Contents are maintained at a logic test function (LLT) STOP.
Contents are cleared when the ladder logic test tool (LLT) is quit.

(11) Handling Non-Keep Devices

Contents are cleared at a logic test function (LLT) STOP or when the ladder logic test tool (LLT) are quit.

(12) Memory Clear

Execute to clear all user data written to the ladder logic test tool (LLT) and initialize.
Also execute this function when unstable logic test function (LLT) operation occurs.

(13) Quick startup of the ladder logic test tool (LLT) with the FX Series CPU

When the ladder logic test tool (LLT) is used combining SW3D5 □ -LLT-E and SW3D5 □ -GPPW-E, the GPPW executes quick startup of the ladder logic test tool (LLT). When other combinations are used, it starts up the LLT at normal speed.

2.4.5 Restrictions and cautions for the Motion controller CPU functions

(1) Motion controller CPU Type Selection and Applicable CPU Type

The range of devices or instructions of a motion controller CPU are those of the applicable CPU.
The table below shows the types of CPU applicable to the motion controller.

Motion Controller CPU	Applicable CPU
A171SH	A2SH
A172SH	A2SH (S1)
A273UH (S3)	A3U

(2) Motion dedicated instructions

The ladder logic test tool (LLT) does not support motion dedicated instructions. Thus, when an attempt is made to use motion dedicated instructions on the ladder logic test tool (LLT), nothing will be processed. (NOP)

Motion dedicated instructions are only the following six;
SVST, CHGA, CHGV, CHGT, SFCS, and ITP.

REMARK

Any restrictions and cautions other than the ones described above are the same as those for the A Series CPU functions. For the restrictions and cautions for the A Series CPU functions, refer to 2.4.2.
For details of the motion controller CPU, refer to the Motion Controller CPU User's Manual.

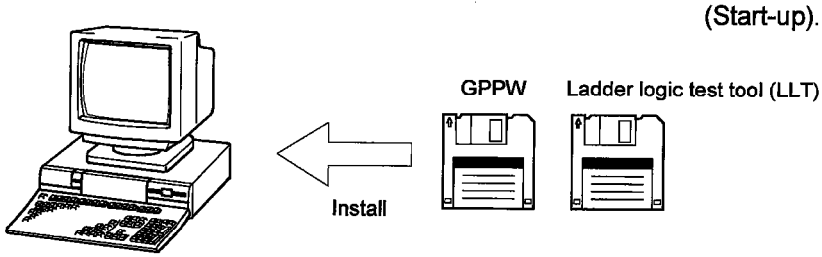
3. COMMON OPERATIONS FOR THE LADDER LOGIC TEST TOOL (LLT)

3.1 Procedure from Installation to Debugging

This section describes the procedures from installing the ladder logic test tool (LLT) to debugging a sequence program.

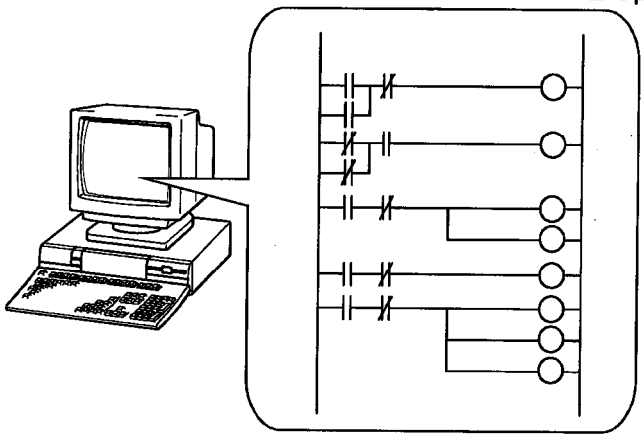
Procedure 1

Install GPPW and the ladder logic test tool (LLT) in the personal computer.
See the SW3D5C-GPPW-E/SW3D5F-GPPW-E Operating Manual (Start-up).



Procedure 2

Use GPPW to create a sequence program.
See the SW3D5C-GPPW-E/SW3D5F-GPPW-E Operating Manual.



Procedure 3

In GPPW, set the parameters to assign the I/Os (for A/QnA Series CPU functions) and make the program settings (for QnA Series CPU functions).
See the SW3D5C-GPPW-E/SW3D5F-GPPW-E Operating Manual.

POINT

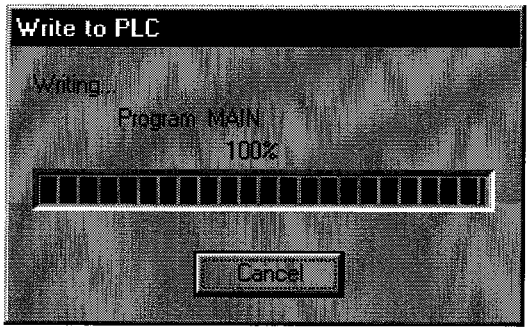
- Always execute the program settings for the QnA series CPU function.
  The restrictions indicated below will apply if the program settings are made without using GPPW.
  (1) In the GPPW project, the sequence program of the active ladder (list) window is written.
  (2) Sequence program is not written if the active window is not the ladder (list) window or if there are no active windows.
- For reading/writing of special function module buffer memory, always execute I/O assignment (for A/QnA series CPU function).

(To next page)

(From previous page)

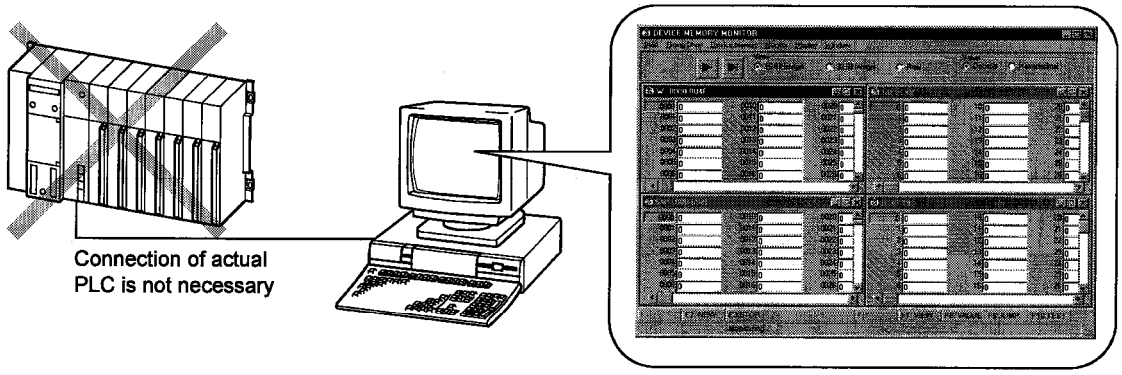
Procedure 4

Select the [Tools] → [Start ladder logic test] GPPW menu items to start the ladder logic test tool (LLT). The sequence program and parameters created with GPPW are automatically written to the ladder logic test tool (LLT) (equivalent to write to PLC).



Procedure 5

Debug the sequence program using the ladder logic test tool (LLT) and GPPW functions.
Debugging is possible by using the device monitor, changing arbitrary device values, or simulation of machine operation.
See Chapter 4 I/O System Setting Functions and Chapter 5 Monitor Test Functions.
See the SW3D5C-GPPW-E/SW3D5F-GPPW-E Operating Manual.



Procedure 6

After debugging, modify the sequence program.
See the SW3D5C-GPPW-E/SW3D5F-GPPW-E Operating Manual.

Procedure 7

Set the execution status in the initial window to STOP.
If necessary, save the contents of the device memory and special function module buffer memory. See Chapter 6 Tool Functions.

Procedure 8

Select the [Online] → [Write to PLC] GPPW menu items to write the modified program to the ladder logic test tool (LLT).
See the SW3D5C-GPPW-E/SW3D5F-GPPW-E Operating Manual.

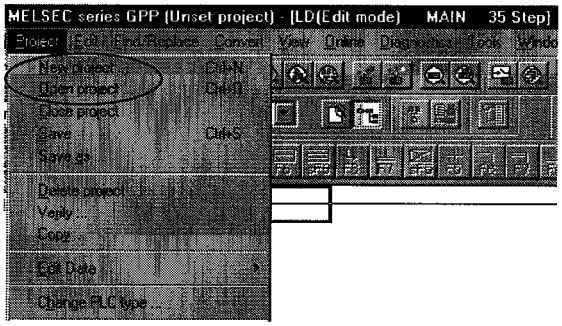
To debug the program again, repeat Procedures 5 to 8.

3.2 GPPW Operations before Debugging

This section describes the GPPW operations required before debugging with the ladder logic test tool (LLT).
Conduct the operations described below before debugging a program with the ladder logic test tool (LLT).

(1) Make the Project to Create the Sequence Program

To create a new project, select [Project] → [New project] from the GPPW menus and make the required settings.
To read an existing project, select [Project] → [Open project] from the GPPW menus and select the project.



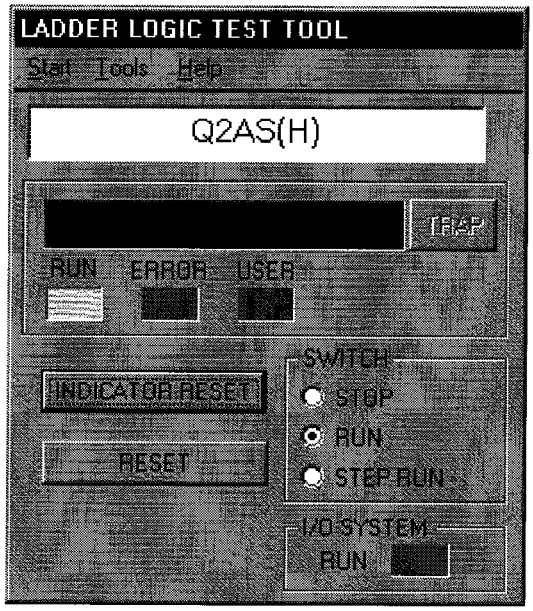
(2) Create the Sequence Program

(3) In GPPW, set the parameters to assign the I/Os (for A/QnA Series CPU functions) and make the program settings (for QnA Series CPU functions).

POINT

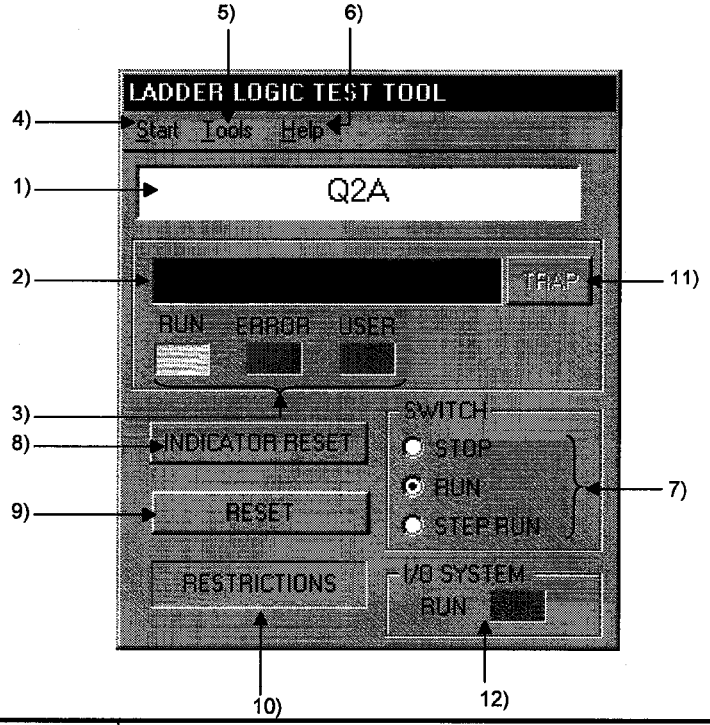
- Always execute the program settings for the QnA series CPU function.
  The restrictions indicated below will apply if the program settings are made without using GPPW.
  (1) In the GPPW project, the sequence program of the active ladder (list) window is written.
  (2) Sequence program is not written if the active window is not the ladder (list) window or if there are no active windows.

(4) Select the [Tools] → [Start ladder logic test] GPPW menu items to start the ladder logic test tool (LLT). An initial window as shown below is displayed. The sequence program and parameters are automatically written to the ladder logic test tool (LLT) when the ladder logic test tool (LLT) are started by GPPW.
Offline debugging of the sequence program using the ladder logic test tool (LLT) is now possible.



3.3 Description of the Initial Window Display

A ladder logic test tool (LLT) initial window as shown below is displayed when the ladder logic test tool (LLT) is started.
This section describes the items displayed in the ladder logic test tool (LLT) initial window.



Number	Name	Description
1)	CPU type	Displays the currently selected CPU type.
2)	LED Indicators	• Can display up to 16 characters. • The indicator display is equivalent to the display of CPU operation errors.
3)	Operation Status LEDs	RUN/ERROR : Enabled for all QnA, A, FX, Motion controller Series CPUs. USER : Displayed for QnA Series functions only.
4)	Start	Enables the selection of [Device Memory Monitor], [I/O System Settings], [I/O System Status], and [Clear I/O Settings].
5)	Tools	Use the Tools menu to execute the tool functions. See Section 6 Tool Functions.
6)	Help	Displays the ladder logic test tool (LLT) licensee name and software version.
7)	Switch Display and Settings	Displays the execution status of the ladder logic test tool (LLT). Click on the radio buttons to change the execution status.
8)	INDICATOR RESET button	Click to clear the LED display.
9)	RESET button	• Click to reset the ladder logic test tool (LLT) • Displayed only for the A, QnA and Motion controller Series CPU functions.
10)	Unsupported information indicator lamp	• Displayed only when unsupported instructions or devices for the ladder logic test tool (LLT) are found. • Double clicking this indicator will display the unsupported instructions that have been changed to NOP instructions and their steps.
11)	Error advance display button	Clicking this button will display the descriptions of issued errors, error steps, and the name of files in which the error is issued. (The names of error files are displayed only when using the QnA Series CPU function.)
12)	I/O system setting LED	• LED lights up during execution of I/O system setting. • Double clicking this will show the contents of current I/O system settings.

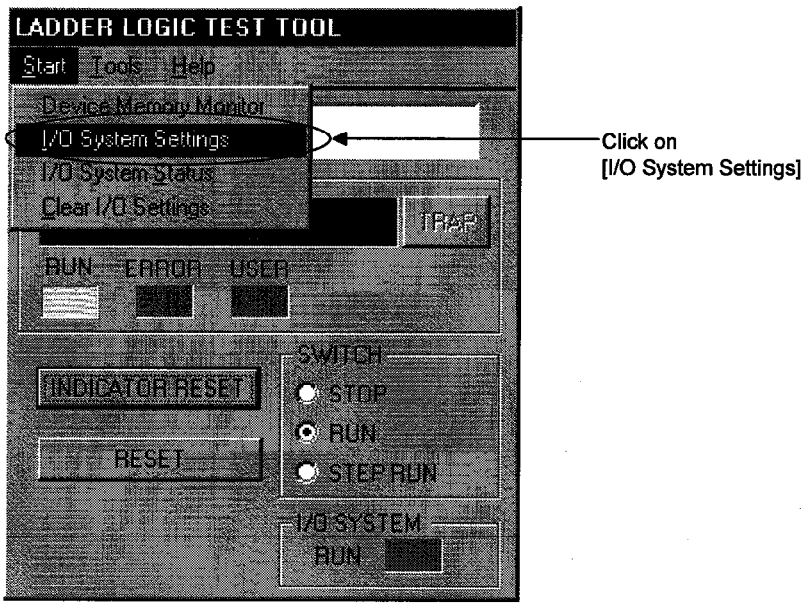
3.4 Screen Operations

This section describes the screen operations common to all functions.

(1) Starting from a Menu

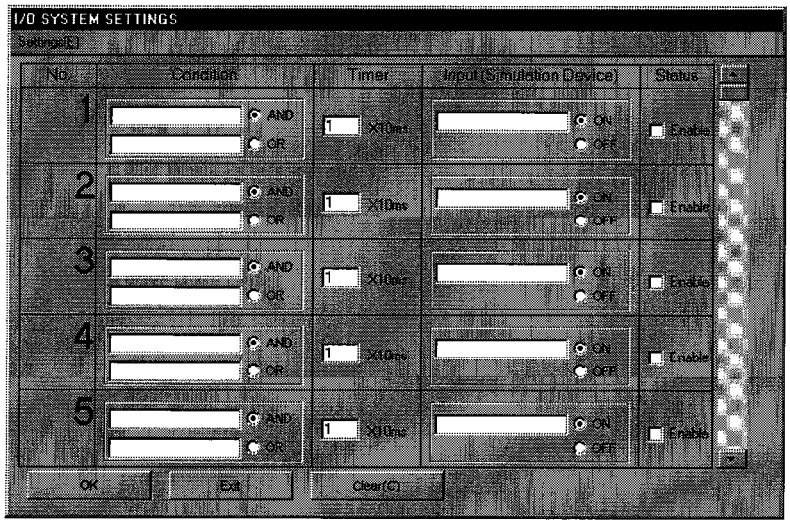
The procedure to use the menus is described below.

(a) Click on [Start] in the initial window to display a drop down menu. Select the required menu item.
To execute the tool function, click on [Tools] and select the required menu item.



(b) The selected menu item is executed.

An example of selecting the [I/O System Settings] is described below.

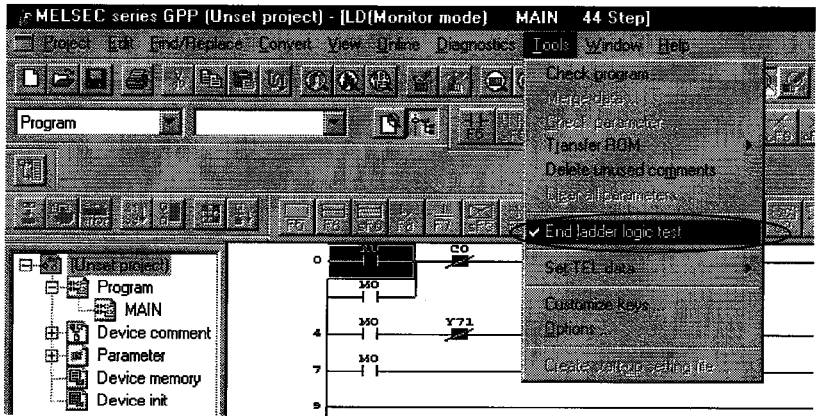


I/O System Setting dialog box

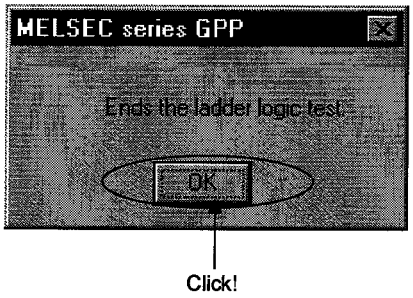
(2) Ending the ladder logic test tool (LLT)

(a) Select the [End ladder logic test] GPPW menu item again.

The ladder logic test tool (LLT) operation ends.



(b) Click "OK" when the following dialog box appears.



MEMO

4. SIMULATION OF EXTERNAL DEVICE OPERATION — I/O SYSTEM SETTING FUNCTIONS

The I/O system setting functions allow simulation of the operation of external devices just by making simple settings.
In conventional debugging, a debugging sequence program was created to simulate the operation of the external devices.
Using the I/O system setting functions, the operation of the external devices can be automatically simulated without the requirement to create a special debugging sequence program,

(1) Differences between Conventional Debugging and Debugging with the I/O System Setting Functions

A comparison between conventional debugging with an actual PLC connected and debugging using the I/O system setting functions is shown below.

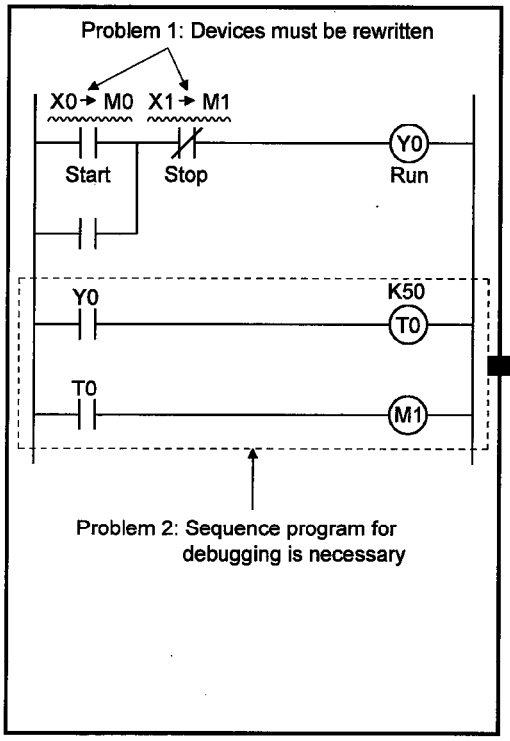
(a) Conventional Debugging

The program must be modified as follows for debugging:
Add a debugging sequence program to simulate operation of the external devices.
As an input (X) can be turned ON/OFF only with an external device connected to the I/O unit, modify the program by changing X0 → M0, X1 → M1, etc. to conduct debugging with no external device connected.

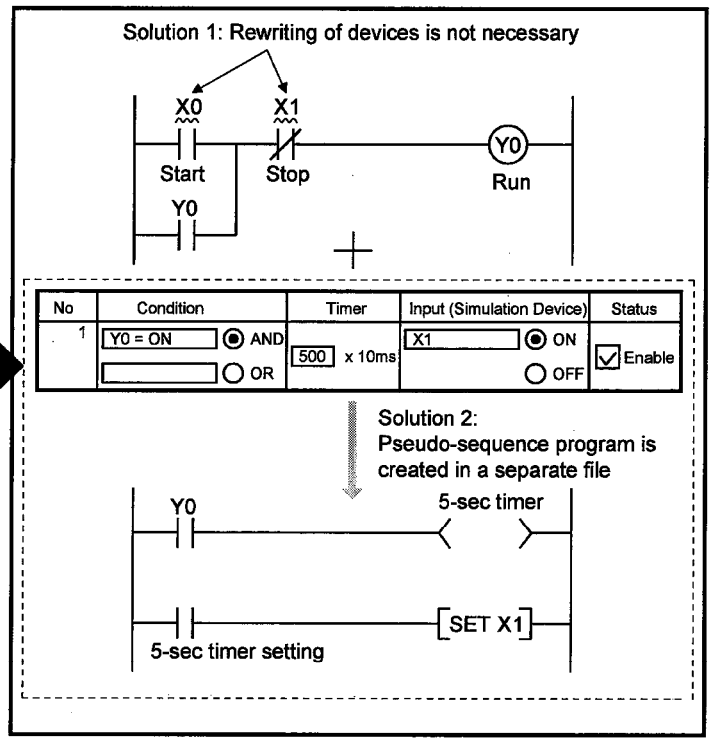
(b) Debugging using the I/O System Settings

The I/O system setting function allows sequence program settings and changes to be made for debugging from the setting window.
It is unnecessary to add a sequence program. It is not necessary to rewrite the devices (X0 → M0, etc.) as the inputs (X) can be directly turned ON/OFF from GPPW.

<Program used in conventional debugging>



<Program used for debugging using the ladder logic test tool (LLT)>



4.1 Simulation with the I/O System Setting Functions

This section uses the example of an actual simulation to describe the procedures between setting up and executing the I/O system setting functions.

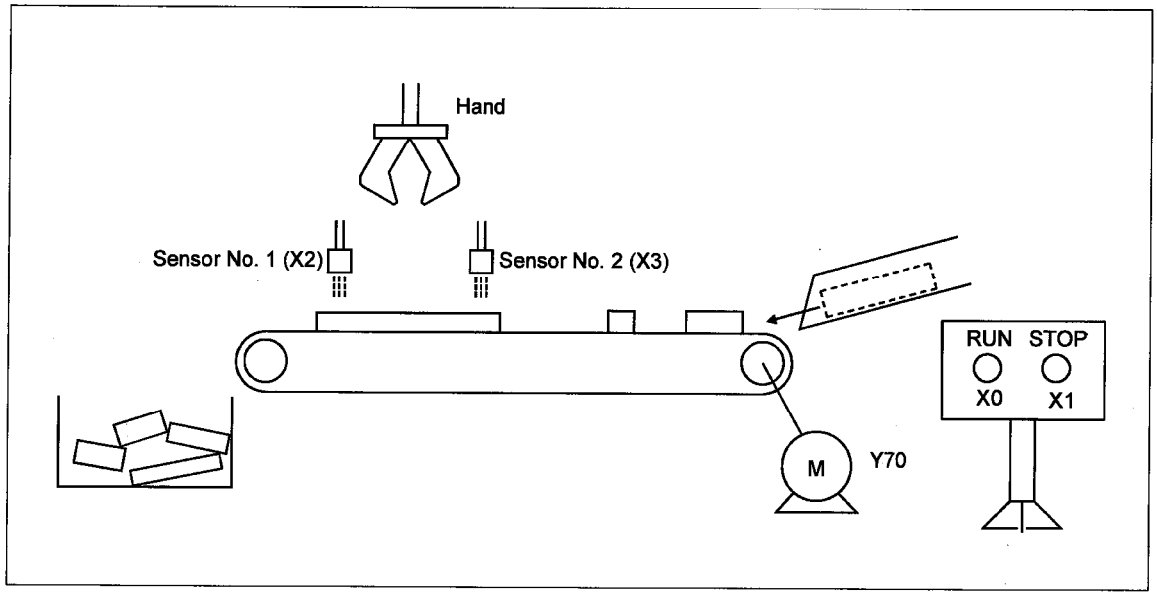
[Simulation Example]

The diagram below shows the control of a system which uses two sensors to select products exceeding a prescribed length from the products of varying lengths arriving on a conveyor, removes these products with a hand and transports them to another production line.

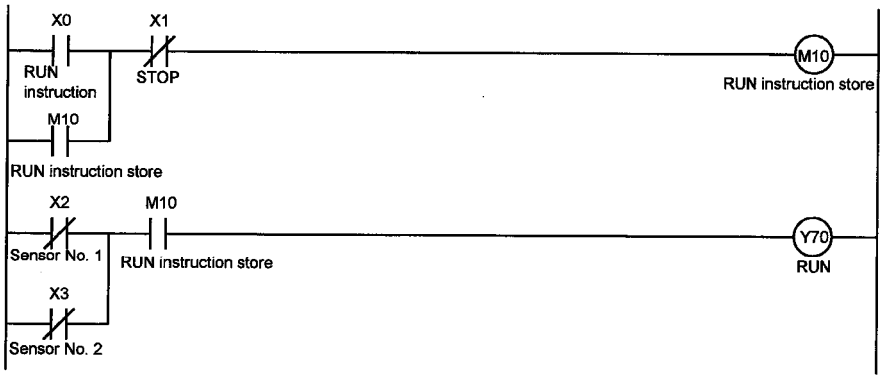
When a product exceeding the prescribed length arrives, sensors No1. (X2) and No. 2 (X3) turn ON simultaneously and operation halts.

This section describes the I/O system settings to simulate a product exceeding the prescribed length arriving, operation halting five seconds after operation started, and operation restarting after another three seconds.

[System Configuration]

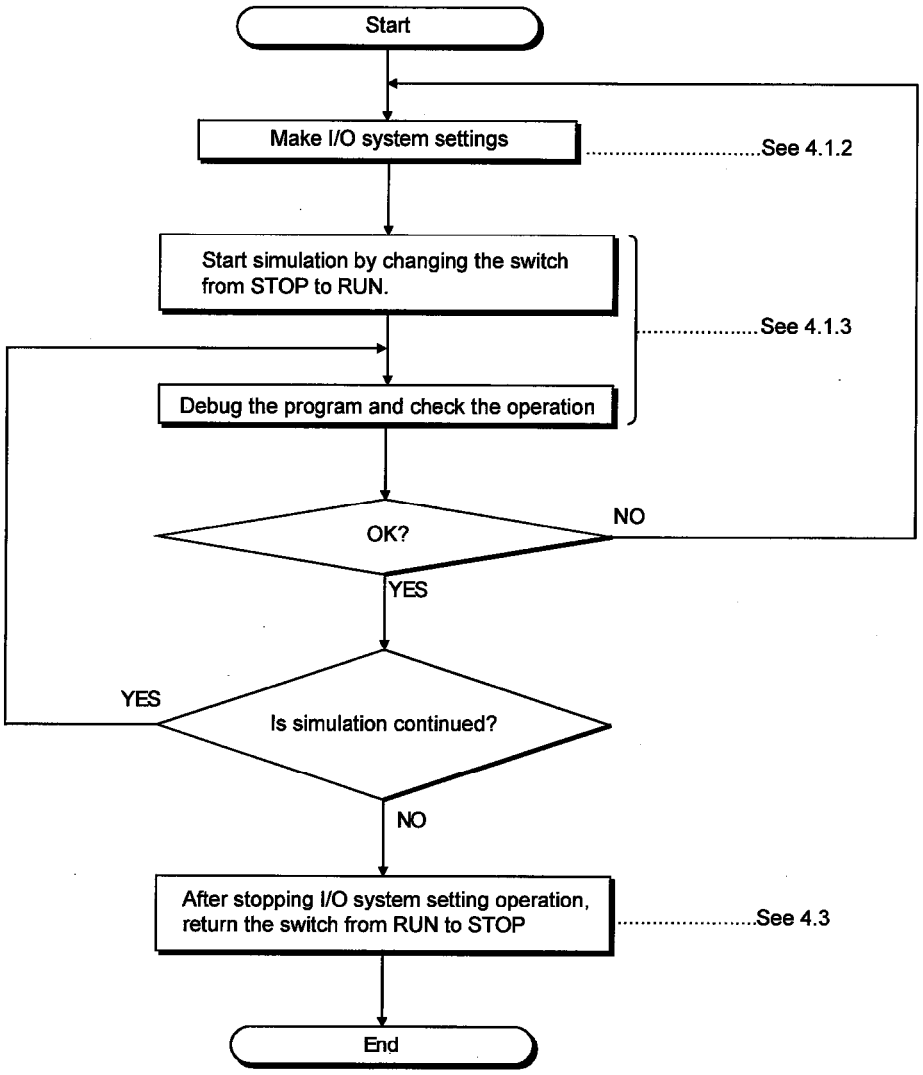


[Sequence Program]



4.1.1 Execution procedure for the I/O System setting functions

The flowchart shows the procedure to execute the I/O system setting functions.



4.1.2 I/O System setting method

[Setting Conditions]

The sequence program shown in Section 4.1 is set up to conduct the simulation in the following example.

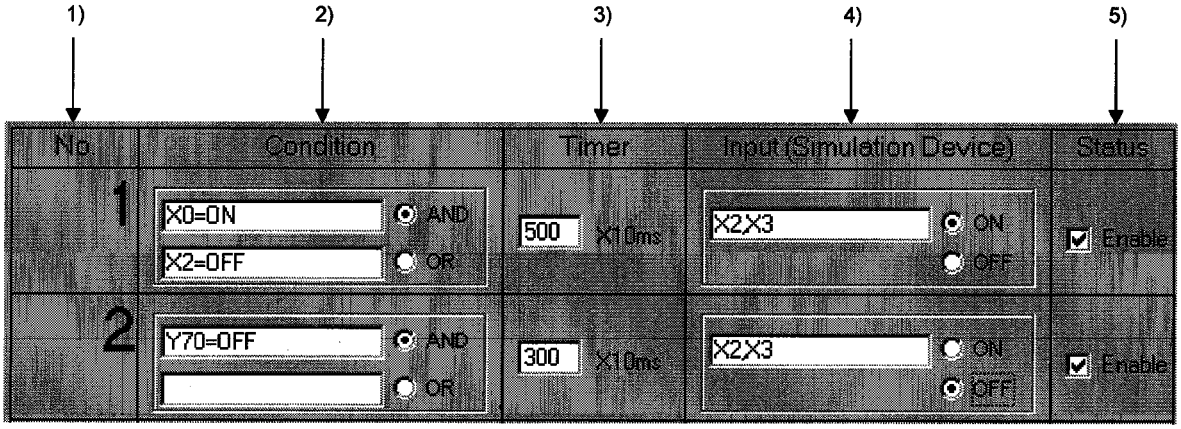
- A product exceeding the prescribed length is detected 5 seconds after operation starts (X0 = ON) and the belt conveyor operation stops (X2, X3 = ON).
- Three seconds after operation stops (Y70 = OFF), operation is restarted (X2, X3 = OFF).

[Operation Procedure]

Select [Start] → [I/O system settings] from the initial window.

[Setting Window]

Make the settings below in the I/O system dialog box.



[Description of the Settings]

1) No.

The number of the setting in the I/O system setting dialog box.
Up to 100 settings can be made.

2) Condition

Designates the input conditions from the ladder logic test tool (LLT).
The input conditions can be designated as a bit device or a word device.
For a bit device, the designated condition is ON/OFF. For a word device, the designated condition is a comparison (=, <>, <, >, <=, >=) with a constant or another word device.

<Sample designations>
Bit device : X0 = OFF, M10 = ON
Word device : D5<20, D15<>5, D20=2, D25>=10, D0=D50

POINT

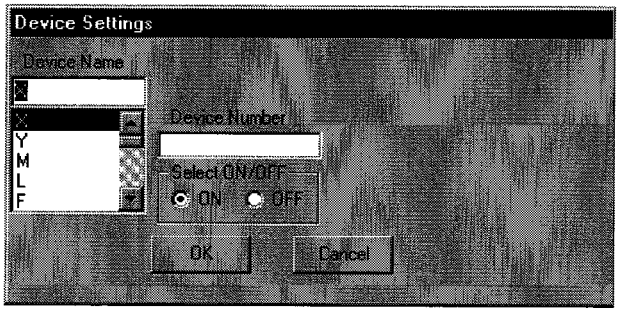
Index representation (eg. D0Z0), representation of a word device in bits form (eg. D0, 0) , and sets of bit device representation (eg. K4X0) are not allowed in the Condition area.

To make a relational condition, specify AND/OR operators by selecting the option buttons.

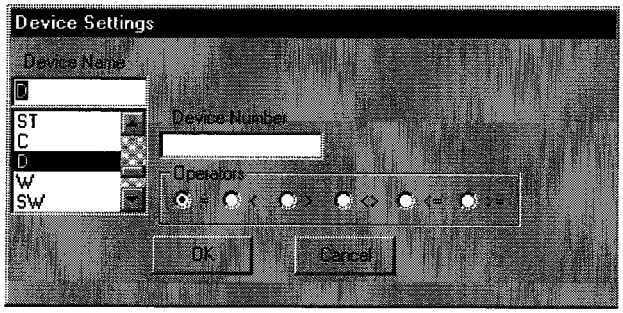
AND... The condition is fulfilled if both designated conditions are achieved. Otherwise, the condition is not fulfilled.

OR..... The condition is fulfilled if one or both of the designated conditions are achieved.
The condition is not fulfilled if neither designated condition is achieved.

- Input
  Enter the condition directly into the Condition area or double-click on the Condition area to display the following dialog box. Enter the device name, device number, and designated condition.
  Appendix 3(1) shows which devices can be entered in the Condition area.



Bit device selected



Word device selected

3) Timer

Sets the time from the designated condition being fulfilled until the input is issued. Enter the time in 10 ms units. The setting range is 0 to 9999 (× 10 ms).

4) Input (Simulation Device)

Designates the device that is turned ON/OFF when the designated condition is fulfilled.

Double-click on the [Input] area and designate the device or enter the device directly.

Multiple devices can be designated using the following method.

Independent device designation..... Designate non-consecutive devices,delimited by commas. For example, X0, X2, X5.

Consecutive device designation..... Designate the start and end device of a series of consecutive devices, separated by a hyphen (-). For example, X0-100.

Mixed device designation..... Designate a mixture independent and consecutive devices. For example, X0, X2, M10-20.

Click a radio button to set whether the designated devices turn ON or OFF when the condition is fulfilled.

Appendix 3(2) shows which devices can be entered in the Input area.

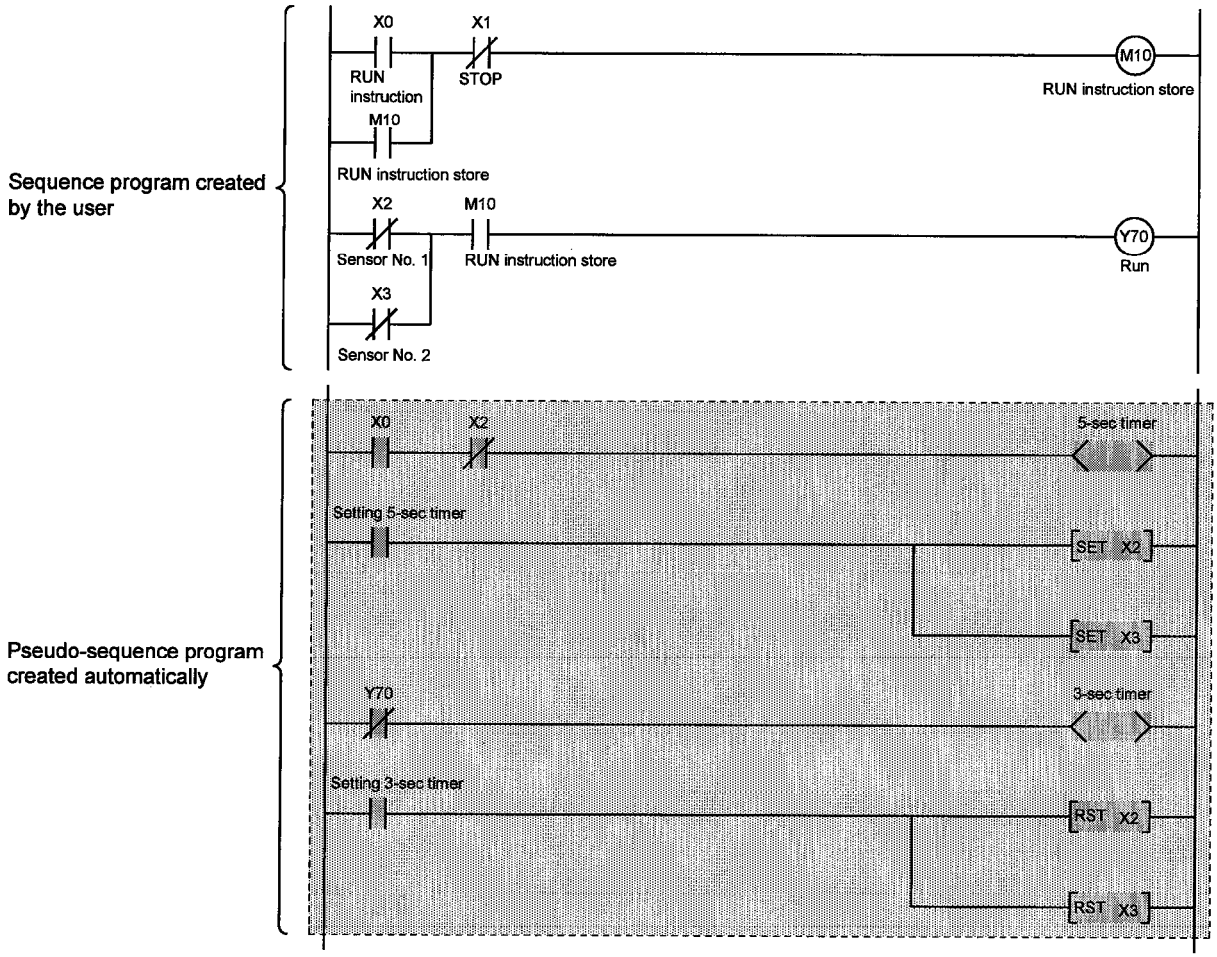
5) Status

Designates whether each setting is enabled or disabled.

A check mark ☑ appears in the check box if the setting is enabled.

REMARK

After the settings above are made, the pseudo-sequence program enclosed in the dotted box in the ladder logic test tool (LLT) is created in a separate file.
During program execution, the pseudo-sequence program is executed after the created sequence program.

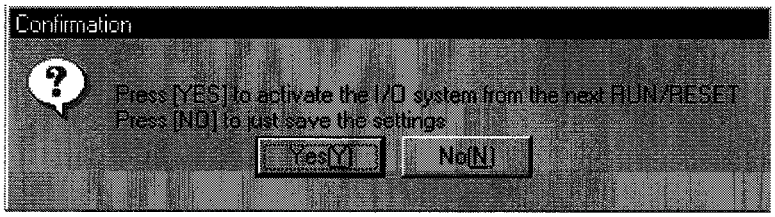


4.1.3 Starting the simulation

1) Click on the [OK] button when all items have been set.

2) When the [OK] button is clicked, the Save I/O System Settings As dialog box is displayed and the settings are saved if no setting error was made. See Section 4.4 for details about saving the settings.
(If a setting error was made, a summary is displayed in a dialog box and the setting window is displayed again.)

3) The following confirm dialog box is displayed after the settings are saved.
[Yes] button..... Simulation of the setting file is conducted the next time the status is switched from STOP → RUN.
[No] button..... Only saves the settings. (No simulation.)
Click the [Yes] button to run the simulation of the setting file.



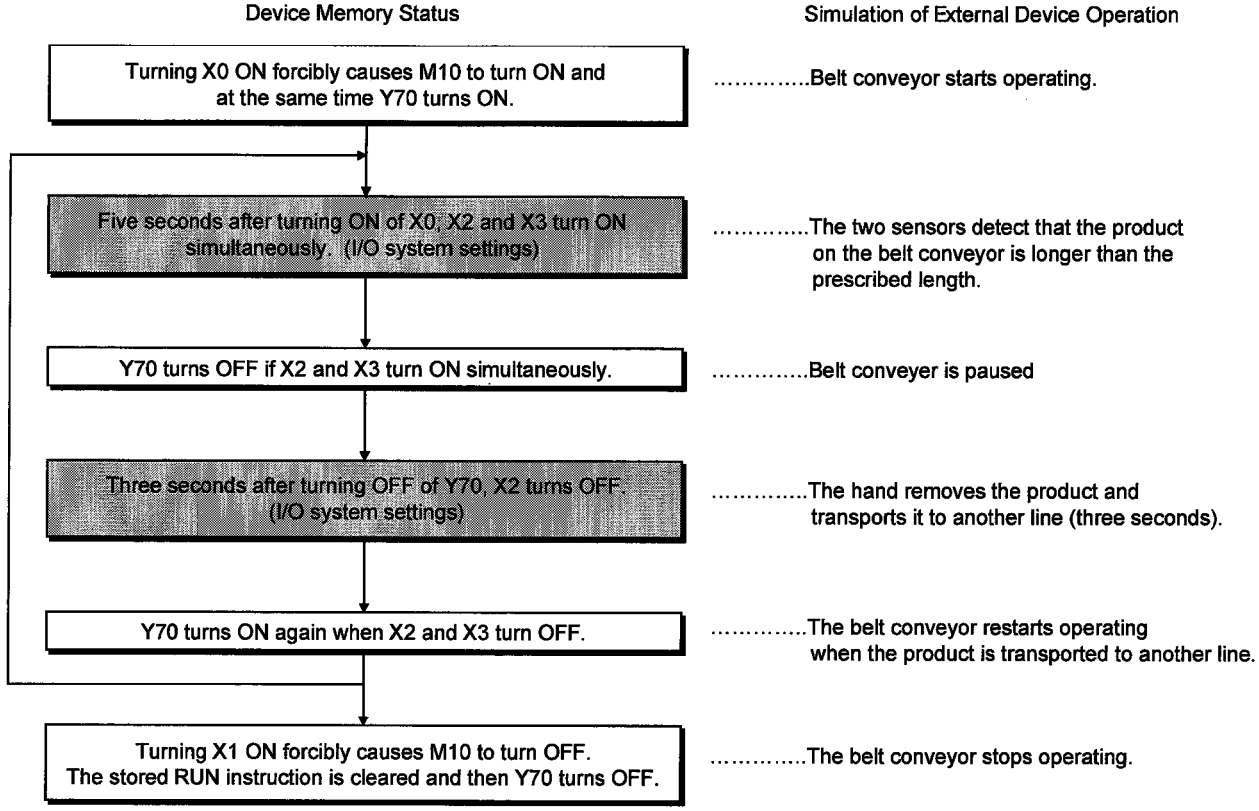
4) The I/O system setting dialog box closes and the initial window is displayed again.

5) The settings are enabled when the switch on the initial window is switched from STOP to RUN.

After the ladder logic test tool (LLT) are started the set I/O system settings remain enabled until they are deleted or the ladder logic test tool (LLT) are quit.
To use the same I/O system settings when the ladder logic test tool (LLT) are restarted, read the I/O system setting data from the saved file, as described in Section 4.5.

POINT
If settings are made in the RUN state, the state must be switched to STOP once and then returned back to RUN to enable the new settings.

[Actual Simulation Sequence]



During an actual simulation, check the device memory status using the ladder logic test tool (LLT) or GPPW device batch monitor.

See Section 5 Monitor Test Functions.

4.2 Checking Current I/O System Setting Status

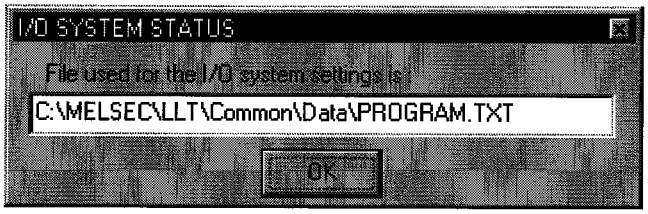
[Purpose]

To check the file name of the current I/O system setting data.

[Operation Procedure]

Select [Start] → [I/O system status] from the initial window.

[Setting Window]



The name of the currently executing I/O system setting file is displayed.
Nothing is displayed if no I/O system setting file is currently executing.

4.3 Stopping Current I/O System Setting Operation

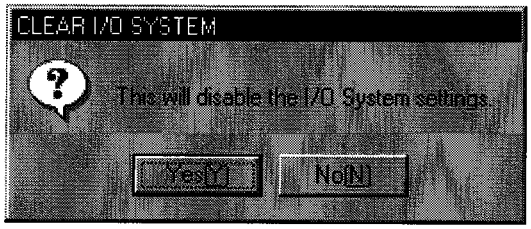
[Purpose]

Stops the currently executing I/O system setting operation.
(Stop execution of the pseudo-sequence program.)

[Operation Procedure]

Select [Start] → [Clear I/O settings] from the initial window.

[Setting Window]



Click on the [Yes] button to stop execution of the current I/O system settings.

POINT

Operation of the pseudo-sequence program stops at the timing the status changes from STOP to RUN.

4.4 Saving I/O System Settings to File

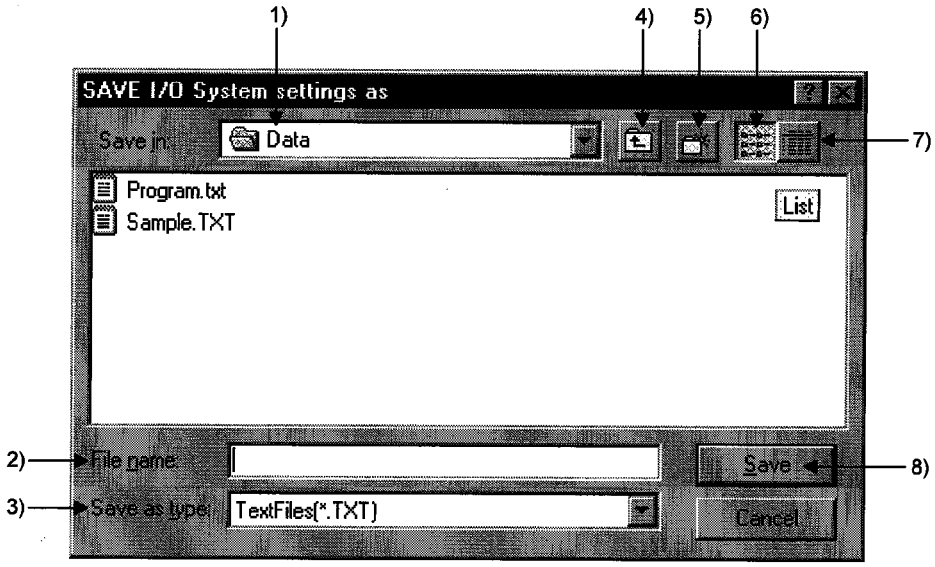
[Purpose]

Saves the settings made in the I/O system setting dialog box to a file.

[Operation Procedure]

Select [Settings] → [Save file] in the I/O system setting dialog box.

[Setting Window]



[Description of the Settings]

1) Save Destination

Designates the folder where the file is to be saved. Designate the folder
from a drop-down menu or double-click on a folder name in the folder list.

2) File name

Sets the name of the created data file.
As the extension is fixed as TXT, set the file name with no extension.

3) Save as type

Sets the type of saved file. Fixed as a text file (*.TXT).

4) Up One Folder

Click to move up one folder from the present folder position.

5) Create New Folder

Click to create a new folder under the designated folder.

6) Display Folder List

Click to display the folder names and file names only.

7) Display Folder Details

Click to display the folder name, file names, size, file type, and last modified date.

8) [Save] button

Click when all settings are complete.

4.5 Reading the I/O System Setting File

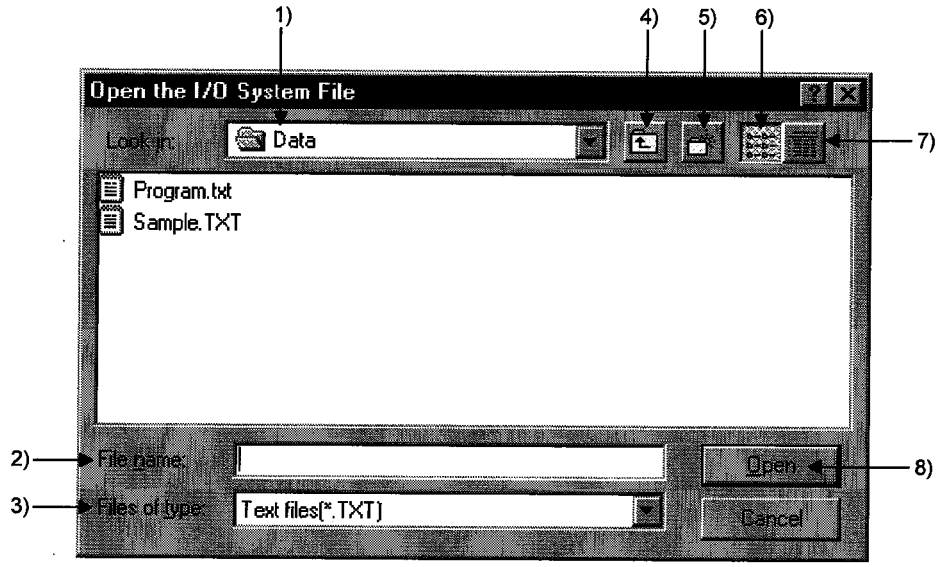
[Purpose]

To read data from a file to re-use previous settings.

[Operation Procedure]

Select [Settings] → [Open file] in the I/O system setting dialog box.

[Setting Window]



[Description of the Settings]

1) File Location

Designates the folder where the file is saved. Designate the folder from a drop-down menu or double-click on a folder name in the folder list.

2) File name

Sets the name of the file to be opened. Enter the file name directly or double-click on the file name in the folder list.

3) Files of type

Sets the type of the file to be opened.
Fixed as a text file (*.TXT).

4) to 7)

See Section 4.4 for details about settings

8) [Open] button

Click when all settings are complete.

MEMO

5. MONITORING DEVICE MEMORY — MONITOR TEST FUNCTION

The monitor test functions monitor the status of the device memory saved in the ladder logic test tool (LLT), force bit devices ON/OFF, and test changes to word device present values.

5.1 GPPW and Ladder Logic Test Tool (LLT) Monitor Test Functions

A combination of the ladder logic test tool (LLT) and GPPW monitor test functions allows the extensive GPPW monitor test functions to be used offline.
All monitor test functions available with the GPPW and ladder logic test tool (LLT) are described below.
If a function is not supported by the ladder logic test tool (LLT), execute a function from a GPPW menu.

Function		Function Executed from a GPPW Menu	Function Executed from a Ladder Logic Test Tool (LLT) Menu
Monitor test functions	Ladder monitor	○	–
	Device batch monitor	○	○
	Device registration monitor	○	–
	Buffer memory batch monitor	○	○
	Device test	○	○
	Skip execution	○	–
	Partial execution	○	–
	Step execution	○	–

○..... Available
–..... Not supported

See the SW3D5C-GPPW-E/SW3D5F-GPPW-E Operating Manual for details of the functions which can be executed from the GPPW menu.

5.2 Monitor Test of the Device Memory

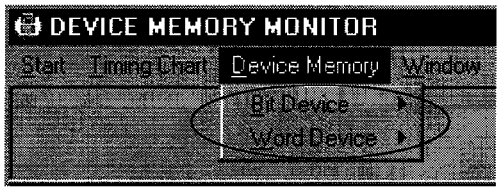
This section describes the operation to conduct the monitor test on the device memory. This section describes only the functions which can be executed from a ladder logic test tool (LLT) menu. See the SW3D5C-GPPW-E/SW3D5F-GPPW-E Operating Manual for details about the functions executed from a GPPW menu.

5.2.1 Selecting the devices for the monitor test

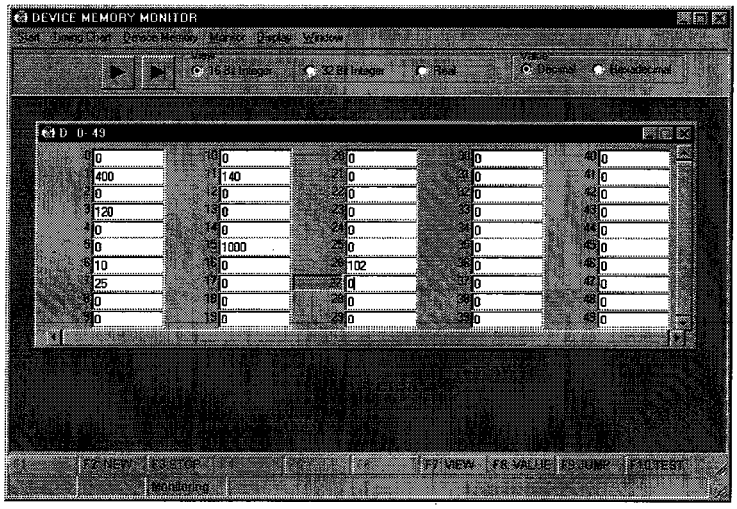
This section describes how to select the devices for the monitor test.

[Operation Procedure]

1. Select [Start] → [Device Memory Monitor] from the initial window.
2. Select [Device Memory] then [Bit Device] or [Word Device] in the device memory monitor window and select the devices to be monitored in the monitor test.



3. The selected device window is displayed.
   The selected device monitor is started automatically.



POINT
To monitor the buffer memory of a special function unit, set the I/O assignment in GPPW parameter setting.

4. Click on the |◀| ◀ ▶ |▶| button or select [Display] → [Jump] (F9) to change the displayed device range.

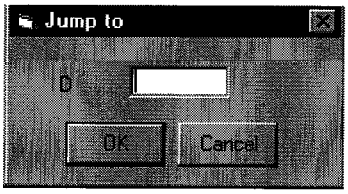
|◀| ..... Click this button to display the first page of currently displayed devices.

◀ ..... Click this button to display the previous page of currently displayed devices.

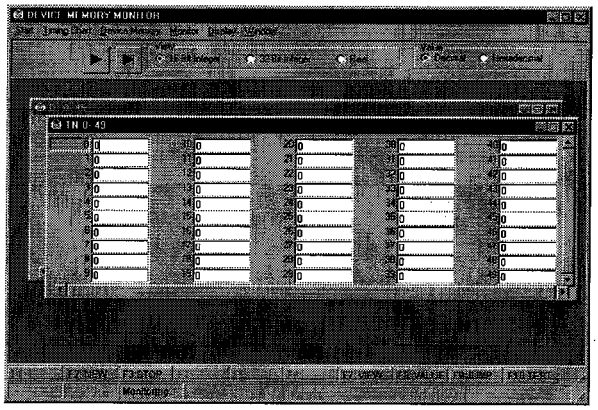
▶ ..... Click this button to display the next page of currently displayed devices.

|▶| ..... Click this button to display the last page of currently displayed devices.

[Display] → [Jump] (F9)... Select these items to open the following setting window. Designate the first device number to be displayed.



5. To open multiple windows, select [Window] → [New] (F2) and designate the device names and device numbers.
The designated device windows are displayed overlapping each other.



POINT

(1) Although the device window opens in either procedure of [Device Memory] → [Bit Device] / [Word Device] or [Window] → [New] (F2), the device window called by the procedure beginning with the selection of [Device Memory] display the devices starting from device number 0.
Select [Window] menu (F2) to specify an arbitrary start device number for display.

(2) Pressing the ESC key closes the device window which is currently active.

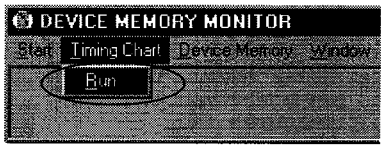
5.2.2 Displaying the timing chart for devices

[Purpose]

To visually confirm a ladder program by displaying the ON/OFF status of a bit device or the change in value of a word device using a chart.

[Starting Method]

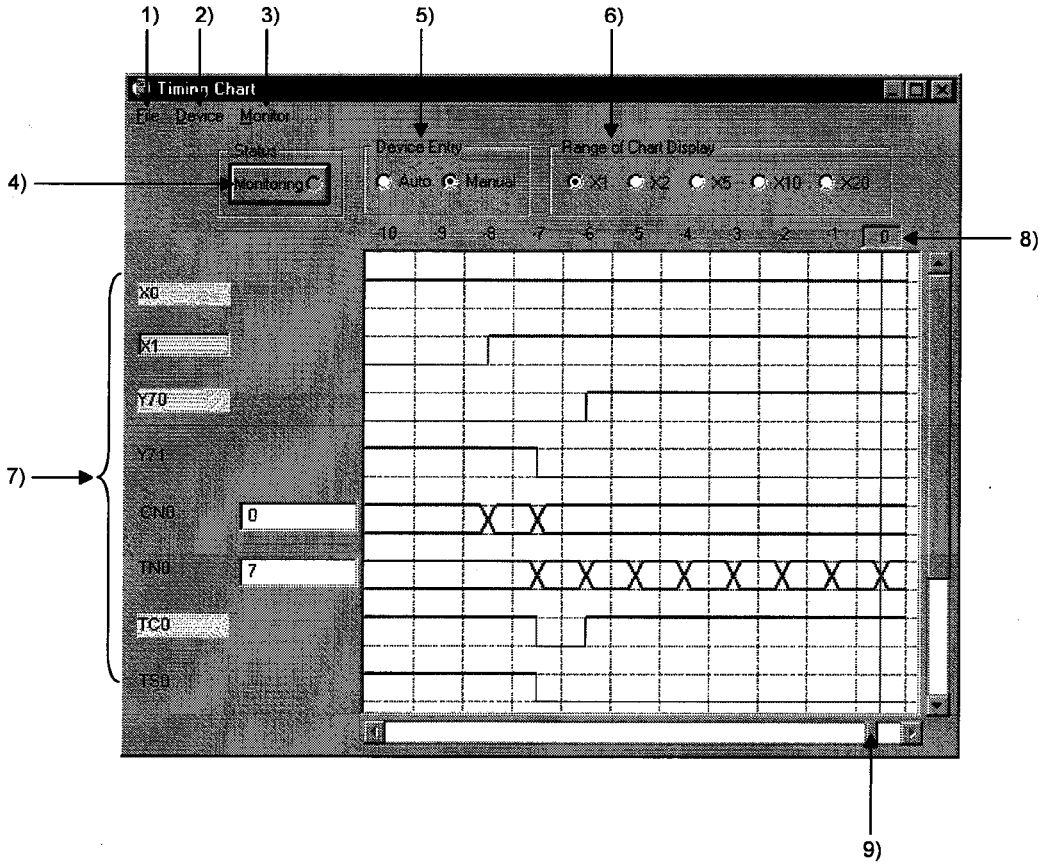
Select [Timing Chart] → [Run] in the device memory monitor window.
Maximum of four timing charts can be displayed.



[Setting Window]

POINT

For an example of timing chart usage, refer to Section 7.3 "Example of Timing Chart Display Usage".



1) File

Open File..... The device name which is going to be registered in the timing chart is read from a file.

Save File As..... Saves the device name registered in the timing chart in the file.

Exit..... Ends timing chart

2) Device

Enter Device..... Displays the dialogue for device registration. (It is capable of registering up to 64 items.)

Delete Device..... Deletes the selected device from the registration.

List Device..... Displays the dialogue of the list of devices.

Property..... Displays the dialogue for changing the display format of the selected word device.

3) Monitor

Start/Stop.....Execute starting and stopping of monitor.

Sampling Period.....Sets the interval for sampling the device values between a range of 1 to 20 scans.
<Example>
If this interval is set to 5 scans, device values are sampled by 5 scans and displayed in the timing chart display window. (Default setting is 1 scan.)

REMARK

If the setting of the sampling interval has been changed, the contents displayed on the timing chart are cleared.

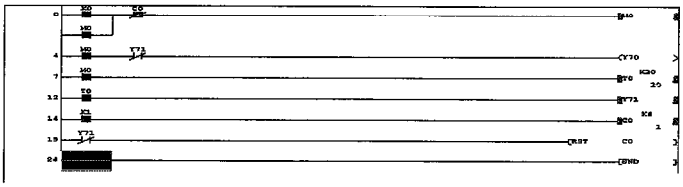
4) Status

Clicking the "Status" button will start or stop the monitor.

5) Device Entry

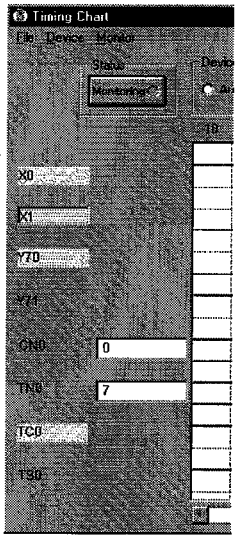
Auto ..... The device registered in the monitor using GPPW is automatically registered. (It is capable of registering up to 64 devices.)
When the monitor registration contents of GPPW have been changed, the device registration will be automatically updated.

<GPPW window>



The device being monitored on the GPPW window is displayed in the timing chart window.

<Timing chart window>



When adding a device to the registration in the timing chart window, switch the device registration setting to "Manual" after a message is displayed.

Manual..... Device is registered manually.

POINT

(1) Devices registered using GPPW are automatically displayed in the timing chart window.
If the timing chart window does not show these devices, switch the device registration setting from "Auto" to "Manual" and execute device registration.

(2) If the FX series CPU is selected, the following instructions displayed on the GPPW ladder monitor window will not be displayed in the timing chart. These instructions are:
(RST T, RST C,
PLS Y, PLS M,
PLF Y, PLF M)

6) Range of Chart Display

When the sampling interval is set to per scan, the chart display range is enlarged by 1, 2, 5, 10, and 20 times.

7) Device name/Device value

Bit device.....When a device is in ON status, the device name lights up. Clicking on the device name will highlight either ON and OFF of the device.

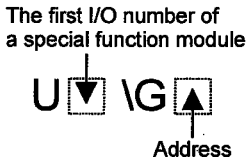
Word device .....Displays the device value in an edit box at the right side of the device name. Double clicking on the device value will edit the device value.

POINT

(1) The expressions in the timing chart are timer (T), counter (C), and retentive timer (ST), and each of them has three types; contact, coil, and current value. In the timing chart, they are expressed as follows.

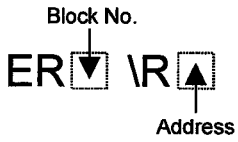
	Expressions used in the timing chart		
	Timer	Counter	Retentive timer
Contact	TS	CS	STS
Coil	TC	CC	STC
Current value	TN	CN	STN

(2) Buffer memory is displayed as follows.



When the first I/O number is 4 and the address is K30, they are displayed as "U4\G30".

(3) Extension file register is displayed as follows.



When the block No is 2 and the address is K30, they are displayed as "ER2\R30".

8) Base line/Scale

The displayed number on the scale indicates the scan number counted back from the current scan.

Clicking the scale moves the base line (vertical line) and displays the device values of the scan in item 7) of the "setting window".

9) Scroll bar

Past status of devices can be stored to the maximum of 1,000 samplings.

By scrolling the window using the scroll bar, the past status of the device can be checked.

[Device]

The device names that can be used (displayed) in the timing chart are shown below.

A Series CPU Functions, Motion Controller CPU Function		
Symbols Displayed on Window		Device Name
Bit device	X	Input
	Y	Output
	M	Internal relay
	F	Annunciator
	B	Link relay
	TS	Timer (contact)
	TC	Timer (coil)
	CS	Counter (contact)
	CC	Counter (coil)
	Sp.M	Special relay
Word device	TN	Timer (Current value)
	CN	Counter (Current value)
	D	Data register
	W	Link register
	Buffer Memory	Buffer memory
	R	File register
	ER	Extension file register
	Z	Index register
	V	
	A	Accumulator
	Sp.D	Special register

FX Series CPU Functions		
Symbols Displayed on Window		Device Name
Bit device	X	Input
	Y	Output
	M	Internal relay
	S	State
	TS	Timer (contact)
	TC	Timer (coil)
	CS	Counter (contact)
	CC	Counter (coil)
	Sp.M	Special relay
Word device	TN	Timer (Current value)
	CN	Counter (Current value)
	D	Data register
	Buffer Memory	Buffer memory
	Z	Index register
	V	
	Sp.D	Special register

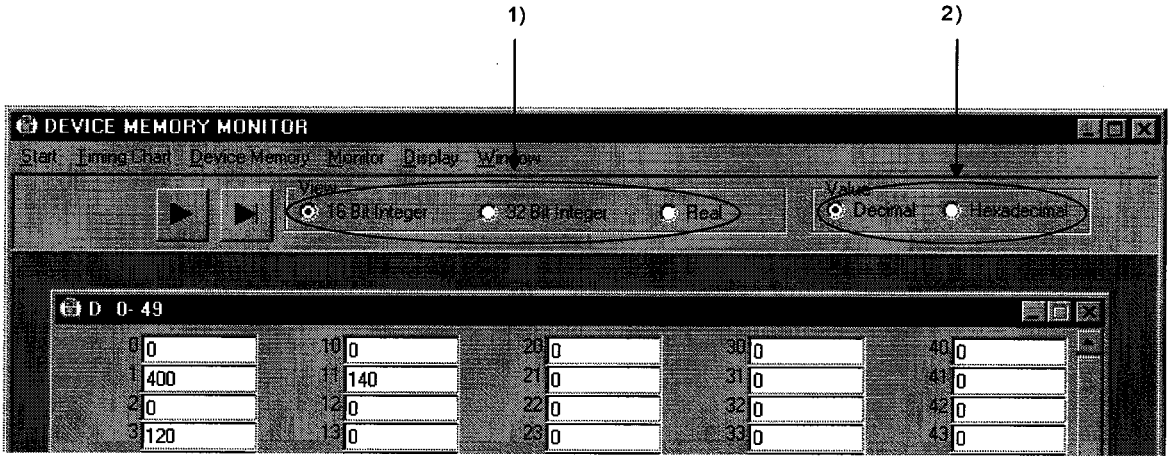
QnA Series CPU Functions		
Symbols Displayed on Window		Device Name
Bit device	X	Input
	Y	Output
	M	Internal relay
	L	Latch relay
	F	Annunciator
	V	Edge relay
	SB	Special link relay
	B	Link relay
	SM	Special relay
	TS	Timer (contact)
	TC	Timer (coil)
	STS	Retentive timer (contact)
	STC	Retentive timer (coil)
	CS	Counter (contact)
	CC	Counter (coil)
	FX	Function input
	FY	Function output
Word device	TN	Timer (Current value)
	STN	Retentive timer (Current value)
	CN	Counter (Current value)
	D	Data register
	W	Link register
	SW	Special link register
	SD	Special register
	R	File register
	ZR	Serial file register
	Z	Index register
	U	Buffer memory

5.2.3 Changing the device memory monitor format

[Purpose]

To switch the display format of the device monitor column to match the data contents.

[Setting Window]



[Description of the Settings]

1) View

Selects whether to display the values in the device monitor column in 16-bit units, 32-bit units, or as a floating decimal-point display when monitoring a word device.

The same operation is possible from the keyboard by pressing the F7 key.

16 Bit Integer ..... Displays the values in 16-bit units.

32 Bit Integer ..... Displays the values in 32-bit units.

Real ..... Displays the value as a floating decimal-point value (single-precision value).

2) Value

Selects whether to display the values in the device monitor column as a decimal or hexadecimal value when monitoring a word device.

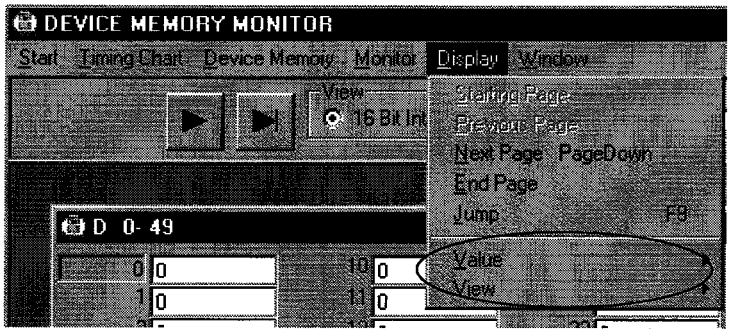
The same operation is possible from the keyboard by pressing the F8 key.

Decimal ..... Displays a decimal value.

Hexadecimal ..... Displays a hexadecimal value.

POINT

The device monitor format can also be changed by selecting the desired format from the drop-down menu of [Display] in the Device memory monitor window.



5.2.4 Running the device test

[Purpose]

To force bit devices ON/OFF or force changes to the present values of word devices while monitoring the devices.

[Operation Procedure]

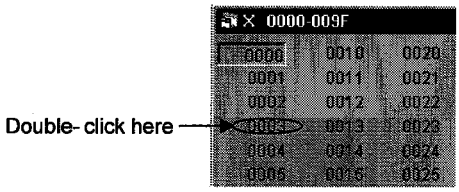
Select [Device Memory] then [Bit Device] or [Word Device] in the Device memory monitor window and select the devices to be monitored in the monitor test.

1. Forcing Bit Devices ON/OFF

   Double-click on the device number to be turned ON/OFF in the bit device monitor window.

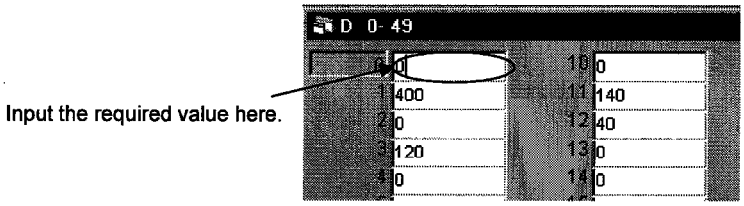
   Or, click on the device number to select it and press the F10 key.

   The ON/OFF status of the selected bit device is highlighted.



2. Changing Word Device's Current Values

   1) Move the cursor to the current value text box for the word device and directly input the required value.



   2) Press the Enter key to change the original present value to the designated value.

A device current value can be changed by the following method.

1) Double-click on the device number.
2) A numeric keypad is displayed. Input a new value and click on the [SET] button.

POINT
Always select the hexadecimal display for numeric values when inputting a hexadecimal using the numeric keypad. Note that character-string cannot be input.

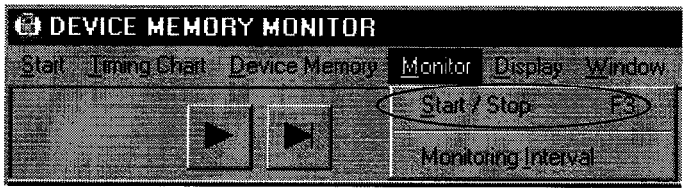
5.2.5 Stopping and restarting the device memory monitor

[Purpose]

To stop the device data changes and view the monitor window.

[Operation Procedure]

1. Select [Monitor] → [Start/Stop] (F3) in the Device memory monitor window while monitoring the device memory.



2. The device memory monitoring stops.
3. To restart the device memory monitoring, select [Monitor] → [Start/Stop] (F3) again.

POINT

The present monitor status is displayed in the guidance column below the device memory monitor window.

- During monitoring

- During monitor stopped

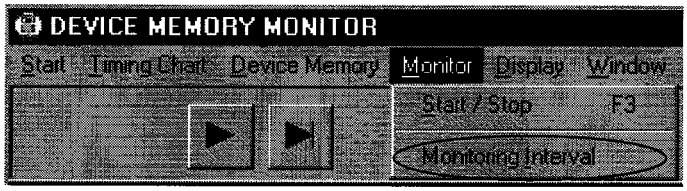
5.2.6 Changing the Monitor Communications Interval

[Purpose]

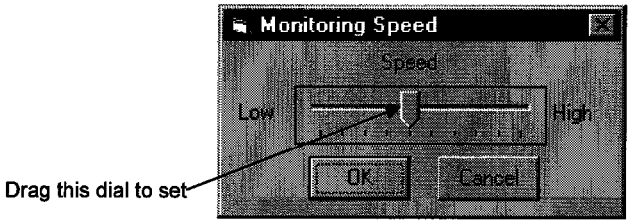
To set the interval at which the ladder logic test tool (LLT) device memory status is monitored.

[Operation Procedure]

1. Select [Monitor] → [Monitor Interval] in the Device memory monitor window.



2. The monitoring interval dialog box is displayed.
   Drag the dial in the dialog box to set the monitoring interval.
   Click on the [OK] button when the setting is complete.



MEMO

6. SAVING AND READING THE DEVICE AND BUFFER MEMORIES — TOOL FUNCTIONS

The tool functions are functions to save the contents of the device memory or special function unit buffer memory at any time and to read the saved data to the ladder logic test tool (LLT).
The tool functions allow the contents of the ladder logic test tool (LLT) device memory or special function unit buffer memory to be saved during debugging. The saved data can then be read to the ladder logic test tool (LLT) when debugging is repeated, to allow debugging to be continued from the status when the data was saved.

6.1 Saving the Device and Buffer Memories

[Purpose]

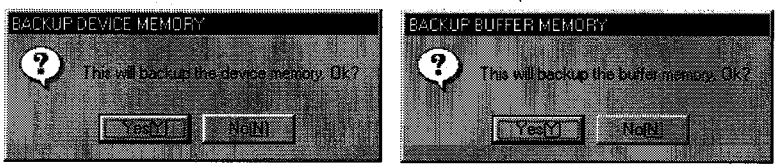
To temporarily save the contents of the device memory and buffer memory to allow debugging to continue after the personal computer is re-booted.

[Operation Procedure]

1. Set the execution status in the initial window to STOP when the device memory or buffer memory contents are to be saved.
   For the FX series CPU function, turn ON special relay M8033 to retain the device memory even if the execution status is STOP.

2. Select [Tools] → [Backup device memory] or [Backup buffer memory].

[Setting Window]



Click on the [Yes] button, to save the entire device memory or the buffer memory for the slots allocated to special function units in the I/O assignment settings.
The buffer memory data is saved to the following directories:

- A Series CPU Functions
  (Directory where the ladder logic test tool (LLT) are installed) \Acpu\Devmem
- QnA Series CPU Functions
  (Directory where the ladder logic test tool (LLT) are installed) \QnAcpu\Devmem
- FX Series CPU Functions
  (Directory where the ladder logic test tool (LLT) are installed) \FXcpu\Devmem
- Motion controller CPU Functions
  (Directories where the ladder logic test tool (LLT) are installed)\Acpu\Devmem

[Example]

If C:\Melsec\LLT is designated as the directory where the ladder logic test tool (LLT) are installed, then the buffer memory data is saved to the following directories:

A Series CPU Functions	C:\Melsec\LLT\Acpu\Devmem
QnA Series CPU Functions	C:\Melsec\LLT\QnAcpu\Devmem
FX Series CPU Functions	C:\Melsec\LLT\FXcpu\Devmem
Motion controller CPU Functions	C:\Melsec\LLT\Acpu\Devmem

POINT

(1) If the execution status is RUN, device memory/buffer memory cannot be saved.
To save the device memory/buffer memory, change the status to STOP.

(2) The ladder logic test tool (LLT) can save only one file.
If data already exists in the ladder logic test tool (LLT), the new file overwrites the existing data (file).

6.2 Reading Saved Device Memory or Buffer Memory Data

[Purpose]

To read the stored data of device memory and buffer memory.

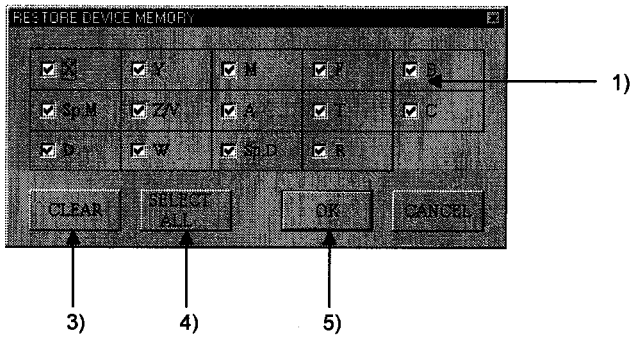
[Operation Procedure]

Set the execution status in the initial window to STOP. Select [Tools] → [Restore device memory] or [Restore buffer memory].

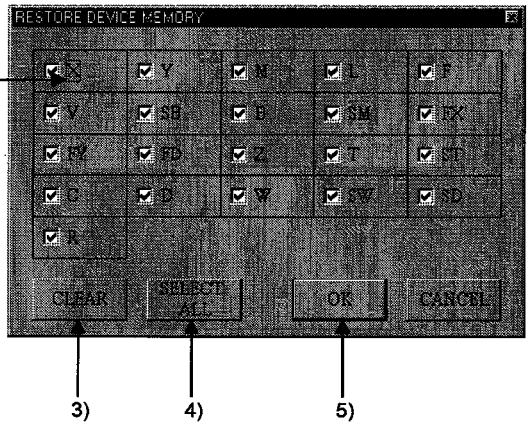
[Setting Window]

Reading device memory

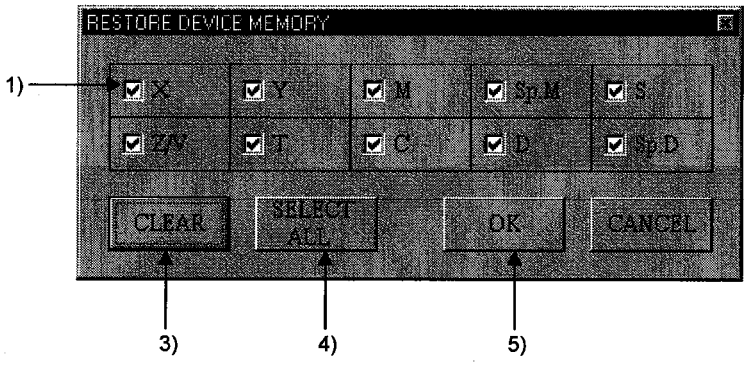
<A Series CPU and Motion controller CPU>



< QnA Series CPU >

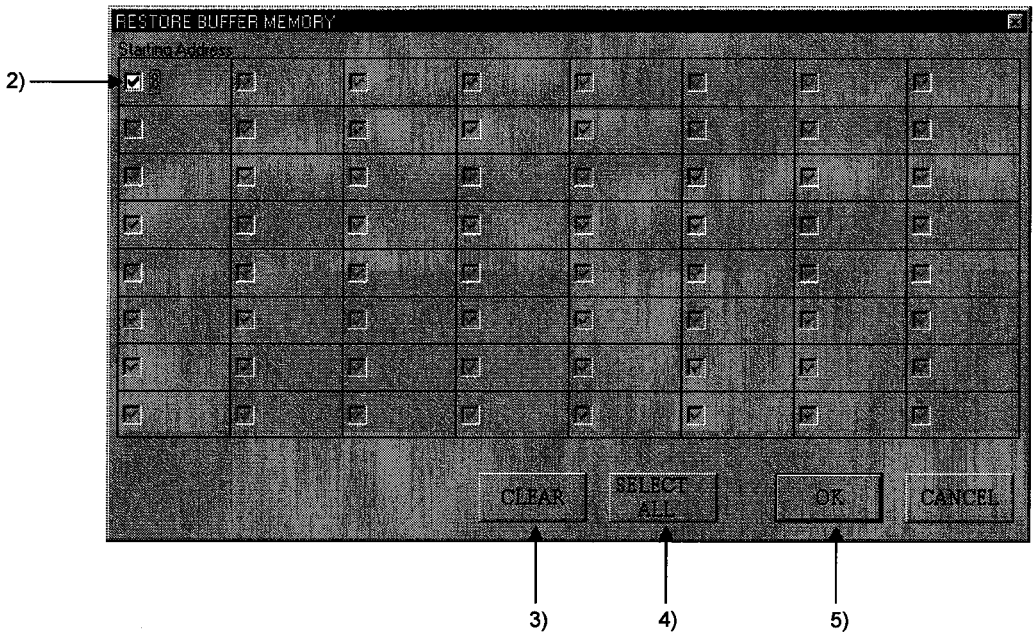


<FX Series CPU>

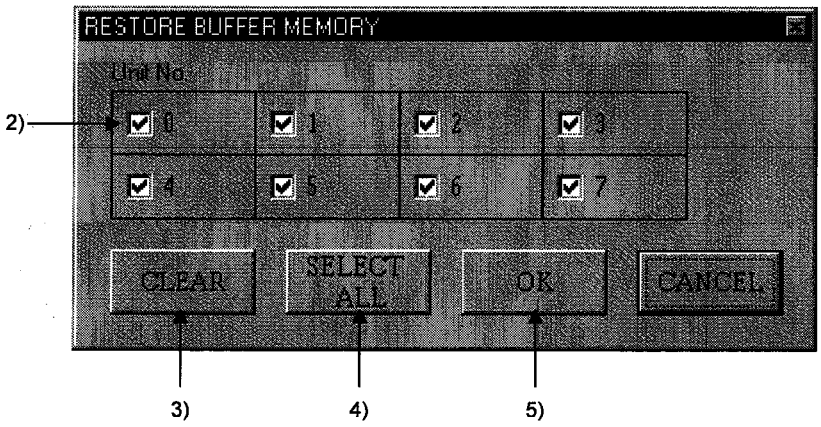


Reading buffer memory

<A Series CPU QnA Series CPU and Motion controller CPU >



<FX Series CPU>



[Description]

1) Read Device Check Boxes

Click in the check boxes to select the devices read to ladder logic test tool (LLT).
Click on a check box again to cancel a selection.
All devices are selected by default.

2) Read Special Function Module Check Boxes

For A Series QnA Series or Motion controller CPU functions, the special function module first I/O number is displayed at the top of the window.
The special function module block number or module block number is displayed at the top of the FX Series window.
Click the check box to select the special function module to be read to the ladder logic test tool (LLT).
Click on a check box again to cancel a selection.
All special function modules are selected by default.
Only the special function module buffer memory can be read.

3) [CLEAR] button

Click to clear all device or special function module selections.

4) [SELECT ALL] button

Click to select all devices or special function modules.

5) [OK] button

Click this button after completing all settings.

POINT
(1) Device memory/buffer memory read is not allowed while the execution status is RUN. Change the execution status to STOP before reading device memory/buffer memory. (2) With the A series, QnA series CPU functions, selection of a slot that is not assigned to a special function module using the GPPW I/O assignment setting is not possible. Before reading buffer memory, set the GPPW I/O assignment.

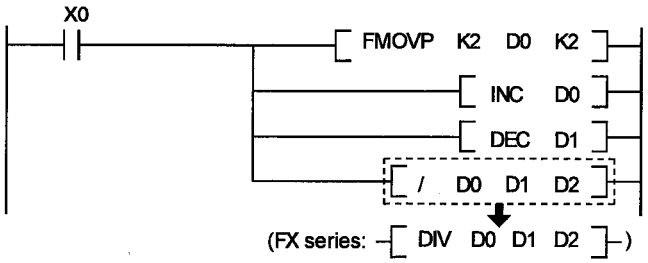
MEMO

7. EXAMPLES OF LADDER LOGIC TEST TOOL (LLT) APPLICATIONS

This section gives an example of debugging an actual program using the ladder logic test tool (LLT).

7.1 Debugging Using GPPW Step Execution Function

Using GPPW alone, it is not possible to turn arbitrary devices ON/OFF or to change device values during step execution. However, using the ladder logic test tool (LLT) allows the device values to be easily changed during step execution.
This section uses the following program to give an example of debugging using step execution.
An "OPERATION ERROR" occurs due to division by zero if the following program example is executed and X0 turns ON.
Step execution can be used to determine in which step the error occurs.



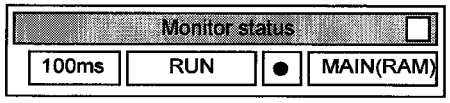
* Some instructions differ between the A/ QnA series and the FX series CPU. For details, refer to the Programming Manual of the individual CPUs.

(1) Debugging Procedure

1) Start up GPPW and create the program above.

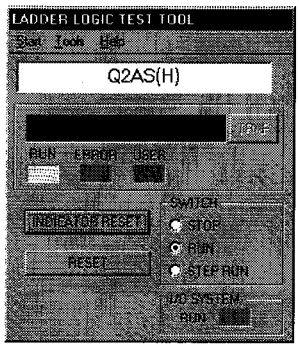
2) Select GPPW [Tools] → [Start ladder logic test] to start the ladder logic test tool (LLT).

3) Select GPPW [Online] → [Monitor] → [Monitor mode] to start monitoring.



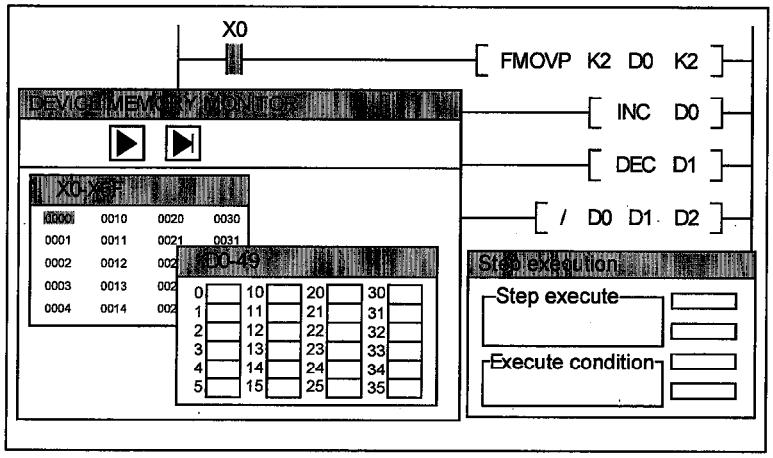
4) Open the device window (X, D) to monitor in the device memory monitor window. Change the size and position of the window, if required.

5) Set the ladder logic test tool (LLT) execution status display to STEP-RUN.



6) Move the cursor to the step execution starting position (step #0).

7) Select GPPW [Online] → [Debug] → [Step execution] to display the Step Execution dialog box.
Click on the task bar at the bottom of the window to activate the device memory monitor window.



8) Double-click on X0 in the DEVICE MEMORY MONITOR window and force X0 ON to run the program above.
One instruction is executed each time the [Step execute] button in the Step execution dialog box is clicked.

9) Repeatedly click the [Step execute] button to execute the program one instruction at a time. An "OPERATION ERROR" occurs when [/ D0 D1 D2] (or [DIV D0 D1 D2] for the FX Series) is executed during the second scan.

REMARK

The number of repeats can be set by clicking the [Option setup] button in the Step execution dialog box.
If a number of repeats is set, skip execution is speeded up because the set number of instructions is automatically executed on each click.

7.2 A/QnA Series Special Function Module Program Debugging Example

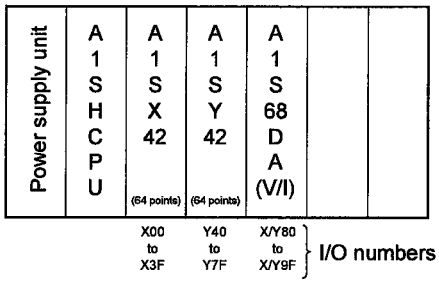
This section shows the procedure for debugging a special function module program that uses the ladder logic test tool (LLT). In the system in this example, the special function module is a digital/analog conversion module (hereafter D/A conversion module).

<Conditions of Example Program>

The values set in the BCD digital switches (X30 to X3F) are written to the digital value setting area (buffer memory address 1) in the D/A conversion module. If an error occurs in the digital values, the error code is read from the error code storage area (buffer memory address 10) to D1.
The procedure to debug this program is described below.

(1) System Configuration Example

Debugging is conducted with no actual PLC connected, assuming the following system configuration.



(2) D/A Conversion Module I/O Signals

(a) Error flag.....X82

(3) Devices Used by the User

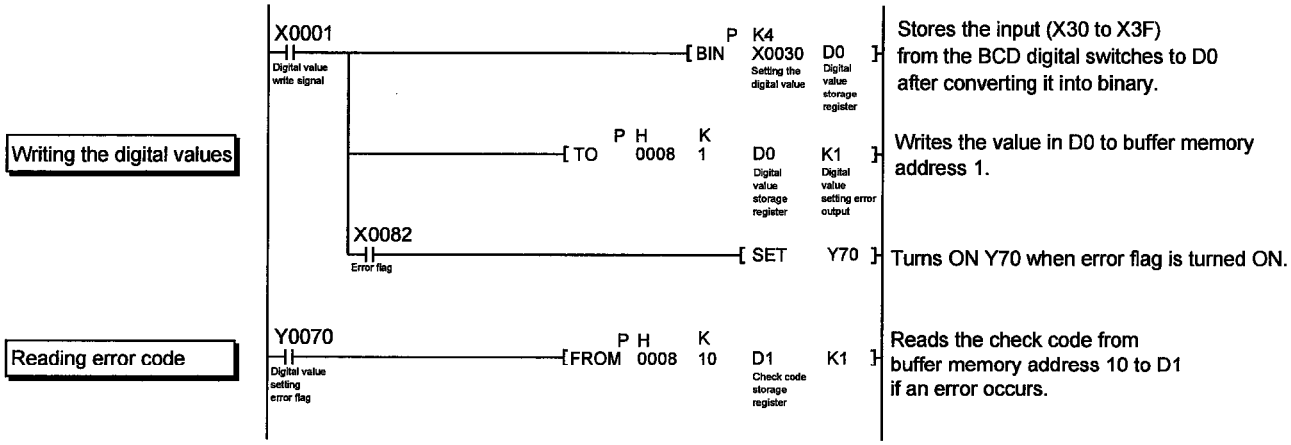
(a) Digital value write signal.....X1

(b) Digital value setting (4-digit BCD).....X30 to X3F

(c) Digital value storage register.....D0

(d) Error code storage register.....D1

(e) Digital value setting error output.....Y70



(4) Debugging Procedure

The procedure for debugging the program above is described below.

<Operations Before Debugging>

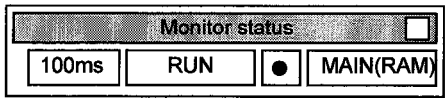
1) Start GPPW and create the program described above.

2) Select GPPW [PLC parameter] menu and click on the [I/O assignment] tab. Make I/O assignment as follows.

	Slot	Type	Model	Points
0	0(0-0)	Input	A1SX42	64 point
1	0(0-1)	Output	A1SY42	64 point
2	0(0-2)	Special	A1S68DA	32 point

3) Select GPPW [Tools] → [Start ladder logic test] to start the ladder ladder logic test tool (LLT).

4) Select GPPW [Online] → [Monitor] → [Monitor mode] to start monitoring.



<Digital Value Write Check>

5) Set the digital values to be written to the digital value setting area (buffer memory address 1) in the D/A conversion module.

The digital value settings use the BCD digital switches (X30 to X3F).
Force X30 to X3F ON/OFF to set the digital values.
Force the devices ON/OFF using the ladder logic test tool (LLT) Device Memory Monitor window.

To set digital value "55", force on X as shown to the right.

X 0030-00CF

0030	0040	0050	0060	0070	0080
0031	0041	0051	0061	0071	0081
0032	0042	0052	0062	0072	0082
0033	0043	0053	0063	0073	0083
0034	0044	0054	0064	0074	0084
0035	0045	0055	0065	0075	0085
0036	0046	0056	0066	0076	0086
0037	0047	0057	0067	0077	0087

6) Force ON X1 (digital value write signal) to write the set digital values to the D/A conversion module buffer memory.

Check the digital values are written by using the device memory monitor to monitor buffer memory address 1 in the D/A conversion module.
Enter the module starting address value as "8".

Digital value "55" is written.

Buffer Memory 0 49 (Starting Address 8)

0	0	10	0	20	0
1	55	11	0	21	0
2	0	12	0	22	0
3	0	13	0	23	0
4	0	14	0	24	0
5	0	15	0	25	0
6	0	16	0	26	0
7	0	17	0	27	0

<Error Code Read Check>

7) To simulate a D/A conversion module error, pre-write the error code to buffer memory address 10 by changing the device present value.

Write error code "100" by changing the present value.

Buffer Memory 0-49 (Starting Address 8)

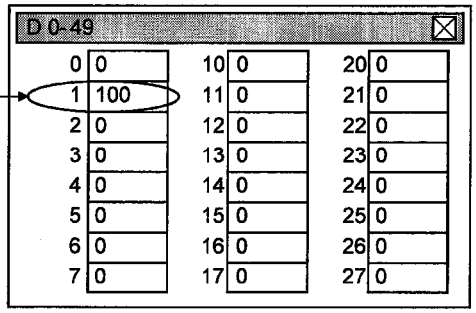
0	0	10	100	20	0
1	55	11	0	21	0
2	0	12	0	22	0
3	0	13	0	23	0
4	0	14	0	24	0
5	0	15	0	25	0
6	0	16	0	26	0
7	0	17	0	27	0

8) Force ON X82 (error flag) in the D/A conversion module.

9) When X82 is forced ON, Y70 (digital value setting error output) turns ON and the error code is written from the buffer memory address 10 to D1.

Check the error code is written by using the device memory monitor to monitor D1.

Error code "100" is read to D1



7.3 Example of Timing Chart Display Usage

This section explains an operation method of the timing chart that displays the device chart by using the ladder logic test tool (LLT).

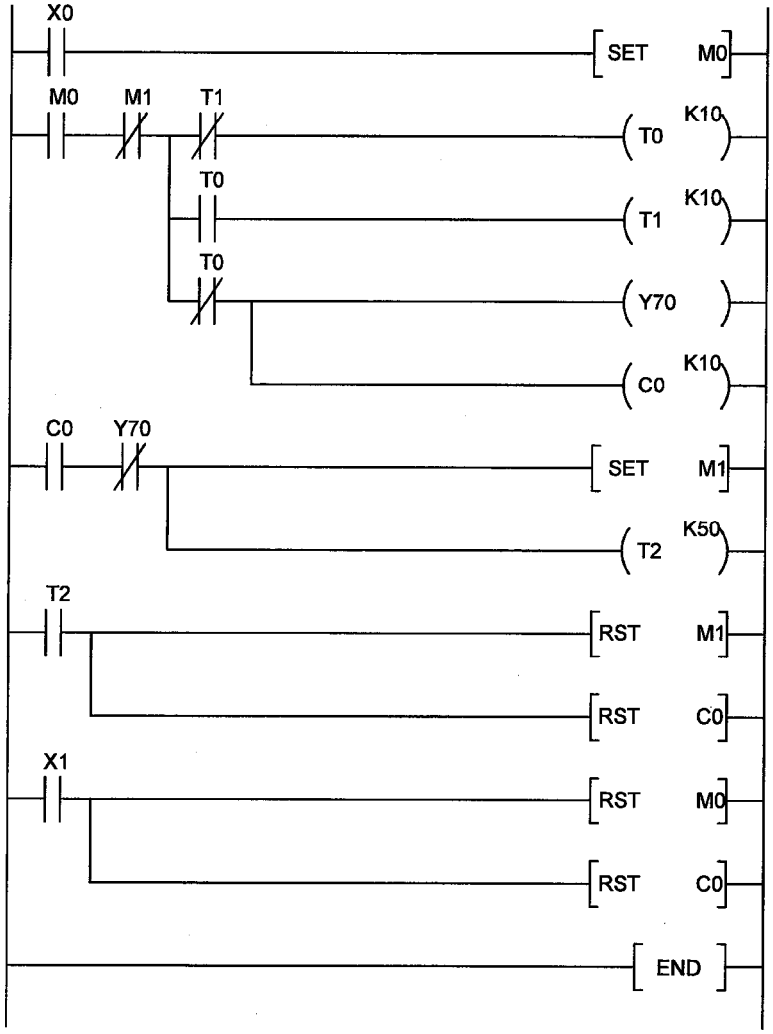
Program example

When X0 turns ON, Y70 will start flickering in 1 second intervals. After Y70 flickers 10 times, it stops for 5 seconds, then starts flickering again. Also, when X1 turns ON, Y70 stops flickering.
An example of a timing chart display usage for this program is shown below.

(1) A display method of the timing chart

(a) Creating program

Start up GPPW and create the program below.

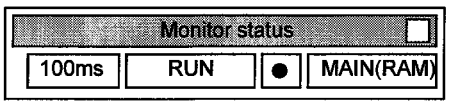


(b) Starting up the ladder logic test tool (LLT) functions

Select GPPW [Tools] → [Start ladder logic test] to start the ladder logic test tool functions (LLT).

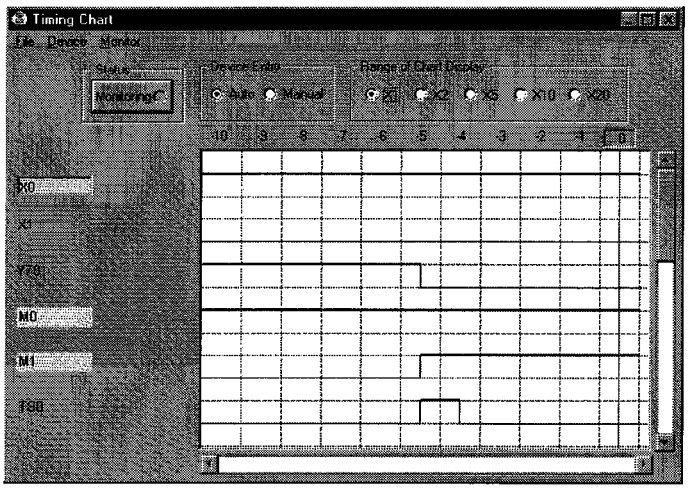
(c) Executing ladder monitor by GPPW

Select [Online] → [Monitor] → [Monitor mode] of GPPW to start monitoring.



(d) Displaying the timing chart

The timing chart window is displayed as shown below by performing operations (a) through (c).



For the starting method of the timing chart, refer to 5.2.2 "Displaying the Timing chart of Devices".

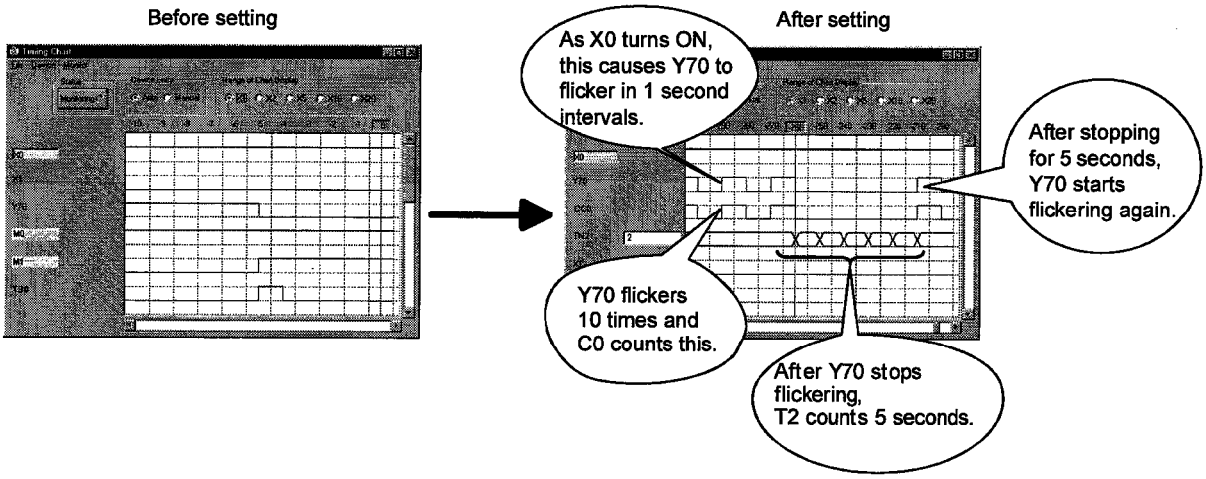
POINT

(1) Devices registered using GPPW are automatically displayed in the timing chart window.
If the timing chart window does not show these devices, switch the device registration setting from "Auto" to "Manual" and execute device registration.

(2) If an FX series CPU is selected, the following instructions displayed on the GPPW ladder monitor window will not be displayed in the timing chart. These instructions are:
(RST T, RST C,
PLS Y, PLS M,
PLF Y, PLF M)

Example of Timing chart display

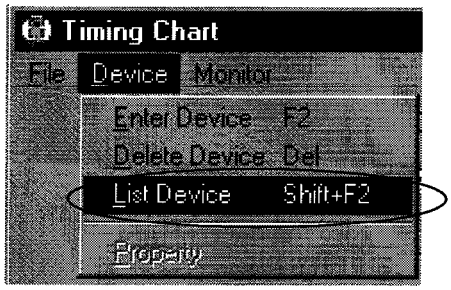
(1) Set the timing chart displayed in (d) by following the procedure used in examples (2) through (5), then check the operation of the program created in (1) by referring to the description in the illustrations below.



(2) Example of timing chart usage (Device registration)

(a) Batch deletion of registration device names

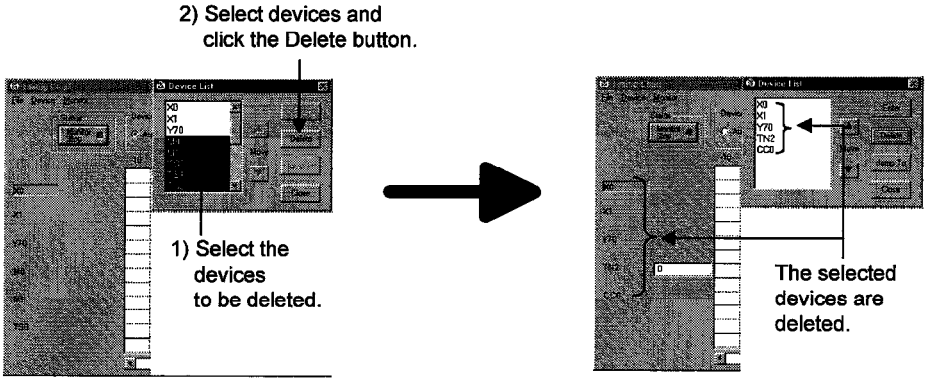
1) Select [Device] → [List Device] in the Timing chart window to display the device list window.



2) Make a setting so that only X0, X1, Y70, TN2, and CC0 are displayed.

Select several device names and click the delete button. The selected device names will be deleted.

Use the key combinations "Shift + Select" or "Ctrl + Select" to select the devices.



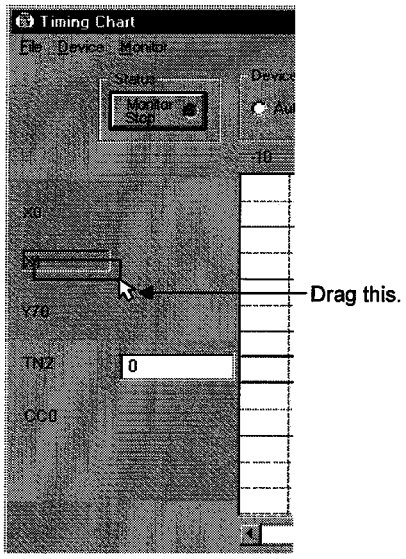
By performing the processes above, X0, X1, Y70, TN2, CC0 are exclusively displayed in the timing chart window.

(3) Example of timing chart usage <Sorting device names>

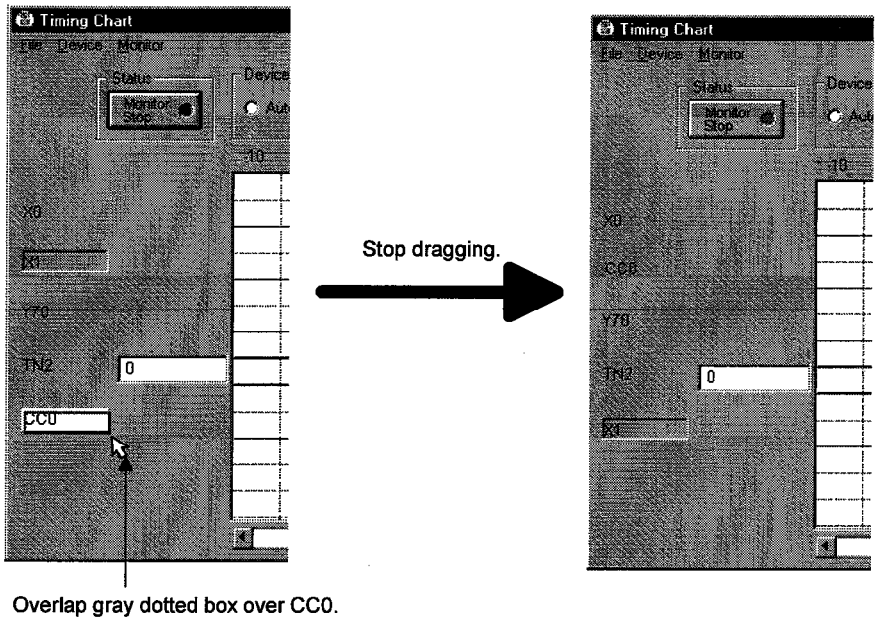
(a) Sorting device names in the timing chart window

1) Switch the positions of X1 and CC0.

Drag the device name (X1). When the device name is dragged, a gray dotted box is displayed.



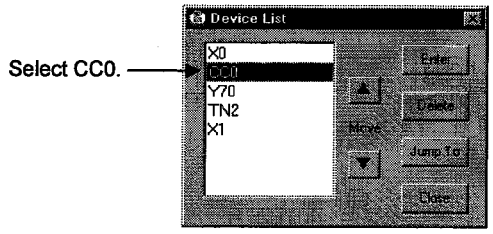
2) The device names can be switched by moving the gray dotted box over the device name (CC0) that is to be replaced.



(b) Sorting in the device list window

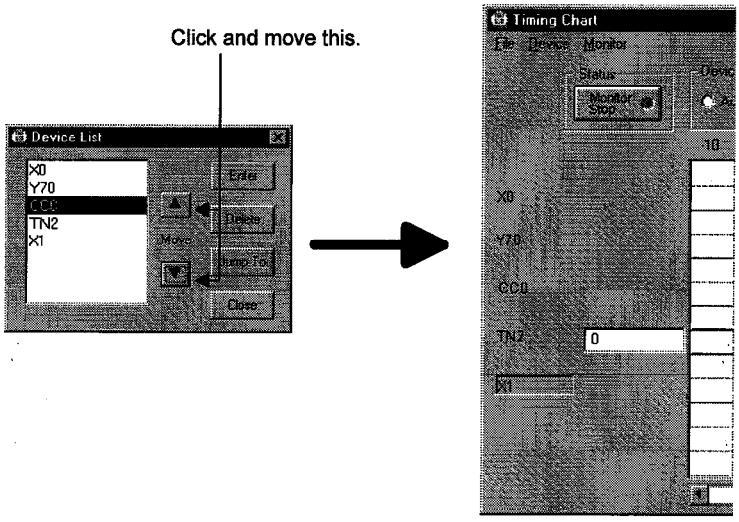
1) Display CC0 in the position between Y70 and TN2.

Select the device name to be moved.



2) Click the "Move" button and move the selected device name (CC0).

When it is moved, the displayed position of the device name (CC0) in the timing chart window changes.



(4) Example of timing chart usage <Changing sampling interval>

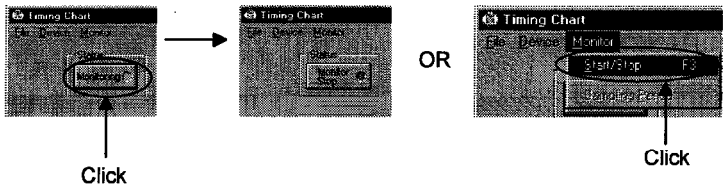
The scale displayed on the horizontal axis of the timing chart window displays a value obtained by the formula below:

(Scale) = (Sampling interval) × (Range of Chart Display)

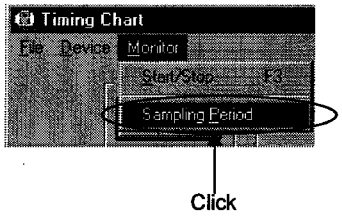
Set the sampling interval to "10 scans" so that the timing chart window becomes easy to read.

In the program created in (1), it is programmed for Y70 flickers in a 1 second interval. Thus, if the sampling interval is set to 1 second, in other words if one sampling is performed every 10 scans, ON and OFF of Y70 can be displayed alternately by a single scale in the timing chart.

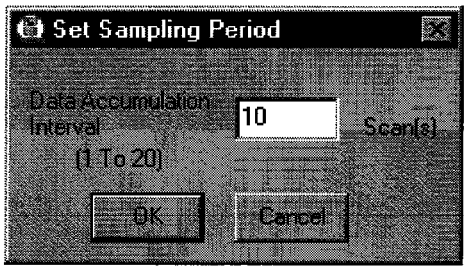
1) Stops the monitoring status of the timing chart.
To stop the monitoring status, click "Status" in the timing chart, or select [Monitor] → [Start/Stop].



2) To display set sampling period window, select [Monitor] [Sampling Period] of the timing chart window.

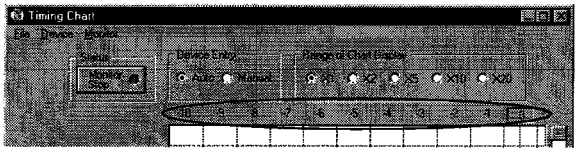


3) Set the data collecting interval to 10 scans and click the "OK" button.

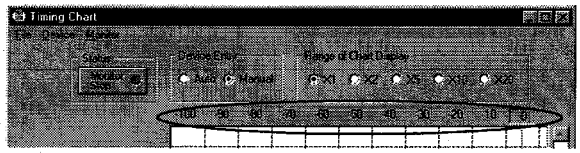


4) Following procedures 1) to 3) sets the scale to a 10 scan interval.

<Before setting>



<After setting>



REMARK

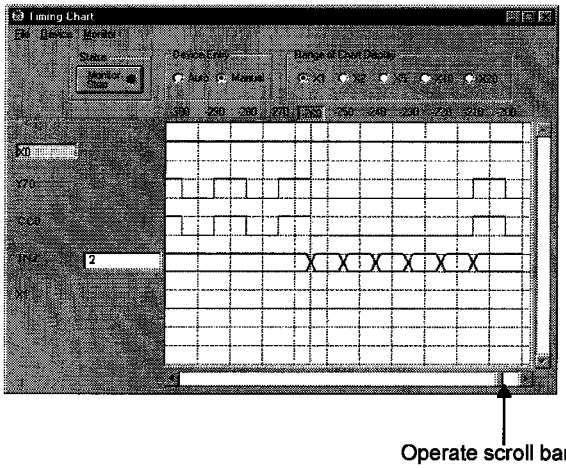
If the setting of sampling intervals has been changed, the contents displayed on the timing chart are cleared.

(5) Example of timing chart usage <Check the change in the status of devices being monitored>

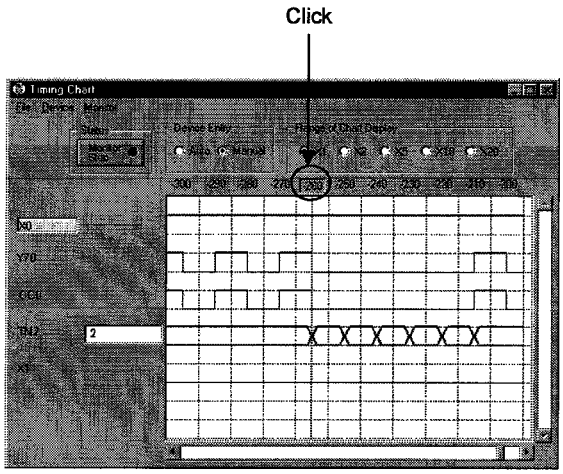
Up to 1,000 samplings of the past status of devices are stored in the ladder logic test tool functions (LLT).

The following example shows how to check the device status at the 260th scan prior to the current scan.

1) Stop monitor status in the timing chart.
   For the procedure, refer to (a) 1) of "Changing the sampling interval".
2) Operate the scroll bar to display the number "-260" in the timing chart window.

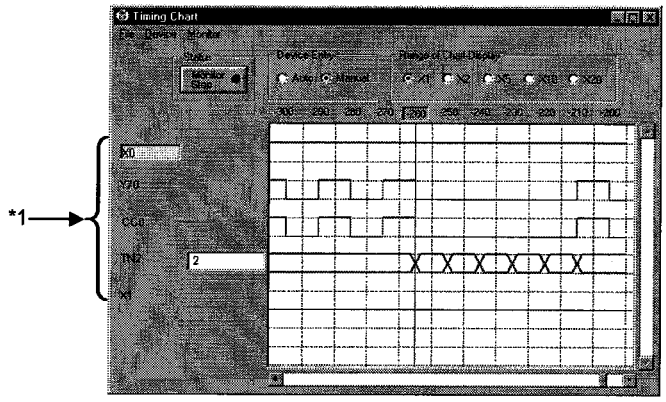


3) Click on "-260" displayed on the horizontal axis in the timing chart window.



4) Procedure 3 displays the device status at the 260th scan prior to the current scan in the parenthesis *1.

In the parenthesis *1 the ON/OFF status of a bit device and the change in the value of a word device are displayed.



If Y70 turns ON and C0 turns OFF, this indicates that T2 starts the count.

MEMO

8. TROUBLESHOOTING

8.1 Error Messages Displayed on the LED Indicators

This section describes error messages and error codes occurring in the ladder logic test tool (LLT), gives a description and cause of the error, and suggests remedies.

(1) Ladder Logic Test Tool (LLT) for A Series CPU Functions

Error Message Table

Error Message	Error Code (D9008) *1	Details Error Code (D9091) *1	Error Description and Cause	Remedy
"INSTRCT CODE ERR." (Checked at RUN → STOP or at the execution of an instruction)	10	101	The program contains an instruction code which could not be decoded by the ladder logic test tool (LLT).	Read the error step using GPPW and modify the program step.
		102	Index qualification used for a 32-bit constant.	
		103	The device specified in the dedicated instruction is incorrect.	
		104	The program structure of the dedicated instruction is incorrect.	
		105	The command name of the dedicated instruction is incorrect.	
		107	(1) The index qualification used for the device number and SV in timer or counter OUT instructions. (2) The index qualification used for the label number of the pointer (P) added at the start of an instruction jump destination or for the label number of the interrupt pointer (I) added at the start of an interrupt program for the following instructions. CJ SCJ CALL JMP LEDA/B FCALL LEDA/B BREAK	
"MISSING END INS." (Checked at RUN → STOP)	12	121	There is no END (FEND) instruction in the main program.	Write END in the end of main program.
		122	A sub program has been allocated in the parameters and there is no END (FEND) instruction.	Write END in the end of the sub-program.
"CAN'T EXECUTE(P)" (Checked at the execution of the instruction)	13	131	The device number of the pointer (P) or the interrupt pointer (I) used as a label added to the destination head is duplicating.	Remove the duplicated number of pointer (P) with the destination head and correct so that the number is not duplicated.
		132	The label of the pointer (P) specified by CJ SCJ CALL CALLP JMP LEDA/B FCALL and LEDA/B BREAK instructions is not specified prior to the END instruction.	Read the error step using GPPW, check the step and insert the destination pointer (P).

Error Message Table (cont.)

Error Message	Error Code (D9008) *1	Details Error Code (D9091) *1	Error Description and Cause	Remedy
"CAN'T EXECUTE(P)" (Checked at the execution of the instruction)	13	133	(1) There is no CALL instruction for the RET instruction in the program. (2) There is no FOR instruction for the NEXT, LEDA/B BREAK instructions in the program. (3) The nesting level of CALL, CALLP, or FOR exceeds the nesting limit six (6) and is executing the sixth level. (4) There is no RET or NEXT instructions for the CALL or FOR instruction.	(1) Read the error step using GPPW. Check and modify the program step. (2) Nesting level for the CALL, CALLP and FOR instructions must be five (5) or less.
		134	There is no parameter settings for the sub program. Can not execute the CHG instruction.	Read the error step using GPPW. Delete the line containing the CHG instruction.
		136	There is no parameter settings for sub program 1. Can not execute the ZCHG1 instruction.	Read the error step using GPPW. Delete the line containing the ZCHG1 instruction.
		137	There is no parameter settings for sub program 2. Can not execute the ZCHG2 instruction.	Read the error step using GPPW. Delete the line containing the ZCHG2 instruction.
		138	There is no parameter settings for sub program 3. Can not execute the ZCHG3 instruction.	Read the error step using GPPW. Delete the line containing the ZCHG3 instruction.
"WDT ERROR" (Checked at the execution of the sequence program.)	22	220	A program instruction is executed infinitely in a single scan.	Read the error step and confirm there is no occurrence of an infinite loop.
"END NOT EXECUTE" (Checked at the execution of the instruction.)	24	241	The entire program has been executed without executing the END instruction. (1) There is no END instruction. (2) The END instruction is replaced with some other instruction.	Please write the program to PLC again.
"SP.UNIT ERROR" (Checked at the execution of the FROM/TO instruction or special function module dedicated instruction.)	46	461	There is no special function module in the area specified by the FROM/TO instruction.	(1) Read the error step using GPPW. Check and modify the FROM/TO instruction in the program step. (2) Correct the I/O unit allocation parameter settings.

Error Message Table (cont.)

Error Message	Error Code (D9008) *1	Details Error Code (D9091) *1	Error Description and Cause	Remedy
"OPERATION ERROR" (Checked at the execution of the instruction)	50	501	(1) Operations using the file register (R), are executed with the device number or block number exceeding the range specified for the file register (R). (2) The file register is used in the program without setting necessary parameters for the file register (R).	(1) Read the error step using GPPW. Check and modify the program step. (2) Set the parameters for the file register (R).
		502	The combination of devices specified by instruction is incorrect.	Read the error step using GPPW. Check and modify the program step.
		503	The storage data or constants are not within the usable range.	
		504	The number of data handling settings exceeds the usable range.	

*1 Characters in parentheses ( ) indicate the special register number where the information is saved.

(2) Ladder Logic Test Tool (LLT) for QnA Series CPU

Error Message Table

Error Message	Error Code (SD0) *1	Error Description and Cause	Remedy
END NOT EXECUTE	1010	The entire program has been executed without executing the END instruction. (1) There is no END instruction. (2) The END instruction is replaced with some other instruction.	Please write the program to PLC again.
	1011		
	1012		
SP.UNIT ERROR	2110	There is no special function module in the area specified by the FROM/TO instruction.	(1) Read the error step and correct the contents of the FROM/TO instruction. (2) Correct the I/O unit parameter settings.
	2111	There is no network function module in the area specified by the link direct device (J#\#).	Check and modify the FROM/TO instruction in the program step.
	2112	There is no network function module or the unit in the area specified is not supporting the instruction.	Check and modify the special function unit dedicated instruction in the error step of the program.
	2113	There is no simulation data for the special function unit simulation.	
MISSING PARA.	2200	Parameter file is missing.	Please write the parameter again.
FILE SET ERROR	2400	The file specified in the parameter settings is not available.	(1) Please delete the file name from the parameter settings. (2) Make a file as specified in the parameter settings.
FILE OPE.ERROR	2410	The file specified in the sequence program is not available.	(1) Check and modify the specified file name. (2) Create the specified file.
CAN'T EXE.PRG.	2500	A program file exists with a device which exceeds the device range specified in the device parameter settings.	Read common information of error using GPPW. Check and correct the device by comparing device allocation parameter settings.
	2501	Multiple program files exist. But, the program settings parameter is set to "None".	Change the parameter settings to "Present" or delete unnecessary programs.
	2502	The program is incompatible with QnA CPU or the file content is not a sequence program.	Please write the program again.
	2503	No program files exist.	Please check the program configuration.
	2504	Two or more Ordinary/Control SFC programs were executed.	Please check the parameter and program configuration.
PARAMETER ERROR	3001	Parameter data is corrupted.	Please write the parameter again.
INSTRCT CODE ERR.	4000	The program contains an instruction code which cannot be decoded by the CPU.	Please write the program again.
MISSING END INS.	4010	The program contains no "END (FEND)" instruction.	Please check and correct the program.
CAN'T SET(P)	4020	The total number of pointers used in the program files exceeds the maximum allowable number defined in the parameter settings.	Check the error step and correct the program.
	4021	Overlapping of common pointers exist.	

Error Message Table (cont.)

Error Message	Error Code (SD0) *1	Error Description and Cause	Remedy
OPERATION ERROR	4100	An instruction contains data that cannot be processed.	Check the error step and correct the program.
	4101	The instruction data exceeds the allowable number of data handled. Or the storage data constants specified in the instruction exceeds the usable range.	
	4102	Incorrect network number or station number is specified in a network dedicated instruction.	
	4103	Illegal configuration of PID dedicated instruction.	
FOR NEXT ERROR	4200	A FOR instruction is executed without NEXT instruction. Or the number of NEXT instructions is lower than the number of FOR instruction.	Check the error step and correct the program.
	4201	A NEXT instruction is executed without a FOR instruction. Or the number of NEXT instructions is greater than the number of FOR instructions.	
	4202	The nesting exceeds 16 loops.	Reduce nesting count to 16 or less loops.
	4203	A BREAK instruction is executed when there is no FOR instruction.	Check the error step and correct the program.
CAN'T EXECUTE (P)	4210	A CALL instruction is executed without a destination pointer.	Check the error step and correct the program.
	4211	The executed subroutine program contains no RET instruction.	
	4212	A RET instruction is existing before the FEND instruction.	
	4213	The nesting exceeds 16 loops.	Reduce nesting count to 16 or less loops.
INST. FORMAT ERROR	4230	Mismatch in the number of CHK and CHKEND instructions.	Check the error step and correct the program.
	4231	Mismatch in the number of IX and IXEND instructions.	
	4232	The structure of FOR - NEXT instructions is incorrect.	
	4233	The structure of DO - WHILE instructions is incorrect.	
	4234	The structure of SELECT- CASE instructions is incorrect.	
	4235	The check condition for the CHK instruction is incorrect.	
	4236	The nesting exceeds 16 loops.	Reduce nesting to 16 or less loops.
	4237	An EXITFOR instruction is executed when there is existence of FOR instruction.	Check the error step and correct the program.
	4238	An EXITDO instruction is executed when there is no existence of DO instruction.	

Error Message Table (cont.)

Error Message	Error Code (SD0) *1	Error Description and Cause	Remedy
WDT ERROR	5000	An instruction in a program of initial execution type is infinitely executed in a single scan.	Read the error step and confirm there is no occurrence of an infinite loop.
	5001	An instruction in the program is infinitely executed in a single scan.	Read the error step and confirm there is no occurrence of an infinite loop.
F***	9000	Annunciator is turned ON by the program.	Check the user condition that turns On the annunciator and make corrective action for that condition.

*1 Characters in parentheses ( ) indicate the special register number where the information is saved.

(3) Ladder Logic Test Tool (LLT) for FX Series CPU Functions

Error Message Table

Error Message	Error Code (D8065, D8066) *1	Error Description and Cause	Remedy
WDT ERROR	6105	Occurrence of an infinite loop.	Check the program or contents of the operands in the application instruction.
FILE NOT FOUND	6409	Illegal parameter settings.	Correct the parameter settings and write parameters again.
INVALID CODE ERROR	6503	Data instruction code is corrupted.	Transfer the program from GPPW again.
EXIST SAME LABEL No.	6504	Overlapping label numbers.	Check the program and correct the overlapping label numbers.
STL-MC INST.ERROR	6505	(1) There is no RET instruction. (2) MC and MCR instructions are designated within an STL state.	Check the program and correct the mutual instructions.
FOR NEXT ERROR	6607	Illegal occurrence of FOR to NEXT instructions. FOR to NEXT nesting exceeds the maximum nesting level of 6.	Check the program or contents of the operands in the application instruction.
OPERATION ERROR	6701	No jump destination is specified for CJ or CALL instruction.	Check the program or contents of the operands in the application instruction.
CAN'T EXECUTE (P)	6702	The nestings of CALL instructions exceed the maximum nesting level of 6.	Check the program or contents of the operands in the application instruction.
FOR NEXT ERROR	6704	FOR - NEXT nestings exceed the maximum nesting level of 6.	Check the program or contents of the operands in the application instruction.
OPERATION ERROR	6705	An incompatible device is specified as an operand of an application instruction.	Check the program or contents of the operands in the application instruction.
	6706	A device is specified outside the allowable range of an application instruction operand.	
	6707	A file register which is not defined in the parameter settings is accessed.	
SP. UNIT ERROR	6708	FROM - TO instruction error.	Check the program or contents of the operands in the application instruction.
OPERATION ERROR	6709	(1) Illegal nesting of FOR - NEXT instructions. (2) Illegal nesting of CALL - SRET instructions.	Check the program or contents of the operands in the application instruction.

*1 Characters in parentheses ( ) indicate the special register number where the information is saved.

Errors not displayed on the LED indicators are stored as operation error codes in the special data register D8067.

Devices related to error displays (see Appendix 1)

M8067 : Operation error generated
M8068 : Operation error latch
D8067 : Operation error code number
D8068 : Latch for step number where operation error was generated
D8069 : Step where M8067 error was generated

MEMO

APPENDICES

Appendix 1 List of Supported Devices

The ladder logic test tool (LLT) supports the devices for an A Series CPU, QnA Series CPU, and FXCPU.
(Non-supported devices are reserved as devices for reading and writing only.)
For the motion controller CPU, refer to the compatible devices of the A Series CPU.
For the compatible CPU, refer to Section 2.2.
The devices supported by the ladder logic test tool (LLT) are listed in Appendix Table 1.1 to Appendix Table 1.13.

(1) The A Series CPU function ladder logic test tool (LLT)

(a) Device list

Appendix Table 1.1 List of Devices Supported by the Ladder Logic Test Tool (LLT)

Device		Device range (points)							
		A0J2H A1FX	A1N A1S A1SJ	A2C A2CJ A2S	A2N(S1)	A3N A1SH A1SJH A2SH	A2A(S1)	A3A	A2U(S1) A2US(S1) A2USH-S1 A3U A4U
Bit device	Input (X) *1	X0 to X1FF (512 points)	X0 to XFF (256 points)	X00 to X1FF (512 points)	X00 to X3FF (1024 points)	X0 to X7FF (2048 points)	X00 to X3FF (1024 points)	X00 to X7FF (2048 points)	X00 to X1FFF (8192 points)
	Output (Y) *1	Y0 to Y1FF (512 points)	Y0 to YFF (256 points)	Y00 to Y1FF (512 points)	Y00 to Y3FF (1024 points)	Y0 to Y7FF (2048 points)	Y00 to Y3FF (1024 points)	Y00 to Y7FF (2048 points)	Y00 to Y1FFF (8192 points)
	Internal relay (M)	M0 to M2047 (2048 points)				M0 to M8191 (8192 points)			
	Special relay (M)	M9000 to M9255 (256 points)							
	Link relay (B)	B0 to B3FF (1024 points)					B0 to BFFF (4096 points)		B0 to B1FFF (8192 points)
	Annunciator (F)	F0 to F255 (256 points)					F0 to F2047 (2048 points)		
Word device	Timer (T)	T0 to T255 (256 points)					T0 to T2047 (2048 points)		
	Counter (C)	C0 to C255 (256 points)					C0 to C1023 (1024 points)		
	Data register (D)	D0 to D1023 (1024 points)					D0 to D6143 (6144 points)		D0 to D8191 (8192 points)
	Special register (D)	D9000 to D9255 (256 points)							
	Link register (W)	W0 to W3FFF (1024 points)					W0 to WFFF (8192 points)		W0 to W1FFF (8192 points)
	File register (R)	R0 to R8191 (8192 points)							
	Extension file register	Block 1 to 64 (8k points) *2							
	Accumulator (A)	A0, A1 (2 points)							
	Index register (Z, V)	Z, V (2 points)					Z, Z1 to Z6, V, V1 to V6 (14 points)		
Nesting (N)		N0 to N7 (8 points)							
Pointer (P)		P0 to P255 (256 points)							
Decimal constant (K)		K-2147483648 to K2147483647							
Hexadecimal constant (H)		H0 to HFFFFFFFF							
Character string constant		"ABC", "123"							

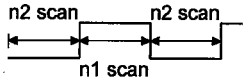
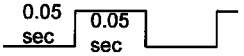
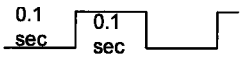
*1 : Remote I/O is included.

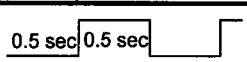
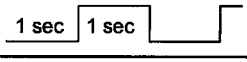
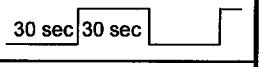
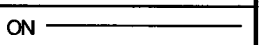
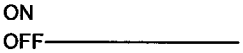
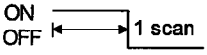
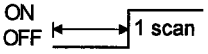
*2 : In the SW2D5□-GPPW, the data of file register can be written in the block No. 1 through 48 only.

(b) Special Relay List

Appendix Table 1.2 lists the special relays supported by the ladder logic test tool (LLT) for the A Series CPU functions. See the A Series actual PLC Users Manual for details about the special relays.

Appendix Table 1.2 List of Special Relays Supported by the Ladder Logic Test Tool (LLT)

Number	Name	Description
M9008	Self-diagnostic error	OFF :No error ON :Error
M9009	Annunciator detected	OFF :Not detected ON :Detected
M9010	Operation error flag	OFF :No error ON :Error
M9011	Operation error flag	OFF :No error ON :Error
M9012	Carry flag	OFF :Carry OFF ON :Carry ON
M9020	User timing clock No. 0	
M9021	User timing clock No. 1	
M9022	User timing clock No. 2	
M9023	User timing clock No. 3	
M9024	User timing clock No. 4	
M9028	Clock data read request	OFF :No processing ON :Read request
M9030*1	0.1-second clock	
M9031*1	0.2-second clock	

Number	Name	Description
M9032*1	1-second clock	
M9033*1	2-second clock	
M9034*1	1-minute clock	
M9036	Normally ON	
M9037	Normally OFF	
M9038	ON one scan only after RUN	
M9039	RUN flag (OFF one scan only after RUN)	
M9042	Stop status contact	OFF :Not stop status ON :Stop status
M9051	CHG instruction execution disabled	OFF :Enabled ON :Disabled
M9054	STEP RUN flag	OFF :Not STEP RUN ON :STEP RUN
M9091	Instruction error flag	OFF :No error ON :Error

*1 : The values obtained are based on the set values of a constant scan.

(c) Special Register List

Appendix Table 1.3 lists the special registers supported by the ladder logic test tool (LLT) for the A Series CPU functions. See the A Series actual PLC Users Manual for details about the special registers.

Appendix Table 1.3 List of Special Registers Supported by the Ladder Logic Test Tool (LLT)

Number	Name	Description
D9008	Self-diagnostic error	Self-diagnostic error number
D9009	Annunciator detected	F number from external breakdown
D9010	Error step	Step number where operation error occurred
D9011	Error step	Step number where operation error occurred
D9015	CPU operation status	CPU operation status
D9016	Program number	Saves the BIN value of the executing sequence program.
D9017*2	Scan time	Minimum scan time (10 ms units)
D9018*2	Scan time	Scan time (10ms units)
D9019*2	Maximum scan time	Maximum scan time (10ms units)
D9020*3	Constant scan	Constant scan time (user settable in 10 ms units)
D9021*2	Scan time	Scan time (1 ms units)
D9022*1	1-second counter	Number of counts in 1-second intervals
D9025	Clock data	Clock data (year, month)
D9026	Clock data	Clock data (day, hour)
D9027	Clock data	Clock data (minute, second)
D9028	Clock data	Clock data (, day of week)
D9035	Extension file register	Block No. used
D9036	Designates device number of extension file register.	Device number for direct access of each extension file register device.
D9037		
D9091	Detailed error number	Self-diagnosis detailed error number
D9124	Quantity of annunciators detected	Quantity of annunciators detected
D9125	Number of detected annunciators	Number of detected annunciators
D9126		
D9127		
D9128		
D9129		
D9130		
D9131		
D9132		

*1 : Value derived from the constant scan set value.

*2 : Value equal to all constant scan set values. Default value is 100 ms.

*3 : The set constant time becomes the time for one scan.

(2) The QnA Series CPU Function Ladder Logic Test Tool (LLT)
(a) Device list

Appendix Table 1.4 List of Devices Supported by the Ladder Logic Test Tool (LLT)

Device Name		Default Value		Comments
		Points	Operation Range	
Bit device	Input (X)	8192 points	X0 to X1FFF	Actual inputs are disabled.
	Output (Y)	8192 points	Y0 to Y1FFF	Actual outputs are disabled.
	Internal relay (M)	32768 points	M0 to M32767	—
	Latch relay (L)	32768 points	L0 to L32767	—
	Annunciator (F)	32768 points	F0 to F32767	—
	Edge relay (V)	32768 points	V0 to V32767	—
	Link special relay (SB)	32768 points	SB0 to SB7FFF	Not compatible with link functions. Same as internal relay (M) and latch relay (L).
	Link relay (B)	32768 points	B0 to B7FFF	
	Special relay (SM)	2048 points	SM0 to SM2047	See (b) Special Relay List for details about the special relays supported.
	Function input (FX)	16 points	FX0 to FXF	—
	Function output (FY)	16 points	FY0 to FYF	—
Word device	Data register (D)	32768 points	D0 to D32767	—
	Special register (SD)	2048 points	SD0 to SD2047	See (c) Special Register List for details about the special registered supported.
	Link register (W)	32768 points	W0 to W7FFF	Not compatible with link functions. Same as data register (D).
	Link special register (SW)	32768 points	SW0 to SW7FFF	Not compatible with link functions. Same as data register (D).
	Timer (T)	32768 points	T0 to T32767	One scan calculated as 100 ms.
	Retentive timer (ST)	0 points	(ST0 to ST32767)	One scan calculated as 100 ms.
	Counter (C)	32768 points	C0 to C32767	—
	Function register (FD)	5 points	FD0 to FD4	—
	File register (R)	1042432 points	R0 to R1042431	—
	Buffer register (Un\G)	16384 points	Un\G0 to Un\G16383	I/O assignments must be set for the parameters.
	Index register (Z)	16 points	Z0 to Z15	—
Nesting (N)		15 points	N0 to N14	—
Pointer (P)		4096 points	P0 to P4095	—
Decimal constant (K)		K-2147483648 to K2147483647		—
Hexadecimal constant (H)		H0 to HFFFFFFFF		—
Real number constant		E±1.17549-38 to E±3.40282+38		—
Character string constant		"ABC", "123"		Maximum 16 characters per instruction.

(b) Special Relay List

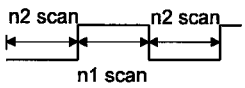
Appendix Table 1.5 lists the special relays supported by the ladder logic test tool (LLT) for the QnA Series CPU functions. See the QnA Series actual PLC Users Manual for details about the special relays.

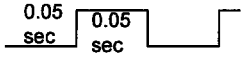
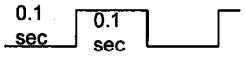
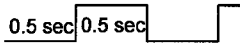
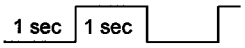
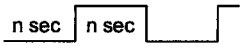
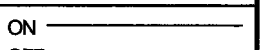
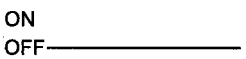
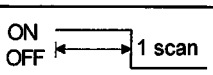
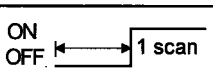
Appendix Table 1.5 List of Special Relays Supported by the Ladder Logic Test Tool (LLT)

Number	Name	Description
SM0	Diagnostic error	OFF :No error ON :Error
SM1	Self-diagnostic error	OFF :No self-diagnostic error ON :Self-diagnostic error
SM5	Error common information	OFF :No error common information ON :Error common information
SM16	Error individual information	OFF :No error individual information ON :Error individual information
SM50	Error reset	OFF → ON :Error reset
SM56	Operation error	OFF :Normal ON :Operation error
SM62	Annunciator detected	OFF :Not detected ON :Detected
SM203	STOP contacts	STOP status
SM205	STEP-RUN contacts	STEP-RUN status
SM213	Clock data read request	OFF :No processing ON :Read request
SM400	Normally ON	ON OFF
SM401	Normally OFF	ON OFF
SM402	ON one scan only after RUN	ON/OFF 1 scan
SM403	OFF one scan only after RUN	ON/OFF 1 scan
SM404	ON one scan only after RUN	ON/OFF 1 scan
SM405	OFF one scan only after RUN	ON/OFF 1 scan

Number	Name	Description
SM410*1	0.1-second clock	0.05 sec / 0.05 sec
SM411*1	0.2-second clock	0.1 sec / 0.1 sec
SM412*1	1-second clock	0.5 sec / 0.5 sec
SM413*1	2-second clock	1 sec / 1 sec
SM414*1	2n-second clock	n sec / n sec
SM420	User timing clock No.0	n2 scan, n2 scan, n1 scan
SM421	User timing clock No.1	
SM422	User timing clock No.2	
SM423	User timing clock No.3	
SM424	User timing clock No.4	
SM430	User timing clock No.5	
SM431	User timing clock No.6	
SM432	User timing clock No.7	
SM433	User timing clock No.8	
SM434	User timing clock No.9	
SM510	Low-speed program execution flag	OFF :Complete or no execution ON :Executing
SM640	Use file register	OFF :File registers not used ON :File registers used
SM700	Carry flag	OFF :Carry OFF ON :Carry ON

Appendix Table 1.5 List of Special Relays Supported by the Ladder Logic Test Tool (LLT) (cont.)

Number	Name	Description
SM703	Sort order	OFF :Ascending ON :Descending
SM704	Block comparison	OFF :Some do not match ON :All match
SM715	EI flag	OFF :DI ON :EI
SM1008	Self-diagnostic error	OFF :No error ON :Error
SM1009	Annunciator detected	OFF :Not detected ON :Detected
SM1010	Operation error	OFF :Normal ON :Operation error
SM1020	User timing clock No.0	
SM1021	User timing clock No.1	
SM1022	User timing clock No.2	
SM1023	User timing clock No.3	
SM1024	User timing clock No.4	

Number	Name	Description
SM1030	0.1-second clock	
SM1031	0.2-second clock	
SM1032	1-second clock	
SM1033	2-second clock	
SM1034	2n-second clock	
SM1036	Normally ON	
SM1037	Normally OFF	
SM1038	ON one scan only after RUN	
SM1039	OFF one scan only after RUN	
SM1042	Stop status contact	OFF :Not stop status ON :Stop status
SM1054	STEP RUN flag	ON :STEP RUN OFF :Not STEP RUN

(c) Special Register List

Appendix Table 1.6 lists the special registers supported by the ladder logic test tool (LLT) for the QnA Series CPU functions. See the QnA Series actual PLC Users Manual for details about the special registers.

Appendix table 1.6 List of Special Registers Supported by the Ladder Logic Test Tool (LLT)

Number	Name	Description
SD0	Diagnostic error	Diagnostic error number
SD1	Time the diagnostic error occurred	Time the diagnostic error occurred
SD2		
SD3		
SD4	Error information class	Error information class code
SD5	Error common information	Error common information
SD6		
SD7		
SD8		
SD9		
SD10		
SD11		
SD12		
SD13		
SD14		
SD15		
SD16	Error independent information	Error independent information
SD17		
SD18		
SD19		
SD20		
SD21		
SD22		
SD23		
SD24		
SD25		
SD26		
SD50	Error reset	Reset error number
SD62	Annunciator No.	Annunciator No.
SD63	Annunciator quantity	Annunciator quantity
SD64	Annunciator detected number table	Annunciator detected number
SD65		
SD66		
SD67		
SD68		
SD69		

Number	Name	Description
SD70	Annunciator detected number table	Annunciator detected number
SD71		
SD72		
SD73		
SD74		
SD75		
SD76		
SD77		
SD78		
SD79		
SD200	Switch status	CPU switch status
SD203	CPU operating status	CPU operating status *3
SD210	Clock data	Clock data (year, month)
SD211	Clock data	Clock data (day, hour)
SD212	Clock data	Clock data (minute, second)
SD213	Clock data	Clock data (, day of week)
SD290	Device assignment	No. of X points assigned
SD291		No. of Y points assigned
SD292		No. of M points assigned
SD293		No. of L points assigned
SD294		No. of B points assigned
SD295		No. of F points assigned
SD296		No. of SB points assigned
SD297		No. of V points assigned
SD298		No. of S points assigned
SD299		No. of T points assigned

*1 : Value derived from the constant scan setting value and number of scans.
*2 : Values equal to all constant scan setting values.
*3 : SD203 supports the CPU operation status only. STOP/PAUSE cause is fixed at 0.

Appendix Table 1.6 List of Special Registers Supported by the Ladder Logic Test Tool (LLT) (cont.)

Number	Name	Description
SD300	Device assignment	No. of ST points assigned
SD301		No. of C points assigned
SD302		No. of D points assigned
SD303		No. of W points assigned
SD304		No. of SW points assigned
SD412*1	1-second counter	Number of counts in 1-second intervals
SD414*1	2n-second clock setting	2n-second clock units
SD420	Scan counter	Number of scans counted
SD430	Low-speed scan counter	Number of scans counted
SD500	Executed program number	Program execution type.
SD510	Low-speed program number	Current low-speed execution file name
SD520*2	Present scan time	Present scan time (1 ms units)
SD521*2		Present scan time (1 μs units)
SD522*2	Initial scan time	Initial scan time (1 ms units)
SD523*2		Initial scan time (1 μs units)
SD524*2	Minimum scan time	Minimum scan time (1 ms units)
SD525*2		Minimum scan time (1 μs units)
SD526*2	Maximum scan time	Maximum scan time (1 ms units)
SD527*2		Maximum scan time (1 μs units)
SD528*2	Current low-speed scan time	Current scan time (1 ms units)
SD529*2		Current scan time (1 μs units)

Number	Name	Description
SD532*2	Minimum low-speed scan time	Minimum low-speed scan time (1 ms units)
SD533*2		Minimum scan time (1 μs units)
SD534*2	Maximum low-speed scan time	Maximum scan time (1 ms units)
SD535*2		Maximum scan time (1 μs units)
SD647	File register capacity	File register capacity
SD648	File register block number	File register block number
SD1008	Self-diagnostic error	Self-diagnostic error number
SD1009	Annunciator No.	Annunciator No.
SD1015	CPU operation status	CPU operation status
SD1017*2	Scan time	Minimum scan time (10 ms units)
SD1018*2	Scan time	Scan time (10 ms units)
SD1019*2	Scan time	Maximum scan time (10 ms units)
SD1021*2	Scan time	Scan time (1 ms units)
SD1022*1	1-second counter	Number of counts of 1-second units
SD1035	Extension file register	Used block number
SD1124	Number of annunciators detected	Number of annunciators detected
SD1125	Number of annunciators detected	Number of annunciators detected
SD1126		
SD1127		
SD1128		
SD1129		
SD1130		
SD1131		
SD1132		

*1 : Value derived from the constant scan setting value and number of scans.

*2 : Values equal to all constant scan setting values.

*3 : SD203 supports the CPU operation status only. STOP/PAUSE cause is fixed at 0.

POINT
Special relays/registers that have contents different from those of Q4ACPU will operate by the contents of special relays/registers of Q4ACPU.

(3) FX Series CPU function ladder logic test tool (LLT)

(a) Device list

Appendix Table 1.7 List of Devices Supported by the Ladder Logic Test Tool (LLT) (CPU type: FX_0/FX_{0S})

Device Name			Default Value		Comments
			Points	Operation Range	
Bit device	Input (X)		16 points	X000 to X017	Octal number. Actual inputs are disabled.
	Output (Y)		14 points	Y000 to Y015	Octal number. Actual outputs are disabled.
	Auxiliary relay (M)	General purpose	496 points	M0 to M495	—
		Hold*1	16 points	M496 to M511	
		Special	57 points	M8000 to M8255	
	State (S)	Initial state	10 points	S0 to S9	—
		General purpose	54 points	S10 to S63	
Word device	Timer (T)	100 ms	56 points	T0 to T55	—
		10 ms	24 points	T32 to T55	M8028 drive
	Counter (C)	16-bit up	14 points	C0 to C13	—
		16-bit up*1	2 points	C14 to C15	
	Data register (D) (32-bit for pair use)	16-bit general purpose	30 points	D0 to D29	—
		16-bit hold*1	2 points	D30 to D31	
		16-bit special	27 points	D8000 to D8255	
		16-bit index	2 points	V, Z	
Nesting (N)		For master control	8 points	N0 to N7	—
Pointer (P)		For JMP, CALL branching	64 points	P0 to P63	—
Decimal constant (K)		16 bits	-32768 to 32767		—
		32 bits	-2147483648 to 2147483647		—
Hexadecimal constant (H)		16 bits	H0 to HFFFF		—
		32 bits	H0 to HFFFFFFFF		—

*1 Fixed battery backup area. This area cannot be changed.

Appendix Table 1.8 List of Devices Supported by the Ladder Logic Test Tool (LLT) (CPU type: FX_{0N})

Device Name			Default Value		Comments
			Points	Operation Range	
Bit device	Input (X)	Total number of points with expansion	128 points	X000 to X177	Octal number. Actual inputs are disabled.
	output (Y)	Total number of points with expansion	128 points	Y000 to Y177	Octal number. Actual outputs are disabled.
	Auxiliary relay (M)	general purpose	384 points	M0 to M383	—
		Hold*1	128 points	M384 to M511	
		Special	67 points	M8000 to M8255	
	State (S)	Initial state*1	10 points	S0 to S9	—
		General purpose*1	118 points	S10 to S127	
Word device	Timer (T)	100 ms	63 points	T0 to T62	—
		10 ms	31 points	T32 to T62	M8028 drive
		1 ms	1 point	T63	—
	Counter (C)	16 bit up	16 points	C0 to C15	—
		16bit up*1	16 points	C16 to C31	
	Data register (D) (32-bit for pair use)	16-bit general purpose	128 points	D0 to D127	—
		16-bit hold*1	128 points	D128 to D255	
		16-bit special	106 points	D8000 to D8255	
		File*1	1500 points	D1000 to D2499	
		16-bit index	2 points	V, Z	
Nesting (N)		For master control	8 points	N0 to N7	—
Pointer (P)		For JMP, CALL branching	64 points	P0 to P63	—
Decimal constant (K)		16 bits	-32768 to 32767		—
		32 bits	-2147483648 to 2147483647		—
Hexadecimal constant (H)		16 bits	H0 to HFFFF		—
		32 bits	H0 to HFFFFFFFF		—

*1 Fixed battery backed-up area. This area cannot be changed.

Appendix Table 1.9 List of Devices Supported by the Ladder Logic Test Tool (LLT) (CPU type: FX_1)

Device Name			Default Value		Comments
			Points	Operation Range	
Bit device	Input (X)	Total number of points with expansion	128 points	X000 to X177	Octal number. Actual inputs are disabled.
	Output (Y)	Total number of points with expansion	128 points	Y000 to Y177	Octal number. Actual outputs are disabled.
	Auxiliary relay (M)	General purpose *1	500 points	M0 to M499	—
		Hold *2	524 points	M500 to M1023	
		Special	156 points	M8000 to M8255	
	State (S)	Initial state *1	10 points	S0 to S9	—
		General purpose *1	490 points	S10 to S499	
		Hold *2	400 points	S500 to S899	
		Annunciator *3	100 points	S900 to S999	
Word device	Timer (T)	100 ms	200 points	T0 to T199	—
		10 ms	46 points	T200 to T245	
	Counter (C)	16 bits up *1	100 points	C0 to C99	—
		16 bits up *2	36 points	C100 to C125	
	Data register (D) (32-bit for pair use)	16-bit general purpose *1	100 points	D0 to D99	—
		16-bit hold *2	28 points	D100 to D127	
		16-bit special	106 points	D8000 to D8255	
		16-bit index	2 points	V, Z	
Nesting (N)		For master control	8 points	N0 to N7	—
Pointer (P)		For JMP, CALL branching	64 points	P0 to P63	—
Decimal constant (K)		16 bits	-32768 to 32767		—
		32 bits	-2147483648 to 2147483647		—
Hexadecimal constant (H)		16 bits	H0 to HFFFF		—
		32 bits	H0 to HFFFFFFFF		—

*1 : Area not backed-up by battery. This area can be changed to battery backed-up area by parameter settings.

*2 : Battery backed-up area. This area can be changed to non-backed-up area by parameter settings.

*3 : Fixed battery backup area. This area cannot be changed.

Appendix Table 1.10 List of Devices Supported by the Ladder Logic Test Tool (LLT) (CPU type: FX/FX$_2$/FX$_{2C}$)

Device Name			Default Value		Comments
			Points	Operation Range	
Bit device	Input (X)	Total number of points with expansion	256 points	X000 to X377	Octal number. Actual inputs are disabled.
	Output (Y)	Total number of points with expansion	256 points	Y000 to Y377	Octal number. Actual outputs are disabled.
	Auxiliary relay (M)	General purpose *1	500 points	M0 to M499	—
		Hold *2	524 points	M500 to M1023	
		Hold *3	512 points	M1024 to M1535	
		Special	156 points	M8000 to M8255	
	State (S)	Initial state *1	10 points	S0 to S9	—
		General purpose *1	490 points	S10 to S499	
		Hold *2	400 points	S500 to S899	
		Annunciator *3	100 points	S900 to S999	
Word device	Timer (T)	100 ms	200 points	T0 to T199	—
		10 ms	46 points	T200 to T245	
		1 ms retentive *3	4 points	T246 to T249	
		100 ms retentive *3	6 points	T250 to T255	
	Counter (C)	16-bit up *1	100 points	C0 to C99	—
		16-bit up *2	100 points	C100 to C199	
		32-bit bi-directional *1	20 points	C200 to C219	
		32-bit bi-directional *2	15 points	C220 to C234	
	Data register (D) (32-bit for pair use)	16-bit general purpose *1	200 points	D0 to D199	—
		16-bit hold *2	312 points	D200 to D511	
		16-bit hold *3	488 points	D512 to D999	
		16-bit special	106 points	D8000 to D8255	
		File *3	2000 points	D1000 to D2999	
		RAM file	2000 points	D6000 to D7999	
		16-bit index	2 points	V, Z	
Nesting (N)		For master control	8 points	N0 to N7	—
Pointer (P)		For JMP, CALL branching	128 points	P0 to P127	—
Decimal constant (K)		16 bits	-32768 to 32767		—
		32 bits	-2147483648 to 2147483647		—
Hexadecimal constant (H)		16 bits	H0 to HFFFF		—
		32 bit	H0 to HFFFFFFFF		—

*1 : Area not backed-up by battery. This area can be changed to battery backed-up area by parameter settings.

*2 : Battery backed-up area. This area can be changed to non-backed-up area by parameter settings.

*3 : Fixed battery backup area. This area cannot be changed.

Appendix Table 1.11 List of Devices Supported by the Ladder Logic Test Tool (LLT) (CPU type: $FX_{2N}/FX2_{NC}$)

Device Name			Default Value		Comments
			Points	Operation Range	
Bit device	Input (X)	Total number of points with expansion	256 points	X000 to X377	Octal number. Actual inputs are disabled.
	Output (Y)	Total number of points with expansion	256 points	Y000 to Y377	Octal number. Actual outputs are disabled.
	Auxiliary relay (M)	General purpose *1	500 points	M0 to M499	—
		Hold *2	524 points	M500 to M1023	
		Hold *3	2048 points	M1024 to M3071	
		Special	156 points	M8000 to M8255	
	State (S)	Initial state *1	10 points	S0 to S9	—
		General purpose *1	490 points	S10 to S499	
		Hold *2	400 points	S500 to S899	
		Annunciator *3	100 points	S900 to S999	
Word device	Timer (T)	100 ms	200 points	T0 to T199	—
		10 ms	46 points	T200 to T245	
		1 ms retentive *3	4 points	T246 to T249	
		100 ms retentive *3	6 points	T250 to T255	
	Counter (C)	16-bit up *1	100 points	C0 to C99	—
		16-bit up *2	100 points	C100 to C199	
		32-bit bi-directional *1	20 points	C200 to C219	
		32-bit bi-directional *2	15 points	C220 to C234	
	Data register (D) (32-bit for pair use)	16-bit general purpose *1	200 points	D0 to D199	—
		16-bit hold *2	312 points	D200 to D511	
		16-bit hold *3	7488 points	D512 to D7999	
		16-bit special	106 points	D8000 to D8255	
		16-bit index	16 points	V0 to V7, Z0 to Z7	
Nesting (N)		For master control	8 points	N0 to N7	—
Pointer (P)		For JMP, CALL branching	128 points	P0 to P127	—
Decimal constant (K)		16 bits	-32768 to 32767		—
		32 bits	-2147483648 to 2147483647		—
Hexadecimal constant (H)		16 bits	H0 to HFFFF		—
		32 bit	H0 to HFFFFFFFF		—

*1 : Area not backed-up by battery. This area can be changed to battery backed-up area by parameter settings.

*2 : Battery backed-up area. This area can be changed to non-backed-up area by parameter settings.

*3 : Fixed battery backup area. This area cannot be changed.

(b) Special Relay List

Appendix Table 1.12 lists the special relays supported by the ladder logic test tool (LLT) for the FX Series CPU functions. See the FX Series actual PLC Programming Manual for details about the special relays.

Appendix Table 1.12 List of Special Relays Supported by the Ladder Logic Test Tool (LLT)

No.	Name	Description	FX_0, FX_{0S}	FX_{0N}	FX_1	FX, FX_2, FX_{2C}	FX_{2N}, FX_{2NC}
M8000	RUN monitor N/O contact	OFF :STOP ON :RUN	○				
M8001	RUN monitor N/C contact	OFF :RUN ON :STOP	○				
M8002	Initial pulse N/O contact	ON one scan after RUN	○				
M8003	Initial pulse N/C contact	OFF one scan after RUN	○				
M8004	Error occurred	ON if any of M8060 to M8067 operates.	○				
M8011	10 ms clock	5 ms 5 ms	○				
M8012	100 ms clock	50 ms 50 ms	○				
M8013	1 s clock	0.5 s 0.5 s	○				
M8014	1 min clock	30 s 30 s	○				
M8018	Internal real-time clock detected	Normally ON	—	—	—	△	△
M8020	Zero	ON if counting result is 0	○				
M8021	Borrow	ON if counting result is less than maximum minus value.	○				
M8022	Carry	ON if counting result increases a digit.	○				
M8023	Decimal-point operation instruction	ON when floating decimal-point instruction is executed.	—	—	—	○	—
M8024	Designate BMOV direction	ON :Write OFF :Read	—	—	—	—	○
M8026	RAMP mode designation	ON :Hold output value OFF :Reset output value	—	—	—	○	○
M8028	Switch timer instruction	OFF :100 ms base ON :10 ms base	○	○	—	—	—

○ : This device or function is supported by the actual PLC.

— : This device or function is not supported by the actual PLC.

△ : This device is supported by actual PLCs with a clock function.
For the ladder logic test tool (LLT), always ON regardless whether the actual PLC has a clock function.

Appendix Table 1.12 List of Special Relays Supported by the Ladder Logic Test Tool (LLT) (cont.)

No.	Name	Description	FX_0, FX_{0S}	FX_{0N}	FX_1	FX, FX_2, FX_{2C}	FX_{2N}, FX_{2NC}
M8029	Instruction execution complete	OFF :Executing ON :Execution complete	○				
M8031	Non-hold memory all clear instruction	OFF :Hold ON :Clear	○				
M8032	Hold memory all clear instruction	OFF :Hold ON :Clear	○				
M8033	Memory hold stop instruction	OFF :Clear ON :Hold	○				
M8034	Disable all outputs instruction	OFF :Output enabled ON :Output OFF	○				
M8038	RAM file clear instruction	OFF :Hold ON :Clear	—	—	—	○	—
M8039	Constant scan mode designation	OFF :Normal scan ON :Constant scan mode	○				
M8040	Disable transition instruction	OFF :Transition enabled ON :Transition disabled	○				
M8041	Transition start instruction (for IST command)	OFF :Stop ON :Transition start	○				
M8042	Start pulse instruction (for IST command)	ON :IST command start instruction	○				
M8043	Home position return complete instruction (for IST command)	ON :IST command home position return instruction	○				
M8044	Home position condition (for IST command)	ON :Home position OFF :Home position return not complete	○				
M8045	All output reset disabled (for IST command)	ON :Reset disabled OFF :Reset enabled	○				
M8046	STL state operation	ON if any of S0 to S899 operates.	○				
M8047	STL monitor enable	ON :D8040 to D8047 enabled	○				
M8048	Annunciator operation	ON if any of S900 to S999 operates.	—	—	○	○	○

○ : This device or function is supported by the actual PLC.
— : This device or function is not supported by the actual PLC.
△ : This device is supported by actual PLCs with a clock function.
For the ladder logic test tool (LLT), always ON regardless whether the actual PLC has a clock function.

Appendix Table 1.12 List of Special Relays Supported by the Ladder Logic Test Tool (LLT) (cont.)

No.	Name	Description	FX_0, FX_{0S}	FX_{0N}	FX_1	FX, FX_2, FX_{2C}	FX_{2N}, FX_{2NC}
M8049	Annunciator enable instruction	ON :D8049 enabled OFF : D8049 enabled	—	—	○	○	○
M8067	Operation error occurred	ON :Operation error OFF :No operation error	○				
M8068	Operation error latch	Holds M8067 status	○				
M8074	RAM file register setting	ON :Use OFF :Do not use	—	—	—	○	—
M8160	XCH SWAP function setting	ON :8-bit conversion OFF :Normal mode	—	—	—	○	○
M8161	8-bit processing mode	ASC, ASCI, HEX processing method	—	○	—	○	○
M8164	Change number of FROM/TO instruction transfer points	Transfer points switch instruction	—	—	—	—	○
M8168	SMOV HEX data handling functions	Digit shift in 4-bit unit	—	—	—	○	○
M8200	Counting direction of counter	ON :C200 down OFF :C200 up	—	—	—	○	○
M8201	Counting direction of counter	ON :C201 down OFF :C201 up	—	—	—	○	○
M8202	Counting direction of counter	ON :C202 down OFF :C202 up	—	—	—	○	○
M8203	Counting direction of counter	ON :C203 down OFF : C203 up	—	—	—	○	○
M8204	Counting direction of counter	ON :C204 down OFF :C204 up	—	—	—	○	○
M8205	Counting direction of counter	ON :C205 down OFF :C205 up	—	—	—	○	○
M8206	Counting direction of counter	ON :C206 down OFF :C206 up	—	—	—	○	○
M8207	Counting direction of counter	ON :C207 down OFF :C207 up	—	—	—	○	○
M8208	Counting direction of counter	ON :C208 down OFF :C208 up	—	—	—	○	○
M8209	Counting direction of counter	ON :C209 down OFF :C209 up	—	—	—	○	○

○ : This device or function is supported by the actual PLC.

— : This device or function is not supported by the actual PLC.

△ : This device is supported by actual PLCs with a clock function.
For the ladder logic test tool (LLT), always ON regardless whether the actual PLC has a clock function.

Appendix Table 1.12 List of Special Relays Supported by the Ladder Logic Test Tool (LLT) (cont.)

No.	Name	Description	FX_0, FX_{0S}	FX_{0N}	FX_1	FX, FX_2, FX_{2C}	FX_{2N}, FX_{2NC}
M8210	Counting direction of counter	ON :C210 down OFF :C210 up	—	—	—	○	○
M8211	Counting direction of counter	ON :C211 down OFF :C211 up	—	—	—	○	○
M8212	Counting direction of counter	ON :C212 down OFF :C212 up	—	—	—	○	○
M8213	Counting direction of counter	ON :C213 down OFF :C213 up	—	—	—	○	○
M8214	Counting direction of counter	ON :C214 down OFF :C214 up	—	—	—	○	○
M8215	Counting direction of counter	ON :C215 down OFF :C215 up	—	—	—	○	○
M8216	Counting direction of counter	ON :C216 down OFF :C216 up	—	—	—	○	○
M8217	Counting direction of counter	ON :C217 down OFF :C217 up	—	—	—	○	○
M8218	Counting direction of counter	ON :C218 down OFF :C218 up	—	—	—	○	○
M8219	Counting direction of counter	ON :C219 down OFF :C219 up	—	—	—	○	○
M8220	Counting direction of counter	ON :C220 down OFF :C220 up	—	—	—	○	○
M8221	Counting direction of counter	ON :C221 down OFF :C221 up	—	—	—	○	○
M8222	Counting direction of counter	ON :C222 down OFF :C222 up	—	—	—	○	○
M8223	Counting direction of counter	ON :C223 down OFF :C223 up	—	—	—	○	○
M8224	Counting direction of counter	ON :C224 down OFF :C224 up	—	—	—	○	○
M8225	Counting direction of counter	ON :C225 down OFF :C225 up	—	—	—	○	○
M8226	Counting direction of counter	ON :C226 down OFF :C226 up	—	—	—	○	○
M8227	Counting direction of counter	ON :C227 down OFF :C227 up	—	—	—	○	○

○ : This device or function is supported by the actual PLC.

— : This device or function is not supported by the actual PLC.

△ : This device is supported by actual PLCs with a clock function.
For the ladder logic test tool (LLT), always ON regardless whether the actual PLC has a clock function.

Appendix Table 1.12 List of Special Relays Supported by the Ladder Logic Test Tool (LLT) (cont.)

No.	Name	Description	FX_0, FX_{0S}	FX_{0N}	FX_1	FX, FX_2, FX_{2C}	FX_{2N}, FX_{2NC}
M8228	Counting direction of counter	ON :C228 down OFF :C228 up	—	—	—	○	○
M8229	Counting direction of counter	ON :C229 down OFF :C229 up	—	—	—	○	○
M8230	Counting direction of counter	ON :C230 down OFF :C230 up	—	—	—	○	○
M8231	Counting direction of counter	ON :C231 down OFF :C231 up	—	—	—	○	○
M8232	Counting direction of counter	ON :C232 down OFF :C232 up	—	—	—	○	○
M8233	Counting direction of counter	ON :C233 down OFF :C233 up	—	—	—	○	○
M8234	Counting direction of counter	ON :C234 down OFF :C234 up	—	—	—	○	○

○ :This device or function is supported by the actual PLC.

— :This device or function is not supported by the actual PLC.

△ :This device is supported by actual PLCs with a clock function.
For the ladder logic test tool (LLT), always ON regardless whether the actual PLC has a clock function.

(c) Special Register List

Appendix Table 1.13 lists the special registers supported by the ladder logic test tool (LLT) for the FX Series CPU functions. See the FX Series actual PLC Programming Manual for details about the special registers.

Appendix Table 1.13 List of Special Registers Supported by the Ladder Logic Test Tool (LLT)

No.	Name	Description	FX_0, FX_{0S}	FX_{0N}	FX_1	FX, FX_2, FX_{2C}	FX_{2N}, FX_{2NC}
D8000	Watchdog timer	200 ms *1	○				
D8001	PLC type and system version	*2	○				
D8002	Memory capacity	Maximum value for model	○				
D8004	Error M number	M8060 to M8068	○				
D8006	Low battery voltage detection level	30 (0.1 V units)	—	—	○	○	○
D8010	Scan present value	0.1 ms units *3	○				
D8011	Minimum scan time	0.1 ms units *3	○				
D8012	Maximum scan time	0.1 ms units *3	○				
D8013	Seconds	Operates as 1-second clock	—	—	—	△	△
D8014	Minutes	Time data	—	—	—	△	△
D8015	Hours	Time data	—	—	—	△	△
D8016	Day	Time data	—	—	—	△	△
D8017	Month	Time data	—	—	—	△	△
D8018	Year	Time data	—	—	—	△	△
D8019	Day of week	Time data	—	—	—	△	△
D8028	Z register contents	Z register contents	○				
D8029	V register contents	Z register contents	○				
D8030	Analog volume 1	*4	—	○	—	—	—
D8031	Analog volume 2	*4	—	○	—	—	—
D8039	Constant scan time	Initial value: 100 ms (1 ms units) *5	○				

○ : This device or function is supported by the actual PLC.

— : This device or function is not supported by the actual PLC.

△ : This device is supported by actual PLCs with a clock function.
For the ladder logic test tool (LLT), always ON regardless whether the actual PLC has a clock function.

*1 : Initial value: 200 ms for all models. Can be changed but no watchdog timer check is conducted.

*2 : FX0, FX0S.....20000
FX0N.....20000
FX1.....21000
FX,FX2, FX2C.....20000
FX2N, FX2NC.....24000

*3 : Values equal to all constant scan setting values. Default value is 100 ms.

*4 : Operates as a general data register. Test by writing values from 0 to 255 using the GPPW device test functions.

*5 : The set constant time becomes the time for one scan.

Appendix Table 1.13 List of Special Registers Supported by the Ladder Logic Test Tool (LLT) (cont.)

No.	Name	Description	FX_0, FX_{0S}	FX_{0N}	FX_1	FX, FX_2, FX_{2C}	FX_{2N}, FX_{2NC}
D8040	ON state number 1	STL monitor contents			○		
D8041	ON state number 2	STL monitor contents			○		
D8042	ON state number 3	STL monitor contents			○		
D8043	ON state number 4	STL monitor contents			○		
D8044	ON state number 5	STL monitor contents			○		
D8045	ON state number 6	STL monitor contents			○		
D8046	ON state number 7	STL monitor contents			○		
D8047	ON state number 8	STL monitor contents			○		
D8049	ON state minimum number	STL monitor contents			○		
D8067	Operation error code number	Error code number			○		
D8068	Operation error occurred step number latch	Saves step number where error occurred			○		
D8069	M8067 error occurred step number	Step number where error occurred			○		
D8102	Memory capacity	Maximum value for model	—	—	—	—	○
D8164	Designate number of FROM/TO instruction transfer points	Write transfer points	—	—	—	—	○
D8182	Z1 register contents	Z1 register contents	—	—	—	—	○
D8183	V1 register contents	V1 register contents	—	—	—	—	○
D8184	Z2 register contents	Z2 register contents	—	—	—	—	○
D8185	V2 register contents	V2 register contents	—	—	—	—	○
D8186	Z3 register contents	Z3 register contents	—	—	—	—	○
D8187	V3 register contents	V3 register contents	—	—	—	—	○
D8188	Z4 register contents	Z4 register contents	—	—	—	—	○
D8189	V4 register contents	V4 register contents	—	—	—	—	○
D8190	Z5 register contents	Z5 register contents	—	—	—	—	○
D8191	V5 register contents	V5 register contents	—	—	—	—	○
D8192	Z6 register contents	Z6 register contents	—	—	—	—	○
D8193	V6 register contents	V6 register contents	—	—	—	—	○
D8194	Z7 register contents	Z7 register contents	—	—	—	—	○
D8195	V7 register contents	V7 register contents	—	—	—	—	○

○ : This device or function is supported by the actual PLC.

— : This device or function is not supported by the actual PLC.

△ : This device is supported by actual PLCs with a clock function.
For the ladder logic test tool (LLT), always ON regardless whether the actual PLC has a clock function.

Appendix 2 List of Supported Instruction

The ladder logic test tool (LLT) supports the A Series/Q4ACPU/FXCPU instructions. However, some instructions are subject to restrictions and some are not supported. Unsupported instructions are not processed (NOP).
See Appendices Table 1.14 to 1.16 for the instructions supported by the ladder logic test tool (LLT).

POINT

Unsupported instructions are not processed (NOP), and the "Unsupported information indicator lamp" lights up on the initial window of the ladder logistic test tool (LLT) functions. (Refer to the display contents in Section 3.3 "Description of the Initial Window Display".

(1) A Series CPU Function Ladder Logic Test Tool (LLT)

Appendix Table 1.14 List of Supported Instructions (A Series CPU Function)

(a) Sequence Instructions

Class	Instruction Symbol	Restriction
Contact instructions	LD, LDI, AND, ANI, OR, ORI	—
Coupling instructions	ANB, ORB, MPS, MRD, MPP	—
Output instructions	OUT, OUT T, OUT C, SET, RST, PLS, PLF	—
Shift instruction	SFT(P)	—
Master control instructions	MC, MCR	—
End instructions	FEND, END	—
Other instructions	STOP, NOP	—

(b) Basic Instructions

Class	Instruction Symbol	Restriction
Comparative operation instructions	=, <>, >, <=, <, >=, D=, D<>, D>, D<=, D<, D>=	—
Arithmetic operation instructions	+(P), -(P), D+(P), D-(P), *(P), /(P), D*(P), D/(P), B+(P), B-(P), DB+(P), DB-(P), B*(P), B/(P), DB*(P), DB/(P), INC(P), DEC(P), DINC(P), DDEC(P)	—
BCD ↔ BIN conversion instructions	BCD(P), DBCD(P), BIN(P), DBIN(P)	—
Data transfer instruction	MOV(P), DMOV(P), CML(P), DCML(P), BMOV(P), FMOV(P), XCH(P), DXCH(P)	—
Program branching instructions	CJ, SCJ, JMP, CALL(P), RET	—
Program switching instructions	CHG	—

Appendix Table 1.14 List of Supported Instructions (A Series CPU Function) (cont.)

(c) Applied Instructions

Class	Instruction Symbol	Restriction
Logical arithmetic instructions	WAND(P), DAND(P), WOR(P), DOR(P), WXOR(P), DXOR(P), WXNR(P), DXNR(P), NEG(P)	—
Rotation instructions	ROR(P), RCR(P), ROL(P), RCL(P), DROR(P), DRCR(P), DROL(P), DRCL(P)	—
Shift instruction	SFR(P), SFL(P), BSFR(P), BSFL(P), DSFR(P), DSFL(P),	—
Data processing instructions	SER(P), SUM(P), DSUM(P), DECO(P), ENCO(P), SEG, BSET(P), BRST(P), DIS(P), UNI(P), ASC	SEG conducts 7-segment decoding regardless of M9052 ON/OFF status.
FIFO instruction	FIFW(P), FIFR(P)	—
Buffer memory access instructions	FROM(P), DFRO(P), TO(P), DTO(P)	—
FOR to NEXT instructions	FOR, NEXT	—
Display instructions	LED, LEDA, LEDB, LEDR	—
Other instructions	STC, CLC, DUTY	STC converted to SET M9012 CLC converted to RST M9012

(d) Dedicated Instructions

Class	Instruction Symbol	Restriction
Direct output instruction	DOUT, DSET(P), DRST(P)	—
Structural program instructions	BREAK(P), FCALL(P)	—
Data operation instructions	DSER(P), SWAP(P), DIS(P), UNI(P), TEST(P), DTEST(P)	—
I/O operation instruction	FF	—
Real number processing instructions	BSQR(P), BDSQR(P), BSIN(P), BCOS(P), BTAN(P), BASIN(P), BACOS(P), BATAN(P), INT(P), DINT(P), FLOAT(P), DFLOAT(P), ADD(P), SUB(P), MUL(P), DIV(P), RAD(P), DEG(P), SIN(P), COS(P), TAN(P), ASIN(P), ACOS(P), ATAN(P), SQR(P), EXP(P), LOG(P)	—
Character string processing instructions	BINDA(P), DBINDA(P), BINHA(P), DBINHA(P), BCDDA(P), DBCDDA(P), DABIN(P), DDABIN(P), HABIN(P), DHABIN(P), DABCD(P), DDABCD(P), LEN(P), STR(P), DSTR(P), VAL(P), DVAL(P), ASC(P), HEX(P), SMOV(P), SADD(P), SCMP(P), WTOB(P), BTOW(P)	—
Data control instructions	LIMIT(P), DLIMIT(P), BAND(P), DBAND(P), ZONE(P), DZONE(P)	—
Clock instructions	DATERD(P)	—
Extension file register instructions	RSET(P), BMOVR(P), BXCHR(P), ZRRD(P), ZRWR(P), ZRRDB(P), ZRWRB(P)	—
Program switching instructions	ZCHG	—

(2) QnA Series Function Ladder Logic Test Tool (LLT)

Appendix Table 1.15 List of Supported Instructions (QnA Series CPU functions)

(a) Sequence Instructions

Class	Instruction Symbol	Restriction
Contact instructions	LD, LDI, AND, ANI, OR, ORI, LDP, LDF, ANDP, ANDF, ORP, ORF	—
Coupling instructions	ANB, ORB, MPS, MRD, MPP, INV, MEP, MEF, EGP, EGF	—
Output instructions	OUT, OUT T, OUT C, OUTH T, SET, RST, PLS, PLF, FF	—
Shift instructions	SFT(P)	—
Master control instructions	MC, MCR	—
End instructions	FEND, END	—
Other instructions	STOP, NOP, NOPLF, PAGE	NOPLF, PAGE processed as NOP.

(b) Basic Instructions

Class	Instruction Symbol	Restriction
Comparative operation instructions	=, <>, >, <=, <, >=, D=, D<>, D>, D<=, D<, D>=, E=, E<>, E>, E<=, E<, E>=, $=, $<>, $>, $<=, $<, $>=, BKCMP□(P)	—
Arithmetic operation instructions	+(P), -(P), D+(P), D-(P), *(P), /(P), D*(P), D/(P), B+(P), B-(P), DB+(P), DB-(P), B*(P), B/(P), DB*(P), DB/(P), E+(P), E-(P), E*(P), E/(P), BK+(P), BK-(P), $+(P), INC(P), DEC(P), DINC(P), DDEC(P)	—
Data conversion instructions	BCD(P), DBCD(P), BIN(P), DBIN(P), INT(P), DINT(P), FLT(P), DFLT(P), DBL(P), WORD(P), GRY(P), DGRY(P), GBIN(P), DGBIN(P), NEG(P), DNEG(P), ENEG(P), BKBCD(P), BKBIN(P)	—
Data transfer instructions	MOV(P), DMOV(P), EMOV(P), $MOV(P), CML(P), DCML(P), BMOV(P), FMOV(P), XCH(P), DXCH(P), BXCH(P), SWAP(P)	—
Program branching instructions	CJ, SCJ, JMP, GOEND	—
Other convenient instructions	TTMR, STMR, RAMP, MTR	—

Appendix Table 1.15 List of Supported Instructions (QnA Series CPU functions) (cont.)

(c) Applied Instructions

Class	Instruction Symbol	Restriction
Logical arithmetic instructions	WAND(P), DAND(P), BKAND(P), WOR(P), DOR(P), BKOR(P), WXOR(P), DXOR(P), BKXOR(P), WXNR(P), DXNR(P), BKNXR(P)	–
Rotation instructions	ROR(P), RCR(P), ROL(P), RCL(P), DROR(P), DRCR(P), DROL(P), DRCL(P)	–
Shift instructions	SFR(P), SFL(P), BSFR(P), BSFL(P), DSFR(P), DSFL(P),	–
Bit processing instructions	BSET(P), BRST(P), TEST(P), DTEST(P), BKRST(P)	–
Data processing instructions	SER(P), DSER(P), SUM(P), DSUM(P), DECO(P), ENCO(P), SEG(P), DIS(P), UNI(P), NDIS(P), NUNI(P), WTOB(P) BTOW(P), MAX(P), MIN(P), DMAX(P), DMIN(P), SORT(P), DSORT(P), WSUM(P), DWSUM(P)	SORT(P), DSORT(P) are executed one scan.
Structural instructions	FOR, NEXT, BREAK(P), CALL(P), RET, FCALL(P), ECALL(P), EFCALL(P)	–
Data table operation instruction	FIFW(P), FIFR(P), FPOP(P), FINS(P), FDEL(P)	–
Buffer memory access instructions	FROM(P), DFRO(P), TO(P), DTO(P)	–
Character string processing instructions	BINDA(P), DBINDA(P), BINHA(P), DBINHA(P), BCDDA(P), DBCDDA(P), DABIN(P), DDABIN(P), HABIN(P), DHABIN(P), DABCD(P), DDABCD(P) LEN(P), STR(P), DSTR(P), VAL(P), DVAL(P), ESTR(P), EVAL(P), ASC(P), HEX(P), RIGHT(P), LEFT(P), MIDR(P), MIDW(P), INSTR(P), EMOD(P), EREXP(P)	–
Special function instructions	SIN(P), COS(P), TAN(P), ASIN(P), ACOS(P), ATAN(P), RAD(P), DEG(P), SQR(P), EXP(P), LOG(P), BSQR(P), BDSQR(P), BSIN(P), BCOS(P), BTAN(P), BASIN(P), BACOS(P), BATAN(P)	–
Data control instructions	LIMIT(P), DLIMIT(P), BAND(P), DBAND(P), ZONE(P), DZONE(P), RSET(P), QDRSET(P)	–
Clock instructions	DATERD(P), DATE+(P), DATE-(P), SECOND(P), HOUR(P)	DATERD(P) reads the computer clock data.
Program control instructions	PSTOP(P), POFF(P), PSCAN(P), PLOW(P)	–
Display instructions	LED, LEDR	–
Other instructions	DUTY, ZRRDB(P), ZRWRB(P), ADRSET(P)	–

(3) FX Series function ladder logic test tool (LLT)

Appendix Table 1.16 List of Supported Instructions (FX Series CPU functions)

(a) Sequence Instructions

Class	Instruction Symbol	Restriction
Contact instructions	LD, LDI, LDP, LDF, AND, ANI, ANDP, ANDF, OR, ORI, ORP, ORF	*1
Coupling instructions	ANB, ORB, MPS, MRD, MPP, INV	*1
Output instructions	OUT, SET, RST, PLS, PLF	—
Master control instructions	MC, MCR	—
Step ladder instructions	STL, RET	—
Other instructions	END, NOP	—

*1: The LDP, LDF, ANDP, ANDF, ORP, ORF, and INV instructions are only compatible with FX_{2N} and FX_{2NC} PLC.

(b) Applied Instructions

Class	FNC No.	Instruction Symbol	32-bit Instruction	Pulses Execution Instruction	Applicable PLCs					Compatibility with Ladder logic test tool (LLT)
					FX_0, FX_{0S}	FX_{0N}	FX_1	FX, FX_2, FX_{2C}	FX_{2N}, FX_{2NC}	
Program flowchart	00	CJ	—	△	○	○	○	○	○	●
	01	CALL	—	YES	—	—	○	○	○	●
	02	SRET	—	—	—	—	○	○	○	●
	03	IRET	—	—	○	○	○	○	○	×
	04	EI	—	—	○	○	○	○	○	×
	05	DI	—	—	○	○	○	○	○	×
	06	FEND	—	—	○	○	○	○	○	●
	07	WDT	—	△	○	○	○	○	○	×
	08	FOR	—	—	○	○	○	○	○	●
	09	NEXT	—	—	○	○	○	○	○	●
	10	CMP	YES	△	○	○	○	○	○	●
	11	ZCP	YES	△	○	○	○	○	○	●
	12	MOV	YES	△	○	○	○	○	○	●
	13	SMOV	—	YES	—	—	—	○	○	●
	14	CML	YES	YES	—	—	—	○	○	●
	15	BMOV	—	△	—	○	—	○	○	●
	16	FMOV	YES	YES	—	—	—	○	○	●
	17	XCH	YES	YES	—	—	—	○	○	●
	18	BCD	YES	△	○	○	○	○	○	●
	19	BIN	YES	△	○	○	○	○	○	●

Appendix Table 1.16 List of Supported Instructions (FX Series CPU functions) (cont.)

Class	FNC No.	Instruction symbol	32-bit Instruction	Pulses Execution Instruction	Applicable PLCs					Compatibility with Ladder logic test tool (LLT)
					FX_0, FX_{0S}	FX_{0N}	FX_1	FX, FX_2, FX_{2C}	FX_{2N}, FX_{2NC}	
Arithmetic/logical operations	20	ADD	YES	△	○	○	○	○	○	●
	21	SUB	YES	△	○	○	○	○	○	●
	22	MUL	YES	△	○	○	○	○	○	●
	23	DIV	YES	△	○	○	○	○	○	●
	24	INC	YES	△	○	○	○	○	○	●
	25	DEC	YES	△	○	○	○	○	○	●
	26	WAND	YES	△	○	○	○	○	○	●
	27	WOR	YES	△	○	○	○	○	○	●
	28	WXOR	YES	△	○	○	○	○	○	●
	29	NEG	YES	YES	–	–	–	○	○	●
Rotation shift	30	ROR	YES	YES	–	–	–	○	○	●
	31	ROL	YES	YES	–	–	–	○	○	●
	32	RCR	YES	YES	–	–	–	○	○	●
	33	RCL	YES	YES	–	–	–	○	○	●
	34	SFTR	–	△	○	○	○	○	○	●
	35	SFTL	–	△	○	○	○	○	○	●
	36	WSFR	–	YES	–	–	–	○	○	●
	37	WSFL	–	YES	–	–	–	○	○	●
	38	SFWR	–	YES	–	–	–	○	○	●
	39	SFRD	–	YES	–	–	–	○	○	●
	40	ZRST	–	△	○	○	○	○	○	●
	41	DECO	–	△	○	○	○	○	○	●
	42	ENCO	–	△	○	○	○	○	○	●
	43	SUM	YES	YES	–	–	–	○	○	●
	44	BON	YES	YES	–	–	–	○	○	●
	45	MEAN	YES	YES	–	–	–	○	○	●
	46	ANS	–	–	–	–	–	○	○	●
	47	ANR	–	YES	–	–	–	○	○	●
	48	SOR	YES	YES	–	–	–	○	○	●
	49	FLT	YES	YES	–	–	–	○	○	●
High-speed processing	50	REF	–	△	○	○	○	○	○	×
	51	REFF	–	YES	–	–	○	○	○	×
	52	MTR	–	–	–	–	–	○	○	×
	53	HSCS	YES	–	○	○	○	○	○	×
	54	HSCR	YES	–	○	○	○	○	○	×
	55	HSZ	YES	–	–	–	–	○	○	×
	56	SPD	–	–	–	–	–	○	○	×
	57	PLSY	YES	–	○	○	–	○	○	×
	58	PWM	–	–	○	○	–	○	○	×
	59	PLSR	YES	–	–	–	–	–	○	×

Appendix Table 1.16 List of Supported Instructions (FX Series CPU functions) (cont.)

Class	FNC No.	Instruction symbol	32-bit Instruction	Pulses Execution Instruction	Applicable PLCs					Compatibility with Ladder logic test tool (LLT)
					FX_0, FX_{0S}	FX_{0N}	FX_1	FX, FX_2, FX_{2C}	FX_{2N}, FX_{2NC}	
Convenient instructions	60	IST	–	–	○	○	○	○	○	●
	61	SER	YES	YES	–	–	–	○	○	●
	62	ABSD	YES	–	–	–	–	○	○	●
	63	INCD	–	–	–	–	–	○	○	●
	64	TTMR	–	–	–	–	–	○	○	●
	65	STMR	–	–	–	–	–	○	○	●
	66	ALT	–	–	○	○	–	○	○	●
	67	RAMP	–	–	○	○	–	○	○	●
	68	ROTC	–	–	–	–	–	○	○	×
	69	SORT	–	–	–	–	–	○	○	●
External devices, I/O	70	TKY	YES	–	–	–	–	○	○	×
	71	HKY	YES	–	–	–	–	○	○	×
	72	DSW	–	–	–	–	–	○	○	×
	73	SEGD	–	YES	–	–	–	○	○	×
	74	SEGL	–	–	–	–	–	○	○	×
	75	ARWS	–	–	–	–	–	○	○	×
	76	ASC	–	–	–	–	–	○	○	●
	77	PR	–	–	–	–	–	○	○	×
	78	FROM	YES	YES	–	○	–	○	○	●
	79	TO	YES	YES	–	○	–	○	○	●
External devices, SER	80	RS	–	–	–	○	–	○	○	×
	81	PRUN	YES	YES	–	–	–	○	○	×
	82	ASCI	–	YES	–	○	–	○	○	●
	83	HEX	–	YES	–	○	–	○	○	●
	84	CCD	–	YES	–	○	–	○	○	×
	85	VRRD	–	YES	–	–	○	○	○	×
	86	VRSC	–	YES	–	–	–	○	○	×
	87	–								–
	88	PID	–	–	–	–	–	○	○	×
	89	–								–
External devices, F2	90	MNET	–	YES	–	–	–	–	–	×
	91	ANRD	–	YES	–	–	–	–	–	×
	92	ANWR	–	YES	–	–	–	–	–	×
	93	RMST	–	–	–	–	–	○	–	×
	94	RMWR	YES	YES	–	–	–	○	–	×
	95	RMRD	YES	YES	–	–	–	○	–	×
	96	RMMN	–	YES	–	–	–	○	–	×
	97	BLK	–	YES	–	–	–	–	–	×
	98	MCDE	–	YES	–	–	–	–	–	×
	99	–								–

Appendix Table 1.16 List of Supported Instructions (FX Series CPU functions) (cont.)

Class	FNC No.	Instruction symbol	32-bit Instruction	Pulses Execution Instruction	Applicable PLCs					Compatibility with Ladder logic test tool (LLT)
					FX_0, FX_{0S}	FX_{0N}	FX_1	FX, FX_2, FX_{2C}	FX_{2N}, FX_{2NC}	
Floating decimal-point	110	ECMP	YES	YES	—	—	—	—	○	●
	111	EZCP	YES	YES	—	—	—	—	○	●
	118	EBCD	YES	YES	—	—	—	—	○	●
	119	EBIN	YES	YES	—	—	—	—	○	●
	120	EADD	YES	YES	—	—	—	—	○	●
	121	ESUB	YES	YES	—	—	—	—	○	●
	122	EMUL	YES	YES	—	—	—	—	○	●
	123	EDIV	YES	YES	—	—	—	—	○	●
	127	ESQR	YES	YES	—	—	—	—	○	●
	129	INT	YES	YES	—	—	—	—	○	●
	130	SIN	YES	YES	—	—	—	—	○	●
	131	COS	YES	YES	—	—	—	—	○	●
	132	TAN	YES	YES	—	—	—	—	○	●
	147	SWAP	YES	YES	—	—	—	—	○	●
Clock operations	160	TCMP	—	YES	—	—	—	—	○	●
	161	TZCP	—	YES	—	—	—	—	○	●
	162	TADD	—	YES	—	—	—	—	○	●
	163	TSUB	—	YES	—	—	—	—	○	●
	166	TRD	—	YES	—	—	—	—	○	●
	167	TWR	—	YES	—	—	—	—	○	×
Gray	170	GRY	YES	YES	—	—	—	—	○	●
	171	GBIN	YES	YES	—	—	—	—	○	●
Contact comparison	224	LD=	YES	—	—	—	—	—	○	●
	225	LD>	YES	—	—	—	—	—	○	●
	226	LD<	YES	—	—	—	—	—	○	●
	228	LD<>	YES	—	—	—	—	—	○	●
	229	LD≤	YES	—	—	—	—	—	○	●
	230	LD≥	YES	—	—	—	—	—	○	●
	232	AND=	YES	—	—	—	—	—	○	●
	233	AND>	YES	—	—	—	—	—	○	●
	234	AND<	YES	—	—	—	—	—	○	●
	236	AND<>	YES	—	—	—	—	—	○	●
	237	AND≤	YES	—	—	—	—	—	○	●
	238	AND≥	YES	—	—	—	—	—	○	●
	240	OR=	YES	—	—	—	—	—	○	●
	241	OR>	YES	—	—	—	—	—	○	●
	242	OR<	YES	—	—	—	—	—	○	●
	244	OR<>	YES	—	—	—	—	—	○	●
	245	OR≤	YES	—	—	—	—	—	○	●
	246	OR≥	YES	—	—	—	—	—	○	●

● : Supported by ladder logic test tool (LLT).
× : Not supported by ladder logic test tool (LLT).
○ : Instruction supported by the actual PLC.
△ : FX0, FX0S, and FX0N actual PLCs do not support pulse-executed instructions.
— : Instruction not supported by the actual PLC.

Appendix 3 List of Devices Usable with the I/O System Settings

Some devices designated in the condition setting area and simulation device area by the I/O system settings are subject to restrictions.
A list of the devices which can be used with the I/O system settings is shown below.

(1) Condition Area

Device Name			Function		
			A Series CPU	QnA Series CPU	FX Series CPU
Bit device	Input (X)		○	○	○
	Output (Y)		○	○	○
	Internal relay (M)		○	○	○
	Latch relay (L)			○	○	–
	Step relay (S)			–	–
	Step relay (S) (for SFC)		–	×	–
	State (S)		–	–	○
	Annunciator (F)		○	○	–
	Edge relay (V)		–	○	–
	Link special relay (SB)		–	○	–
	Link relay (B)		○	○	–
	Special relay	(M)	○	–	○
		(SM)	–	○	–
	Timer (T)	Contacts	○ *1	○ *1	○ *1
		Coil	×	×	×
	Retentive timer (ST)	Contacts	–	○ *1	○ *1,*2
		Coil	–	×	×
	Counter (C)	Contacts	○ *1	○ *1	○ *1
		Coil	×	×	×
	Function input (FX)		–	○	–
	Function output (FY)		–	○	–
	Link input (Jn\X)		–	×	–
	Link output (Jn\Y)		–	×	–
	Link relay (Jn\B)		–	×	–
	Link special relay (Jn\SB)		–	×	–
	SFC block (BL)		–	×	–
	SFC transition device(TR)		–	×	–
Word device	Data register (D)		○	○	○
	Special register	(D)	○	–	○
		(SD)	–	○	–
	Link register (W)		○	○	–
	Link special register (SW)		–	○	–

○.....Can be used
×.....Cannot be used
–.....Not supported
*1 : Only T, ST, and C contacts can be designated.
*2 : In the FX Series, the device name becomes "T".

Device Name			Function		
			A Series CPU	QnA Series CPU	FX Series CPU
Word device	Timer (present value) (T)		×	×	×
	Retentive timer (present value) (ST)		—	×	—
	Counter (present value) (C)		×	×	×
	Function register (FD)		—	×	—
	File register (R or D)		○	×	○
	Extension file register	(ER)	×	—	—
		(ZR)	—	○	—
	Buffer register (Un\G)		—	×	—
	Link register (Jn\W)		—	×	—
	Link direct device (Jn\SW)		—	×	—
	Index register	(Z)	○	○	○
		(V)	○	—	○
	Accumulator (A)		○	—	—

○.....Can be used
×.....Cannot be used
—.....Not supported

(2) Simulation Device Area

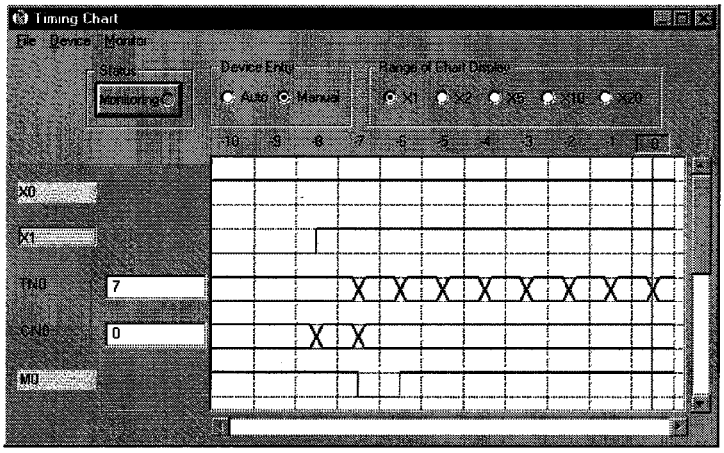
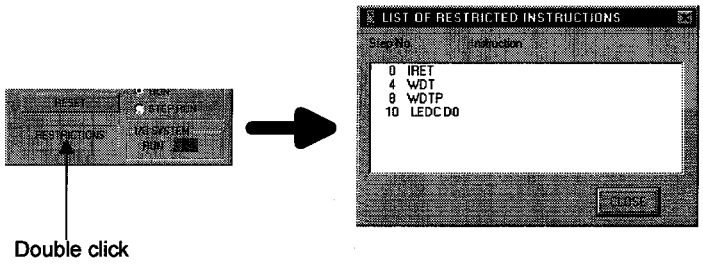
Device Name			Function		
			A Series CPU	QnA Series CPU	FX Series CPU
Bit device	Input (X)		○	○	○
	Output (Y)		○	○	○
	Internal relay (M)		○	○	○
	Latch relay (L)			○	–
	Step relay (S)			–	–
	Step relay (S) (for SFC)		–	×	–
	State (S)		–	–	○
	Annunciator (F)		○	○	–
	Edge relay (V)		–	○	–
	Link special relay (SB)		–	○	–
	Link relay (B)		○	○	–
	Special relay	(M)	○	–	○
		(SM)	–	○	–
	Timer (T)	Contacts	×	×	×
		Coil	×	×	×
	Retentive timer (ST)	Contacts	–	×	×
		Coil	–	×	×
	Counter (C)	Contacts	×	×	×
		Coil	×	×	×
	Function input (FX)		–	○	–
	Function output (FY)		–	○	–
	Link input (Jn\X)		–	×	–
	Link output (Jn\Y)		–	×	–
	Link relay (Jn\B)		–	×	–
	Link special relay (Jn\SB)		–	×	–
	SFC block (BL)		–	×	–
	SFC transition device(TR)		–	×	–

○.....Can be used
×.....Cannot be used
–.....Not supported

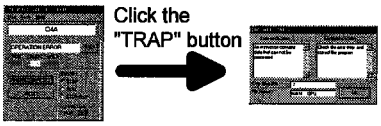
Appendix 4 Comparison between SW3D5-LLT-E and SW2D5-LLT-E

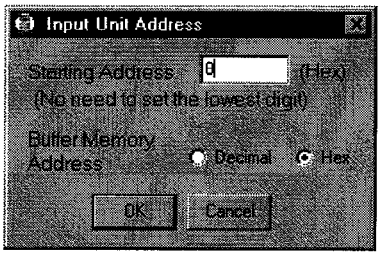
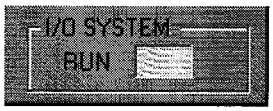
The following table describes the functions added and improved in the ladder logic test tool (LLT) as upgrade from SW2D5-LLT-E to SW3D5-LLT-E took place.

(1) List of the additional functions of SW3D5-LLT-E

Function	Description
Timing chart display	Function to visually show ON/OFF status of the bit device and the change in value of the word device. 
Unsupported information display	Displays instructions which are not supported in the ladder logic test tool (LLC) with step numbers attached to these instructions. 
Functions equivalent to WDT	Function to issue WDT error when sequence program is written in such a way that it falls into infinite loop.
Motion controller CPU function	Supports three types of motion controller CPU: A171SH, A172SH, and A273UH (S3).
CPU board compatible	• CPU board (A80BD-A2USH-S1) compatible • Select A2USH-S1 on the selection of CPU type if a CPU board is used.

(2) List of the Improved functions of SW3D5-LLT-E

<table>
<tr><th>Function</th><th>Description of SW2D5-LLT-E Operation</th><th>Description of SW3D5-LLT-E Operation</th><th>Applicable CPU</th></tr>
<tr><td>Error detail display</td><td>When an error occurs, an LED similar to the sequencer CPU is displayed on the initial screen of the ladder logic test tool (LLT).</td><td>In addition to the conventional LED display, further details of error (error description, error step, error fail name) are displayed.
 
Click the "TRAP" button</td><td>● ACPU
● QnACPU
● FXCPU
● Motion controller CPU</td></tr>
<tr><td>Buffer memory batch monitor</td><td>The buffer memory of the A Series CPU can be displayed and changed only on the device memory monitor of the ladder logic test tool functions (LLT).</td><td>The buffer memory of the A Series CPU can be displayed also on GPPW buffer memory batch monitor.</td><td>● ACPU</td></tr>
<tr><td>Device range check
Device range check in I/O system settings</td><td>It is checked in the A4UCPU device range when the A Series CPU is selected and in the Q4ACPU device range when the QnA Series CPU is selected.</td><td>For rigor error check, the device range is checked depending on the types and parameters of CPU.</td><td>● ACPU
● QnACPU
● Motion controller CPU</td></tr>
<tr><td>Supporting LEDA instruction</td><td>● LEDA (display instruction) is not supported.
● Dedicated instruction using LEDA is partially supported.</td><td>LEDA instruction is rigorously checked by distinguishing whether the instruction is a display instruction or a dedicated instruction depending on the selected A Series CPU type.
The following table lists the LEDA display instructions that are supported by the ladder logic test tool (LLT).
<table><tr><th>Applicable CPU</th><th>Display Instruction</th></tr><tr><td>A Series CPU other than AnA/AnU type</td><td>LEDA, LEDB, LED, LEDR</td></tr></table></td><td>● ACPU</td></tr>
<tr><td>Processing timer</td><td>END refresh turns ON the timer contact. Thus, this may differentiate computing timing from the actual result.</td><td>The timing for turning ON the timer contact is set when required conditions are met as it is done in a sequencer CPU.</td><td>● QnACPU</td></tr>
</table>

Function	Description of SW2D5-LLT-E Operation	Description of SW3D5-LLT-E Operation	Applicable CPU
Buffer memory display format	An address is always displayed in decimal number when the buffer memory is monitored in device memory monitor.	The buffer memory address can be displayed in either decimal or hexadecimal numbers. 	• ACPU • QnACPU • FXCPU • Motion controller CPU
Operating/Non-operating indicator for I/O system setting	In order to check whether the I/O system setting is operating, the menu of the ladder logic test tool (LLT) initial screen must be selected, then operation must be confirmed.	The operating status can be checked at the I/O system setting LED of the ladder logic test tool (LLT) initial screen. The I/O system setting LED shows that device value may be changed by I/O system setting. 	• ACPU • QnACPU • FXCPU • Motion controller CPU

MEMO

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Ladder Logic Test Function software for Windows
SW3D5C-LLT-E(V)
SW3D5F-LLT-E(V)
Operating Manual

MODEL	SW3D5C-LLT-O-E
MODEL CODE	13J952
IB(NA)-0800001-A(9904)MEE	

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