Introduction

Thank you for purchasing the Mitsubishi general-purpose MELSEC series sequencer.
Read this manual and make sure you understand the functions and performance of MELSEC series sequencer thoroughly in advance to ensure correct use.
Please make this manual available to the end user.

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Appendix 3 Using Data of Other Applications

3.1 Using Excel Files as Device Comments

A	QnA	FX
•	•	•

[Purpose]

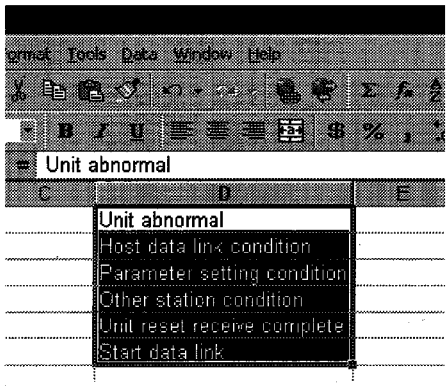
Uses data created with Excel as device comments.

[Operating Procedure]

This explanation assumes that you have already started up Excel and GPPW.

(1) Drag the Excel cell and designate the range that will enable it to be used as a comment in GPPW.

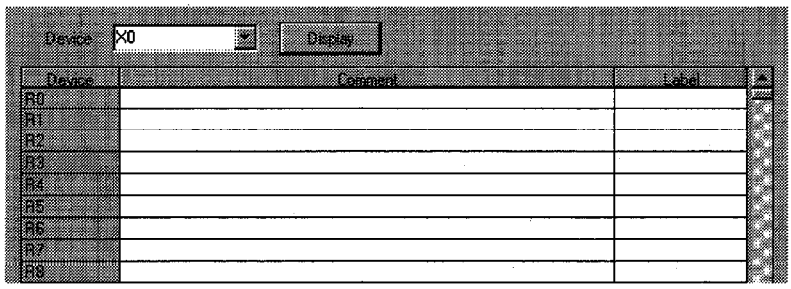
(Operation in Excel)



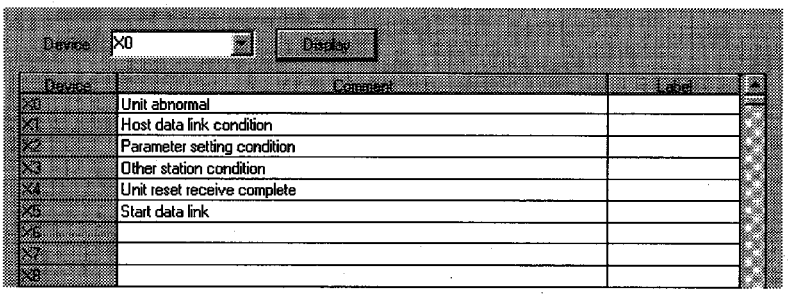
(2) In Excel, select [Edit] → [Copy], or click (Ctrl + C).

(3) Click the position where the comment is to be pasted and move the cursor.

(Operation at GPPW)



(4) In GPPW, select [Edit] → [Paste], or click (Ctrl + V) to paste the Excel comment to GPPW.



3.2 Using a Word File as a Device Comment

A	QnA	FX
•	•	•

[Purpose]

Uses data created in Word as device comments.

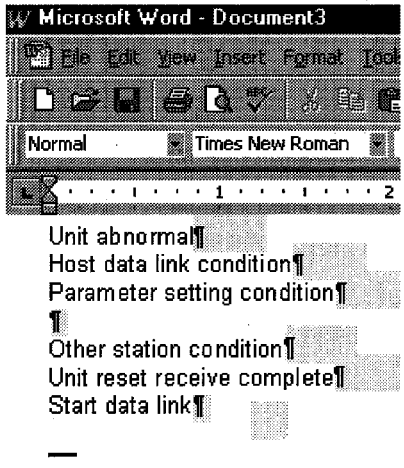
[Operating Procedure]

This explanation assumes that you have already started up Word and GPPW.

(1) Enter the comments in Word.
After each device comment, press the Enter key to insert a carriage return.

(2) Drag the created comments and designate the range for their use as GPPW comments.

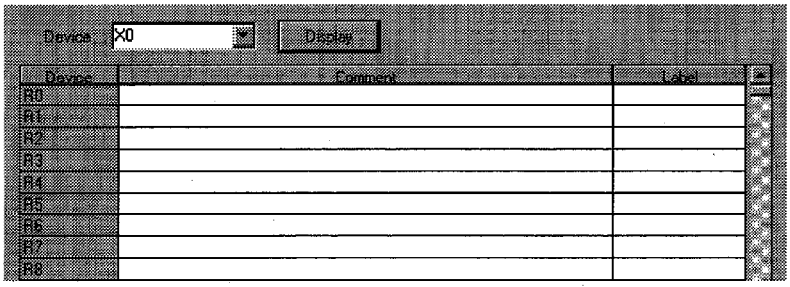
(Operation in Word)



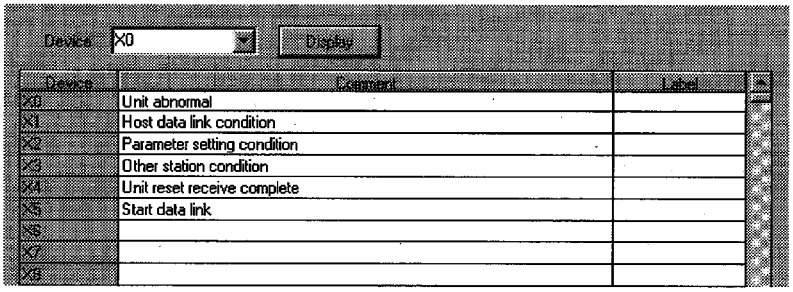
(2) In Word, select [Edit] → [Copy], or click (Ctrl + C).

(3) Click the location where the comment is to be pasted and move the cursor.

(Operation at GPPW)



(4) In GPPW, select [Edit] → [Paste], or click (Ctrl + V) to paste the Word comment in GPPW.



POINTS

- When entering device comments, inserting a carriage return between two comments makes one line of the comment table blank.
- When creating comments in Word, if they are entered continuously without carriage returns they are handled as a single comment: always insert carriage returns between individual comments.

Appendix 4 Restrictions Depending on PLC Type Change

The restrictions on PLC parameters and network parameters when the PLC type has been changed are indicated below.

4.1 A series - Changing to the A series

A	QnA	FX
•	×	×

Item		A Series	QnA Series
PLC parameters	Memory capacity	• If the capacity before the change is smaller than the maximum memory capacity of the PLC type changed to, the memory capacity before the change is used. • If it is larger than the maximum memory capacity of the PLC type changed to, the maximum memory capacity of the PLC type is used. (1) When the change is to a PLC type that cannot create subprograms, subprograms are deleted. (2) If the program capacity decreases, the number of program steps is cut to match the capacity. • If sequence and microcomputer programs exceed the capacity of the PLC type changed to, the microcomputer capacity is set to "0." For details, see Appendix 1.	-
	PLC system PLC RAS Device setting I/O allocations	If the same item or range exists at the PLC changed to, the data before the change is retained. However, if, as a result of the PLC type change, there are devices that cannot be used at the PLC changed to, the default is set. For details, see Appendix 1.	-
Network parameters	MELSECNET MELSECNET II MELSECNET II combination MELSECNET/10 MELSECNET/ MINI	For details, see Appendix 2.	With the QnA series, the data before the change is retained.
Sequence programs		Devices outside the range of the PLC can be displayed. If there are devices outside the range that the PLC can handle, an error occurs if they are written to the PLC without correction.	-

The table shows whether the PLC parameter and network parameter settings are retained as the settings before the change, or returned to their defaults, as a result of the PLC type change.

• : Retain settings before the change
- : Settings before change are defaults

Table 1 PLC Parameters

After the change / Before the change	A0J2H	A1FX	A1N	A2N, A2N-S1	A3N	A1S, A1SJ	A1SH, A1SJH	A2S	A2SH	A2C, A2CJ	A2A, A2A-S1	A3A	A2USH-S1	A2U, A2U-S1, A2US, A2US-S1	A3U	A4U	A2AS-S30	A2AS-S60	A2AS(S1)	A2SH(S1)
A0J2H	•	-	•	•	•	-	•	•	•	-	-	-	-	-	-	-	-	-	-	-
A1FX	-	•	-	•	•	-	•	•	•	-	-	-	-	-	-	-	-	-	-	-
A1N	•	-	•	•	•	•	•	•	•	-	-	-	-	-	-	-	-	-	-	-
A2N A2N-S1	-	-	-	•	•	-	•	•	•	-	-	-	-	-	-	-	-	-	-	-
A3N A2SH(S1)	-	-	-	-	•	-	-	-	-	-	-	-	-	-	-	-	-	-	-	•
A1S A1SJ	-	-	-	•	•	•	•	•	•	-	-	-	-	-	-	-	-	-	-	-
A1SH A1SJH	-	-	-	-	•	-	•	-	•	-	-	-	-	-	-	-	-	-	-	-
A2S	-	-	-	•	•	-	•	•	•	-	-	-	-	-	-	-	-	-	-	-
A2SH	-	-	-	-	•	-	•		•	-	-	-	-	-	-	-	-	-	-	-
A2C A2CJ	-	-	-	-	-	-	-	-	-	•	-	-	-	-	-	-	-	-	-	-
A2A A2A-S1	-	-	-	-	-	-	-	-	-	-	•	•	•	•	•	•	-	-	-	-
A3A	-	-	-	-	-	-	-	-	-	-	-	•	•	•	•	•	-	-	-	-
A2U A2U-S1 A2US A2US-S1 A2AS(S1)	-	-	-	-	-	-	-	-	-	-	-	-	•	•	•	•	-	-	•	-
A2USH-S1	-	-	-	-	-	-	-	-	-	-	-	-	•	•	•	•	-	-	-	-
A3U A2AS-S30 A2AS-S60	-	-	-	-	-	-	-	-	-	-	-	-	-	-	•	•	•	•	-	-
A4U	-	-	-	-	-	-	-	-	-	-	-	-	-	-	•	•	-	-	-	

Table 2 Network Parameters

CPU Type	Explanation
A0J2H,A1N,A2N,A2N-S1,A3N,A1S,A1SJ,A1SH,A1SJH A2S,A2SH,A2C,A2CJ,A2SH(S1)	All the network parameters between PLCs indicated to the left are retained.
A2A,A2A-S1,A3A	All the network parameters between PLCs indicated to the left are retained.
A2U,A2U-S1,A2US,A2US-S1,A2USH-S1,A3U,A4U A4U,A2AS(S1),A2AS-30,A2AS-60	All the network parameters between PLCs indicated to the left are retained.

If there is even one module among the types A2U, A2U-S1, A2US, A2US-S1, A2USH-S1, A3U, and A4U for which the first network I/O number exceeds the actual I/O range of the PLC changed to, the first I/O numbers are automatically allocated to 0H, 20H, 40H, 60H.

4.2 Changing Between A Series and QnA Series

A	QnA	FX
•	×	×

The effects on the parameter settings when the PLC type is changed from the A series to the QnA series, or from the QnA series to the A series are described below.

<table>
<tr><th></th><th colspan="3">Change from A to QnA</th><th colspan="3">Change from QnA to A</th></tr>
<tr><td>Memory capacity</td><td colspan="3">No change</td><td colspan="3">The maximum capacity of the PLC changed to is set for MAIN, SUB1, SUB2, and SUB3. Comments, extension comments, etc. are returned to their default settings.</td></tr>
<tr><td rowspan="12">Latch range</td><td colspan="3">The devices subject to change are T, C, D, B, and W.
A series setting items are changed in the ranges indicated below.</td><td colspan="3">The devices subject to change are T, C, D, B, and W.
QnA series setting items are changed in the ranges indicated below.</td></tr>
<tr><td>A series</td><td>→</td><td>QnA series</td><td>QnA</td><td>→</td><td>A</td></tr>
<tr><td>L</td><td rowspan="11">→</td><td>No change</td><td>B</td><td rowspan="11">→</td><td>B</td></tr>
<tr><td>Extension counters</td><td>No change</td><td>F</td><td>Not subject to change</td></tr>
<tr><td>Retentive timers</td><td>No change</td><td>V</td><td>Not subject to change</td></tr>
<tr><td>C latch range</td><td>C latch range</td><td>T</td><td>Low speed timers</td></tr>
<tr><td>D latch range</td><td>D latch range</td><td>ST</td><td>Not subject to change</td></tr>
<tr><td>B latch range</td><td>B latch range</td><td>C</td><td>C</td></tr>
<tr><td>W latch range</td><td>W latch range</td><td>D</td><td>D</td></tr>
<tr><td rowspan="2">Lowest device number of:
Low-speed timers
High-speed timers
Extension low-speed timers
Extension high-speed timers</td><td rowspan="2">Head of T latch range</td><td>W</td><td>W</td></tr>
<tr><td colspan="2" rowspan="2">[Restrictions when changing from QnA to A]
When changing from QnA to A, it may happen that the change exceeds the A device range; when device numbers exceed the ACPU device range, the maximum value for that device is set.</td></tr>
<tr><td>Highest device number of:
Low-speed timers
High-speed timers
Extension low-speed timers
Extension high-speed timers</td><td>End of T latch range</td></tr>
<tr><td>I/O allocation</td><td colspan="3">The set data is used without change</td><td colspan="3">The set data is used without change</td></tr>
<tr><td></td><td>Slots 0 to 511 (for AnUCPU)</td><td>→</td><td>Slots 0 to 63</td><td>Slots 0 to 511 (for AnUCPU)</td><td>→</td><td>Slots 0 to 63</td></tr>
</table>

<table>
<tr><th></th><th colspan="3">Change from A to QnA</th><th colspan="3">Change from QnA to A</th></tr>
<tr><td rowspan="5">Network parameters
MELSECNET (II, /10)</td><td>A series</td><td>→</td><td>QnA series</td><td>QnA series</td><td>→</td><td>A series</td></tr>
<tr><td>AnACPU,AnNCPU</td><td rowspan="3">→</td><td>The set data is used without change. *1</td><td rowspan="4">All QnACPU models (including Q4ARCPU)</td><td rowspan="4">→</td><td>For the network type, MELSECNET master, and MELSECNET combination master, the QnA series data is used without change.</td></tr>
<tr><td>AnUCPU</td><td>The set data is used without change.</td><td>The network type, MELSECNET master, MELSECNET combination master, and MELSECNET II data are used unchanged as QnA series data.</td></tr>
<tr><td colspan="3">*1 : When changing from AnNCPU/AnACPU to QnACPU, make the first I/O number of the network module "00H." (Because in the network parameters of AnNCPU and AnACPU, there is no "first module I/O number".)</td><td>When changing to AnUCPU, any data set for the items indicated below is deleted.
SB → SB and SW → SW refresh in the refresh parameters for MELSECNET/10 (standby station), MELSECNET/10 (multiplex remote master station), MELSECNET (parallel remote master station), MELSECNET/10 (multiplex remote substation), multiplex/10 (parallel remote substation), Ethernet; and CC-Link are cleared.
Apart from these items, the data set with GPPQ is used without change</td></tr>
<tr><td colspan="3"></td></tr>
<tr><td>MELSECNET/MINI</td><td colspan="3">All settings are retained.</td><td colspan="3">All settings are retained.
However, in the event of a line error there is no send status so the setting is deleted.</td></tr>
</table>

4.3 FX Series Changing to the FX Series

A	QnA	FX
×	×	•

		Details
PLC parameters	Memory capacity	If the maximum capacity of the PLC type changed to is smaller than the maximum capacity of the PLC type changed from, the maximum capacity value is set. If the capacity can be changed, you are prompted to specify the details of the change in a dialog box.
	Comment capacity	If the PLC type changed to is not compatible with this function, it is set to 0 blocks. If it is compatible, you are prompted to specify the details of the change in a dialog box.
	File register capacity	
Sequence programs		• If a program in the PLC type changed from includes device numbers and application instructions that are not compatible with the PLC type changed to, the program contents cannot be corrected. Correct to an appropriate program either before the change or after the change. (If the program before the change is transmitted to the programmable controller, a program error occurs.) • The excess part of the program after the change is deleted. • If an FX0 or FX0S is designated as the PLC changed to, the memory capacity is set to 2000 but the part that exceeds the actual number of steps of these programmable controllers - which is 800 - is deleted. • The device numbers of file registers and RAM file registers are used without change. After the PLC type change, change them to appropriate device numbers using, for example, a device search.

The table shows the details of changes to each item in FX.FX conversions.

◎ The settings before the change are retained.
● The defaults of the PLC type changed to are set.
□ Changed to this value.
★ Change can be designated in a dialog box

Change Type	Memory Capacity	Comment 1 Capacity	File Rregister Capacity	Latch Range	Entry Code	Title	PLC mode: Serial Setting	I/O Allocations
FX2N → FXU/FX2C	★ (2000 to 8000)	★	★	◎	◎	◎	●	◎
FX2N → FX1	★ (2000 to 4000)	★	● (Block 0)	●	◎	◎	●	●
FX2N → FX0N	□ (Set to 2000)	★	★	●	◎	◎	●	●
FX2N → FX0/0S	□ (Set to 2000)	● (Block 0)	● (Block 0)	●	◎	●	●	●
FXU/FX2C → FX2N	★ (2000 to 16000)	★	★	◎	◎	◎	●	◎
FXU/FX2C → FX1	□ (Set to 2000)	★	● (Block 0)	●	◎	◎	●	●
FXU/FX2C → FX0N	□ (Set to 2000)	★	★	●	◎	◎	●	●
FXU/FX2C → FX0/0S	□ (Set to 2000)	● (Block 0)	● (Block 0)	●	◎	●	●	●
FX1 → FX2N	★ (2000 to 16000)	★	★	◎	◎	◎	●	●
FX1 → FXU/FX2C	★ (2000 to 8000)	★	★	◎	◎	◎	●	●
FX1 → FX0N	□ (Set to 2000)	★	★	●	◎	◎	●	●
FX1 → FX0/0S	□ (Set to 2000)	● (Block 0)	● (Block 0)	●	◎	●	●	●
FX0N → FX2N	★ (2000 to 16000)	★	★	◎	◎	◎	●	●
FX0N → FXU/FX2C	★ (2000 to 8000)	★	★	◎	◎	◎	●	●
FX0N → FX1	★ (2000 to 4000)	★	● (Block 0)	●	◎	◎	●	●
FX0N → FX0/0S	□ (Set to 2000)	● (Block 0)	● (Block 0)	●	◎	●	●	●
FX0/0S → FX2N	★ (2000 to 16000)	★	★	◎	◎	●	●	●
FX0/0S → FXU/FX2C	★ (2000 to 8000)	★	★	◎	◎	●	●	●
FX0/0S → FX1	★ (2000 to 4000)	★	● (Block 0)	◎	◎	●	●	●
FX0/0S → FX0N	◎	★	★	◎	◎	●	●	●

4.4 A Series Changing to FX Series

A	QnA	FX
•	×	•

		Change from A to FX	Change from FX to A
PLC parameters	Memory capacity	Made the maximum capacity of the PLC designated as the type changed to	
	File register capacity	0 blocks	Made the default of the PLC designated as the type changed to
	Comment capacity		
	Network parameters	Cannot be changed since they do not exist at FX.	Made the default of the PLC designated as the type changed to
Sequence program		• The dedicated instructions of AnA and AnU cannot be changed. • The excess part of the program after the change is deleted. • Devices that do not exist in the A series are all changed to M9255/D9255. • Devices that do not exist in the FX series are all changed to M8255/D8255. • Instructions that do not exist in the A series are all changed to OUT M9255. However, the LDP, LDF, ORP, ORF, ANDP, and ANDF instructions become contact instructions without P or F, and the devices are changed to M9255. INV is changed to AND M9255, and STL is changed to OUT M9255. • Instructions that do not exist in the FX series are all changed to OUT M8255. • For devices changed to M9255/D9255 or M8255/D8255, change the device number as appropriate, e.g. by conducting a device search. However, when using an FX0, FX0S, FX0N, or FX1 CPU, it is not possible to conduct a search for these device numbers and a device check must therefore be executed under the program check function.	
Statement (ladder comment) Note (coil comment)		Not altered in the change. However, the range that exceeds the capacity is deleted.	
Device comments Device memory		Not altered in the change. However, devices that do not exist in the PLC changed to, and data that exceed the available range, are deleted.	

Appendix 5 RS-232C Cable Setting Method to C24, UC24, and QC24

5.1 RS-232C Cable Setting Method to C24 and UC24

A	QnA	FX
•	•	×

- Connection of RS-232C interface

(1) When a 25-pin connector is used in a computer link module

Computer Link Module Side			GPPW Side
Signal Name	Pin No.		Signal Name
FG	1	⟷	FG
SD(TXD)	2	→	SD(TXD)
RD(RXD)	3	←	RD(RXD)
RS	4	⟷	RS
CS(CTS)	5	←	CS(CTS)
DSR(DR)	6	→	DSR(DR)
SG	7	⟷	SG
CD	8	→	CD
DTR(ER)	20	←	DTR(ER)

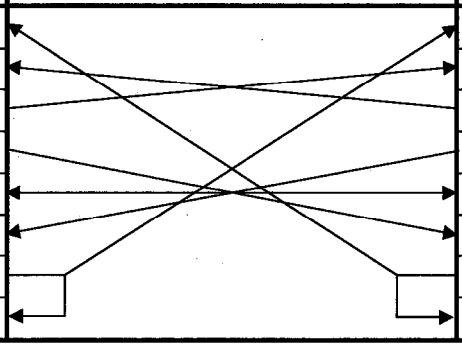
(2) When a 25-pin connector is used in a computer link module

If the connection between the computer link module and the GPPW is made in the manner shown below, designate "without CD terminal check".

Computer Link Module Side			GPPW Side
Signal Name	Pin No.		Signal Name
FG	1	⟷	FG
SD(TXD)	2	→	SD(TXD)
RD(RXD)	3	←	RD(RXD)
RS	4	⟷	RS
CS(CTS)	5	⟷	CS(CTS)
DSR(DR)	6	→	DSR(DR)
SG	7	⟷	SG
CD	8		CD
DTR(ER)	20	←	DTR(ER)

Buffer memory setting
CD terminal check (address 10Bh): Without check
DTR control (address 11Ah): Yes (C24-S8, UC24)

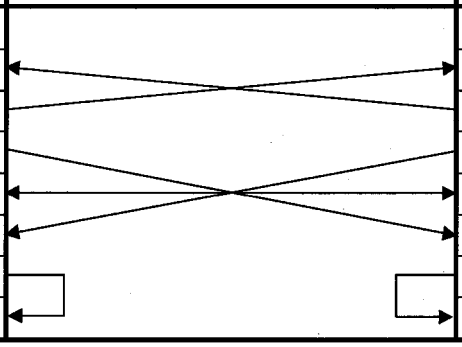
(3) When an 9-pin connector is used in a computer link module
(Example of connection)

Computer Link Module Side		Cable Connection and Signal Direction	External Device Side
Signal Name	Pin No.		Signal Name
CD	1		CD
RD(RXD)	2		RD(RXD)
SD(TXD)	3		SD(TXD)
DTR(ER)	4		DTR(ER)
SG	5		SG
DSR(DR)	6		DSR(DR)
RS(RTS)	7		RS(RTS)
CS(CTS)	8		CS(CTS)

Set "without CD terminal check".

(4) When an 9-pin connector is used in a computer link module

(Example of connection)

Computer Link Module Side		Cable Connection and Signal Direction	External Device Side
Signal Name	Pin No.		Signal Name
CD	1		CD
RD(RXD)	2		RD(RXD)
SD(TXD)	3		SD(TXD)
DTR(ER)	4		DTR(ER)
SG	5		SG
DSR(DR)	6		DSR(DR)
RS(RTS)	7		RS(RTS)
CS(CTS)	8		CS(CTS)

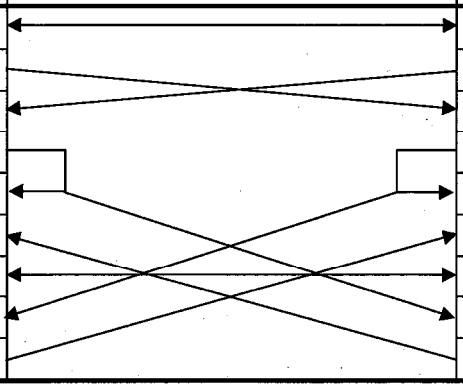
*: DC code control or DTR/DSR control is enabled by connecting the DTR and DSR signals of the computer link module to an external device as shown above.

5.2 RS-232C Cable Setting Method to QC24

A	QnA	FX
×	•	×

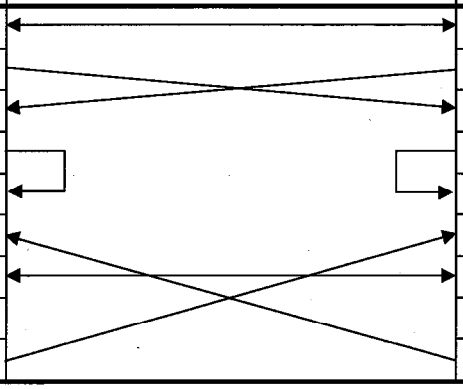
(1) For large-scale QC24 (N)

(a) Example of connection to an external device that allows the CD signal (No. 8 pin) to be turned ON/OFF

Large-scale QC24 (N) Side		Cable Connection and Signal Direction (Full-/Half-Duplex Communication)	External Device Side
Signal Name	Pin No.		Signal Name
FG	1		FG
SD(TXD)	2		SD(TXD)
RD(RXD)	3		RD(RXD)
RS	4		RS
CS(CTS)	5		CS(CTS)
DSR(DR)	6		DSR(DR)
SG	7		SG
CD	8		CD
DTR(ER)	20		DTR(ER)

DC code control or DTR/DSR control is enabled by connecting the QC24 (N) to an external device as shown above.

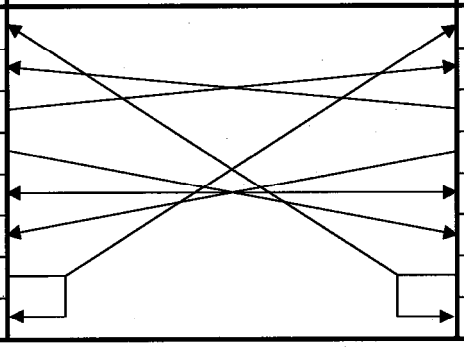
(b) Example of connection to an external device that does not allow the CD signal (No. 8 pin) to be turned ON/OFF

Large-scale QC24 (N) Side		Cable Connection and Signal Direction (Full-Duplex Communication)	External Device Side
Signal Name	Pin No.		Signal Name
FG	1		FG
SD(TXD)	2		SD(TXD)
RD(RXD)	3		RD(RXD)
RS	4		RS
CS(CTS)	5		CS(CTS)
DSR(DR)	6		DSR(DR)
SG	7		SG
CD	8		CD
DTR(ER)	20		DTR(ER)

DC code control or DTR/DSR control is enabled by connecting the QC24 (N) to an external device as shown above.

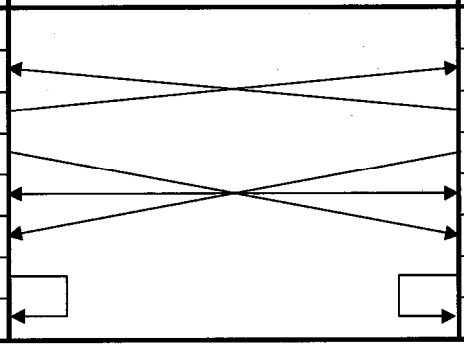
(2) For compact QC24 (N)

(a) Example of connection to an external device that allows the CD signal (No. 1 pin) to be turned ON/OFF

Compact QC24 (N) Side		Cable Connection and Signal Direction (Full- / Half-Duplex Communication)	External Device Side
Signal Name	Pin No.		Signal Name
CD	1		CD
RD(RXD)	2		RD(RXD)
SD(TXD)	3		SD(TXD)
DTR(ER)	4		DTR(ER)
SG	5		SG
DSR(DR)	6		DSR(DR)
RS(RTS)	7		RS(RTS)
CS(CTS)	8		CS(CTS)

DC code control or DTR/DSR control is enabled by connecting the QC24 (N) to an external device as shown above.

(b) Example of connection to an external device that does not allow the CD signal (No. 1 pin) to be turned ON/OFF

Large-scale QC24 (N) Side		Cable Connection and Signal Direction (Full-Duplex Communication)	External Device Side
Signal Name	Pin No.		Signal Name
CD	1		CD
RD(RXD)	2		RD(RXD)
SD(TXD)	3		SD(TXD)
DTR(ER)	4		DTR(ER)
SG	5		SG
DSR(DR)	6		DSR(DR)
RS(RTS)	7		RS(RTS)
CS(CTS)	8		CS(CTS)

DC code control or DTR/DSR control is enabled by connecting the QC24 (N) to an external device as shown above.

Appendix 6 ROM Writer Wiring Examples

A	QnA	FX
•	×	•

The wiring of the RS-232C cable that connects a peripheral device and ROM writer is shown here.
Make the cable used for the wiring shown below yourself in accordance with the specifications of the ROM writer to be used.

Peripheral Device		Cable Connection and Signal Direction	ROM WRITER	
Signal Name	Pin No.		Pin No.	Signal Name
FG	–		1	FG
SD	3		2	SD
RD	2		3	RD
RST	7		4	RTS
CTS	8		5	CTS
DSR	6		6	DSR
SG	5		7	SG
DTR	4		20	DTR

An example of wiring of the RS-232C cable that connects a peripheral device and ROM writer is shown here.
If RTS and CTS are not used at the ROM writer side, short RTS and CTS at the peripheral device side.

Appendix 7 QnA Series Version Compatibility Table

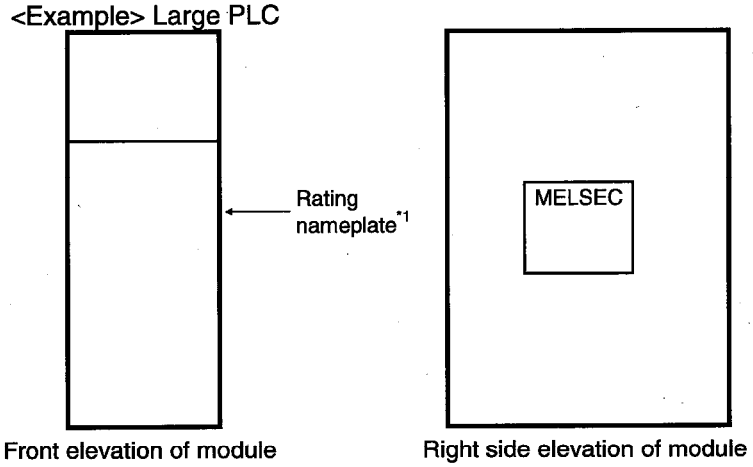
A	QnA	FX
×	•	×

Restrictions apply to each version of QnACPU (with the exception of Q4ARCPU) modules, Ethernet interface modules, and CC-Link system master and local modules with regard to the use of the following functions, which are described in this manual. If the module you are using is the version in the table or a later version, the corresponding function can be used.

Module / Function	PLC	Ethernet	CC-Link
	Q2ACPU,Q2AS1CPU,Q3ACPU,Q4ACPU,Q2AS(H)CPU,Q2AS(H)S1	AJ71QE71(B5), A1SJ71QE71-B2, A1SJ71QE71-B5	AJ61QBT11, A1SJ61QBT11
Local device Monitoring/testing	9707B or later	-	-
High-speed communication	9707B or later	-	-
Ethernet parameters	9707B or later	9707B or later	-
CC-Link parameters	9707B or later	-	9707B or later

- : Irrelevant function

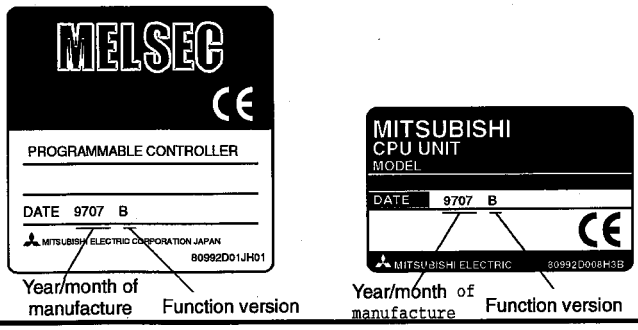
- Positioning of rating nameplate
  <Example> Large PLC



*1 : Some compact PLC have the rating nameplate affixed to their left side.

POINT

- When using the functions above, use a module that has the following code (9707B or later) inscribed in the DATE entry on the ratings nameplate.



Appendix 8 Restrictions and Cautions

A	QnA	FX
•	•	•

The following is a list of restrictions and cautions to be observed when operating GPPW.
Read these restrictions before attempting GPPW operations.
The symbol "^" is appended to those restrictions in the list that also apply to GPPA/GPPQ.
Items in the list that are marked "<Caution>" are cautions relating to GPPW only.

[Interpreting the Lists]
Example:

GPPA	GPPQ
•	-

.....Indicates that the restriction when using ACPU with GPPW is the same as that which applies when using GPPA.

GPPA	GPPQ
• <Caution>	-

.....Indicates that the caution when using ACPU with GPPW is the same as that which applies when using GPPA.

GPPA	GPPQ
- <Caution>	-

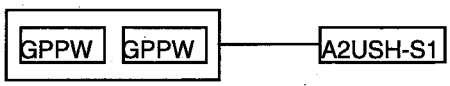
.....Indicates that the caution when using ACPU with GPPW is exclusive to GPPW.

Item	Restrictions/Cautions	GPPA	GPPQ
Comment reading/writing	When editing comments there is no particular need to set a comment capacity. However, an error is displayed on writing to the CPU if no capacity is found to be set on checking the parameters of the peripheral device.	- <Caution>	-
	When extension comments have been designated for a program created with GPPA (valid program setting), when these extension comments are read by GPPW, they are assigned to common comments regardless of the GPPA designation.	- <Caution>	-
	When a file created with ACPU or GPPA is written to GPPW, if there is any duplication between the comments for common devices and extension comments, the extension comments take priority and therefore the common device comments cannot be read.	-	-
	When comments created with GPPW are written in GPPA format to the FD or HD of a peripheral device, the comments can be written regardless of the comment capacity in the parameters. The comments can be used when GPPA is started up by carrying out comment memory capacity setting, then reading the comments in the file maintenance mode.	•	-
	With GPPW, device comments and device memories can be created within the ranges designated in the parameters, but even after completing writing to the GPPQ format, it may not be possible to write to GPPQ. In this case the size of the data to be written must be reduced.	-	-
	When second half M comments for main and sub use are read to GPPW, since the range setting is included in S, they are allocated to S.	-	-

Item	Restrictions/Cautions	GPPA	GPPQ
Comment reading/writing	If X/Y comments 2 are written without range setting at GPPW, reading is carried out in accordance with the X and Y attributes respectively.	-	-
	The restriction on sub-system names is up to 10 characters for GPPQ and up to 8 characters for GPPW. On reading subsystem names from GPPQ format, they are shortened to 8 characters. If these subsystem names are written back to GPPQ, they are written as 8 characters.	-	•
	When peripheral statements/notes created with GPPQ are written to a PLC, they cannot be read out with GPPW; they must be read with GPPQ.	-	- <Caution>
	When comments are written in GPPA format, one of the original files at the GPPA side is deleted. When writing comments 2, comments 1 are deleted; when writing comments 1, comments 2 are deleted.	- <Caution>	-
	When comments are written to an A1NCPU, if MAIN (program-classified comment) is selected when writing to the PLC, comments F0 to F127 are written unconditionally to the PLC, regardless of range selection. Reading is carried out in the same way.	- <Caution>	-
	When comments edited as comments 2 at GPPW are written to an ACPU/GPPA format file as comments 1, they are displayed as incorrect characters by GPPA.	- <Caution>	-
	When comments are written to an ACPU/GPPA format file, if a two-byte character starts at the 16th character (for comments 2)/15th character (for comments 1), writing is carried out with the 16th/15th character left blank.	-	-
Parameter setting	When using a memory cassette larger than A3MCA-18, if the total capacity - excluding extension comments - set in capacity setting in the parameters exceeds 144 K bytes, when the extension comments are written it may not be possible to write the second half. In this case the first half 1024 points must be divided into 64-point units.	•	-
	When local device or latch clear key valid/invalid designations are made in the parameters, set a range in device setting.	-	•
	When file registers are set, a file register capacity must be set in the parameters.	•	-
	When parameters for which no settings have been made with GPPA, or whose parameter screens have been opened in GPPA but then closed with "END" without making any settings, are verified - in GPPA - against GPPW parameters set in the same way, a verification mismatch may occur. The mismatch occurs due errors, for example, in the initial value data of blank items, but there is no difference in operation when the parameter data is written to a PLC and executed, so there is no problem in actual use.	-	-
	When file registers are designated in the MELSECNET/10 refresh parameter settings, a capacity setting must be made for file registers in the memory capacity settings.	•	-
	Since MELSECNET/10 network parameters store the time at which the parameter settings were made with GPPW, when network parameters are verified between GPPA/GPPQ and GPPW, the result my be a setting time mismatch even if the set data matches.	- <Caution>	•
	If MELSECNET/10 (multiplex remote master) or MNET/10 (parallel remote master) is set for four modules in the network parameters and these settings are written in GPPQ format and verified against the same parameter settings in GPPQ, a verification error will occur. Since the parameters themselves are correct, there is no problem in actual use.	-	-

<table>
<tr><th>Item</th><th>Restrictions/Cautions</th><th>GPPA</th><th>GPPQ</th></tr>
<tr><td rowspan="4">Parameter settings</td><td>If a blanks are set for "refresh parameters" and "link parameter constant scan (GPPA only)" in the GPPA/GPPQ and GPPW parameters, this is the same as settings of "0 points" and "0 ms." respectively at GPPA.</td><td>-</td><td>-</td></tr>
<tr><td>When the device settings are changed, the following files that have already been written to the PLC must be written again:
Sequence programs, SFC programs, monitor registration, sampling trace data, device initial values.</td><td>-</td><td>•</td></tr>
<tr><td>With regard to PLC data reading of the network parameters:
1. When parameters are set (written) in the PLC, the written parameters are read.
2. When parameters have not been set in the PLC, the actual link module mounting status detected by the PLC is read.</td><td>-</td><td>•</td></tr>
<tr><td>When verification against parameters created with SW0/IVD-GPPQ or SW1NX/IVD is executed, a "parameter mismatch" may occur even if the settings match.
If this happens, first read the parameters with SW2/IVD-GPPQ, then write the parameters again.</td><td>-</td><td>•</td></tr>
<tr><td>Change PLC type</td><td>To create a subsequence, a capacity of 2K or more must be set in the parameter mode.</td><td>•</td><td>-</td></tr>
<tr><td rowspan="4"></td><td>If a PLC type change is made to a PLC type that does not allow the creation of subprograms, subprograms are deleted.</td><td>-
<Caution></td><td>-</td></tr>
<tr><td>When a program is written to the PLC after changing the PLC type, out-of-range devices/instructions cause an error and cannot be written. When data is written to a GPPA format file and read with GPPA, instruction code abnormalities are displayed. The same applies when data is written to a GPPQ format file and read with GPPQ.</td><td>-</td><td>-</td></tr>
<tr><td>If the PLC type is changed in the network system shown below, all the network parameters before the change are retained.
However, in the case of AnUCPU, if there is even one module for which the first network I/O number exceeds the actual I/O range of the PLC type changed to, the first I/O numbers are automatically allocated to 0H, 20H, 40H, 60H (assuming there are four modules).
(Where A4U changes to A3U, A4U changes to A2U, A3U changes to A2U)
For changes between network systems, the changes are to the defaults.
<table>
<tr><th>Network system</th><th>PLC system</th></tr>
<tr><td>AnN systems</td><td>A0J2H system, A1N system, A2N system, A3N system, A1S system, A1SH system, A2S system, A2SH system, A2C system</td></tr>
<tr><td>AnA systems</td><td>A2A system, A3A system</td></tr>
<tr><td>AnU systems</td><td>A2U system, A2USH-S1 system, A3U system, A4U system</td></tr>
</table></td><td>-</td><td>-</td></tr>
<tr><td>If microcomputer programs cannot be accommodated when a PLC type change is made, all microcomputer programs are deleted.</td><td>-</td><td>-</td></tr>
<tr><td>If the capacity before the change is smaller than the maximum capacity of the PLC type changed to, the memory capacity is set as that before the change.
If it is larger than the maximum memory capacity of the PLC type to be changed to, the memory capacity is set as the maximum memory capacity of the PLC type changed to.</td><td>•</td><td>-</td></tr>
</table>

Item	Restrictions/Cautions	GPPA	GPPQ
Change PLC type	If the program capacity decreases, the programs are curtailed at the number of steps equivalent to the reduced capacity. (If this curtailment occurs part way through a ladder program, the entire block is eliminated.)	-	-
	If the sequence programs + microcomputer programs exceed the capacity of the PLC type changed to, the microcomputer program capacity is set to 0.	-	-
	To execute "PLC read" when connected to a CPU that is not in the PLC type list, carry out a PLC type change as follows. • When connecting to A1SCPU with a PLC type other than A1S at the GPPW side, read by changing the PLC type to A2N.	-	-
	When a PLC type change is executed, if there are devices that cannot be used at the PLC after the change, that range of devices is automatically deleted. (For the "A" series, this includes device comments.)	•	-
	When a PLC type change is executed, if a setting that exceeds the maximum device range for the PLC after the change is made, the setting is automatically changed to the maximum possible. (For the "A" series, this includes device comments.)	•	-
PLC type	A connected CPU that does not support A1, A2, or A3 is recognized as AnN but cannot be used.	-	-
Ladder input	The ladder block has 24 lines of parallel contacts and line insertion is not possible.	-	•
	The line return destination and source must have the same number. The same number cannot be used more than once. The line return numbers must be serial numbers. It is not possible to insert a ladder between the line return source and destination.	•	•
	If the contacts/coils to be overwritten straddle multiple contacts, ladder input is not possible.	-	•
	Inserting a contact in the first row does not make it possible to make an insertion at a line return.	-	•
	If a vertical line that crosses an instruction is drawn, conversion will not be possible.	-	•
	In a ladder block with two or more lines where an instruction cannot be accommodated on one line, you must create a line return and input the instruction on the next line.	-	-
	[Enter] When ladder information has been read into the key-in data field by pressing the [Enter] key, the cursor cannot be moved.	-	-
	The maximum number of instruction and device characters that can be written at one contact is eight. If the total number of characters is more than this, multiple rows must be used.	-	-
	If a vertical line that crosses a statement is drawn, a conversion error occurs on attempting conversion.	-	•
	A CHG instruction input check is not performed on programs of PLCs that do not allow the creation of subprograms, such as A2ACPU and A2UCPU. When the PLC is set to RUN an error occurs.	- <Caution>	-
Online change	When online change is executed with respect to an A4UMCA-128E memory cassette, the transmission may take several minutes. During the transmission, operation continues in accordance with the program before the change. After the transmission, sequence processing stops for a maximum of 2 seconds.	•	-
	When online change is executed with respect to an A3NCPU, the CHG instruction is automatically disabled. On completion of conversion, the CHG instruction is executed.	•	-
	During online change, RUN/STOP/PAUSE/STEP RUN key switch operations are prohibited.	•	•
	If there is a pulse instruction in the program to be written, the PLC does not execute this instruction after the PLC write operation. It is executed after its execution condition changes from OFF to ON.	•	•

Item	Restriction/Note	GPPA	GPPQ
Import file /Export file	Depending on the GPPA, there are versions that cannot be selected although the same model name exists in the PLC type list. If the PLC type is not represented with GPPA, change to a PLC type that is represented with GPPA (at GPPW) and then write the data. Example: GPPW side: Create with A2U □ change to A2A → SW0SRXV-GPPA side: write in GPPA format → treated as A2A	-	-
	Since they are not represented in the PLC type list at the GPPA side, files created with models such as A3HCPU cannot be read with GPPW. (It is not possible to read or write files of incompatible PLCs.)	-	-
	When a GPPA/GPPQ format program that contains an END instruction part way through is read to GPPW, the part of the program up to the END instruction is read. The part after the END instruction is not read.	-	-
	On reading a device memory from ACPU/GPPA format with GPPW, the information of the preceding coils of T/C devices is not read out, and consequently when the data is written again to ACPU/GPPA format and verified at GPPA, a preceding coil mismatch occurs.	-	-
Device test	When a forced set/reset operation is executed while the PLC is in the RUN state, program execution at the PLC is given priority.	•	•
	When an input (X) is forcibly reset, the PLC operates as though it were ON even if program input is OFF. If a process input is ON the PLC will process it as ON even if a forced reset is executed.	•	•
	The local device test requires a range to be set in the parameters in advance.	-	•
	Even if the present value is set to a smaller value than the set value after time up of a timer or counter, the time up status is retained.	•	•
PLC write/read	When a ladder with peripheral statements is written to a PLC, the statements are not written to the PLC, and the ladder must therefore be stored in the HD.	• <Caution>	• <Caution>
	When the PLC read dialog box is opened again after writing a ladder to the PLC and displaying the list, and then using another programming tool (GPPW/GPPA/GPPQ, etc.) to, for example, delete PLC data, the contents of the data list may differ from the current status of the PLC data. In this case the list must be updated.	-	-
PLC communication	When communicating with a PLC, no distinction is made between A2US(S1)CPU and A2U(S1)CPU, and therefore access to a CPU when using an A2US(S1)/A2U(S1) is dealt with as access to A2U(S1)CPU.	-	-
	PLC communication is not possible with a GPPW started up. PLC communication is possible with one of these only, under the conditions indicated below. • When GPPW is used, check if there is a system (control panel) COM port. If there is not, one must be registered. In this state, PLC communication using GPPA/GPPQ is not possible. • When using GPPA/GPPQ, eliminate the system (control panel) COM port. In this state, PLC communication using GPPW is not possible. • PLC communication with respect to A2USH-S1 with two GPPWs started up is not possible. 	-	-

Item	Restriction/Note	GPPA	GPPQ
TC set value	When a TC set value change is applied twice, the change is made to the first set value. If there is a duplicated set value change, the program contents must be checked in a program data check.	-	-
	Since GPPA allows reading/writing of T/C set values alone, there are T/C set values that are not used in the program. Since GPPW only reads and writes set values for T/C values that exist in the program, set values that do not exist in the program cannot be handled. (When T/C set values are read and written, unused T/C set values at an ACPU are deleted.)	-	-
	T/C set values used in SAP2 are not handled by GPPW and they are therefore cleared to 0 when written to an APC/GPPA format file.	-	-
Printing	Data is not printed and displayed in accordance with PAGEn (the designated No. becomes the printed page number).	-	-
	GPPA/ACPU print titles are not read/written.	-	-
	Since #CPU# prints the data for the CPU type from the designated position, if the CPU type exceeds 5 characters, blanks must be created at the rear.	-	-
File reading/writing	For file reading/writing with respect to a GPPA that does not allow selection of the same PLC model name, the PLC is treated as a PLC type within the range supported by the GPPA.	-	-
	Reading/writing to files created with SW0S is not possible.	-	-
Note creation	Notes cannot be created for instructions that straddle multiple lines.	-	-
	Notes cannot be created for dedicated instructions.	-	-
	If the coil associated with a note is deleted, the note is also deleted.	-	• <Caution>
	The note of the first coil in a ladder block is made to correspond to the first step of the ladder block. Other notes are written to the steps of individual coils.	-	-
Find/Replace	It is not possible to search for character strings in comments and device names in the ladder display window. (This is possible for notes and statements only.)	-	•
	When the device with the searched device name has both common and program-specific device name settings, the comment reflection destination/reference destination in the options is not followed.	-	-
	When an online change setting is made for a write conversion setting, the find/Replace menu cannot be selected.	-	•
Statements/notes	P/I statements that are not used in a program with GPPA are not written to GPPW.	-	-
	When multiple P,I statements have been created for the same P,I with GPPW, the first P,I statement encountered is written in GPPA format. The other, redundant, P,I statements are not written.	-	-
	When line statements/notes are created other than at the head of a ladder block with GPPA, statements at steps part way through a block are not written to GPPW. If a note is allocated to the first step of a ladder block, it is read in association with the first coil of the ladder block. For other notes, if the step they are assigned to is a coil, they are read in association with that coil.	-	-

Item	Restriction/Note	GPPA	GPPQ
Use of other packages at the same port	It is not possible to communicate with a PLC while using GPPA/GPPQ at the same port. Either use a different port or quit GPPA/GPPQ (close the DOS prompt too), before using the port.	-	-
	When using the Windows version of, for example, SW[]NIW-GOT800P, simultaneous access to the same port is not possible. Communication with one of the packages only is possible.	-	-
Step execution/ Partial execution	After the set break condition has been satisfied, the PLC breaks operation after running for several steps.	-	•
	Step run via A7BD-J71AP21/AR21 is only possible with A2ACPU and A3ACPU.	•	-
Fault history	If storing the fault history file at a location other than the internal RAM, use the drive name and file name.	-	•
Video card	When using an S3 TRIO64V+ video card, the display may not be normal; in this case "none" must be set for "hardware accelerator" in the graphics detailed setting dialog box.	-	-
Ladder display	Out-of-range devices can be displayed in the ladder display. However, an error occurs if an out-of-range designation is made in ladder editing. Out-of-range devices can be checked in the program check.	-	• <Caution>
	For an illegal ladder that has no MPP corresponding to MPS, a ladder error is displayed by GPPA, but GPPW displays the ladder, treating this as a ladder creation fault.	-	-
Processing at GPPW	When operations that take some time, such as PLC memory clear, are executed, it may not be possible to redisplay the GPPW display, or the operation of another application may be held up.	-	-
Device memory clear	Since latch clear/non-clearance follows the latch range of the PLC parameters of the project that is currently opened at the personal computer, if there is a discrepancy between the parameters stored in the CPU and the latch range, the latch range may be cleared even if latched devices are designated as not included in the range for clearance.	-	-
Writing to a memory cassette	When using an A4UMCA-*E EEPROM, the memory setting switch must be set to the ROM side.	•	-
Device name registration	With GPPA, the first 8 characters of a comment are input as the device name, but with GPPW the device name must be registered. Similarly, when printing with device names, the device names must be registered.	-	-
Starting the initialization file	The maximum number of windows that can be automatically opened by starting program restart or initialization files is 20.	-	-
Instruction input by device name	When instructions are input in a ladder by using device names (LD, 'LS11), they are input by searching for the device that corresponds to the device name from the comment data, but when the same device name is set more than once, the device found first in the search is used.	-	-
Short cut keys	Numeric keys cannot be used as shortcut keys.	-	-
Windows	Up to ten monitor windows (ladder monitor, registration monitor, etc.) can be displayed. When more than one GPPW is started up, up to ten windows can be used with each GPPW.	-	-

Item	Restriction/Note	GPPA	GPPQ
Windows task bar	When GPPW is started up while "Always on Top" or "Auto hide" is not specified in the property settings of the Windows task bar, nothing can be displayed in front of the task bar. To display in front of the task bar, set " Always on Top " or " Auto hide " for the task bar.	-	-
Parameter mismatch	When the same data as parameter data written in GPPA format is created with GPPA, there may be a mismatch in the data contents. However, both are correct as parameters and can be used without problems.	-	-
Memory capacity setting	When A1NCPU is selected with GPPA, the default for the comment capacity in memory capacity setting is 64K bytes, but the GPPW default for comment capacity is 0K bytes.	-	-
Window No.	When the device batch monitor, registration monitor, or buffer memory batch monitor window is opened, the window whose number is one higher than the window last opened is displayed. Even if you close the open window and open another one, the number of the window opened last is counted up.	-	-
Compare	If verification is executed when there is an END instruction part way through the program in the PLC, the part of the program up to the END instruction is verified.	-	-
Duplicate coil result display	The duplicate coil check result display displays details of the step positions where duplicate coils were found in a search from the head of the program.	-	-
About access to remote I/O	When a cable is connected to a master station/control station/remote I/O and remote I/O is designated, communication is not possible. A master station/other station that is not remote I/O must be designated.	-	-
Printing	When printing with device names, device comments and contact use destinations appended on the right, characters in the final line of device comments may be missing, depending on the printer. This problem can be avoided by making the left and right margins smaller in page setting.	-	-
	When printing a large quantity of data, set the printer spool setting to "send printing data directly to the printer."	-	-
Monitoring	When ladder monitoring is executed after setting a monitor condition and monitor stop condition, it is not possible to carry out device test/batch/registration monitoring, or PLC diagnosis.	-	-
Personal computer	Depending on the personal computer, the GPPW may be sent incorrect information on the remaining capacity of the main memory, leading to problems with starting and operation. In this case, you must close other applications and increase the free memory area.	-	-
Import file (reading immediately after starting GPPW)	This applies to A series. When a project has been created at the reading destination PLC type and the data is read (the status is "project name not set"), comments are read in accordance with the comment range at the GPPA side.	-	-
Monitoring with Ethernet	It is not possible to simultaneously monitor with another GPP via an Ethernet connection.	-	-
Open project	Read-only and write-protected (e.g. FD) projects cannot be opened. When a project which was saved when displayed in a large GPPW window on a personal computer with high resolution is opened on a low-resolution personal computer, it may be displayed at the original large window size and project off the screen. Projects that are saved in their maximized state present no problem.	-	-

Appendix 9 Compatibility of Japanese version, English version

English version GPPW, ladder logic test tool (LLT) are enable only when the GPPW,LLT is used in combination with the English version GPPW,LLT.
It is not possible to use the English version GPPW, LLT with the Japanese version GPPW,LLT .

Appendix 10 GPPW and LLT Operations

The version combinations when the logic test function (LLT) is used with GPPW are indicated below.

		GPPW
		SW2D5-GPPW-E
Logic test function (LLT)	SW2D5-LLT-E	•

English version GPPW, ladder logic test tool (LLT) are enable only when the GPPW,LLT is used in combination with the English version GPPW,LLT.
It is not possible to use the English version GPPW, LLT with the Japanese version GPPW,LLT .

Appendix 11 Notes on FX Series Programming

The points to note when programming with the FX series are given here. For general points of difference and notes, see Section 1.3.

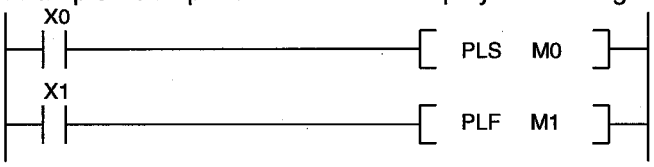
11.1 Ladder Monitor Display

A	QnA	FX
×	×	•

The differences between the FXGP(DOS)/FXGP(WIN) monitor display and GPPW monitor display are indicated here.

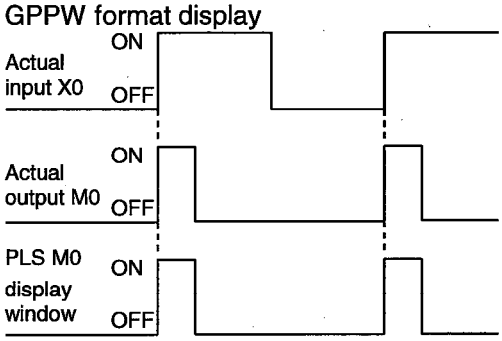
- Differences in monitor display of PLS and PLF instructions
  In GPPW, the GPPW format display method is set as the default, but if the "PLSPLF instruction ladder monitor" check box in the [Tools] → [Options] <<program common>> sheet is checked, display is in the FXGP(DOS) or FXGP(WIN) format. Whichever display is selected, there is no effect on the actual operation of FXCPU.

  Example: Comparison of monitor displays according to setting contents

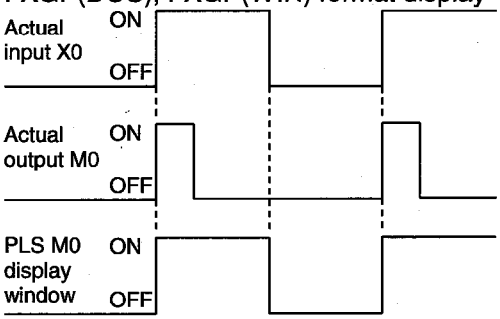


(1) Monitoring PLS instructions

- GPPW format display

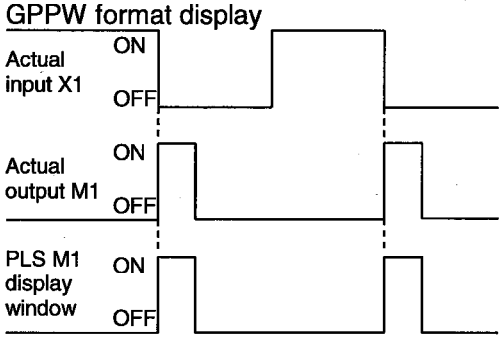


- FXGP(DOS), FXGP(WIN) format display

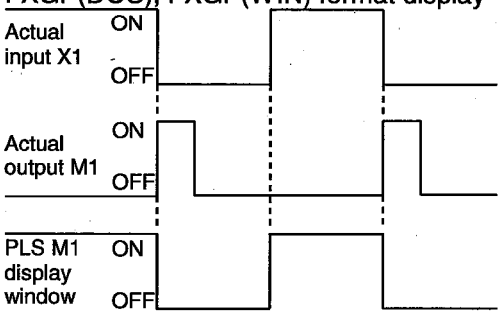


(2) Monitoring PLF instructions

- GPPW format display

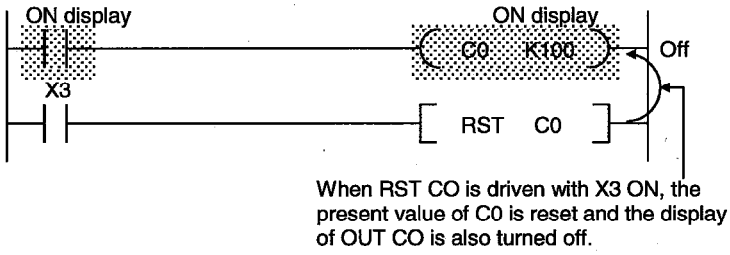


- FXGP(DOS), FXGP(WIN) format display



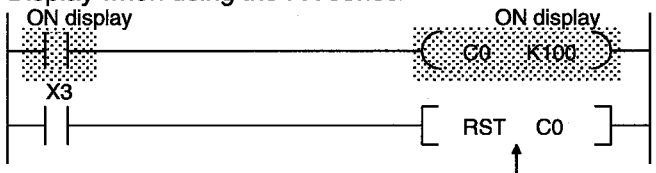
- Differences in monitoring OUT T and OUT C instructions
  The OUT coil monitor display on resetting timer and counter present values is different when using the "A" series or QnA series than it is when using the FX series.

  - Display when using the "A" series or QnA series



When RST CO is driven with X3 ON, the present value of C0 is reset and the display of OUT CO is also turned off.

  - Display when using the FX series



When RST CO is driven with X3 ON, the present value of C0 is reset but the display of OUT CO remains unchanged. (ON display continues until the drive contact of OUT CO goes OFF.)

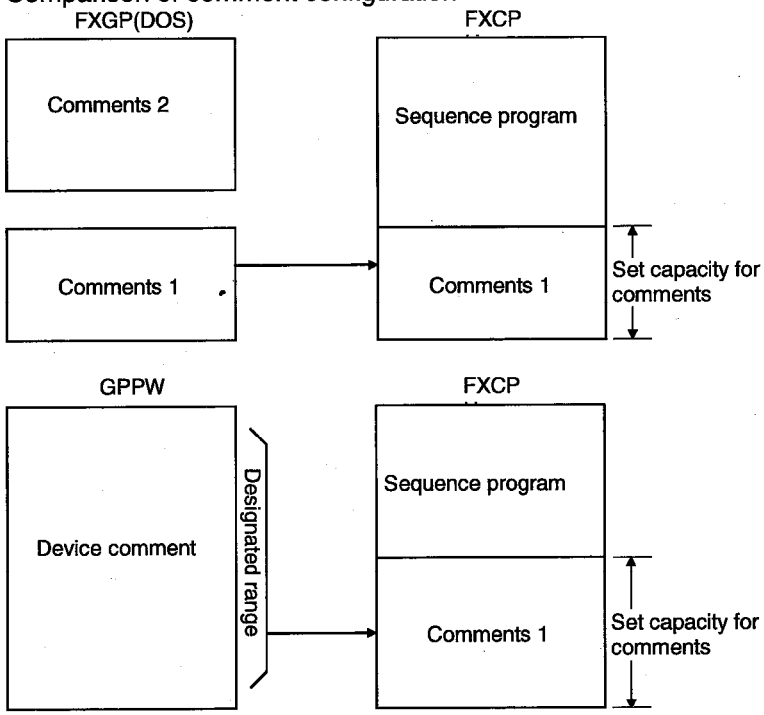
11.2 Handling of Comments

A	QnA	FX
×	×	•

- With FXGP(DOS), a distinction is made when entering comments: comments written in the PLC are called "comments 1", and comments held only at the peripheral device side are called "comments 2."
  With GPPW, all comments are managed as device comments, and the distinction between comments 1 and comments 2 does not exist.
  When device comments are written to a PLC, a comment capacity must be secured in "PLC parameter setting" (see Section 13.18), and the comment range among the device comments to be written to the PLC must be set in "comment range setting" (see Section 9.9.)

- Comments of up to 16 characters can be written to a PLC, but some models, such as FXGP(DOS) and A6GPP, can only handle up to 15 characters, which means that the 16th character cannot be displayed. When comments are used in common, enter device comments of up to 15 characters (see Section 9.1.2(3)).

- Comparison of comment configuration



Appendix 12 Instruction Conversion Lists

12.1 Instruction Conversion List for A <-> QnA Conversions

A	QnA	FX
•	•	×

A ↔ QnA conversions will not be successful under the following conditions: in these cases make the necessary correction after executing the conversion instruction by referring to the following lists.

The instruction conversion list for conversions from A to QnA is given in pages 51 to 66.
The instruction conversion list for conversions from QnA to A is given in pages 67 to 79.
The indications *, *1, *2, *3, *4, *5, *6, and *7 in the lists refer to sources and destinations.

Device correspondence table for A → QnA conversions

A Series	QnA Series	Remarks
M	M	
M9000 to	SM1000 to	
L	L	
F	F	
S	M	
X	X	
Y	Y	
B	B	
D	D	
D9000 to	SD1000 to	
A0, 1	SD718, 719	
R	R	
W	W	
T	T, ST	ST is governed by the parameter settings
C	C	

Device correspondence table for A → QnA conversions (continued)

A Series	QnA Series	Remarks
P	P	If out-of-range, the instruction becomes OUT SM1255
I	I	If out-of-range, the instruction becomes OUT SM1255
N	N	If out-of-range, the instruction becomes OUT SM1255
K	K	
H	H	
" "	" "	Character strings are handled
Z, Z1~Z6	Z0~Z6	
K	K	
V, V1~V6	Z7~Z13	

Devices that contain out-of-range device parts or extension parts are changed to SM1255 if bits and SD1255 if words.

Converting "A" standard instructions to QnA series:

A Series	QnA Series	Remarks
OUT T* *2	OUT T* *2	H(OUTH) and ST are governed by the parameter settings
	OUT ST* *2	
	OUT C* *2	
OUT C* *2	OUTH T* *2	
	OUTH ST* *2	
	OUTH C* *2	
SUB *1	OUT SM1255	A dedicated instructions are excepted.
CHG	OUT SM1255	
SUM *1	SUM *1 SD718	
DSUM *1	DSUM *1 SD718	
ASC *1 *2	OUT SM1255	
LRDP *1 *2 *3 *4	OUT SM1255	
LWTP *1 *2 *3 *4	OUT SM1255	
RFRP *1 *2 *3 *4	OUT SM1255	
RTOP *1 *2 *3 *4	OUT SM1255	

Converting "A" standard instructions to QnA series:

A Series	QnA Series	Remarks
LEDA *1	OUT SM1255	"A" dedicated instructions are excepted.
LEDB *2	OUT SM1255	"A" dedicated instructions are excepted.
CHK *1 *2	OUT SM1255	
STC	OUT SM1255	
CLC	OUT SM1255	

Converting structured program dedicated instructions to QnA series:
Refer to the QnACPU Programming Manual (Common Instructions) (for AnACPU/AnUCPU)

A Series	QnA Series	Remarks
LEDA(LEDB) IX LEDC *1 LEDR	OUT SM1255 LEDC *1 LEDR	Section 7.6.9 Index qualification of entire ladder
LEDA IXEND	OUT SM1255	
LEDA/LEDB BREAK LEDC *1 LEDC *2 LEDR	OUT SM1255 LEDC *1 LEDC *2 LEDR	Section 7.6.2 Forced end of FOR to NEXT instruction loop
LEDA/LEDB FCALL LEDC *1 LEDR	OUT SM1255 LEDC *1 LEDR	Section 7.6.5 Sub-routine program output OFF calls
LEDA CHK	OUT SM1255	Section 7.10.1 Special format failure checks
LEDA CHKEND	OUT SM1255	Section 7.10.2 Changing check format of CHK instruction

Converting character string processing instructions to QnA series (for AnACPU/AnUCPU)

A Series	QnA Series	Remarks
LEDA/LEDB SCMP LEDC *1 LEDC *2 LEDC *3 LEDR	OUT SM1255 LEDC *1 LEDC *2 LEDC *3 LEDR	Section 6.1.4 Character string data comparisons

Converting instructions for file registers to QnA series (for AnACPU/AnUCPU)

A Series	QnA Series	Remarks
LEDA/LEDB RSET LEDC/SUB *1 LEDR	OUT SM1255 LEDC *1/OUT SM1255 LEDR	Section 7.14.1 Switching file register numbers
LEDA/LEDB BMOVR LEDC *1 LEDC *2 LEDC/SUB *3 LEDR	OUT SM1255 LEDC *1 LEDC *2 LEDC *3/OUT SM1255 LEDR	Section 6.4.5 Block 16-bit data transfers
LEDA/LEDB BXCHR LEDC *1 LEDC *2 LEDC/SUB *3 LEDR	OUT SM1255 LEDC *1 LEDC *2 LEDC *3/OUT SM1255 LEDR	Section 6.4.8 Block 16-bit data exchanges
LEDA/LEDB ZRRD	OUT SM1255	Section 7.18.3 Direct 1-byte read from file register
LEDA/LEDB ZRWR	OUT SM1255	Section 7.18.4 File register direct 1-byte write
LEDA/LEDB ZRRDB	OUT SM1255	Section 7.18.3 Direct 1-byte read from file register
LEDA/LEDB ZRWRB	OUT SM1255	Section 7.18.4 File register direct 1-byte write

Converting instructions for data link to QnA series (for AnACPU/AnUCPU)

A Series	QnA Series	Remarks
LEDA/LEDB LRDP SUB *1 LEDC *2 LEDC *3 SUB *4 LEDC *5 LEDR	OUT SM1255 OUT SM1255 LEDC *2 LEDC *3 OUT SM1255 LEDC *5 LEDR	Section 8.3.2 Reading device data from local stations (MELSECNET)
LEDA/LEDB LWTP SUB *1 LEDC *2 LEDC *3 SUB *4 LEDC *5 LEDR	OUT SM1255 OUT SM1255 LEDC *2 LEDC *3 OUT SM1255 LEDC *5 LEDR	Section 8.3.4 Writing data to devices at local stations (MELSECNET)
LEDA/LEDB RFRP SUB K/H* SUB *1 LEDC *2 SUB *3 LEDC *4 LEDR	OUT SM1255 OUT SM1255 OUT SM1255 LEDC *2 OUT SM1255 LEDC *4 LEDR	Section 8.3.5 Reading data from a remote I/O station special function module (MELSECNET)
LEDA/LEDB RTOP SUB K/H* SUB *1 LEDC *2 SUB *3 LEDC *4 LEDR	OUT SM1255 OUT SM1255 OUT SM1255 LEDC *2 OUT SM1255 LEDC *4 LEDR	Section 8.3.6 Writing data to special function modules of remote I/O stations (MELSECNET)
LEDA/LEDB ZCOM LEDC/SUB *1 LEDR	OUT SM1255 LEDC *1/OUT SM1255 LEDR	Section 8.1.1 Network refresh
LEDA/LEDB ZNRD SUB K/H* SUB *1 LEDC *2 LEDC *3 SUB *4 LEDC *5 LEDR	OUT SM1255 OUT SM1255 OUT SM1255 LEDC *2 LEDC *3 OUT SM1255 LEDC *5 LEDR	Section 8.3.1 Reading device data from other stations (MELSECNET/10)
LEDA/LEDB ZNWR SUB K/H* SUB *1 LEDC *2 LEDC *3 SUB *4 LEDC *5 LEDR	OUT SM1255 OUT SM1255 OUT SM1255 LEDC *2 LEDC *3 OUT SM1255 LEDC *5 LEDR	Section 8.3.3 Writing device data to other stations (MELSECNET/10)

Converting instructions for data link to QnA series (for AnACPU/AnUCPU) (Continued)

A Series	QnA Series	Remarks
LEDA/LEDB ZNFR SUB K/H* SUB *1 LEDC *2 SUB *3 SUB *4 LEDC *5 LEDR	OUT SM1255 OUT SM1255 OUT SM1255 LEDC *2 OUT SM1255 OUT SM1255 LEDC *5 LEDR	Section 8.2.8 Reading data from special function modules at remote I/O stations
LEDA/LEDB ZNTO SUB K/H* SUB *1 LEDC *2 SUB *3 SUB *4 LEDC *5 LEDR	OUT SM1255 OUT SM1255 OUT SM1255 LEDC *2 OUT SM1255 OUT SM1255 LEDC *5 LEDR	Section 8.2.9 Writing data to special function module of remote I/O station

Converting special function module instructions (AD61 control instructions) to QnA series
Refer to the QnACPU Programming Manual (Special Function Module) (for AnACPU/AnUCPU)

A Series	QnA Series	Remarks
LEDA/LEDB PVWR1 SUB K/H* LEDC *1 LEDR	OUT SM1255 OUT, SM1255 LEDC *1 LEDR	Section 5.1 Setting Preset Value Data
LEDA/LEDB PVWR2 SUB K/H* LEDC *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDR	
LEDA/LEDB SVWR1 SUB K/H* LEDC *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDR	Section 5.2 Setting Set Value Data for Greater/Smaller/Egual Judgments
LEDA/LEDB SVWR2 SUB K/H* LEDC *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDR	
LEDA/LEDB PVRD1 SUB K/H* LEDC *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDR	Section 5.3 Reading Present Value
LEDA/LEDB PVRD2 SUB K/H* LEDC *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDR	

Converting special function module instructions (AD59 control instructions) to QnA series (for AnACPU/AnUCPU)

A Series	QnA Series	Remarks
LEDA/LEDB PRN SUB K/H* LEDC/SUB *1 LEDC *2 LEDC *3 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *2 LEDC *3 LEDR	Section 6.1 Sending to the Printer any Number of Character Data
LEDA/LEDB PR SUB K/H* LEDC *1 LEDC *2 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDC *2 LEDR	Section 6.2 Sending to the Printer Characters up to "00_H" Code
LEDA/LEDB GET SUB K/H* LEDC *1 LEDC/SUB *2 LEDC *3 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDC *2/OUT SM1255 LEDC *3 LEDR	Section 6.3 Reading Data from Memory Card
LEDA/LEDB PUT SUB K/H* LEDC *1 LEDC/SUB *2 LEDC *3 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDC *2/OUT SM1255 LEDC *3 LEDR	Section 6.4 Writing Data to a Memory Card

Converting special function module (AJ71C24 control instructions) to QnA series (for AnACPU/AnUCPU)

A Series	QnA Series	Remarks
LEDA/LEDB PRN SUB K/H* LEDC/SUB *1 LEDC *2 LEDC *3 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *2 LEDC *3 LEDR	Section 9.1 No-Protocol Mode Data Send of Designated Number of Bytes
LEDA/LEDB PR SUB K/H* LEDC *1 LEDC *2 LEDR	OUT SM1255 OUT SM1255 LEDC *2 LEDC *3 LEDR	Section 9.2 No-Protocol Mode Data Send Up until "00_H" Code
LEDA/LEDB INPUT SUB K/H* LEDC *1 LEDC *2 LEDC *3 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDC *2 LEDC *3 LEDR	Section 9.3 No-Protocol Mode Data Receive

Converting special function module instructions (AJ71C24 control instructions) to QnA series (for AnACPU/AnUCPU) (Continued)

A Series	QnA Series	Remarks
LEDA/LEDB SPBUSY SUB K/H* LEDC *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDR	Section 9.4 Reading Communication Status
LEDA/LEDB SPCLR SUB K/H* LEDC *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDR	Section 9.5 Forced Cancellation of Communications Processing

Converting special function module instructions (AJ71C21 control instructions) to QnA series (for AnACPU/AnUCPU)

A Series	QnA Series	Remarks
LEDA/LEDB PRN2 SUB K/H* LEDC/SUB *1 LEDC *2 LEDC *3 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *2 LEDC *3 LEDR	Section 8.1 Sending Designated Number of Bytes of Data
LEDA/LEDB PRN4 SUB K/H* LEDC/SUB *1 LEDC *2 LEDC *3 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *2 LEDC *3 LEDR	
LEDA/LEDB PR2 SUB K/H* LEDC *1 LEDC *2 LEDR	OUT SM1255 OUT SM1255 LEDC *2 LEDC *3 LEDR	Section 8.2 Data Send up to "00_H" Code
LEDA/LEDB PR4 SUB K/H* LEDC *1 LEDC *2 LEDR	OUT SM1255 OUT SM1255 LEDC *2 LEDC *3 LEDR	
LEDA/LEDB INPUT2 SUB K/H* LEDC *1 LEDC *2 LEDC *3 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDC *2 LEDC *3 LEDR	Section 8.3 Receiving Data

Converting special function module instructions (AJ71C21 control instructions) to QnA series (for AnACPU/AnUCPU) (Continued)

A Series	QnA Series	Remarks
LEDA/LEDB INPUT4 SUB K/H* LEDC *1 LEDC *2 LEDC *3 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDC *2 LEDC *3 LEDR	Section 8.3 Receiving Data
LEDA/LEDB GET SUB K/H* LEDC *1 LEDC/SUB *2 LEDC *3 LEDC *4 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDC *2/OUT SM1255 LEDC *3 LEDC *4 LEDR	Section 8.4 Read RAM Memory
LEDA/LEDB PUT SUB K/H* LEDC *1 LEDC/SUB *2 LEDC *3 LEDC *4 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDC *2/OUT SM1255 LEDC *3 LEDC *4 LEDR	Section 8.5 Write to RAM Memory
LEDA/LEDB SPBUSY SUB K/H* LEDC *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDR	Section 8.6 Reading Communication Status
LEDA/LEDB SPCLR SUB K/H* LEDC *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDR	Section 8.7 Forced Stop of Communication Processing

Converting special function module instructions (AJ71PT32-S3 control instructions) to QnA series (for AnACPU/AnUCPU)

A Series	QnA Series	Remarks
LEDA/LEDB INPUT SUB K/H* LEDC *1 LEDC *2 LEDC *3 LEDC/SUB *4 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDC *2 LEDC *3 LEDC *4/OUT SM1255 LEDR	Section 7.1 Key Input from Operation Box
LEDA/LEDB PRN SUB K/H* LEDC/SUB *1 LEDC *2 LEDC *3 LEDC/SUB *4 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *2 LEDC *3 LEDC *4/OUT SM1255 LEDR	Section 7.2 No-Protocol Mode Data Send of Designated Number of Bytes
LEDA/LEDB PR SUB K/H* LEDC *1 LEDC *2 LEDC/SUB *3 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDC *2 LEDC *3/OUT SM1255 LEDR	Section 7.3 No-Protocol Mode Data Send up until "00_H" Code
LEDA/LEDB INPUT SUB K/H* LEDC *1 LEDC *2 LEDC *3 LEDC/SUB *4 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDC *2 LEDC *3 LEDC *4/OUT SM1255 LEDR	Section 7.4 No-Protocol Mode Data Receive
LEDA/LEDB MINI SUB K/H* LEDR	OUT SM1255 OUT SM1255 LEDR	Section 7.5 Remote Terminal Module Communication
LEDA/LEDB SPBUSY SUB K/H* LEDC *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDR	Section 7.7 Reading Communication Status
LEDA/LEDB SPCLR SUB K/H* LEDC *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDR	Section 7.8 Forced Stop of Communication Processing

Converting program switching instructions to QnA series (for AnACPU/AnUCPU)

A Series	QnA Series	Remarks
LEDA ZCHG0	OUT SM1255	Model Q2AS(H) CPU(S1) User's Manual Appendix 4.5
LEDA ZCHG1	OUT SM1255	
LEDA ZCHG2	OUT SM1255	
LEDA ZCHG3	OUT SM1255	Q2A(S1)/Q3A/Q4ACPU User's Manual Appendix 4.5

Converting instructions for CC-Link to QnA series

Refer to the CC-Link System Master Local Module type AJ61QBT11 /A1SJQBT11 User's Manual (for AnSHCPU)

A Series	QnA Series	Remarks
LEDA/LEDB RLPA SUB K/H* LEDC *1 LEDC *2 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDC *2 LEDR	QnACPU PROGRAMING MANUAL (Common Instructions) Section 7.8.1 Special function modules 1-and 2-word data read operations
LEDA/LEDB RRPA SUB K/H* LEDC *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDR	Section 7.8.2 Special function modules 1-and 2-word data write operations
LEDA/LEDB RIFR SUB K/H* LEDC/SUB *1 LEDC/SUB *2 LEDC *3 LEDC/SUB *4 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *2/OUT SM1255 LEDC *3 LEDC *4/OUT SM1255 LEDR	Section 15.6.8 RIFR instruction
LEDA/LEDB RITO SUB K/H* LEDC/SUB *1 LEDC/SUB *2 LEDC *3 LEDC/SUB *4 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *2/OUT SM1255 LEDC *3 LEDC *4/OUT SM1255 LEDR	Section 15.6.9 RITO instruction
LEDA/LEDB RITO SUB K/H* SUB *1 LEDC *2 LEDC *3 LEDR	OUT SM1255 OUT SM1255 OUT SM1255 LEDC *2 LEDC *3 LEDR	
LEDA/LEDB RIWT SUB K/H* SUB *1 LEDC *2 LEDC *3 LEDR	OUT SM1255 OUT SM1255 OUT SM1255 LEDC *2 LEDC *3 LEDR	Section 15.6.5 RIWT instruction
LEDA/LEDB RIRCV SUB K/H* SUB *1 LEDC *2 LEDC *3 LEDC *4 LEDR	OUT SM1255 OUT SM1255 OUT SM1255 LEDC *2 LEDC *3 LEDC *4 LEDR	Section 15.6.7 RIRCV instruction

Converting instructions for CC-Link to QnA series (for AnSHCPU) (Continued)

A Series	QnA Series	Remarks
LEDA/LEDB RISEND SUB K/H* SUB *1 LEDC *2 LEDC *3 LEDC *4 LEDR	OUT SM1255 OUT SM1255 OUT SM1255 LEDC *2 LEDC *3 LEDC *4 LEDR	Section 15.6.6 RISEND instruction
LEDA/LEDB RDGET SUB K/H* SUB *1 LEDC *2 LEDC *3 LEDR	OUT SM1255 OUT SM1255 OUT SM1255 LEDC *2 LEDC *3 LEDR	Section 15.6.10 RDGET instruction
LEDA/LEDB RDPUT SUB K/H* SUB *1 LEDC *2 LEDC *3 LEDR	OUT SM1255 OUT SM1255 OUT SM1255 LEDC *2 LEDC *3 LEDR	Section 15.6.11 RDPUT instruction
LEDA/LEDB RDMON SUB K/H* SUB *1 LEDC *2 LEDC *3 LEDR	OUT SM1255 OUT SM1255 OUT SM1255 LEDC *2 LEDC *3 LEDR	Section 15.6.12 RDMON instruction

Converting PID operation instructions to QnA series

Refer to the QnACPU PROGRAMMING MANUAL (AD57 Instructions) (for AnSHCPU)

A Series	QnA Series	Remarks
LEDA/LEDB CODE SUB K/H* LEDC/SUB *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDR	Section 7.1.1 Display mode setting
LEDA/LEDB CPS1 SUB K/H* LEDC/SUB *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDR	Section 7.2.1 Canvas screen display
LEDA/LEDB CPS2 SUB K/H* LEDC/SUB *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDR	Section 7.2.2 VRAM display address change
LEDA/LEDB CMOV SUB K/H* LEDC/SUB *1 LEDC/SUB *2 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *2/OUT SM1255 LEDR	Section 7.2.3 Canvas screen transmission to VRAM areas

Converting PID operation instructions to QnA series (for AnSHCPU) (Continued)

A Series	QnA Series	Remarks
LEDA/LEDB CLS SUB K/H* LEDR	OUT SM1255 OUT SM1255 LEDR	Section 7.2.4 Screen clear
LEDA/LEDB CLV SUB K/H* LEDC/SUB *1 LEDC/SUB *2 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *2/OUT SM1255 LEDR	Section 7.2.5 VRAM area clear
LEDA/LEDB CSCRU SUB K/H* LEDR	OUT SM1255 OUT SM1255 LEDR	Section 7.2.6 Screen scroll
LEDA/LEDB CSCRD SUB K/H* LEDR	OUT SM1255 OUT SM1255 LEDR	
LEDA/LEDB CON1 SUB K/H* LEDR	OUT SM1255 OUT SM1255 LEDR	Section 7.3.1 Cursor display ON
LEDA/LEDB CON2 SUB K/H* LEDR	OUT SM1255 OUT SM1255 LEDR	
LEDA/LEDB COFF SUB K/H* LEDR	OUT SM1255 OUT SM1255 LEDR	Section 7.3.2 Cursor display OFF
LEDA/LEDB LOCATE SUB K/H* LEDC/SUB *1 LEDC/SUB *2 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *2/OUT SM1255 LEDR	Section 7.3.3 Cursor position setting
LEDA/LEDB CNOR SUB K/H* LEDR	OUT SM1255 OUT SM1255 LEDR	Section 7.4.1 Normal/highlighted display of characters
LEDA/LEDB CREV SUB K/H* LEDR	OUT SM1255 OUT SM1255 LEDR	
LEDA/LEDB CRDSP SUB K/H* LEDC/SUB *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDR	Section 7.4.2 Normal/highlighted display switching of characters being displayed
LEDA/LEDB CRDSPV SUB K/H* LEDC/SUB *1 LEDC/SUB *2 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *2/OUT SM1255 LEDR	Section 7.4.3 Normal/highlighted display switching of characters in the VRAM areas
LEDA/LEDB COLOR SUB K/H* LEDC/SUB *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDR	Section 7.4.4 Character color designation

Converting PID operation instructions to QnA series (for AnSHCPU) (Continued)

A Series	QnA Series	Remarks
LEDA/LEDB CCDSP SUB K/H* LEDC/SUB *1 LEDC/SUB *2 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *2/OUT SM1255 LEDR	Section 7.4.5 Change of character color being displayed
LEDA/LEDB CCDSPV SUB K/H* LEDC/SUB *1 LEDC/SUB *2 LEDC/SUB *3 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *2/OUT SM1255 LEDC *2/OUT SM1255 LEDR	Section 7.4.6 Change of character color in the VRAM areas
LEDA/LEDB PRN SUB K/H* LEDC/SUB *1 LEDC *2 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *2 LEDR	Section 7.5.1 Display of designated number of the ASCII characters
LEDA/LEDB PR SUB K/H* LEDC *1 LEDR	OUT SM1255 OUT SM1255 LEDC *2 LEDR	Section 7.5.2 Display of the ASCII characters up to code 00_H
LEDA/LEDB PRNV SUB K/H* LEDC/SUB *1 LEDC/SUB *2 LEDC *3 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *1/OUT SM1255 LEDC *2 LEDR	Section 7.5.3 Store of the ASCII characters of designated number of characters
LEDA/LEDB PRV SUB K/H* LEDC/SUB *1 LEDC *2 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *2 LEDR	Section 7.5.4 Storage of the designated number of ASCII characters up to code 00_H in the VRAM areas
LEDA/LEDB EPRN SUB K/H* LEDC/SUB *1 LEDC *2 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *2 LEDR	Section 7.5.5 Display of designated number of designated characters
LEDA/LEDB EPR SUB K/H* LEDC *1 LEDR	OUT SM1255 OUT SM1255 LEDC *2 LEDR	Section 7.5.6 Display of designated characters up to code 00_H
LEDA/LEDB EPRNV SUB K/H* LEDC/SUB *1 LEDC/SUB *2 LEDC *3 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *1/OUT SM1255 LEDC *2 LEDR	Section 7.5.7 Storage of designated number of designated characters in the VRAM areas

Converting PID operation instructions to QnA series (for AnSHCPU) (Continued)

A Series	QnA Series	Remarks
LEDA/LEDB EPRV SUB K/H* LEDC/SUB *1 LEDC *2 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *2 LEDR	Section 7.5.8 Storage of designated characters up to code 00_H in the VRAM areas
LEDA/LEDB CR1 SUB K/H* LEDC/SUB *1 LEDC/SUB *2 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *1/OUT SM1255 LEDR	Section 7.5.9 Horizontal repeated display of a designated character
LEDA/LEDB CR2 SUB K/H* LEDC/SUB *1 LEDC/SUB *2 LEDC/SUB *3 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *1/OUT SM1255 LEDC *1/OUT SM1255 LEDR	Section 7.5.10 Horizontal repeated display of a pair of designated characters
LEDA/LEDB CC1 SUB K/H* LEDC/SUB *1 LEDC/SUB *2 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *1/OUT SM1255 LEDR	Section 7.5.11 Vertical repeated display of a designated character
LEDA/LEDB CC2 SUB K/H* LEDC/SUB *1 LEDC/SUB *2 LEDC/SUB *3 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDC *1/OUT SM1255 LEDC *1/OUT SM1255 LEDR	Section 7.5.12 Vertical repeated display of a pair of designated characters
LEDA/LEDB CINMP SUB K/H* LEDC/SUB *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDR	Section 7.6.1 Display of a minus symbol ("-")
LEDA/LEDB CINHP SUB K/H* LEDC/SUB *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDR	Section 7.6.2 Display of a hyphen ("-")
LEDA/LEDB CINPT SUB K/H* LEDC/SUB *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDR	Section 7.6.3 Display of a period or a decimal point (".")
LEDA/LEDB CIN0 : LEDA/LEDB CIN9 SUB K/H* LEDC/SUB *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDR	Section 7.6.4 Display of the alphanumeric characters "0" to "9" and "A" to "Z"

Converting PID operation instructions to QnA series (for AnSHCPU) (Continued)

A Series	QnA Series	Remarks
LEDA/LEDB CINA : LEDA/LEDB CINZ SUB K/H* LEDC/SUB *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDR	Section 7.6.4 Display of the alphanumeric characters "0" to "9" and "A" to "Z"
LEDA/LEDB CINSP SUB K/H* LEDC/SUB *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDR	Section 7.6.5 Display of a space ("␣")
LEDA/LEDB CINCLR SUB K/H* LEDC/SUB *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1/OUT SM1255 LEDR	Section 7.7.1 Designated column clear
LEDA/LEDB INPUT SUB K/H* LEDC *1 LEDC *2 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDC *2 LEDR	Section 7.8.1 ASCII code conversion of displayed characters
LEDA/LEDB GET SUB K/H* LEDC *1 LEDC/SUB *2 LEDC *3 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDC *2/OUT SM1255 LEDC *3 LEDR	Section 7.9.1 VRAM data read
LEDA/LEDB PUT SUB K/H* LEDC *1 LEDC/SUB *2 LEDC *3 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDC *2/OUT SM1255 LEDC *3 LEDR	Section 7.9.2 VRAM data write
LEDA/LEDB STAT SUB K/H* LEDC *1 LEDR	OUT SM1255 OUT SM1255 LEDC *1 LEDR	Section 7.10.1 Display state read

Device correspondence table for QnA → A conversions

QnA Series	A Series	Remarks
M	M	
SM	M9255	
SM1000 to	M9000 to	
L	L	
F	F	
V	M9255	
S	M9255	
TR	M9255	
X	X	
Y	Y	
FX	M9255	
FY	M9255	
B	B	
SB	M9255	
DX	X	
DY	Y	
D	D	
SD	D9255	
SD718, 719	A0, 1	
SD1000 to	D9000 to	
FD	D9255	
G	D9255	
SG	D9255	
VD	D9255	
A	D9255	
R	R	
ZR0 to 8191	R0 to 8191	
ZR8192 to	D9255	
W	W	
SW	D9255	
T	T	
C	C	
ST	T	
Z0 to Z6	Z, Z1 to Z6	
Z7 to Z13	V, V1 to V6	
Z14 to	D9255	
P	P	If out-of-range, the instruction becomes OUT M9255
I	I	If out-of-range, the instruction becomes OUT M9255
N	N	If out-of-range, the instruction becomes OUT M9255
U	M9255	All instructions become OUT M9255
J	M9255	All instructions become OUT M9255
BL	M9255	All instructions become OUT M9255
K	K	
H	H	
E	D9255	
" "	" "	

Device correspondence table for QnA → A conversions (Continued)

QnA Series	A Series	Remarks
Z0 to Z6	Z, Z1 to Z6	If the device part is a device that cannot be converted, all devices containing this code become M9255 or D9255.
Z7 to Z13	V, V1 to V6	If the device part is a device that cannot be converted, all devices containing this code become M9255 or D255.
Z14 to	M9255, D9255	All devices containing this code become M9255 or D9255.
K	K	If the device part is a device that cannot be converted, all devices containing this code become M9255 or D255.
.	M9255, D9255	All devices containing this code become M9255 or D9255.
@	M9255, D9255	All devices containing this code become M9255 or D9255.
U	M9255, D9255	All devices containing this code become M9255 or D9255.
J	M9255, D9255	All devices containing this code become M9255 or D9255.
BL	M9255, D9255	All devices containing this code become M9255 or D9255.

Devices that contain out-of-range device parts or extension parts are changed to M9255 if bits and D9255 if words.

Converting QnA series instructions to A series instructions

QnA Series	A Series	
	Common Instructions	Dedicated Instructions (for AnA, AnUCPU)
LDP *1	LD M9255	
LDF *1	LD M9255	
ORP *1	OR M9255	
ORF *1	OR M9255	
ANDP *1	AND M9255	
ANDF *1	AND M9255	
EGP *1	AND M9255	
EGF *1	AND M9255	
MEP	AND M9255	
MEF	AND M9255	
INV	AND M9255	
OUT DY*	OUT M9255	LEDA DOUT LEDC Y* LEDR
OUT T/ST/C256 *2	OUT M9255	
OUTH T/ST/C256 *2	OUT M9255	
SET DY*	OUT M9255	LEDA/LEDB DSET LEDC Y* LEDR

Converting QnA series instructions to A series instructions (continued)

QnA Series	A Series	
	Common Instructions	Dedicated Instructions (for AnA, AnUCPU)
RST DY*	OUT M9255	LEDA/LEDB DRST LEDC Y* LEDR
FF *1	OUT M9255	LEDB FF LEDC *1 LEDR
DELTA *1	OUT M9255	
PAGE *1	OUT M9255	
LDE= *1 *2 ORE= *1 *2 ANDE= *1 *2	LD= D9255 D9255 OR= D9255 D9255 AND= D9255 D9255	
LDE<> *1 *2 ORE<> *1 *2 ANDE<> *1 *2	LD<> D9255 D9255 OR<> D9255 D9255 AND<> D9255 D9255	
LDE> *1 *2 ORE> *1 *2 ANDE> *1 *2	LD> D9255 D9255 OR> D9255 D9255 AND> D9255 D9255	
LDE>= *1 *2 ORE>= *1 *2 ANDE>= *1 *2	LD>= D9255 D9255 OR>= D9255 D9255 AND>= D9255 D9255	
LDE< *1 *2 ORE< *1 *2 ANDE< *1 *2	LD< D9255 D9255 OR< D9255 D9255 AND< D9255 D9255	
LDE<= *1 *2 ORE<= *1 *2 ANDE<= *1 *2	LD<= D9255 D9255 OR<= D9255 D9255 AND<= D9255 D9255	
LD$= *1 *2 OR$= *1 *2 AND$= *1 *2	LD= D9255 D9255 OR= D9255 D9255 AND= D9255 D9255	
LD$<> *1 *2 OR$<> *1 *2 AND$<> *1 *2	LD<> D9255 D9255 OR<> D9255 D9255 AND<> D9255 D9255	
LD$> *1 *2 OR$> *1 *2 AND$> *1 *2	LD> D9255 D9255 OR> D9255 D9255 AND> D9255 D9255	
LD$>= *1 *2 OR$>= *1 *2 AND$>= *1 *2	LD>= D9255 D9255 OR>= D9255 D9255 AND>= D9255 D9255	
LD$< *1 *2 OR$< *1 *2 AND$< *1 *2	LD< D9255 D9255 OR< D9255 D9255 AND< D9255 D9255	
LD$<= *1 *2 OR$<= *1 *2 AND$<= *1 *2	LD<= D9255 D9255 OR<= D9255 D9255 AND<= D9255 D9255	

Converting QnA series instructions to A series instructions (continued)

QnA Series	A Series	
	Common Instructions	Dedicated Instructions (for AnA, AnUCPU)
BKCMP= *1 *2 *3 *4	OUT M9255	
BKCMP<> *1 *2 *3 *4	OUT M9255	
BKCMP> *1 *2 *3 *4	OUT M9255	
BKCMP>= *1 *2 *3 *4	OUT M9255	
BKCMP< *1 *2 *3 *4	OUT M9255	
BKCMP<= *1 *2 *3 *4	OUT M9255	
E+ *1 *2	OUT M9255	
E+ *1 *2 *3	OUT M9255	LEDA/LEDB ADD LEDC *1 LEDC *2 LEDC *3 LEDR
E- *1 *2	OUT M9255	
E- *1 *2 *3	OUT M9255	LEDA/LEDB SUB LEDC *1 LEDC *2 LEDC *3 LEDR
E* *1 *2 *3	OUT M9255	LEDA/LEDB MUL LEDC *1 LEDC *2 LEDC *3 LEDR
E/ *1 *2 *3	OUT M9255	LEDA/LEDB DIV LEDC *1 LEDC *2 LEDC *3 LEDR
$+ *1 *2	OUT M9255	
$+ *1 *2 *3	OUT M9255	LEDA/LEDB SADD LEDC *1 LEDC *2 LEDC *3 LEDR
BK+ *1 *2 *3 *4	OUT M9255	
BK- *1 *2 *3 *4	OUT M9255	
INT *1 *2	OUT M9255	LEDA/LEDB INT LEDC *1 LEDC *2 LEDR
DINT *1 *2	OUT M9255	LEDA/LEDB DINT LEDC *1 LEDC *2 LEDR

Converting QnA series instructions to A series instructions (continued)

QnA Series	A Series	
	Common Instructions	Dedicated Instructions (for AnA, AnUCPU)
FLT *1 *2	OUT M9255	LEDA/LEDB FLOAT LEDC/SUB *1 LEDC *2 LEDR
DFLT *1 *2	OUT M9255	LEDA/LEDB DFLOAT LEDC/DXNR *1 LEDC *2 LEDR
DBL *1 *2	OUT M9255	
WORD *1 *2	OUT M9255	
GRY *1 *2	OUT M9255	
DGRY *1 *2	OUT M9255	
GBIN *1 *2	OUT M9255	
DGBIN *1 *2	OUT M9255	
DNEG *1	OUT M9255	
ENEG *1	OUT M9255	
BKBCD *1 *2 *3	OUT M9255	
BKBIN *1 *2 *3	OUT M9255	
EMOV *1 *2	OUT M9255	
$MOV *1 *2	OUT M9255	LEDA/LEDB SMOV LEDC *1 LEDC *2 LEDR
BXCH *1 *2	OUT M9255	
SWAP *1	OUT M9255	LEDA/LEDB SWAP LEDC *1 LEDR
GOEND	OUT M9255	
RFS *1 *2	OUT M9255	
DAND *1 *2 *3	OUT M9255	
DOR *1 *2 *3	OUT M9255	
DXOR *1 *2 *3	OUT M9255	
DXNR *1 *2 *3	OUT M9255	
BKAND *1 *2 *3 *4	OUT M9255	
BKOR *1 *2 *3 *4	OUT M9255	
BKXOR *1 *2 *3 *4	OUT M9255	
BKXNR *1 *2 *3 *4	OUT M9255	
TEST *1 *2 *3	OUT M9255	LEDA/LEDB TEST LEDC *1 LEDC/SUB *2 LEDC *3 LEDR

Converting QnA series instructions to A series instructions (continued)

QnA Series	A Series	
	Common Instructions	Dedicated Instructions (for AnA, AnUCPU)
DTEST *1 *2 *3	OUT M9255	LEDA/LEDB DTEST LEDC *1 LEDC/SUB *2 LEDC *3 LEDR
BKRST *1 *2	OUT M9255	
DSER *1 *2 *3 *4	OUT M9255	LEDA/LEDB DSER LEDC *1 LEDC *2 LEDC/SUB *4 LEDR
NDIS *1 *2 *3	OUT M9255	LEDA/LEDB DIS LEDC *1 LEDC *2 LEDC *3 LEDR
NUNI *1 *2 *3	OUT M9255	LEDA/LEDB UNI LEDC *1 LEDC *2 LEDC *3 LEDR
WTOB *1 *2 *3	OUT M9255	LEDA/LEDB WTOB LEDC *1 LEDC *2 LEDC/SUB *3 LEDR
BTOW *1 *2 *3	OUT M9255	LEDA/LEDB BTOW LEDC *1 LEDC *2 LEDC/SUB *3 LEDR
MAX *1 *2 *3	OUT M9255	
DMAX *1 *2 *3	OUT M9255	
MIN *1 *2 *3	OUT M9255	
DMIN *1 *2 *3	OUT M9255	
SORT *1 *2 *3 *4 *5	OUT M9255	
DSORT *1 *2 *3 *4 *5	OUT M9255	
WSUM *1 *2 *3	OUT M9255	
DWSUM *1 *2 *3	OUT M9255	
BREAK *1 *2	OUT M9255	
CALL *1 *2	OUT M9255	
CALL *1 *2 *3	OUT M9255	
CALL *1 *2 *3 *4	OUT M9255	
CALL *1 *2 *3 *4 *5	OUT M9255	

Converting QnA series instructions to A series instructions (continued)

QnA Series	A Series	
	Common Instructions	Dedicated Instructions (for AnA, AnUCPU)
CALL *1 *2 *3 *4 *5 *6	OUT M9255	
FCALL *1	OUT M9255	
FCALL *1 *2	OUT M9255	
FCALL *1 *2 *3	OUT M9255	
FCALL *1 *2 *3 *4	OUT M9255	
FCALL *1 *2 *3 *4 *5	OUT M9255	
FCALL *1 *2 *3 *4 *5 *6	OUT M9255	
ECALL *1 *2	OUT M9255	
ECALL *1 *2 *3	OUT M9255	
ECALL *1 *2 *3 *4	OUT M9255	
ECALL *1 *2 *3 *4 *5	OUT M9255	
ECALL *1 *2 *3 *4 *5 *6	OUT M9255	
ECALL *1 *2 *3 *4 *5 *6 *7	OUT M9255	
EFCALL *1 *2	OUT M9255	
EFCALL *1 *2 *3	OUT M9255	
EFCALL *1 *2 *3 *4	OUT M9255	
EFCALL *1 *2 *3 *4 *5	OUT M9255	
EFCALL *1 *2 *3 *4 *5 *6	OUT M9255	
EFCALL *1 *2 *3 *4 *5 *6 *7	OUT M9255	
IXSET *1 *2	OUT M9255	
FPOP *1 *2	OUT M9255	
FINS *1 *2 *3	OUT M9255	
FDEL *1 *2 *3	OUT M9255	
CHKST	OUT M9255	
CHK	OUT M9255	
CHKCIR	OUT M9255	
CHKEND	OUT M9255	
PTRA	OUT M9255	
PTRAR	OUT M9255	
PTRAEXE	OUT M9255	
BINDA *1 *2	OUT M9255	LEDA/LEDB BINDA LEDC/SUB *1 LEDC *2 LEDR
DBINDA *1 *2	OUT M9255	LEDA/LEDB DBINDA LEDC/DXNR *1 LEDC *2 LEDR
BINHA *1 *2	OUT M9255	LEDA/LEDB BINHA LEDC/SUB *1 LEDC *2 LEDR

Converting QnA series instructions to A series instructions (continued)

QnA Series	A Series	
	Common Instructions	Dedicated Instructions (for AnA, AnUCPU)
DBINHA *1 *2	OUT M9255	LEDA/LEDB DBINHA LEDC/DXNR *1 LEDC *2 LEDR
BCDDA *1 *2	OUT M9255	LEDA/LEDB BCDDA LEDC/SUB *1 LEDC *2 LEDR
DBCDDA *1 *2	OUT M9255	LEDA/LEDB DBCDDA LEDC/DXNR *1 LEDC *2 LEDR
DABIN *1 *2	OUT M9255	LEDA/LEDB DABIN LEDC *1 LEDC *2 LEDR
DDABIN *1 *2	OUT M9255	LEDA/LEDB DDABIN LEDC *1 LEDC *2 LEDR
HABIN *1 *2	OUT M9255	LEDA/LEDB HABIN LEDC *1 LEDC *2 LEDR
DHABIN *1 *2	OUT M9255	LEDA/LEDB DHABIN LEDC *1 LEDC *2 LEDR
DABCD *1 *2	OUT M9255	LEDA/LEDB DABCD LEDC *1 LEDC *2 LEDR
DDABCD *1 *2	OUT M9255	LEDA/LEDB DDABCD LEDC *1 LEDC *2 LEDR
COMRD *1 *2	OUT M9255	LEDA/LEDB COMRD LEDC *1 LEDC *2 LEDR
LEN *1 *2	OUT M9255	LEDA/LEDB LEN LEDC *1 LEDC *2 LEDR

Converting QnA series instructions to A series instructions (continued)

QnA Series	A Series	
	Common Instructions	Dedicated Instructions (for AnA, AnUCPU)
STR *1 *2 *3	OUT M9255	LEDA/LEDB STR LEDC *1 LEDC/SUB *2 LEDC *3 LEDR
DSTR *1 *2 *3	OUT M9255	LEDA/LEDB DSTR LEDC *1 LEDC/DXNR *2 LEDC *3 LEDR
VAL *1 *2 *3	OUT M9255	LEDA/LEDB VAL LEDC *1 LEDC *2 LEDC *3 LEDR
DVAL *1 *2 *3	OUT M9255	LEDA/LEDB DVAL LEDC *1 LEDC *2 LEDC *3 LEDR
ESTR *1 *2 *3	OUT M9255	
EVAL *1 *2	OUT M9255	
ASC *1 *2 *3	OUT M9255	LEDA/LEDB ASC LEDC *1 LEDC *2 LEDC/SUB *3 LEDR
HEX *1 *2 *3	OUT M9255	LEDA/LEDB HEX LEDC *1 LEDC *2 LEDC/SUB *3 LEDR
RIGHT *1 *2 *3	OUT M9255	
LEFT *1 *2 *3	OUT M9255	
MIDR *1 *2 *3	OUT M9255	
MIDW *1 *2 *3	OUT M9255	
INSTR *1 *2 *3 *4	OUT M9255	
EMOD *1 *2 *3	OUT M9255	
EREXP *1 *2 *3	OUT M9255	
SIN *1 *2	OUT M9255	LEDA/LEDB SIN LEDC *1 LEDC *2 LEDR

Converting QnA series instructions to A series instructions (continued)

QnA Series	A Series	
	Common Instructions	Dedicated Instructions (for AnA, AnUCPU)
COS *1 *2	OUT M9255	LEDA/LEDB COS LEDC *1 LEDC *2 LEDR
TAN *1 *2	OUT M9255	LEDA/LEDB TAN LEDC *1 LEDC *2 LEDR
ASIN *1 *2	OUT M9255	LEDA/LEDB ASIN LEDC *1 LEDC *2 LEDR
ACOS *1 *2	OUT M9255	LEDA/LEDB ACOS LEDC *1 LEDC *2 LEDR
ATAN *1 *2	OUT M9255	LEDA/LEDB ATAN LEDC *1 LEDC *2 LEDR
RAD *1 *2	OUT M9255	LEDA/LEDB RAD LEDC *1 LEDC *2 LEDR
DEG *1 *2	OUT M9255	LEDA/LEDB DEG LEDC *1 LEDC *2 LEDR
SQR *1 *2	OUT M9255	LEDA/LEDB SQR LEDC *1 LEDC *2 LEDR
EXP *1 *2	OUT M9255	LEDA/LEDB EXP LEDC *1 LEDC *2 LEDR
LOG *1 *2	OUT M9255	LEDA/LEDB LOG LEDC *1 LEDC *2 LEDR
BSQR *1 *2	OUT M9255	LEDA/LEDB BSQR LEDC/SUB *1 LEDC *2 LEDR

Converting QnA series instructions to A series instructions (continued)

QnA Series	A Series	
	Common Instructions	Dedicated Instructions (for AnA, AnUCPU)
BDSQR *1 *2	OUT M9255	LEDA/LEDB BDSQR LEDC/DXNR *1 LEDC *2 LEDR
BSIN *1 *2	OUT M9255	LEDA/LEDB BSIN LEDC/SUB *1 LEDC *2 LEDR
BCOS *1 *2	OUT M9255	LEDA/LEDB BCOS LEDC/SUB *1 LEDC *2 LEDR
BTAN *1 *2	OUT M9255	LEDA/LEDB BTAN LEDC/SUB *1 LEDC *2 LEDR
BASIN *1 *2	OUT M9255	LEDA/LEDB BASIN LEDC *1 LEDC *2 LEDR
BACOS *1 *2	OUT M9255	LEDA/LEDB BACOS LEDC *1 LEDC *2 LEDR
BATAN *1 *2	OUT M9255	LEDA/LEDB BATAN LEDC *1 LEDC *2 LEDR
LIMIT *1 *2 *3 *4	OUT M9255	LEDA/LEDB LIMIT LEDC/SUB *1 LEDC/SUB *2 LEDC/SUB *3 LEDC *4 LEDR
DLIMIT *1 *2 *3 *4	OUT M9255	LEDA/LEDB DLIMIT LEDC/DXNR *1 LEDC/DXNR *2 LEDC/DXNR *3 LEDC *4 LEDR

Converting QnA series instructions to A series instructions (continued)

QnA Series	A Series	
	Common Instructions	Dedicated Instructions (for AnA, AnUCPU)
BAND *1 *2 *3 *4	OUT M9255	LEDA/LEDB BAND LEDC/SUB *1 LEDC/SUB *2 LEDC/SUB *3 LEDC *4 LEDR
DBAND *1 *2 *3 *4	OUT M9255	LEDA/LEDB DBAND LEDC/DXNR *1 LEDC/DXNR *2 LEDC/DXNR *3 LEDC *4 LEDR
ZONE *1 *2 *3 *4	OUT M9255	LEDA/LEDB ZONE LEDC/SUB *1 LEDC/SUB *2 LEDC/SUB *3 LEDC *4 LEDR
DZONE *1 *2 *3 *4	OUT M9255	LEDA/LEDB DZONE LEDC/DXNR *1 LEDC/DXNR *2 LEDC/DXNR *3 LEDC *4 LEDR
RSET *1	OUT M9255	
QDRSET *1	OUT M9255	
QCDSET *1	OUT M9255	
DATERD *1	OUT M9255	LEDA/LEDB DATERD LEDC *1 LEDR
DATEWR *1	OUT M9255	LEDA/LEDB DATEWR LEDC *1 LEDR
DATE+ *1 *2 *3	OUT M9255	
DATE- *1 *2 *3	OUT M9255	
SECOND *1 *2	OUT M9255	
HOUR *1 *2	OUT M9255	
PIDINIT *1	OUT M9255	LEDA/LEDB PIDINIT LEDC *1 LEDR
PIDCONT *1	OUT M9255	LEDA PIDCONT LEDC *1 LEDR

Converting QnA series instructions to A series instructions (continued)

QnA Series	A Series	
	Common Instructions	Dedicated Instructions (for AnA, AnUCPU)
PID57 *1 *2 *3	OUT M9255	LEDA PID57 SUB *1 LEDC/SUB *2 LEDC *3 LEDR
PIDSTOP *1	OUT M9255	
PIDRUN *1	OUT M9255	
PIDPRMW *1 *2	OUT M9255	
MSG *1	OUT M9255	
PKEY *1	OUT M9255	
PSTOP *1	OUT M9255	
POFF *1	OUT M9255	
PSCAN *1	OUT M9255	
PLOW *1	OUT M9255	
ZRRDB *1 *2	OUT M9255	
ZRWRB *1 *2	OUT M9255	
ADRSET *1 *2	OUT M9255	
KEY *1 *2 *3 *4	OUT M9255	LEDA KEY LEDC *1 LEDC *2 LEDC *3 LEDC *4 LEDR
UDCNT1 *1 *2 *3	OUT M9255	
UDCNT2 *1 *2 *3	OUT M9255	
TTMR *1 *2	OUT M9255	
STMR *1 *2 *3	OUT M9255	
ROTC *1 *2 *3 *4	OUT M9255	
RAMP *1 *2 *3 *4 *5	OUT M9255	
SPD *1 *2 *3	OUT M9255	
PLSY *1 *2 *3	OUT M9255	
PWM *1 *2 *3	OUT M9255	
MTR *1 *2 *3 *4	OUT M9255	
IMASK *1	OUT M9255	
IX *1	OUT M9255	
IXEND	OUT M9255	
IXDEV	OUT M9255	
S. ****	OUT M9255	
Z. ****	OUT M9255	
G. ****	OUT M9255	
J. ****	OUT M9255	

12.2 A Instruction Conversion List for FX Series Conversions

A	QnA	FX
•	×	•

The rules for device and instruction conversions when performing A <-> FX conversions are given here.
For instructions that cannot be converted, make a correction after instruction conversion by referring to the lists.
The instruction conversion list for conversions from A to FX is given in pages 80 to 85.
The instruction conversion list for conversions from FX to A is given in pages 86 to 92.
The indications *, *1, *2, *3, *4, *5, *6, and *7 in the lists refer to sources and destinations.

Device correspondence table for A → FX conversions

A Series	FX Series	Remarks
M	M	
M9000 to	M8255	
L	M8255	
F	M8255	
S	S	
X	X	The hexadecimal input numbers of the "A" series are condensed as octal numbers headed by X0 for the FX series
Y	Y	The hexadecimal input numbers of the "A" series are condensed as octal numbers headed by X0 for the FX series
B	M8255	
D	D	
D9000 to	D8255	
A0¤1	D8255	
R	D1000 to	
W	D8000 to	
T	T	
C	C	
Z, Z1 to Z6	Z, Z1 to Z6	
172.16.	V, V1 to V6	
P	P	If out-of-range, the instruction becomes OUT M8255
I	I	If out-of-range, the instruction becomes OUT M8255
N	N	If out-of-range, the instruction becomes OUT M8255
K	K	
H	H	
" "	" "	
Z, Z1 to Z6	Z, Z1 to Z6	
K	K	
V, V1 to V6	V, V1 to V6	

Devices that contain out-of-range device parts or extension parts are changed to M8255 if bits and D8255 if words.

Converting A series to FX series

A Series	FX Series	Remarks
NOP	NOP	
LD *1	LD *1	
LDI *1	LDI *1	
OR *1	OR *1	
ORI *1	ORI *1	
AND *1	AND *1	
ANI *1	ANI *1	
ORB	ORB	
ANB	ANB	
MPS	MPS	
MRD	MRD	
MPP	MPP	
OUT *1	OUT *1	
OUT T/C* *2	OUT T/C* *2	
SET *1	SET *1	
RST *1	RST *1	
PLS *1	PLS *1	
PLF *1	PLF *1	
SFT *1	OUT M8255	
SFTP *1	OUT M8255	
MC *1 *2	MC *1 *2	
STOP	OUT M8255	
MCR *1	MCR *1	
FEND	FEND	
END	END	
NOPLF	OUT M8255	
P*,I*	P*,I*	
LD= *1 *2 OR= *1 *2 AND= *1 *2	LD= *1 *2 OR= *1 *2 AND= *1 *2	For models other than FX2N(C): LD/OR/AND M8255
LD<> *1 *2 OR<> *1 *2 AND<> *1 *2	LD<> *1 *2 OR<> *1 *2 AND<> *1 *2	For models other than FX2N(C): LD/OR/AND M8255
LD> *1 *2 OR> *1 *2 AND> *1 *2	LD> *1 *2 OR> *1 *2 AND> *1 *2	For models other than FX2N(C): LD/OR/AND M8255
LD>= *1 *2 OR>= *1 *2 AND>= *1 *2	LD>= *1 *2 OR>= *1 *2 AND>= *1 *2	For models other than FX2N(C): LD/OR/AND M8255
LD< *1 *2 OR< *1 *2 AND< *1 *2	LD< *1 *2 OR< *1 *2 AND< *1 *2	For models other than FX2N(C): LD/OR/AND M8255

(continued on next page)

A Series	FX Series	Remarks
LD<= *1 *2 OR<= *1 *2 AND<= *1 *2	LD<= *1 *2 OR<= *1 *2 AND<= *1 *2	For models other than FX2N(C): LD/OR/AND M8255
LDD= *1 *2 ORD= *1 *2 ANDD= *1 *2	LDD= *1 *2 ORD= *1 *2 ANDD= *1 *2	For models other than FX2N(C): LD/OR/AND M8255
LDD<> *1 *2 ORD<> *1 *2 ANDD<> *1 *2	LDD<> *1 *2 ORD<> *1 *2 ANDD<> *1 *2	For models other than FX2N(C): LD/OR/AND M8255
LDD> *1 *2 ORD> *1 *2 ANDD> *1 *2	LDD> *1 *2 ORD> *1 *2 ANDD> *1 *2	For models other than FX2N(C): LD/OR/AND M8255
LDD>= *1 *2 ORD>= *1 *2 ANDD>= *1 *2	LDD>= *1 *2 ORD>= *1 *2 ANDD>= *1 *2	For models other than FX2N(C): LD/OR/AND M8255
LDD< *1 *2 ORD< *1 *2 ANDD< *1 *2	LDD< *1 *2 ORD< *1 *2 ANDD< *1 *2	For models other than FX2N(C): LD/OR/AND M8255
LDD<= *1 *2 ORD<= *1 *2 ANDD<= *1 *2	LDD<= *1 *2 ORD<= *1 *2 ANDD<= *1 *2	For models other than FX2N(C): LD/OR/AND M8255
+ *1 *2	ADD *1 *2 D8255	
+ *1 *2 *3	ADD *1 *2 *3	
- *1 *2	SUB *1 *2 D8255	
- *1 *2 *3	SUB *1 *2 *3	
D+ *1 *2	DADD *1 *2 D8255	
D+ *1 *2 *3	DADD *1 *2 *3	
D- *1 *2	DSUB *1 *2 D8255	
D- *1 *2 *3	DSUB *1 *2 *3	
* *1 *2 *3	MUL *1 *2 *3	
/ *1 *2 *3	DIV *1 *2 *3	
D* *1 *2 *3	DMUL *1 *2 *3	
D/ *1 *2 *3	DDIV *1 *2 *3	
B+ *1 *2	OUT M8255	
B+ *1 *2 *3	OUT M8255	
B- *1 *2	OUT M8255	
B- *1 *2 *3	OUT M8255	
DB+ *1 *2	OUT M8255	
DB+ *1 *2 *3	OUT M8255	
DB- *1 *2	OUT M8255	
DB- *1 *2 *3	OUT M8255	
B* *1 *2 *3	OUT M8255	
B/ *1 *2 *3	OUT M8255	
DB* *1 *2 *3	OUT M8255	
DB/ *1 *2 *3	OUT M8255	

(continued on next page)

A Series	FX Series	Remarks
INC *1	INC *1	
DINC *1	DINC *1	
DEC *1	DEC *1	
DDEC *1	DDEC *1	
BCD *1 *2	BCD *1 *2	
DBCD *1 *2	DBCD *1 *2	
BIN *1 *2	BIN *1 *2	
DBIN *1 *2	DBIN *1 *2	
NEG *1	NEG *1	FX1, FX0N, FX0: OUT M8255
MOV *1 *2	MOV *1 *2	
DMOV *1 *2	DMOV *1 *2	
CML *1 *2	CML *1 *2	For FX1, FX0N, FX0: OUT M8255
DCML *1 *2	DCML *1 *2	For FX1, FX0N, FX0: OUT M8255
BMOV *1 *2 *3	BMOV *1 *2 *3	For FX1, FX0: M8255
FMOV *1 *2 *3	FMOV *1 *2 *3	For FX1, FX0N, FX0: OUT M8255
XCH *1 *2	XCH *1 *2	For FX1, FX0N, FX0: OUT M8255
DXCH *1 *2	DXCH *1 *2	For FX1, FX0N, FX0: OUT M8255
CJ *1	CJ *1	
SCJ *1	CJ *1	
SUB *1	OUT M8255	
CHG	OUT M8255	
WAND *1 *2	WAND *1 *2 D8255	
WAND *1 *2 *3	WAND *1 *2 *3	
WOR *1 *2	WOR *1 *2 D8255	
WOR *1 *2 *3	WOR *1 *2 *3	
WXOR *1 *2	WXOR *1 *2 D8255	
WXOR *1 *2 *3	WXOR *1 *2 *3	
WXNR *1 *2	OUT M8255	
WXNR *1 *2 *3	OUT M8255	
DAND *1 *2	DAND *1 *2 D8255	
DOR *1 *2	DOR *1 *2 D8255	
DXOR *1 *2	DXOR *1 *2 D8255	
DXNR *1 *2	OUT M8255	
ROR *1	ROR D8255 *1	For FX1, FX0N, FX0: OUT M8255
RCR *1	RCR D8255 *1	For FX1, FX0N, FX0: OUT M8255
ROL *1	ROL D8255 *1	For FX1, FX0N, FX0: OUT M8255
RCL *1	RCL D8255 *1	For FX1, FX0N, FX0: OUT M8255
DROR *1	OUT M8255	
DRCR *1	OUT M8255	
DROL *1	OUT M8255	
DRCL *1	OUT M8255	
SFR *1 *2	OUT M8255	
SFL *1 *2	OUT M8255	

(continued on next page)

A Series	FX Series	Remarks
BSFR *1 *2	OUT M8255	
BSFL *1 *2	OUT M8255	
DSFR *1 *2	OUT M8255	
DSFL *1 *2	OUT M8255	
BSET *1 *2	OUT M8255	
BRST *1 *2	OUT M8255	
DECO *1 *2 *3	DECO *1 *2 *3	
ENCO *1 *2 *3	ENCO *1 *2 *3	
SEG *1 *2	SEGD *1 *2	For FX1, FX0N, FX0: OUT M8255
DIS *1 *2 *3	OUT M8255	
UNI *1 *2 *3	OUT M8255	
SER *1 *2 *3	SER *1 *2 D8255 *3	For FX1, FX0N, FX0: OUT M8255
SUM *1	SUM *1 D8255	For FX1, FX0N, FX0: OUT M8255
DSUM *1	DSUM *1 D8255	For FX1, FX0N, FX0: OUT M8255
ASC *1 *2	ASC *1 *2	For FX1, FX0N, FX0: OUT M8255
CALL *1	CALL *1	For FX0N, FX0: M8255
FIFW *1 *2	OUT M8255	
FIFR *1 *2	OUT M8255	
FROM *1 *2 *3 *4	FROM *1 *2 *3 *4	For FX1, FX0: M8255
DFRO *1 *2 *3 *4	DFROM *1 *2 *3 *4	For FX1, FX0: M8255
TO *1 *2 *3 *4	TO *1 *2 *3 *4	For FX1, FX0: M8255
DTO *1 *2 *3 *4	DTO *1 *2 *3 *4	For FX1, FX0: M8255
LRDP *1 *2 *3 *4	OUT M8255	
LWTP *1 *2 *3 *4	OUT M8255	
RFRP *1 *2 *3 *4	OUT M8255	
RTOP *1 *2 *3 *4	OUT M8255	
PR *1 *2	PR *1 *2	For FX0N, FX0: M8255
PRC *1 *2	OUT M8255	
LED *1	OUT M8255	
LEDC *1	OUT M8255	
LEDR	OUT M8255	
LEDA *1	OUT M8255	
LEDB *1	OUT M8255	
SLT	OUT M8255	
SLTR	OUT M8255	
STRA	OUT M8255	
STRAR	OUT M8255	
WDT	WDT	
DUTY *1 *2 *3	OUT M8255	
CHK *1 *2	OUT M8255	
STC	SET M8022	
CLC	RST M8022	
JMP *1	CJ *1	

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A Series	FX Series	Remarks
DI	DI	
EI	EI	
IRET	IRET	
FOR *1	FOR *1	
NEXT	NEXT	
RET	SRET	For FX1, FX0: M8255
COM	OUT M8255	

Device correspondence table for FX → A conversions

FX Series	A Series	Remarks
M	M	
M8000 to	M9255	
S	M9255	The octal input numbers of the FX series are condensed as hexadecimal numbers headed by X0 for the "A" series
X	X	The octal input numbers of the FX series are condensed as hexadecimal numbers headed by X0 for the "A" series
Y	Y	
D	D	
D8000 to	D9255	
T	T	
C	C	
Z, Z1 to Z6	Z, Z1 to Z6	
V, V1 to V6	V, V1 to V6	
V7, Z7	D9255	
P	P	If out-of-range, the instruction becomes OUT M9255
I	I	If out-of-range, the instruction becomes OUT M9255
N	N	If out-of-range, the instruction becomes OUT M9255
K	K	
H	H	
""	""	
Z, Z1 to Z6	Z, Z1 to Z6	If the device part is a device that cannot be converted, all devices containing this code become M9255 or D255.
V, V1 to V6	V, V1 to V6	If the device part is a device that cannot be converted, all devices containing this code become M9255 or D255.
V7, Z7	M9255, D9255	All devices containing this code become M9255 or D9255.
K	K	If the device part is a device that cannot be converted, all devices containing this code become M9255 or D255.

Devices that contain out-of-range device parts or extension parts are changed to M9255 if bits and D9255 if words.

Converting FX series to A series

FX Series	A Series	Remarks
NOP	NOP	
LD *1	LD *1	
LDI *1	LDI *1	
LDP *1	LD M9255	FX2N(C) only
LDF *1	LD M9255	FX2N(C) only
OR *1	OR *1	
ORI *1	ORI *1	
ORP *1	OR M9255	FX2N(C) only
ORF *1	OR M9255	FX2N(C) only
AND *1	AND *1	
ANI *1	ANI *1	
ANDP *1	AND M9255	FX2N(C) only
ANDF *1	AND M9255	FX2N(C) only
INV	AND M9255	FX2N(C) only
ORB	ORB	
ANB	ANB	
MPS	MPS	
MRD	MRD	
MPP	MPP	
OUT *1	OUT *1	
OUT T/C0 to 199 *2	OUT T/C *2	
OUT C200 to *2	OUT M9255	32-bit counters are not changed.
SET *1	SET *1	
RST *1	RST *1	
PLS *1	PLS *1	
PLF *1	PLF *1	
MC *1 *2	MC *1 *2	
MCR *1	MCR *1	
FEND	FEND	
END	END	
P*,I*	P*,I*	
LD= *1 *2 OR= *1 *2 AND= *1 *2	LD= *1 *2 OR= *1 *2 AND= *1 *2	FX2N(C) only
LD<> *1 *2 OR<> *1 *2 AND<> *1 *2	LD<> *1 *2 OR<> *1 *2 AND<> *1 *2	FX2N(C) only
LD> *1 *2 OR> *1 *2 AND> *1 *2	LD> *1 *2 OR> *1 *2 AND> *1 *2	FX2N(C) only
LD>= *1 *2 OR>= *1 *2 AND>= *1 *2	LD>= *1 *2 OR>= *1 *2 AND>= *1 *2	FX2N(C) only

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FX Series	A Series	Remarks
LD< *1 *2 OR< *1 *2 AND< *1 *2	LD< *1 *2 OR< *1 *2 AND< *1 *2	FX2N(C) only
LD<= *1 *2 OR<= *1 *2 AND<= *1 *2	LD<= *1 *2 OR<= *1 *2 AND<= *1 *2	FX2N(C) only
LDD= *1 *2 ORD= *1 *2 ANDD= *1 *2	LDD= *1 *2 ORD= *1 *2 ANDD= *1 *2	FX2N(C) only
LDD<> *1 *2 ORD<> *1 *2 ANDD<> *1 *2	LDD<> *1 *2 ORD<> *1 *2 ANDD<> *1 *2	FX2N(C) only
LDD> *1 *2 ORD> *1 *2 ANDD> *1 *2	LDD> *1 *2 ORD> *1 *2 ANDD> *1 *2	FX2N(C) only
LDD>= *1 *2 ORD>= *1 *2 ANDD>= *1 *2	LDD>= *1 *2 ORD>= *1 *2 ANDD>= *1 *2	FX2N(C) only
LDD< *1 *2 ORD< *1 *2 ANDD< *1 *2	LDD< *1 *2 ORD< *1 *2 ANDD< *1 *2	FX2N(C) only
LDD<= *1 *2 ORD<= *1 *2 ANDD<= *1 *2	LDD<= *1 *2 ORD<= *1 *2 ANDD<= *1 *2	FX2N(C) only
CMP	OUT M9255	
DCMP	OUT M9255	
ZCP	OUT M9255	
DZCP	OUT M9255	
DECMP	OUT M9255	
DEZCP	OUT M9255	
ADD *1 *2 *2	+ *1 *2 *3	
SUB *1 *2 *2	- *1 *2 *3	
DADD *1 *2 *2	D+ *1 *2 *3	
DSUB *1 *2 *2	D- *1 *2 *3	
MUL *1 *2 *3	* *1 *2 *3	
DIV *1 *2 *3	/ *1 *2 *3	
DMUL *1 *2 *3	D* *1 *2 *3	
DDIV *1 *2 *3	D/ *1 *2 *3	
DEADD *1 *2 *3	OUT M9255	
DESUB *1 *2 *3	OUT M9255	
DEMUL *1 *2 *3	OUT M9255	
DEDIV *1 *2 *3	OUT M9255	
INC *1	INC *1	
DINC *1	DINC *1	

(continued on next page)

FX Series	A Series	Remarks
DEC *1	DEC *1	
DDEC *1	DDEC *1	
BCD *1 *2	BCD *1 *2	
DBCD *1 *2	DBCD *1 *2	
BIN *1 *2	BIN *1 *2	
DBIN *1 *2	DBIN *1 *2	
INT *1 *2	OUT M9255	FX2N(C) only
DINT *1 *2	OUT M9255	FX2N(C) only
GRY *1 *2	OUT M9255	FX2N(C) only
DGRY *1 *2	OUT M9255	FX2N(C) only
GBIN *1 *2	OUT M9255	FX2N(C) only
DGBIN *1 *2	OUT M9255	FX2N(C) only
NEG *1	NEG *1	
DNEG *1	OUT M9255	
DEBCD	OUT M9255	
DEBIN	OUT M9255	
MOV *1 *2	MOV *1 *2	
DMOV *1 *2	DMOV *1 *2	
CML *1 *2	CML *1 *2	
DCML *1 *2	DCML *1 *2	
BMOV *1 *2 *3	BMOV *1 *2 *3	
FMOV *1 *2 *3	FMOV *1 *2 *3	
XCH *1 *2	XCH *1 *2	
DXCH *1 *2	DXCH *1 *2	
SWAP *1	OUT M9255	FX2N(C) only
SMOV	OUT M9255	
DSWAP *1	OUT M9255	FX2N(C) only
DFMOV *1 *2 *3	OUT M9255	
CJ *1	CJ *1	
REF	OUT M9255	
REFF	OUT M9255	
HSCS	OUT M9255	
DHSCS	OUT M9255	
HSCR	OUT M9255	
DHSCR	OUT M9255	
HSZ	OUT M9255	
DHSZ	OUT M9255	
WAND *1 *2 *3	WAND *1 *2 *3	
WOR *1 *2 *3	WOR *1 *2 *3	
WXOR *1 *2 *3	WXOR *1 *2 *3	
DAND *1 *2 *3	DAND *1 *2	
DOR *1 *2 *3	DOR *1 *2	
DXOR *1 *2 *3	DXOR *1 *2	
ROR *1 *2	ROR *2	

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FX Series	A Series	Remarks
RCR *1 *2	RCR *2	
ROL *1 *2	ROL *2	
RCL *1 *2	RCL *2	
DROR *1 *2	DROR *2	
DRCR *1 *2	DRCR *2	
DROL *1 *2	DROL *2	
DRCL *1 *2	DRCL *2	
SFTR *1 *2 *3 *4	OUT M9255	
SFTL *1 *2 *3 *4	OUT M9255	
WSFR *1 *2 *3 *4	OUT M9255	
WSFL *1 *2 *3 *4	OUT M9255	
SFWR *1 *2 *3	OUT M9255	
SFRD *1 *2 *3	OUT M9255	
SER *1 *2 *3 *4	SER *1 *2 *4	
DSER *1 *2 *3 *4	OUT M9255	
DECO *1 *2 *3	DECO *1 *2 *3	
ENCO *1 *2 *3	ENCO *1 *2 *3	
SORT *1 *2 *3 *4 *5	OUT M9255	
ASC *1 *2	ASC *1 *2	
ZRST *1 *2	OUT M9255	
SUM *1 *2	SUM *1	
DSUM *1 *2	DSUM *1	
BON *1 *2 *3	OUT M9255	
DBON *1 *2 *3	OUT M9255	
MEAN *1 *2 *3	OUT M9255	
DMEAN *1 *2 *3	OUT M9255	
ANS *1 *2 *3	OUT M9255	
ANR	OUT M9255	
FLT *1 *2	OUT M9255	FX2N(C) only
DFLT *1 *2	OUT M9255	FX2N(C) only
CALL *1	CALL *1	
FROM *1 *2 *3 *4	FROM *1 *2 *3 *4	
DFROM *1 *2 *3 *4	DFRO *1 *2 *3 *4	
TO *1 *2 *3 *4	TO *1 *2 *3 *4	
DTO *1 *2 *3 *4	DTO *1 *2 *3 *4	
PR *1 *2	PR *1 *2	
HEX *1 *2 *3	OUT M9255	
ASCI *1 *2 *3	OUT M9255	
SQR *1 *2	OUT M9255	
DSQR	OUT M9255	
DESQR *1 *2	OUT M9255	
DSIN *1 *2	OUT M9255	FX2N(C) only
DCOS *1 *2	OUT M9255	FX2N(C) only
DTAN *1 *2	OUT M9255	FX2N(C) only

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FX Series	A Series	Remarks
TCMP	OUT M9255	
TZCP	OUT M9255	
TADD	OUT M9255	
TSUB	OUT M9255	
TRD	OUT M9255	
TWR	OUT M9255	
PID	OUT M9255	
TKY	OUT M9255	
DTKY	OUT M9255	
HKY	OUT M9255	
DHKY	OUT M9255	
DSW	OUT M9255	
SEGD	OUT M9255	
SEGL	OUT M9255	
ARWS	OUT M9255	
RS	OUT M9255	
PRUN	OUT M9255	
DPRUN	OUT M9255	
CCD	OUT M9255	
VRRD	OUT M9255	
VRSC	OUT M9255	
MNET	OUT M9255	
ANRD	OUT M9255	
ANWR	OUT M9255	
RMST	OUT M9255	
RMWR	OUT M9255	
DRMWR	OUT M9255	
RMRD	OUT M9255	
DRMRD	OUT M9255	
RMMN	OUT M9255	
BLK	OUT M9255	
MCDE	OUT M9255	
WDT	WDT	
TTMR	OUT M9255	
STMR	OUT M9255	
ROTC	OUT M9255	
SPD	OUT M9255	
PLSY	OUT M9255	
PWM	OUT M9255	
MTR	OUT M9255	
DPLSY	OUT M9255	
IST	OUT M9255	
ABSD	OUT M9255	
DABSD	OUT M9255	

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FX Series	A Series	Remarks
INCD	OUT M9255	
ALT	OUT M9255	
RAMP	OUT M9255	
PLSR	OUT M9255	
OPT	OUT M9255	
DPLSR	OUT M9255	
DOPT	OUT M9255	
FNC**/FNCD**	OUT M9255	
DI	DI	
EI	EI	
IRET	IRET	
SRET	RET	
FOR *1	FOR *1	
NEXT	NEXT	
STL *1	OUT M9255	
RET	OUT M9255	

GPP Function software for Windows
SW2D5C-GPPW-E
SW2D5F-GPPW-E
Operating Manual

MODEL	SW2D5-GPPW-OPE-E
MODEL CODE	13J937
IB(NA)-66877-A(9810)MEE	

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