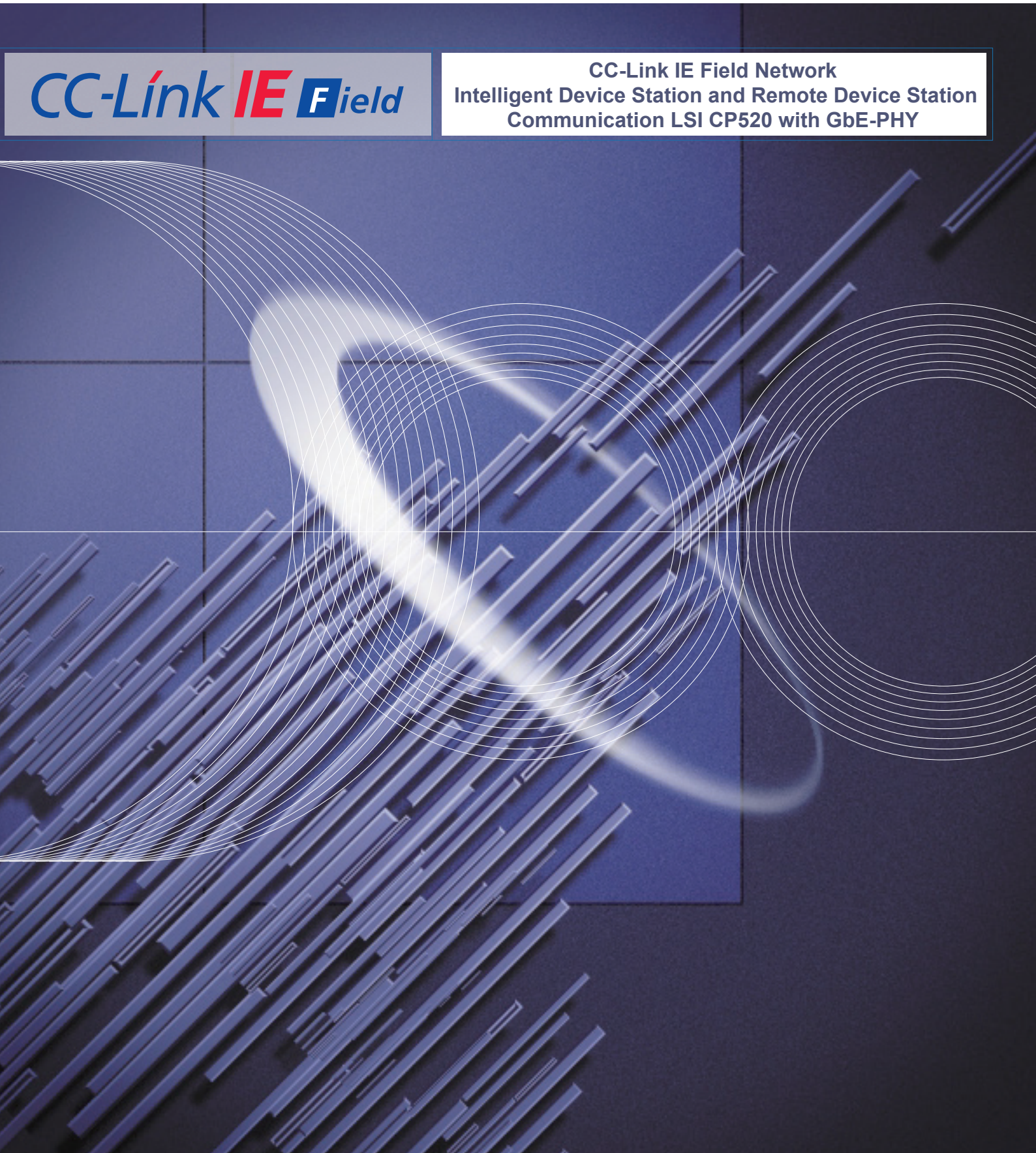
MITSUBISHI ELECTRIC

Changes for the Better

Ethernet Based Open Network
CC-Link IE Compatible Product Reference Manual



CC-Link IE Field Network
Intelligent Device Station and Remote Device Station
Communication LSI CP520 with GbE-PHY

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CONTENTS

Relevant Manuals

This manual does not describe the details on terms and functions of CC-Link IE Field Network.
For the details, please refer to the following manuals.

Related Manual Titles	Manual Number (Model Name Code)
[MELSEC iQ-R Ethernet/CC-Link IE User's Manual (Startup)] Specifications, procedures before operation, system configuration, wiring, and communication examples of Ethernet, CC-Link IE Controller Network, and CC-Link IE Field Network	SH(NA)-081256ENG (13JX09)
[MELSEC iQ-R CC-Link IE Field Network User's Manual (Application)] Functions, parameter settings, programming, troubleshooting, I/O signals, and buffer memory of CC-Link IE Field Network	SH(NA)-081259ENG (13JX18)
[MELSEC-Q CC-Link IE Field Network Master/Local Module User's Manual] Specifications, procedures before operation, system configuration, settings, functions, programming, and troubleshooting of the CC-Link IE Field Network and MELSEC-Q series master/local module	SH(NA)-080917ENG (13JZ47)
[MELSEC-L CC-Link IE Field Network Master/Local Module User's Manual] Specifications, procedures before operation, system configuration, installation, settings, functions, programming, and troubleshooting of the CC-Link IE Field Network and MELSEC-L series master/local module	SH(NA)-080972ENG (13JZ54)
[MELSEC-L CC-Link IE Field Network Head Module User's Manual] Specifications, procedures before operation, system configuration, installation, settings, and troubleshooting of the head module	SH(NA)-080919ENG (13JZ48)
[SLMP Reference Manual] Protocol (SLMP) used by external devices to read/write data from/to SLMP-compatible devices	SH(NA)-080956ENG (13JV23)

Terms

Unless otherwise specified, this manual uses the following terms.

Term	Description
Another station	A station other than own station
Buffer memory	Memory in a user application, where data (such as setting values and monitoring values) are stored
CP520	A GbE-PHY built-in communication LSI for intelligent device stations and remote device stations of CC-Link IE Field Network
CP520 application circuit	A communication circuit of CC-Link IE Field Network. A circuit consists of CP520 and peripheral devices.
CP520 application product	A CC-Link IE Field Network compatible product manufactured with reference to this manual
CSP+	An abbreviation for Control & Communication System Profile. This is the specifications for describing information required for start-up, operation, and maintenance of CC-Link family compatible devices.
Cyclic transmission	A function by which data are periodically exchanged among stations on the same network using link devices
Data link	A generic term for cyclic transmission and transient transmission
Device	Memory (X, Y, M, D, or others) in a programmable controller CPU, or memory in a user application, where data communicated with CP520 are stored
Disconnection	A process of stopping data link if a data link error occurs
End user	A purchaser and user of CC-Link family compatible products developed by users
GbE-PHY	An abbreviation for Gigabit Ethernet PHY. In this manual, the term refers to an IEEE 802.3 1000BASE-T compatible physical layer that has GMII.
GMII	An abbreviation for Gigabit Media-Independent Interface. This is an interface for communicating data between the MAC port (MAC layer) and the PHY (physical layer) of CP520.
GX Works2/GX Works3	The product name of the software package for the MELSEC programmable controllers
Intelligent device station	A station that exchanges I/O signals (bit data) and I/O data (word data) with the master station by cyclic transmission. This station can also perform transient transmission. This station responds to a transient transmission request from another station and also issues a transient transmission request to another station.
Link device	A device in a network module (RX, RY, RWr, and RWw)
Local station	A station that performs cyclic transmission and transient transmission with the master station and other local stations. This station receives data in RX, RY, RWr, and RWw of other slave stations in cyclic transmission.
Management interface	An interface for accessing PHY registers from CP520. The interface consists of MDIO and MDC.
Master station	A station that controls CC-Link IE Field Network. This station can perform cyclic transmission and transient transmission with all stations.
Master/local module	An abbreviation for the RJ71GF11-T2, QJ71GF11-T2, or LJ71GF11-T2 CC-Link IE Field Network master/local module, and also a generic term for the RJ71EN71 and RnENCPU modules when the CC-Link IE Field Network function is used
MDC	An abbreviation for Management Data Clock. This is an MDIO clock specified in GMII. This configures a management interface together with MDIO.
MDI	An abbreviation for Medium Dependent Interface. This is an interface for communicating data between CP520 and a pulse transformer and between a pulse transformer and an RJ-45 connecter.
MDIO	An abbreviation for Management Data Input/Output. This is a data input/output bus for accessing PHY registers specified in GMII. This configures a management interface together with MDC.
MIB	An abbreviation for Management Information Base. This is a management information base for saving the communication status of CP520.
Own station	An intelligent device station or remote device station to be developed based on this manual
PHY	An abbreviation for the physical layer. In this manual, the term refers to a portion of CP520 functions, that converts logic signals into actual electrical signals in an interface such as Ethernet.
Remote device station	A station that exchanges I/O signals (bit data) and I/O data (word data) with the master station by cyclic transmission. This station responds to a transient transmission request from another station
Remote input (RX)	Bit data input from a slave station to the master station
Remote output (RY)	Bit data output from the master station to a slave station
Remote register (RWr)	Word data input from a slave station to the master station

Term	Description
Remote register (RWw)	Word data output from the master station to a slave station
Return	A process of restarting data link when a station recovers from an error
R-IN32M4-CL2	An industrial Ethernet communication LSI of Renesas Electronics Corporation
Slave station	A generic term for stations other than a master station: local station, intelligent device station, remote device station, remote I/O station
SLMP	An abbreviation for Seamless Message Protocol. This is a protocol used to access an SLMP-compatible device or a programmable controller connected to an SLMP-compatible device from an external device.
Station	An element that forms a network and sends/receives/transfers data. The term, node, is used with the same meaning.
Station number	A unique number assigned to stations in a network
Transient transmission	A function that communicates data with another station when requested by a user application
User	A manufacturer who develops and sells CC-Link family compatible products based on this manual. The terms, vendor and partner manufacturer, are used with the same meaning.

Usage Precautions

(1) The intellectual property rights of the information provided on the CD-ROM included with this manual belong to Mitsubishi Electric. Reprinting the information without the consent of Mitsubishi Electric and reproduction of the information for any purpose other than the development of an intelligent device station or a remote device station is prohibited. Distribution of a product (object code or the like) after sample code compilation, however, is unrestricted.

(2) Before using the software provided on the CD-ROM included with this manual, check the "END-USER SOFTWARE LICENSE AGREEMENT" (CP520_Software_License_Agreement_e.pdf) provided on the same CD-ROM.

(3) The sample code described in this manual is for the development of an intelligent device station or a remote device station using CP520. The sample code indicates an example of use of the materials herein; its operation is not guaranteed by Mitsubishi Electric.

Address Notation

This manual uses byte addresses, unless otherwise specified.

Radix Notation

This manual uses the following radix notation, unless otherwise specified.

Radix	Description	Example
Binary	"b" is added at the end of the number to indicate bit.	"0b"
Decimal	Nothing is added at the end of the number.	"0"
Hexadecimal	"H" is added at the end of the number to indicate hexadecimal.	"10BAH"

CC-Link Partner Association

(1) Specifications

The materials related to this manual include the specifications published by the CC-Link Partner Association below. For CC-Link IE Field Network and SLMP details, download and refer to these specifications from the CC-Link Partner Association website.

Document Title	Document No.
CC-Link IE Field Network Specification (Overview)	BAP-C2005ENG-001
CC-Link IE Field Network Specification (Physical Layer and Data Link Layer)	BAP-C2005ENG-002
CC-Link IE Field Network Specification (Application Layer Service)	BAP-C2005ENG-003
CC-Link IE Field Network Specification (Application Layer Protocol)	BAP-C2005ENG-004
CC-Link IE Field Network Specification (Communication Profile)	BAP-C2005ENG-005
CC-Link IE Field Network Specification (Implementation Rules)	BAP-C2005ENG-006
CC-Link IE Field Network Specification (Device Profile)	BAP-C2005ENG-007
SLMP (Seamless Message Protocol) Specification (Overview)	BAP-C2006ENG-001
SLMP (Seamless Message Protocol) Specification (Services)	BAP-C2006ENG-002
SLMP (Seamless Message Protocol) Specification (Protocol)	BAP-C2006ENG-003
SLMP Reference Manual	BAP-C3002-001

(2) CC-Link IE Field Utility

This is a tool that simulates the master station on a personal computer. The user can simulate the master station on a personal computer without having the actual master station. Download the tool from the CC-Link Partner Association website as necessary.

Document Title/Related Tool	Document No.
CC-Link IE Field Utility	-
CC-Link IE Field Utility Operation manual	-

(3) Conformance test

When a product is developed based on the information in this manual, the product must undergo a conformance test implemented by the CC-Link Partner Association. For conformance test details, download and refer to the following document from the CC-Link Partner Association website.

Document Title	Document No.
CC-Link IE Field Network Intelligent Device Station Conformance Test Specifications	BAP-C0401ENG-037
CC-Link IE Field Network Remote Device Station Conformance Test Specification	BAP-C0401ENG-041

(4) Creating a Control & Communication System Profile (CSP+)

The conformance test includes verification of CSP+. CSP+ files must be created in advance. For CSP+ details, download and refer to the following documents from the CC-Link Partner Association website.
From the same website, other relevant documents and tool that help users create CSP+ files can also be download.

Document Title/Related Tool	Document No.
Control & Communication System Profile Specification	BAP-C2008ENG-001
Control & Communication System Profile Creation Guidelines	-
CSP+ profile creation support tool	-
Sample CSP+ Files	-
CSP+ Templates	-

(5) 1000BASE-T compliance test

The conformance test includes verification by a 1000BASE-T compliance test (a waveform test based on IEEE 802.3 specifications), which requires implementation by the user.

There are testing laboratories capable of implementing the 1000BASE-T compliance test. For details, contact the CC-Link Partner Association.

(6) Inquiries

To request materials published by the CC-Link Partner Association and for conformance test details, please contact the following:

TEL: +81-52-919-1588

FAX: +81-52-916-8655

E-mail: info@cc-link.org

Web: http://www.cc-link.org/

1 OVERVIEW

This manual describes how to develop an intelligent device station or remote device station for CC-Link IE Field Network using "CC-Link IE Field Network intelligent device stations and remote device stations communication LSI CP520 with GbE-PHY".
The main information included in this manual is as follows:

- CP520 specifications
- CP520 application circuit design
- User program design
- CP520 driver specifications

1.1 Development Features

CP520 is an LSI that integrates the communication IP core for CC-Link IE Field Network, CPU, and GbE-PHY.
This integrated LSI allows you to reduce CPU and GbE-PHY related development costs and manhours.
CP520-based development offers the following features:

(1) CP520-based development allows you to develop an intelligent device station or remote device station for CC-Link IE Field Network without awareness of protocol.

(2) GbE-PHY in CP520 facilitates the designing of communication circuit patterns. In addition, only a small number of peripheral components and circuits are required for CPU and GbE-PHY, allowing the development of more compact circuit boards.

(3) A sample code is provided that can be easily customized in accordance with user hardware specifications and applications.

(4) CP520 includes HW-RTOS, reducing the CPU load and achieving low power consumption in the developed device.

1.2 Specifications of CP520 Hardware

The following table lists the specifications of CP520 hardware.

Table 1.2-1 Hardware Specifications

Item		Description
Outer appearance	Number of pins	BGA 484 pins
	Size	23mm × 23mm
Power supply voltage		3.3V±5%, 2.5V±5%, 1.0V±5%
Operating ambient temperature		-40 to 85ºC
CPU		Integrated Arm® Cortex®-M4F processor with FPU (100 MHz)
Instruction RAM		768 Kbytes, built in (ECC compatible)
Data RAM		512 Kbytes (ECC compatible)
Buffer RAM		64 Kbytes (ECC compatible)
I/O ports		CMOS I/Os: 106 maximum
Ethernet PHY		1000BASE-T GbE-PHY (built-in) × 2 ports

1.3 Communication Specifications of CP520 Application Products

The following table lists the CP520 communication specifications related to CC-Link IE Field Network.

Table 1.3-1 Communication Specifications of CC-Link IE Field Network

Item			Description	
Station type			Intelligent device station or remote device station	
Station number			1 to 120	
Network number			1 to 239	
Communication speed			1Gbps	
Network topology			Line, star, and ring (Coexistence of line topology and star topology is possible.)	
Connection cable			Ethernet cable that satisfies 1000BASE-T standards (Category 5e or higher, double shielded, STP, straight cable)	
Maximum station-to-station distance			100m	
Overall cable distance			Line topology: 12000m (when cables are connected to 1 master station and 120 slave stations) Star topology: Depends on the system configuration. Ring topology: 12100m (when cables are connected to 1 master station and 120 slave stations)	
Number of cascade connections			Up to 20	
Cyclic transmission			Intelligent device station	Remote device station
	Maximum number of link points per station	RX	2048 points (2048 bits), 256 bytes	128 points (128 bits), 16 bytes
		RY	2048 points (2048 bits), 256 bytes	128 points (128 bits), 16 bytes
		RWr	1024 points (1024 words), 2048 bytes	64 points (64 words), 128 bytes
		RWw	1024 points (1024 words), 2048 bytes	64 points (64 words), 128 bytes
Transient transmission			Intelligent device station	Remote device station
	Client function		Supported	Not supported
	Server function		Supported	Supported
	Data size[*1]		2048 bytes	1024 bytes
	Dedicated instruction		RIRD/RIWT can be received by customizing the sample code.	
Other functions			-	
	Diagnostic function		CC-Link IE Field Network diagnostic function	
	Temporary error invalid station		Supported	
	Fast linkup		Supported	

*1: When the transient frame to be sent or received exceeds 1518 bytes, the transient frame is divided and sent or received in blocks.

1.4 Enclosed CD-ROM

The following describes the folder configuration and files included in the CD-ROM provided with this manual.
The folder configuration and files of data downloaded from the Mitsubishi Electric FA site are the same as those of the CD-ROM.

(1) Folder configuration of CD-ROM
The following shows the CD-ROM folder configuration.

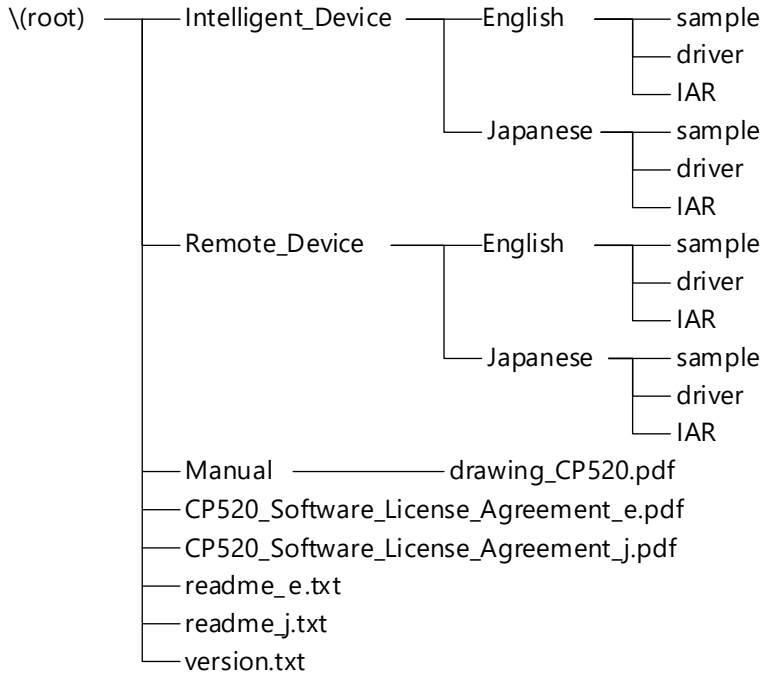


Figure 1.4-1 CD-ROM Folder Configuration Diagram

(2) CD-ROM file overview

The following provides an overview of the files included in the CD-ROM.

Table 1.4-1 File Overview

Folder Name			File Name	Description
Intelligent_ Device	English	sample, driver	*1	Intelligent device station sample code The sample code consists of the following program: • User program (English comment version) • CP520 driver main body • CP520 driver interface functions (English comment version) • CP520 driver callback functions (English comment version)
		IAR		IAR Embedded Workbench file (Compiler settings, link settings, build settings, etc.)
	Japanese	sample, driver, IAR	*1	Intelligent device station sample code, IAR Embedded Workbench files (Japanese comment versions of the above)
Remote_ Device	English	sample, driver, IAR	*1	Remote device station sample code, IAR Embedded Workbench files (Same as for intelligent device station)
	Japanese	sample, driver, IAR		
Manual			drawing_CP520.pdf	CP520 application circuit diagram examples (reference circuit diagrams of CP520, CP520 peripheral circuits, and CP520 power supply circuit)
-			readme_e.txt	Description of contents of enclosed CD-ROM (English)
-			CP520_Software_License_Agreement_e.pdf	END-USER SOFTWARE LICENSE AGREEMENT (English)*2
-			CP520_Software_License_Agreement_j.pdf	END-USER SOFTWARE LICENSE AGREEMENT (Japanese)*2
-			readme_j.txt	Description of contents of enclosed CD-ROM (Japanese)
-			version.txt	Version information of enclosed CD-ROM

*1: For file names, refer to readme_e.txt or readme_j.txt.

*2: Be sure to check the file.

1.5 Sample Code Overview

The sample code consists of the user program, CP520 driver interface functions, CP520 driver callback functions, and the CP520 driver main body.

*: The sample code describes only the information related to CC-Link IE Field Network (communication function information).

(1) The user program is an application program created by the user. The program in the sample code is provided for your reference for checking intelligent device station or remote device station logic. Customize the program in accordance with user requirement specifications.
(Refer to Chapter 10 "CREATING USER PROGRAMS".)

(2) CP520 driver interface functions are functions called when a CP520 driver function is used by the user program. Customization is not required. (Refer to Section 11.2 "CP520 Driver Interface Function List".)

(3) CP520 driver callback functions describe examples of processing on the user program side in response to events that occur on the CP520 driver side. Customize the functions in accordance with user requirement specifications. (Refer to Section 11.4 "CP520 Driver Callback Function List".)

(4) The CP520 driver main body is the main body of the driver area that is called by CP520 driver interface functions and controls CP520. Customization is not required.

1.6 System Configuration

(1) Software configuration

The following describes an example of the software configuration of a CP520 application product.
With usage of the OS driver library*1 and various functions provided by the CP520 driver, the user program can utilize various CP520 functions, such as cyclic transmission and transient transmission.
*1: For details, refer to Section 2.5 "Preparing for Software Development".

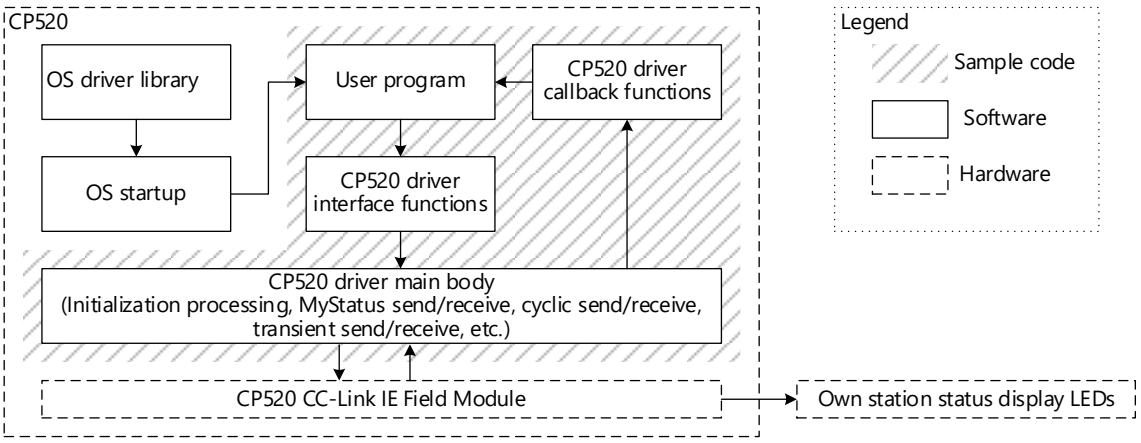


Figure 1.6-1 Software Configuration Overview

(2) Hardware configuration

The following describes an example of the hardware configuration of a CP520 application product. The hardware consists of CP520, peripheral components, and two Ethernet ports. Note that the term "CPU" used in the following chapters refers to the areas other than GbE-PHY areas in CP520.

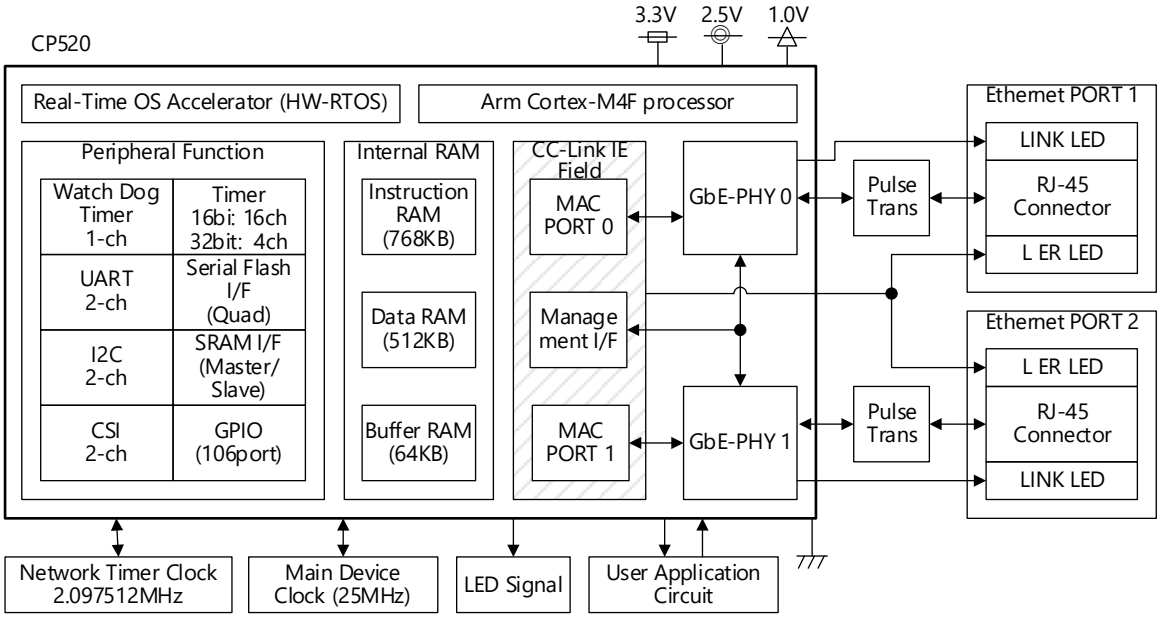


Figure 1.6-2 Hardware Configuration Overview

This manual identifies the GbE-PHY and LED signals connected to Ethernet Port 1 and Ethernet Port 2 using the numbering below.

Ethernet PORT	GbE-PHY	LINK LED	L ER LED
Ethernet PORT1	GbE-PHY0	PHY0_LED0	CCI_LERR0LEDZ
Ethernet PORT2	GbE-PHY1	PHY1_LED0	CCI_LERR1LEDZ

1.7 Relationship with R-IN32M4-CL2

CP520 shares the same LSI functions and specifications as those of R-IN32M4-CL2 manufactured by Renesas Electronics Corporation.

[Related documents]
The following documents may be used as reference for LSI functions and specifications.
Download the documents from the Renesas Electronics website (http://www.renesas.com/index.jsp).
Note: The asterisks ("****") at the end of each document number indicate the version.

Table 1.7-1 Renesas Electronics Related Documents

Title	Document No.
R-IN32M4-CL2 User's Manual	R18UZ0033EJ****
R-IN32M4-CL2 User's Manual: Peripheral Modules	R18UZ0035EJ****
R-IN32M4-CL2 User's Manual: Board Design	R18UZ0046EJ****
R-IN32M4-CL2 Programming Manual: Driver	R18UZ0038EJ****
R-IN32M4-CL2 Programming Manual: OS	R18UZ0040EJ****
R-IN32M4-CL2 User's Manual: Gigabit Ethernet PHY	R18UZ0043EJ****

[Driver library]
The sample code provided in this manual describes only the information related to CC-Link IE Field Network (communication function information).
For CPU and peripheral functions, the driver library below is required.
Download the files from the Renesas Electronics website (http://www.renesas.com/index.jsp).

Table 1.7-2 Renesas Electronics Driver Library

Downloaded Product Name	File Name
Driver/Middleware Set for IAR KickStart Kit	an-r18an0031jj0240-r-in32m4-iar-bsp.zip

[Arm Cortex-M4]
For the CPU functions and specifications, refer to the documents published by Arm Limited.
Download the documents from the Arm Limited website (http://www.arm.com/index.php).

2 STUDYING AND PREPARING SPECIFICATIONS PRIOR TO DEVELOPMENT

This chapter describes the specifications to be investigated and preparations to be made when developing a CP520 application product.

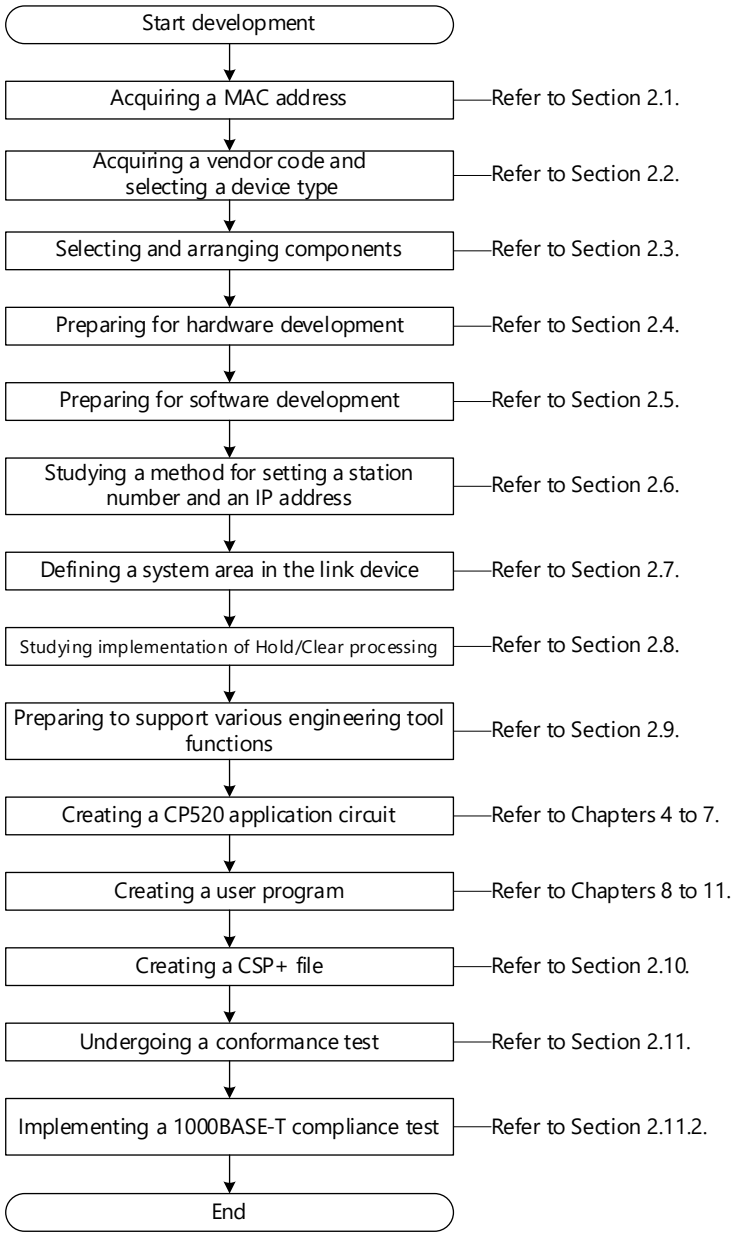


Figure 2-1 Development Process Example

2.1 Acquiring a MAC Address

CP520 application products are Ethernet (IEEE 802.3ab) compliant. Be sure to acquire a MAC address MA-L (MAC Address Block Large) unique to the device to be developed.
To acquire a MAC address, contact the following authority (department) in the USA.
The IEEE Registration Authority
Website: https://standards.ieee.org/products-services/regauth/oui/index.html (As of March 2021)

2.2 Acquiring a Vendor Code and Selecting a Device Type

CP520 application products require registration of a vendor code and device type. The vendor code and device type are assigned and managed by the CC-Link Partner Association. If you have any questions, contact the CC-Link Partner Association.

Table 2.2-1 Vendor Code and Device Type

Item	Description
Vendor code (vendorCode)	ID number (fifth to eighth digits) issued when the vendor joined the CC-Link Partner Association. For example, when the ID number is 123-456-7890, the vendor code will be 5678.
Device type (deviceType)	Select the applicable device type from the "CC-Link IE Field Network Specification (Device Profile)". If an applicable device type does not exist, consult with the CC-Link Partner Association.

2.3 Arranging Components

The components used in a CP520 application circuit are classified into CP520 and general components.

(1) CP520
CP520 can be ordered using the model names below. Purchase the product at a retail location that handles Mitsubishi Electric products.

Table 2.3-1 CP520 Model Names

Product Name	Model	Package Quantity	Manufacturer
CP520 (PC15001R-B)	NZ2GACP520-60	60 units	Mitsubishi Electric Corporation

(2) General components
General components are components selected according to the hardware specifications of the CP520 application product.
Select equivalent components with reference to Section 7.1 "CP520 Application Circuit Diagram Example" and Section 7.2 "Component List".

Remarks
Some components need to be selected carefully. Refer to Section 7.3.1 "Component selection precautions".

2.4 Preparing for Hardware Development

Precautions related to component selection, circuit design, and pattern design during hardware development for CP520 application products are described in check sheets. Prior to hardware development, refer to the following:

- Section 7.3.1 "Component selection precautions".
- Section 7.3.2 "Circuit design precautions".
- Section 7.3.3 "Pattern design precautions".

2.4.1 Pins connected to hardware switches

In the circuit diagram examples described in Chapter 7 "DEVELOPING A CP520 APPLICATION CIRCUIT", settings are switched using hardware switches listed in the table below.
The pins listed in the table can be changed by the user. Consider whether to connect the pins to hardware switches.
For details on each pin, refer to Chapter 5 "PIN FUNCTIONS".

Table 2.4.1-1 Pins Connected to Hardware Switches

Symbol	Switch	Pins	Reference
SW1	Station number setting switch (x1)	P70, P71, P72, P73	Section "2.6 Studying a Method for Setting a Station Number and Network Number"
SW2	Station number setting switch (x10)	P74, P75, P76, P77	
SW3	Network No. 1 (x1)	P60, P61, P62, P63	
SW4	Network No. 16 (x16)	P64, P65, P66, P67	
SW5	Fast linkup function enable/disable setting switch	P30, P31, P32, P33	Section "3.8.1 Fast linkup function enable/disable setting"

If you do not use hardware switches, add processing for writing the various settings from the engineering tool (peripheral device) of the CP520 application product.

2.5 Preparing for Software Development

CP520 shares the same LSI functions and specifications as those of R-IN32M4-CL2 manufactured by Renesas Electronics Corporation.

(1) Development environment
Use the following tools for developing the software of a CP520 application product.
- R-IN32M4-CL2 Programming Manual (Driver)
- R-IN32M4-CL2 Programming Manual (OS)

(2) Driver library
The sample code provided in this manual describes only the information related to CC-Link IE Field Network (communication function information).
For CPU and peripheral functions, the driver library below is required.
Download these files from the Renesas Electronics website (http://www.renesas.com/index.jsp).

Table 2.5-1 Renesas Electronics Driver Library

Downloaded Product Name	File Name
Driver/Middleware Set for IAR KickStart Kit	an-r18an0031jj0240-r-in32m4-iar-bsp.zip

Store the folders and files in the "\Intelligent_Device\English" or "\Remote_Device\English" folder on the CD-ROM in the directory under the downloaded file.
Note that the "cie_intelligent_device" and "cie_remote_device" folders in the folder below are not used.
"\an-r18an0031jj0240-r-in32m4-iar-bsp\r-in32m4_samplesoft\Device\Renesas\RIN32M4\Source\Project\IAR_StarterKit_CL2"

2.5.2 Software development procedure

This section describes the procedure for developing the software for a CP520 application product.
Step 1: Creating a user program
Create a user program while referring to Chapter 10 "CREATING USER PROGRAMS".

Step 2: Creating the CP520 driver library
Compile the files for the CP520 driver main body, execute the librarian, and create the CP520 driver library files.

Step 3: Compiling the user program and CP520 driver callback functions
Compile the customized user program and CP520 driver callback functions.

Step 4: Connecting the object module files and library files
Based on link information files, connect the compiled files (object module files), OS driver library files, and CP520 driver library files, and create the load module files.

Step 5: Writing the execution file
Using debugger, ICE, or other device, load the load module files into the CP520 application product (target).

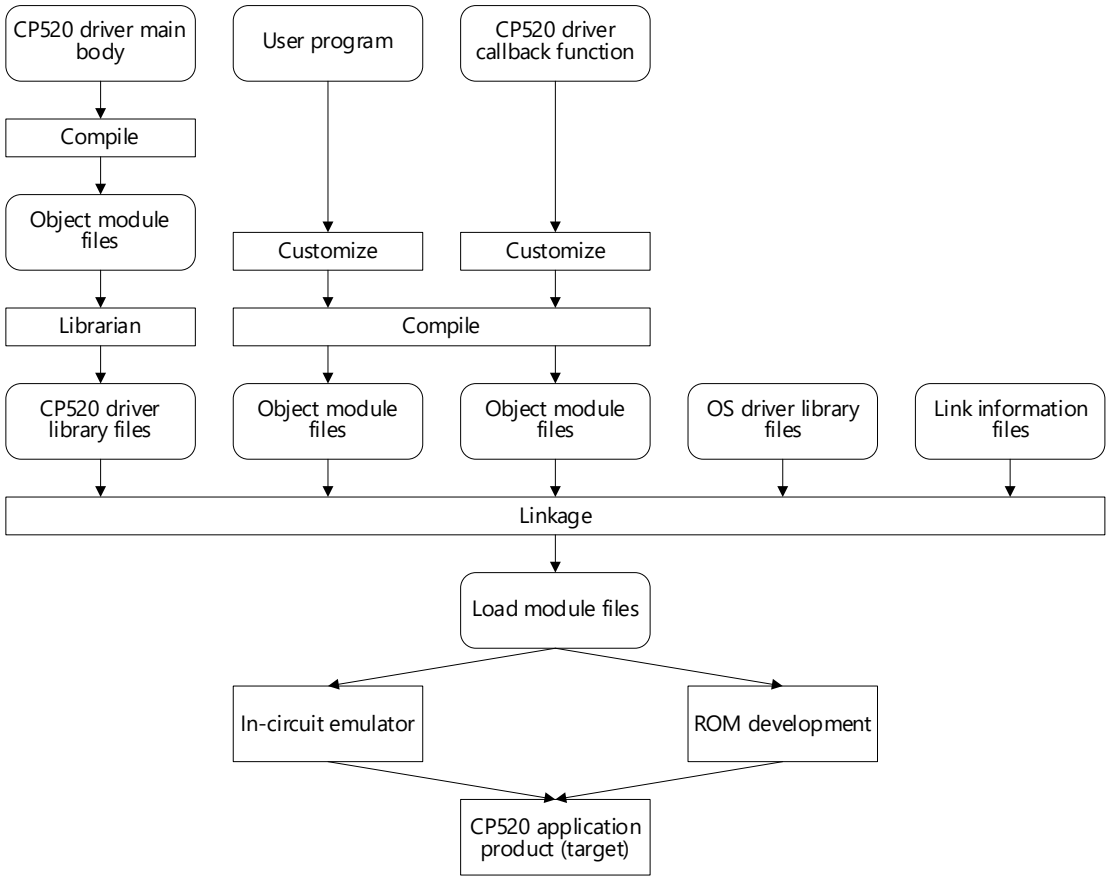


Figure 2.5.2-1 Software Development Procedure Example

2.6 Studying a Method for Setting a Station Number and Network Number

To create a data link to the own station, a station number and network number need to be set in CP520.
Consider a method for setting the station number and network number in accordance with the specifications of the CP520 application product in advance.

For reference, this section provides setting examples: one that uses a hardware switch and the other that uses the peripheral connected to the CP520 application product.
For either method, call "Station number and network number setting" (Section 11.3.1(3)gerCP52_SetNodeAndNetworkNumber) of the CP520 driver interface functions in the user program "iUserInitialization" (Section 10.2.2 "Initialization processing").

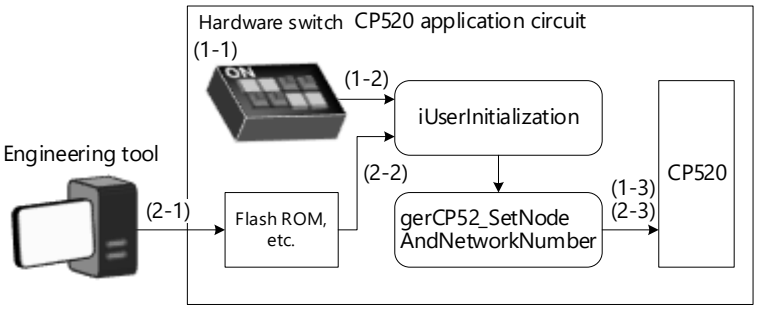


Figure 2.6-1 Image of Setting Station Number and Network Number

<Example 1: Using a hardware switch>

Step	Description
(1-1)	Set the station number and network number using a hardware switch.
(1-2)	The user-created processing in iUserInitialization acquires the current values of the hardware switch and sets the values in the argument of "gerCP52_SetNodeAndNetworkNumber".
(1-3)	"gerCP52_SetNodeAndNetworkNumber" sets the argument values in CP520.

Select a hardware switch that corresponds to the value range of the station number and network number.

Table 2.6-1 Hardware Switch Range

Item	Value Range
Station number	01H to 78H (1 to 120)
Network number	01H to EFH (1 to 239)

<Example 2: Using the peripheral connected>

Step	Description
(2-1)	Set the station number and network number data into the flash ROM using the peripheral.
(2-2)	The user-created processing in iUserInitialization acquires the data set in the flash ROM and sets the data in the argument of "gerCP52_SetNodeAndNetworkNumber".
(2-3)	"gerCP52_SetNodeAndNetworkNumber" sets the argument values in CP520.

2.7 Studying Assignment of Link Device Properties

Link devices are classified into three property groups. Consider the property groups to be assigned to the link devices of CP520 application product in advance.
(For details, refer to "CC-Link IE Field Network Specification (Device Profile)".)

(1) Direct input/output group
The direct input/output group uses link devices for general input/output and not for specific functions.
(For example, input/output of master/local modules, remote I/O modules, and others.)

(2) System input/output group
The system input/output group uses link devices for interlock between the master station and its own station, notification of own station status.
(For details, refer to Chapter 12 "LINK DEVICE SYSTEM AREA".)

Table 2.7-1 Example of Link Device Property Definitions (System Area)

Link Device	Name	Link Device	Name
RX07	Warning status flag	-	-
RX08	Initial data processing request flag	RY08	Initial data processing complete flag
RX09	Initial data setting complete flag	RY09	Initial data setting request flag
RX0A	Error status flag	RY0A	Error reset request flag
RX0B	Remote ready	-	-

(3) Vendor input/output group
The vendor input/output group uses arbitrarily defined link devices.

Table 2.7-2 Example of Link Device Property Definitions (Inverter)

Link Device	Name	Link Device	Name
RX10	Forward rotation status/stop status	RY10	Forward rotation command/stop command
RX11	Reverse rotation status/stop status	RY11	Reverse rotation command/stop command
RWr00	Output frequency status	RWw00	Output frequency setting

2.8 Studying Implementation of Hold/Clear Processing

This function determines the output status (Hold or Clear) when the master station application has stopped or entered in an error state, or when the own station disconnects from the data link, if the CP520 application product controls external output.

Consider whether to implement this function as a fail-safe measure when an error described above occurs or not.

For details on the Hold/Clear processing when the master station application has stopped or entered in an error state, refer to Section 10.2.7 "MyStatus from master station and cyclic receive processing".

For details on the Hold/Clear processing when the own station disconnects from the data link, refer to Section 10.2.10 "Communication status update processing".

Precautions
Cyclic data received in a slave station (own station) differs depending on the operation/error status or data link status of the master station application. For details on the acquired cyclic data, refer to Section 10.2.7 "MyStatus from master station and cyclic receive processing" and Section 10.2.10 "Communication status update processing".

2.9 Preparing to Support Various Engineering Tool Functions

The following functions can be executed by using the engineering tool connected to the programmable controller CPU of the master station. Consider whether the specifications of the CP520 application product (slave station) support the engineering tool functions or not in advance.

Table 2.9-1 Engineering Tool Functions

No.	Function		Items Required in CP520 Application Products
1	CC-Link IE Field Network diagnostics		・ SLMP frame request receive and response send processing
	a	Selected station communication status monitor	
	b	Communication test	
	c	Cable test	
2	Parameter processing/command execution of slave stations		・ Description of a CSP+ file up to scope [3] in Figure 2.10-1 ・ SLMP frame request receive and response send processing

[CC-Link IE Field Network diagnostics]
The engineering tool graphically displays the status of CC-Link IE Field Network.
For details, refer to Section 3.7 "CC-Link IE Field Network Diagnostics".

[Parameter processing/command execution of slave stations]
By using the engineering tool, parameter setup and command execution can be performed on the developed device without programming.
For details, refer to Section 2.10 "Preparing to Create CSP+ Files".

The above two functions are performed using transient transmission (SLMP frames).
The CP520 application product (slave station) needs to respond to SLMP request frames from the master station.
Consider whether to implement the SLMP frame send/receive processing or not in advance.

For SLMP frame send/receive processing, refer to Section 10.3 "User Program Details (Transient Transmission Related)", and subsequent sections.
(SLMP frame send/receive processing is described in the sample code. Use the processing described.)

2.10 Preparing to Create CSP+ Files

CSP+ is specifications for describing required information for starting, operating, and maintaining CC-Link Family compatible products.
Providing CSP+ files to the end users of CP520 application products allows them to manage all stations on CC-Link IE Field Network using one engineering tool.

For CSP+ details, refer to "Control & Communication System Protocol Specification".
To create CSP+ files, use "CSP+ profile creation support tool".

The following shows the scope in which CSP+ files are to be created for the intelligent device station or the remote device station.
The conformance test includes CSP+ check. Create a CSP+ file of scope [1].
Also, consider which functions (scopes [2] and [3]) are to be supported in advance.

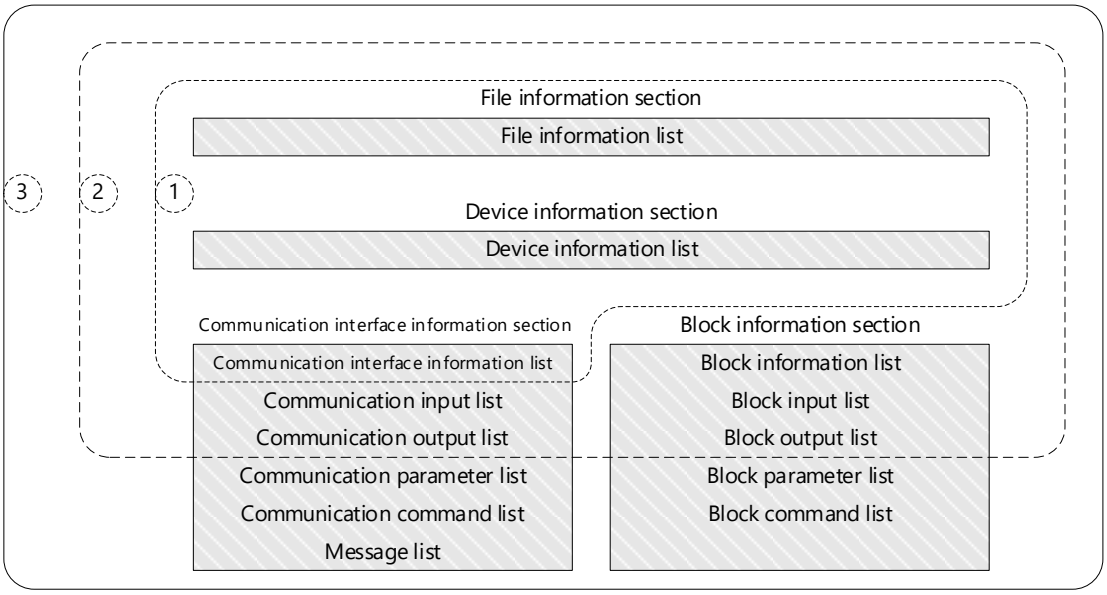


Figure 2.10-1 CSP+ File Section Configuration

Scope	Description	Necessity
[1]	Information required for verifying mandatory items in the CC-Link Partner Association conformance test [GX Works2, GX Works3] CP520 application products are displayed in the CC IE Field Configuration window and the network configuration can be easily created.	Required
[2]	Information required for displaying slave station link device and master station device assignments	Optional
[3]	Information required for executing parameter processing/command execution of slave stations [GX Works2, GX Works3] The parameters of CC-Link IE Field Network compatible products can be easily set from the CC IE Field Configuration window.	Optional

Supplementary explanation of parameter processing/command execution of slave stations

1) CP520 application products support parameter processing/command execution of slave stations. This function helps the end users of the products to reduce the programming required for setting parameters and executing commands.

2) Parameter processing/command execution of slave stations can be achieved by satisfying the following:
• Describing a CSP+ file up to scope [3] in Figure 2.10-1 CSP+ File Section Configuration.
• Implementing the SLMP frame send/receive processing described in the CSP+ file for CP520 application products.

2.11 Preparing for the Conformance Test

The conformance test is a test implemented for each device in order to ensure high reliability in the communication of CC-Link IE Field Network compatible products. The test verifies that the user product satisfies the CC-Link IE Field Network communication specifications and is connectable to the network.
Acquire the conformance test specifications when preparing for development, and design the CP520 application product so that it satisfies the test requirement specifications.

A CC-Link IE Field Network compatible product that passes the conformance test can be included as a qualified product in the "CC-Link Partner Product Catalog" and other media.

Point
Some functions may not be supported depending on the development timing. When implementing the conformance test, contact the CC-Link Partner Association.

2.11.1 Items required for the conformance test

The following functions and processing described in this manual are required for the conformance test.

[Cyclic transmission function]
The cyclic transmission function is required throughout the conformance test.
・ Implement the processing whose "Implementation Required" is "Required" in Table 10.1-1.

[Transient transmission function]
The response to Transient1 detailed node information acquisition is necessary.
・ Implement the processing whose "Implementation Required" is "Required" in Table 10.1-2.
・ Implement "gerCP52_ReceivedUnitInfoRequest" described in Section 11.3.11(3).

[1000BASE-T compliance test]
Transmission path waveforms must be verified based on IEEE 802.3 specifications.
・ Implement the processing whose "Implementation Required" is "Required" in Table 10.1-3.

[CSP+]
Create a CSP+ file up to scope [1] in Figure 2.10-1.

2.11.2 1000BASE-T compliance test

CC-Link IE Field Network is 1000BASE-T compliant. Therefore, the CP520 application product requires implementation of the 1000BASE-T compliance test based on IEEE 802.3ab specifications. Verify the results of the 1000BASE-T compliance test using the CC-Link Partner Association conformance test.

The 1000BASE-T compliance test measures four test waveforms from the Ethernet ports as verification of transmission path waveforms. Processing that outputs waveforms is described in the user program[*1] included in the sample code. Note, however, that four test waveforms cannot be switched at desired timings within the processing. Consider a waveform switching method, for example using the hardware switch.
*1: Refer to "UserIEEETest" (Section 10.4.1 "Hardware test (IEEE 802.3ab compliance test)").

3 FUNCTIONS OF THE CP520 APPLICATION PRODUCT

This chapter describes an overview of the communication functions of the CP520 application product.

Table 3-1 Communication Functions of CP520 Application Product

No.	Function	Processing Category	Reference
1	Cyclic transmission	User program*1	Section 3.1
2	Transient transmission	User program*1 or CP520 driver*2	Section 3.2
3	MyStatus send/receive	User program*1	Section 3.3
4	Status display	User program*1 or CP520 driver*2	Section 3.4
5	Bypass mode	CP520 driver*2	Section 3.5
6	CC-Link IE Field Network diagnostics	CP520 driver*2	Section 3.7
7	Fast linkup	CP520 driver*2	Section 3.8

*1: The processing described in Chapter 10 "CREATING USER PROGRAMS" needs to be implemented.

*2: These functions are implemented in the CP520 driver, so the user does not need to do anything.

The cyclic transmission function periodically exchanges data with the master station using link devices.

The status of each link device (RY and RWw) of the master station is stored in the link device (RY and RWw) of its own station by a link scan.
The status of each link device (RX and RWr) of its own station is stored in the link device (RX and RWr) of the master station by a link scan.

The following shows the flow of cyclic data.

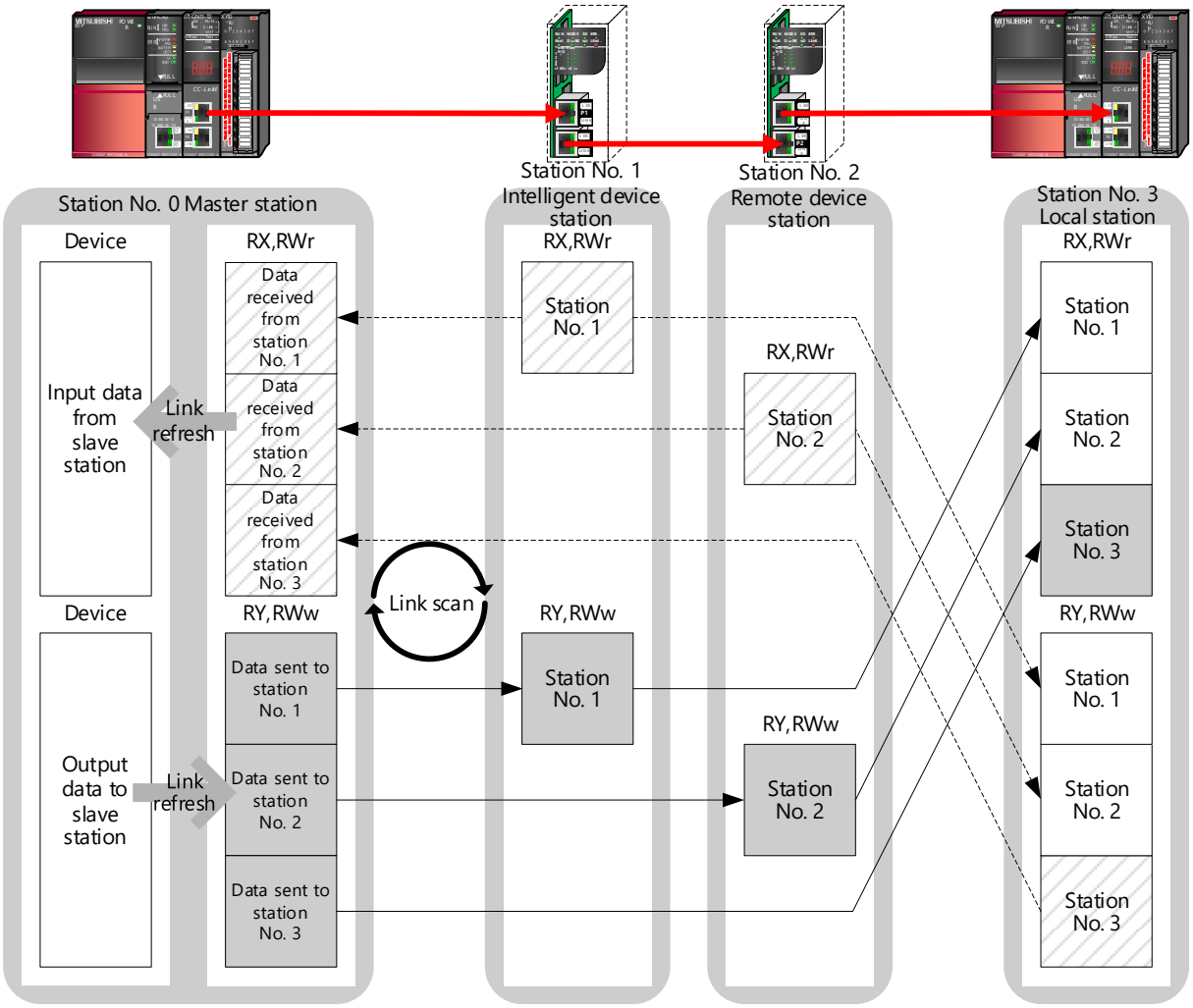


Figure 3.1-1 Flow of Cyclic Data

For cyclic transmission, refer to Section 10.2.7 "MyStatus from master station and cyclic receive processing" for reception and Section 10.2.9 "Cyclic send processing" for send.

3.2 Transient Transmission Function

Transient transmission communicates data when there is a communication request from another station or its own station. The function directly accesses the device/buffer memory of the other station and communicates the data.

Transient transmission achieves send/receive easier than cyclic transmission in the following cases:

- When reading and writing a large volume of data that exceeds the number of own/other station link device points
- When there is no send/receive area for general-purpose data (such as error history and parameter setting values) in the own/other station link device

The following shows the flow of transient data with a read instruction.

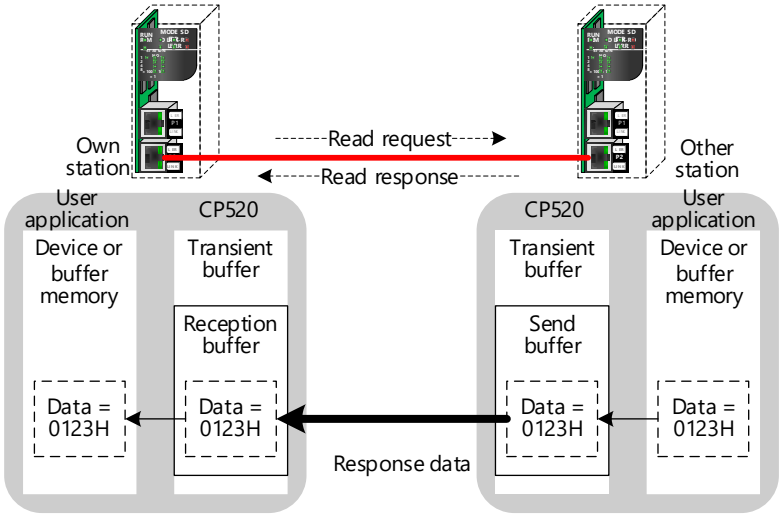


Figure 3.2-1 Flow of Transient Data

For transient transmission processing details, refer to Section 10.3 "User Program Details (Transient Transmission Related)" and subsequent sections.

Remarks
To use the transient transmission function, set "blTransientReceiveEnable" (transient reception function) to "CP52_TRUE" in initial settings. (Refer to No. 6 in "Table 11.3.1-2 CP52_UNITINIT_T List" in Section 11.3.1(2)gerCP52_Initialize.)

3.2.1 Transient transmission client and server functions

Transient transmission includes a client function and server function.
The client function sends transient requests to stations with a server function.
The server function sends transient responses to transient requests from stations with a client function.

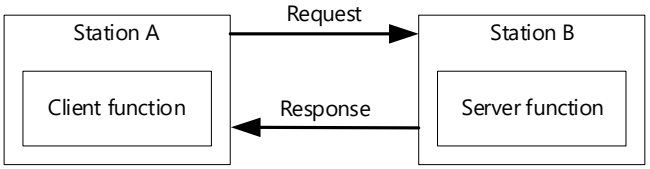


Figure3.2.1-1 Transient Client/Server Function

The intelligent device station can implement a client function and a server function.
The remote device station can implement a server function only.
For a processing overview of client and server functions, refer to Section 10.3(1) "Transient transmission processing overview".

3.2.2 Transient transmission frames

The following table lists the frames of transient transmission supported by CP520 application products, and indicates whether the send/receive processing for each frame needs to be implemented.

Table 3.2.2-1 Transient Transmission Frame List and Need for Implementation

No.	Frame Name[*1]	Frame Type (FType)		Data Type (DataType)		Data Sub-Type (DataSubType)		Implementation
1	CC-Link IE Field specific transient[*2]	22H	Transient1	07H	CC-Link IE Field specific	0002H	System specific	Required
2	SLMP[*3]	22H	Transient1	05H	Network common	0002H	SLMP	Optional
3	CC-Link compatible transient[*4]	25H	Transient2	04H	CC-Link compatible	-	-	Optional
4	TransientAck[*5]	23H	TransientAck	*6	*6	*6	*6	Required

*1: In this manual, each frame is described using the above names.
*2: The CC-Link IE Field specific transient frame is used by the master station to collect slave station information and manage the network.
*3: The SLMP frame is used by extension functions (CC-Link IE Field Network diagnostics, parameter processing/command execution of slave stations, etc.) that use the engineering tool.
*4: The CC-Link compatible transient frame is mainly used in communication between CP520 application products. The frames are compatible with CC-Link transient frames.
*5: TransientAck is used to issue verification responses to the send source when Transient1 and Transient2 frames are received.
*6: Extracted from the received frame.

3.2.3 Transient transmission commands

The following table lists the transient transmission commands described in this manual, and indicates whether or not implementation by the client or server function is required for each command. The remote device station does not require the client function of the commands in the table below.

Table 3.2.3-1 List of Transient Transmission Commands and Implementation Necessity

◎: Required △: Optional ×: Not required

Frame Name	Command Type	Intelligent Device Station		Remote Device Station	Processing Category	Remarks
		Client Function (Request)	Server Function (Response)	Server Function (Response)		
CC-Link IE Field specific transient	Node information distribution	×	△	△	CP520 driver	*1
	Statistical information acquisition	×	△	△	CP520 driver	*2
	Detailed node information acquisition	×	◎	◎	CP520 driver	*3
	Option information acquisition	×	△	△	CP520 driver	*4
SLMP	Selected station information acquisition	×	△	△	CP520 driver	*5
	Communication test	×	△	△	CP520 driver	
	Cable test	×	△	△	CP520 driver	
	Remote reset	×	△	△	CP520 driver	*6
	Memory read	△	△	△	User program	*7
	Memory write	△	△	△	User program	*7
CC-Link compatible transient	Memory read	△	△	△	User program	*8
	Memory write	△	△	△	User program	*9

*1: A command for the master station to distribute information that indicates the correspondence between the station numbers and MAC addresses by multicast.
Node information is used when an intelligent device station sends a transient request to another station.
Note that TransientAck and response are not required for this command. Only processing that receives the distributed node information is required.

*2: A command for the master station to collect error information related to Ethernet PORT1 and PORT2 of the slave station

*3: A command for the master station to collect information specific to the slave station.
For details on node information, refer to "Table 11.3.1-1 CP52_UNITINFO_T List".

*4: A command for the master station to confirm the option status of the slave station.
Option information is information indicating whether the slave station supports extension functions of CC-Link IE Field Network, such as SLMP frame send/receive and CC-Link IE Field Network diagnostics.

*5: Commands required for the CC-Link IE Field Network diagnostics. Refer to Section 3.7 "CC-Link IE Field Network Diagnostics".

*6: A command that resets the target station over a network

*7: Commands that read/write the general-purpose data from/to the memory of the target station (such buffer memory)

*8: A command which is equivalent to the master/local module dedicated instruction RIRD

*9: A command which is equivalent to the master/local module dedicated instruction RIWT

3.3 MyStatus Send/Receive Function

The MyStatus send/receive function is used by CP520 to periodically send and receive MyStatus frames.
MyStatus is used to report the status of stations connected to the network. Sending and receiving MyStatus makes it possible to report the status of the own station to the master station and monitor the status of the master station.

3.3.1 Sending MyStatus

Setting the information (own station status) outlined in the table below in the arguments of the CP520 driver interface function "Own station status setting" (Section 11.3.5(1)gerCP52_SetNodeStatus) in the user program "UserSendMyStatus" (Section 10.2.8 "MyStatus send processing") makes it possible to report the status of the own station to the master station.

Table 3.3.1-1 Information Related to Sending MyStatus

No.	Item	Description
1	Detailed application operation status	Stores the operation status of the user application. 0000H: Detailed application operation status notification not supported 0001H: Application stopped 0002H: Application running 0003H: Application does not exist Other than the above: Not used
2	Detailed application error status*1	Stores the error status when a user application error occurs. 0000H: No error 0001H: Minor error 0002H: Moderate error 0003H: Major error Other than the above: Not used

*1: When a Mitsubishi Electric programmable controller CPU is used, the following error status is defined.
Minor error: An error in which the CPU module continues operation such as a battery error
Moderate error: An error which the CPU module stops operation such as a WDT error
Major error: An error which the CPU module stops operation such as a RAM error
(A major error is more severe than a moderate error such as a hardware failure.)

3.3.2 Receiving MyStatus

The status of the master station can be monitored by acquiring the information (master station status) in the table below from the address specified in the CP520 driver interface function "Master station status acquisition" (Section 11.3.4(4)gerCP52_GetMasterNodeStatus) in the user program "UserReceiveCyclic" (Section 10.2.7 "MyStatus from master station and cyclic receive processing").

Table 3.3.2-1 Information Related to Receiving MyStatus

No.	Item	Description
1	Master station application operation status	Stores the operation status of the master station application.*1 0b: Application stopped 1b: Application running
2	Master station application error status	Stores the error status of the master station application.*2 0b: No error 1b: Error

*1: When a Mitsubishi Electric master station is used, the following status of the programmable controller CPU module will be stored.
[Application stopped]
Operation stop of a sequence program (when the RUN/STOP switch is set to "STOP" or a moderate/major error occurs).
[Application running]
Operation execution of a sequence program (when the RUN/STOP switch is set to "RUN").

*2: When a Mitsubishi Electric master station is used, the following status of the programmable controller CPU module will be stored.
[No error]
No error, or an error in which the CPU module continues operation such as a battery error (minor error).
[Error]
An error in which the CPU module stops operation such as a WDT error (moderate error), and an error in which the CPU module stops operation such as a hardware failure (major error).

3.4 Status Display Function

3.4.1 Status display by LEDs

CP520 can display the status of its own station and the status of the Ethernet PORT using LEDs.
From the viewpoint of ease of use by the end user, mounting all LEDs other than the USER LEDs in the table below is recommended.

Mount the LEDs so that the LED lights are visible from the housing of the CP520 application product. The LED colors and shapes are not specified. Select the LEDs in accordance with user specifications.

Table 3.4.1-1 LED Status Display List

Type	LED Name		Description
Own station status display	RUN		Indicates the operating status.
		On	Operating normally
		Off	A hardware failure or a watchdog timer error has occurred.
	RD		Indicates the reception status of data.
		On	Receiving data
		Off	Data not received
	SD		Indicates the sending status of data.
		On	Sending data
		Off	Data not sent
	D LINK		Indicates the status of the data link.
		On	Data link in operation (cyclic transmission in progress)
		Off	Data link not performed (disconnected)
		Blinking	Data link in operation (cyclic transmission stopped)
	ERR.		Indicates the CP520 error status.
		On	Error in own station
		Off	Normal operation
	L ERR.		Indicates the error status of the received data and the line, and loopback status. When this LED is on, you can check the port that detected the error using the L ER LED.
		On	Abnormal data received or loopback in progress
		Off	Normal data received or loopback not performed
	User LED1, 2		Indicates a user-defined status.
Ethernet PORT1 status display	LINK	On	Link up
		Off	Link down
	L ER	On	Abnormal data received or loopback in progress
		Off	Normal data received or loopback not performed
Ethernet PORT2 status display	LINK	On	Link up
		Off	Link down
	L ER	On	Abnormal data received or loopback in progress
		Off	Normal data received or loopback not performed

3.4.2 Controlling the LEDs

Some LEDs are controlled by hardware and some LEDs are controlled by software.

The LEDs controlled by hardware are turned on/off by CP520, in accordance with the status of the own station. These LEDs do not need to be controlled by software.

The LEDs controlled by software are turned on/off by the CP520 driver interface functions in accordance with the status of the own station. (For CP520 driver interface functions, refer to Section 11.3.7 "LED control".)

The following table lists the LED control at reset/error.

Table 3.4.2-1 LED Control List

LED Type	LED Name	CP520 Output Signal Name	Control Classification	Power-on Reset*1	System Reset*1	Internal WDT Error, External WDT Error, Own Station Error*2
Own station status display	RUN	CCI_RUNLEDZ	Hardware or software	Off	Off	Off
	RD	CCI_RDLEDZ	Hardware	Off	-	-
	SD	CCI_SDLEDZ	Hardware	Off	-	-
	D LINK	CCI_DLINKLEDZ	Hardware or software	Off	Off	Off
	ERR.	CCI_ERRLEDZ	Hardware or software	Off	Off	On
	L ERR.	-	Hardware or software	-	-	-
	USER LED1	CCI_USER1LEDZ	Software	Off	Off	Off
	USER LED2	CCI_USER2LEDZ	Software	Off	Off	Off
Ethernet PORT1 status display	LINK	PHY0_LED0	Hardware	Off	Off	-*3
	L ER	CCI_LERR0LEDZ	Hardware or software	Off	Off	Off
Ethernet PORT2 status display	LINK	PHY1_LED0	Hardware	Off	Off	-*3
	L ER	CCI_LERR1LEDZ	Hardware or software	Off	Off	Off

*1: For reset details, refer to Chapter 8 "RESET".
*2: This is an error that occurs for user application reasons. For details, refer to Section 10.2.4 "Own station error processing".
*3: These LEDs turn on if the mode is bypass mode.

3.4.3 Controlling USER LEDs

USER LEDs can be freely defined in accordance with the specifications of the CP520 application product.
For example, the on/off/blinking status of a USER LED can be controlled to indicate the following:

- Status of online/offline mode (hardware test mode) of own station
- Normal/Error status of various tests such as the hardware test

Control the USER LEDs using the CP520 driver interface functions "gerCP52_SetUSER1LED" and "gerCP52_Set USER2LED". For details of the CP520 driver interface functions, refer to Section 11.3.7 "LED control".

3.4.4 Controlling the L ERR. LED

The L ERR. LED turns on and off according to the logical sum of CCI_LERR0LEDZ and CCI_LERR1LEDZ.
In addition, the LED can be controlled from the user program using the signals from the CP520 port pins and the logical sum.
Mount the OR circuit in the CP520 application circuit and connect the signals.
Note that this manual illustrates a case where port pin P57 is used. Change the port pin as necessary.

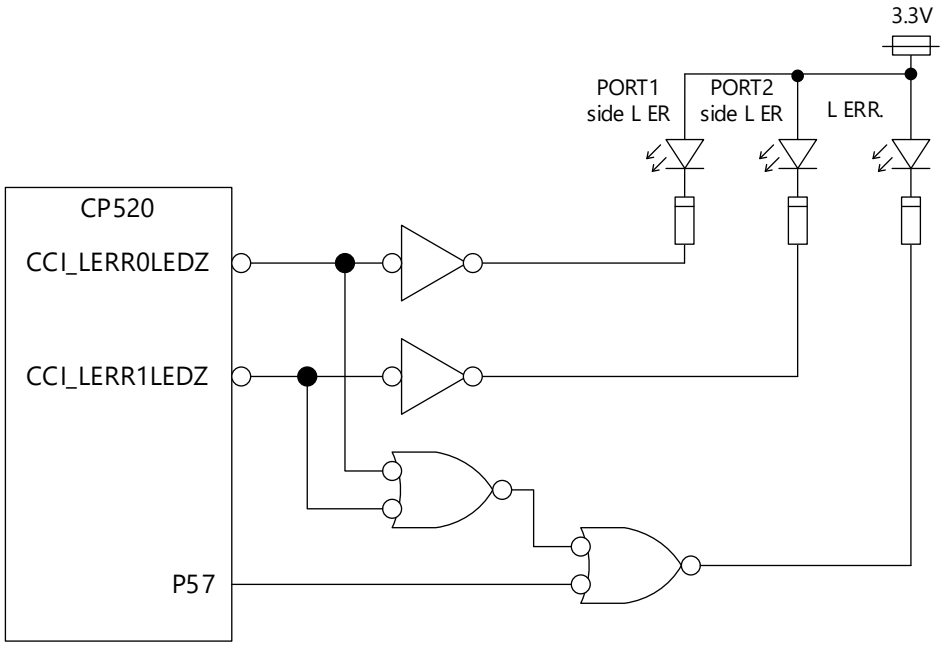


Figure 3.4.4-1 L ERR. On Circuit (P57 Usage Example)

[P57 pin]
The P57 pin output and L ERR. LED status have the relationship indicated in the table below.

Table 3.4.4-1 L ERR. LED On Conditions

X: High or Low

CCI_LERR0LEDZ	CCI_LERR1LEDZ	P57	L ERR. LED
X	X	Low	On (error)
Low (error)	X	High	On (error)
X	Low (error)	High	On (error)
High (normal)	High (normal)	High	Off (normal)

At startup, the P57 pin status is as follows:
・ During reset: Hi-Z (High)
・ During I/O standby: High

To use the P57 pin, the following register setting is required.

Table 3.4.4-2 Register Setting Required for Using P57 Pin as Output Pin

No.	Register Name	Function	Initial Value	Setting
1	PM5B	Input/output switch	FFH (input mode)	7FH (output port)

Table 3.4.4-3 (Reference) Registers Related to P57 Pin

No.	Register Name	Function	Initial Value	Setting
1	PMC5B	Port multiplexed function switch	00H (port mode)	Change not required
2	DRCTLP5H	Buffer function switch	0000 9000H (pull-up resistor)	Change not required

3.4.5 Enabling/Disabling the LED function

The function of the LEDs in the table below can be enabled and disabled.

Table 3.4.5-1 LEDs for which Function Can Be Enabled/Disabled

LED Name	Description
RUN	Operating status
ERR	Error status
D LINK	Data link status
USER LED 1, USER LED 2	User-defined status
L ER 1, L ER 2	Ethernet PORT 1, 2 reception data error status

Determine the LED function enable/disable specifications as necessary.
(Example)
Disable the L ER.LEDs of Ethernet PORT1 and PORT2 in a link down state since the LED sometimes stays ON when the link is down.

To disable the LED function, use the function "gerCP52_DisableLED".
To enable the LED function, use the function "gerCP52_EnableLED".
For details of the functions "gerCP52_DisableLED" and "gerCP52_EnableLED", refer to Section 11.3.7 "LED control".

3.5 Bypass Mode

Bypass mode maintains network connection (linkup), even when the system resets or an error that affects communication occurs in a line or ring topology, so that communication with downstream stations from the own station is not affected.
CP520 transitions its own station to bypass mode when the causes below occur.

[Causes for mode change to bypass mode]
- System reset (Refer to Chapter 8 "RESET".)
- WDT error (internal WDT error or CCI_WDTIZ input)
- Own station error (An error that occurs for user application reasons. For details, refer to Section 10.2.4 "Own station error processing".)

3.6 MIB Information

MIB information is information, such as the Ethernet PORT1 and PORT2 frame reception count and error frame reception count, collected by CP520 and used to manage the communication status.
The user program uses MIB information to identify the communication status of the Ethernet ports of its own station.
For MIB information details, refer to Section 10.2.13 "MIB information acquisition processing".

3.7 CC-Link IE Field Network Diagnostics

The CC-Link IE Field Network diagnostics graphically displays the status of CC-Link IE Field Network using the engineering tool. Error locations, error causes, corrective actions, and event history can be checked using the engineering tool. For function details, refer to the user's manual of the master/local module.

This function displays the CP520 application product on the CC-Link IE Field Network diagnostics window by responding to SLMP frame requests from the master station. The function also allows you to execute various tests and operations.

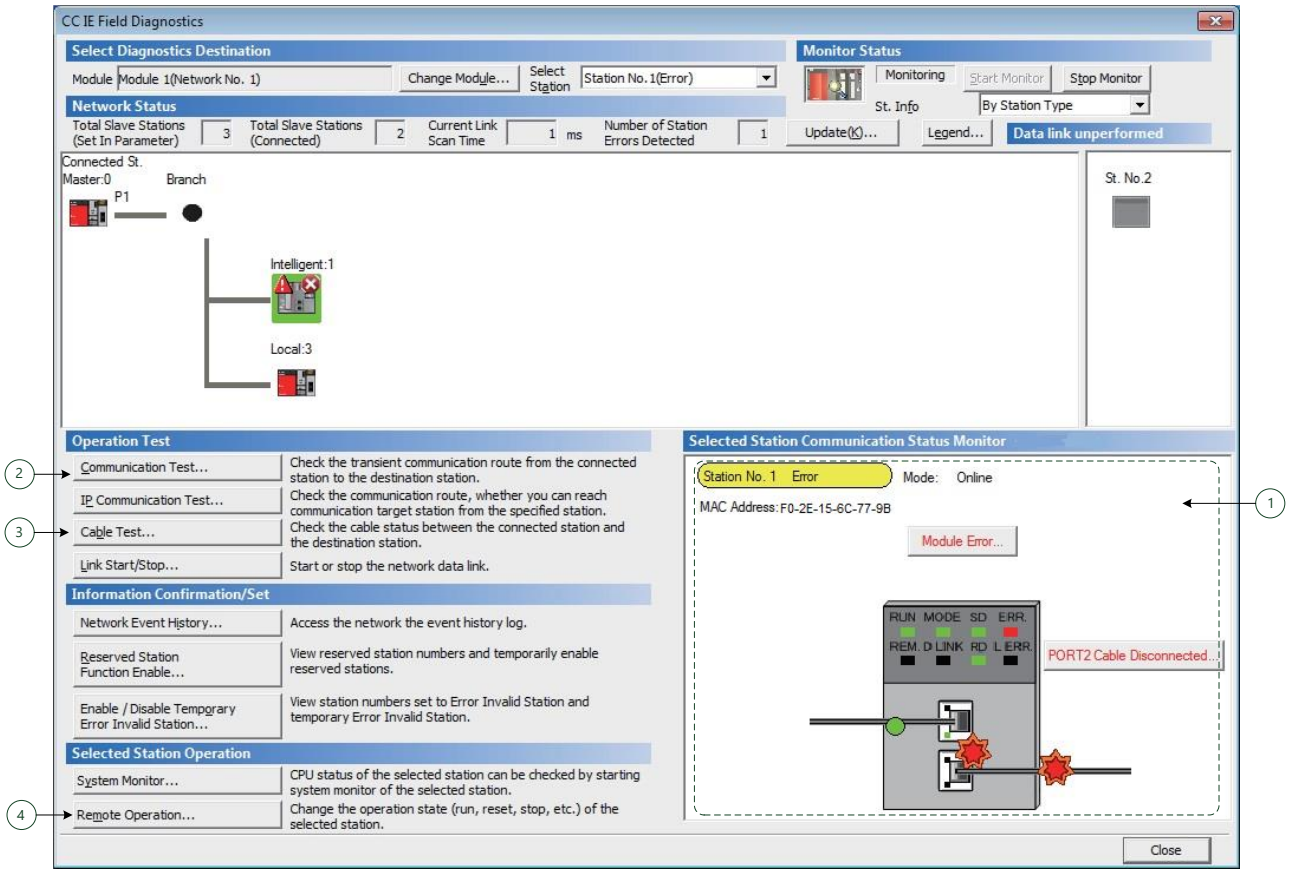


Figure 3.7-1 Diagnostic Window/Operation Locations (GX Works2)

Table 3.7-1 Diagnostic Window/Operation Locations and SLMP Requests

No.	Item	Description	SLMP Request Frame (Command)
1	Selected station communication status monitor	Displays the status of the selected station and error details.	Selected station communication status request (3119H)
2	Communication test	Tests the communication path of transient transmission from the own station to the communication destination.	Communication test request (3040H)
3	Cable test	Tests cable disconnection and no connection.	Cable test request (3050H)
4	Remote operation	Resets the status of the CP520 application product without hardware switch operation.	Remote reset request (1006H)

[SLMP request frame response]
In the user program "UserHandleReceivedTransient1" (Section 10.3.2 "Transient1 receive data processing"), the CP520 driver interface functions ((5) to (8) in the Section 11.3.11 "Transient request reception") performs the applicable SLMP frame response processing (request frame receive processing).
The processing of the above No.1 to 4 is described in the sample code. Use the processing described. (Implementation of the above No.1 to 3 is recommended.)

3.7.1 Selected station communication status monitor LEDs

The LED status of the own station can be displayed on the selected station communication status monitor by creating LED information in "UserHandleReceivedTransient1" (Section 10.3.2 "Transient1 receive data processing") and issuing a response to the selected station communication status request.

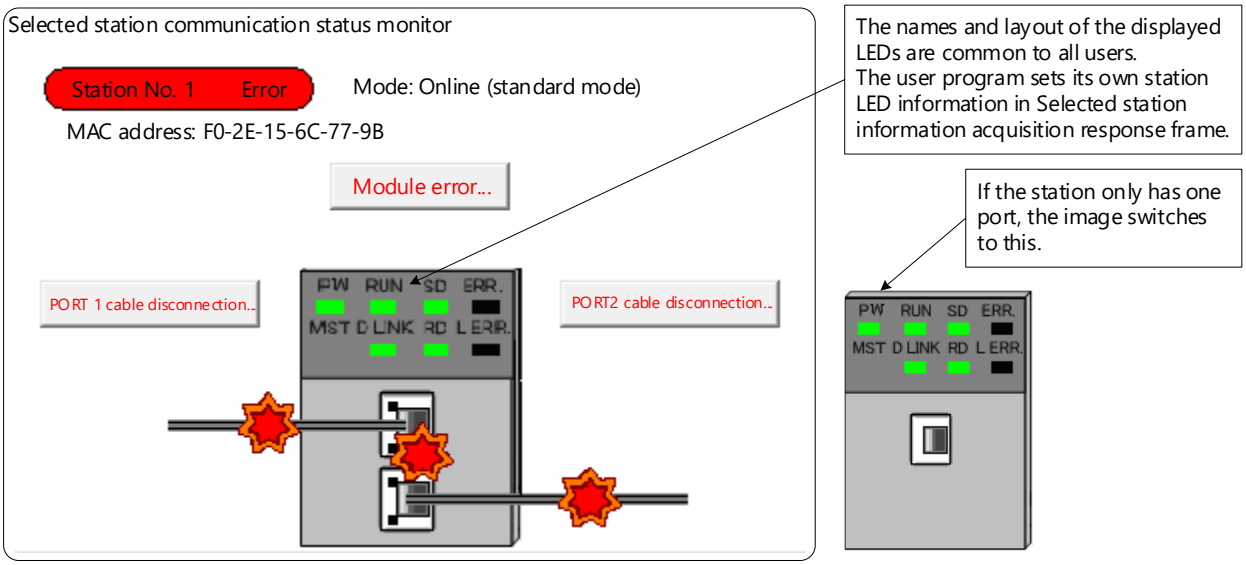


Figure 3.7.1-1 Display Example of Selected Station Communication Status Monitor

[Example of LED Use of Selected Station Communication Status Monitor]
When the LED status of the CP520 application product is not visible during end user troubleshooting, the LED status can be checked by using CC-Link IE Field Network diagnostics.

[Displayable LEDs]
The LED names[*1] and LED layout that can be displayed on the selected station communication status monitor are as shown in the figure above.
*1: PW, RUN, SD, ERR., MST (not used; grayed out), D LINK, RD, L ERR.

*1: For details on creating LED information, refer to Section 10.3.2 "Transient1 receive data processing" (3) Creating LED information.

3.8 Fast Linkup Function

The fast linkup function shortens the time period from CP520 application product power-on to linkup.
The linkup time can be shortened by disabling functions such as the GbE-PHY auto-negotiation function (a function that automatically selects the optimum communication speed and communication mode).
Examples of use include a system that uses a replacement mechanism (tool changer) for an arm end tool of an industrial robot.

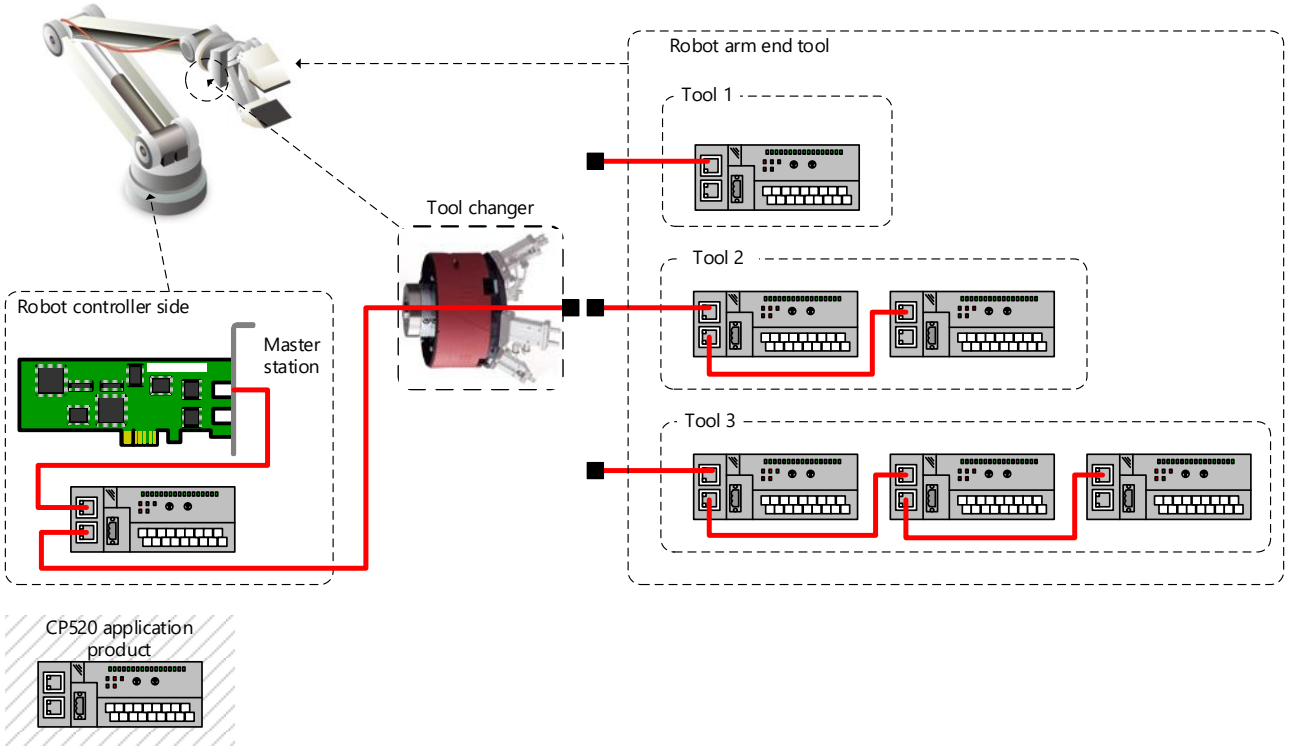


Figure 3.8-1 Example of Fast Linkup Function Use (Industrial Robot Arm)

To implement this function, the following is required.

[Hardware]
- A hardware switch for switching the enable/disable setting of the fast linkup function is required. For details, refer to Section 3.8.1 "Fast linkup function enable/disable setting".

[Software]
- Add processing for reading the value of the hardware switch described above and determining whether the function is enabled and disabled in the user program "iUserInitialization" (Section 10.2.2 "Initialization processing").
  (When the hardware switch is not to be used, add processing for writing fast linkup function enable/disable from the engineering tool (peripheral device) of the CP520 application product.)
- When the function is enabled, fast linkup setup (PHY setting initial value) needs to be performed during CP520 initialization.
  Refer to Section 11.3.1(2)gerCP52_Initialize and "Initial value of PHY setting" in "Table 11.3.1-2 CP52_UNITINIT_T List".

Note
Enabling this function on both of own station port and the adjacent port shortens the linkup time between the ports. The linkup time is not shortened when the port of a station with the function disabled or not supported is connected with a port with the function enabled.

3.8.1 Fast linkup function enable/disable setting

When the fast linkup function is implemented, the function will need to be enabled or disabled for each port.

When the fast linkup function of the adjacent stations are disabled or not supported, linkup is not possible. Taking into consideration cases where whether or not the function is supported or not supported in the adjacent stations is unclear, a method that allows the end user to easily switch the fast linkup function between enabled and disabled is required.

This manual describes a case where a fast linkup enable/disable setting switch (SW5 of the CP520 application circuit diagram example) is mounted on the CP520 application circuit.

Table 3.8.1-1 Fast Linkup Enable/Disable Setting Switch

Bit	Name	Description	Connected Pin
0	- (Reserved)	For future expansion	P30
1	F LINK P1	ON: Port 1 fast linkup function enabled, OFF: Port 1 fast linkup function disabled	P31
2	F LINK P2	ON: Port 2 fast linkup function enabled, OFF: Port 2 fast linkup function disabled	P32
3	- (Reserved)	For future expansion	P33

Note

The enabled/disabled state of this function is determined by the status of the above switch when the CP520 application product is started.
Changing the fast linkup enable/disable switch after CP520 application product startup does not change the enabled/disabled status of the function. To reflect a change after startup, turning the power supply off and on is required.

3.8.2 System configuration for fast linkup

The following illustrates the system configuration when the fast linkup function is used for an industrial robot arm.

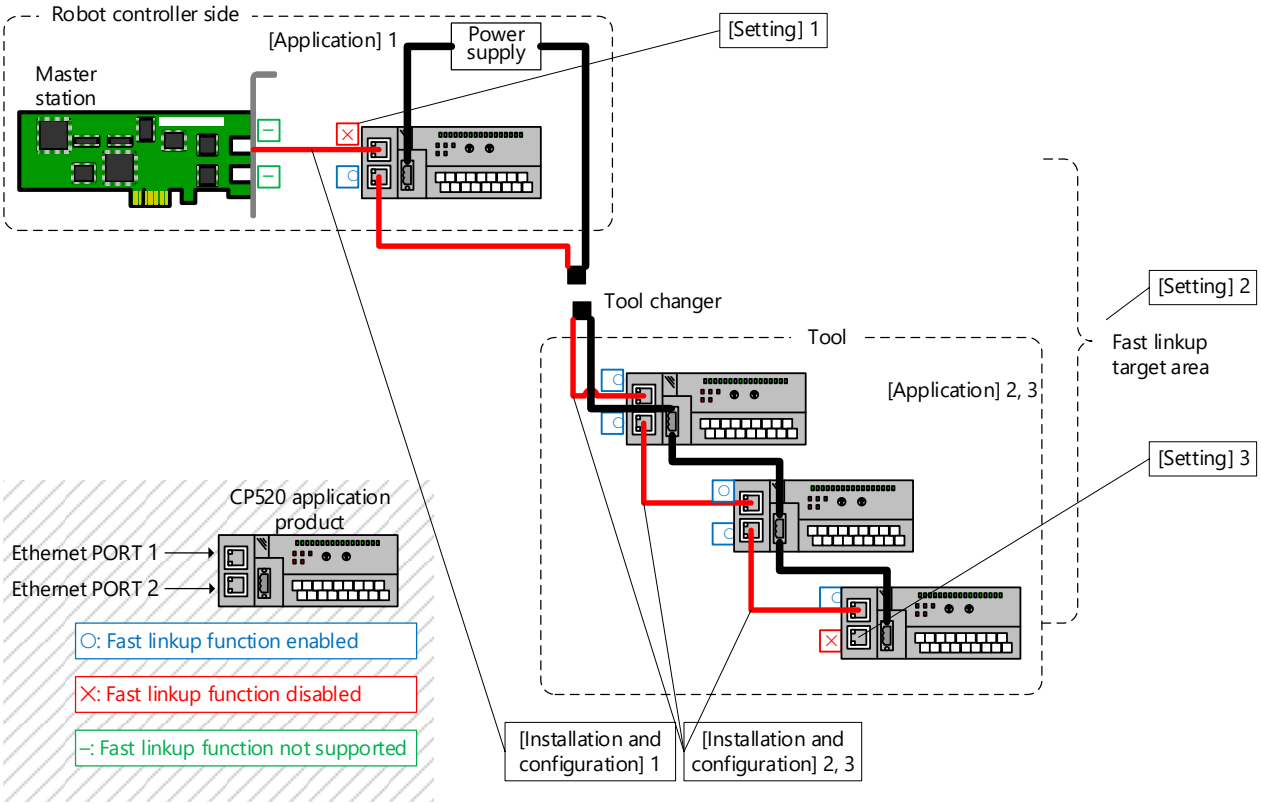


Figure 3.8.2-1 System Configuration for Fast Linkup (Industrial Robot Arm)

[Installation and configuration]

1	Connect PORT1 of the CP520 application product on the robot controller side to the master station, and PORT2 to the tool side. In the 1000-BASE-T clock settings of the CP520 application product, PORT1 is fixed to "Master" and PORT2 is fixed to "Slave". The clock settings are set by setting the "Slave" first and then the "Master". By starting the clock settings from PORT2 (slave), the linkup time with the tool is shortened.
2	When CP520 application products are to be connected together by fast linkup, connect PORT2 of the upstream station with PORT1 of the downstream station. As described above, in the CP520 application product, PORT1 is fixed to "Master" and PORT2 is fixed to "Slave". As a result, even if the fast linkup function is enabled, linkup does not occur if the PORT1 ports are connected to each other or if the PORT2 ports are connected to each other.
3	Connect the CP520 application products within the tool using a line topology. A network topology other than a line topology sometimes causes delays in the linkup time. The number of products connected also sometimes delays the linkup time.

[Setting]

1	For the PORT1 of the application product connected with a station (master station) that does not support the fast linkup function, set the fast linkup function to "Disabled". When a port with the fast linkup function enabled is connected to a port that does not support or has the fast linkup function disabled, linkup does not occur.
2	For the ports of all CP520 application products included in the fast linkup target area, set the fast linkup function to "Enabled".
3	When the CP520 application product is the tool end, set the fast linkup function of the non-connected port to "Disabled".

[Application]

1	Always keep the power of the master station and the CP520 application product on the robot controller side ON.
2	After switching the tool, simultaneously turn on the power of all CP520 application products within the tool.
3	Reconnection (cable connection and power-on) after tool switching must be performed after the master station has detected[*1] tool side disconnection (separation). When connection is performed before disconnection detection, linkup may be delayed. The CP520 internal GbE-PHY takes approximately 0.4 to 0.8 seconds from after the tool is switched to disconnection detection. When connection (power-on) is performed before disconnection detection, disconnection cannot be detected based on normal timing, causing a delay in linkup. *1: Disconnection can be detected by monitoring Data link status (each station) (SW00B0 to SW00B7) of the master station.

3.8.3 Precautions for fast linkup function

The extent to which the time period is shorted by use of the fast linkup function depends on the CP520 application circuit and user program.
Design the circuit and program so that the following time periods are shortened:

- Time period until reset cancellation
- Time period for loading F/W from boot memory
- Time period for setup of fast linkup related F/W

4 CP520 SPECIFICATIONS AND FUNCTION OVERVIEW

4.1 Function Overview

This section describes CP520 functions.

CP520 has the following functions:

- Integrated Arm Cortex-M4 core with FPU
- Integrated real-time OS accelerator with support for µITRON version 4.0
- On-chip physical layer for 1000 BASE-T
- Multiple timers, serial interfaces, general-purpose I/O ports (GPIO), external memory interfaces
- Communication functions of an intelligent device station and a remote device station for CC-Link IE Field Network

Table 4.1-1 CP520 Function Overview

Item		Description
CPU cores		Arm Cortex-M4F 32-bit RISC CPU Real-time OS accelerator (hardware real-time OS)
	Operating frequency	100MHz
	Instruction set	Thumb®-2 instruction ARMv7-ME architecture
	Floating point UNIT	ARMv7M FPv4-SP (32-bit single precision)
Instruction RAM		768 Kbytes (RAM with ECC)
Data RAM		512 Kbytes (RAM with ECC)
Buffer RAM		64 Kbytes (RAM with ECC)
Internal system bus		32-bit system bus at 100MHz 128-bit communication bus at 100MHz
DMA function (system bus side)		4 channels + 1 channel (for real-time port). Supports software and various interrupt-triggered DMA.
Boot options		Serial flash ROM boot, External memory boot, External MCU boot
Support for external memory access		・ Bus-size selection (16 or 32 bits) ・ Paged ROM/ROM/SRAM interface ・ Synchronous burst memory interface ・ Four chip select signals for static memory ・ External memory space: 256 Mbytes maximum ・ Programmable wait function
External MCU interface		・ Bus-size selection (16 or 32 bits) ・ General-purpose interface for static memory ・ Address space: 2 Mbytes (Instruction RAM, Data RAM, Register area)
Serial flash ROM memory controller		・ Supports serial interface compatible with SPI of companies. ・ Supports direct boot from serial memory device. ・ Supports fast reading, fast reading with dual output, fast reading with dual I/O, fast reading with quad output, and fast reading with quad I/O. ・ Direct layout in memory space
Interrupt		・ 29 external interrupt ports
I/O standby function		・ Supported[*1]
Ethernet PHY		• 2 ports IEEE 802.3 • 1000BASE-T
CC-Link IE Field		Intelligent device station or remote device station • Internal bus: Fixed to 32 bits • 1000BASE-T
On-chip debugging		• Selecting serial wire or JTAG • Full trace (built-in ETM)
Internal peripheral modules	I/O port	CMOS I/O: 106 maximum
	Timers (4 sub-systems)	• Internal timer of hardware RTOS • Internal timer of the CPU • 32-bit timer (4 channels) • 16-bit timer (16 channels)

Item		Description
	Watchdog timer	• 1 channel • Software-triggered start mode • Watchdog error response options: Generation of a non-maskable interrupt (NMI), Generation of a reset • Interrupt when the counter reaches 75% of its overflow value
	Asynchronous serial interface	• 2 channels • Full duplex transfer • FIFOs: 10 bits × 16 receive and 8 bits × 16 send • Support output of receive errors and status • Character length: 7 or 8 bits • Parity bit options: Odd, even, 0, none • Send stop bits: 1 bit or 2 bits
	I2C serial interface	• 2 channels • Operating modes: Normal or high-speed • Transfer modes: Single-transfer mode or continuous-transfer mode • Transfer data length: 8 bits
	Clocked serial interface	• 2 channels • Synchronized serial data transmission by three-wire system • Master mode or slave mode selectable • Built-in baud-rate generator • Transfer data length: 7 to 16 bits
Internal PLL		• Generates various clocks from 25 MHz input clock. The lock time of two PLLs is as follows: • System: 200 µs (MAX) • GbE-PHY: 110 µs (MAX)
Power supply voltage		VDD33 = 3.3±0.165V[*2] (CPU area, GbE-PHY area) VDD10 = 1.0±0.05V[*2] (CPU area, GbE-PHY area) VDD25 = 2.5±0.125V[*2] (GbE-PHY area)

*1: P53 to P56 are not supported.

*2: Ripple incorporated value. As a target value, set the DC component to within ±3% and the ripple component to within ±2%.

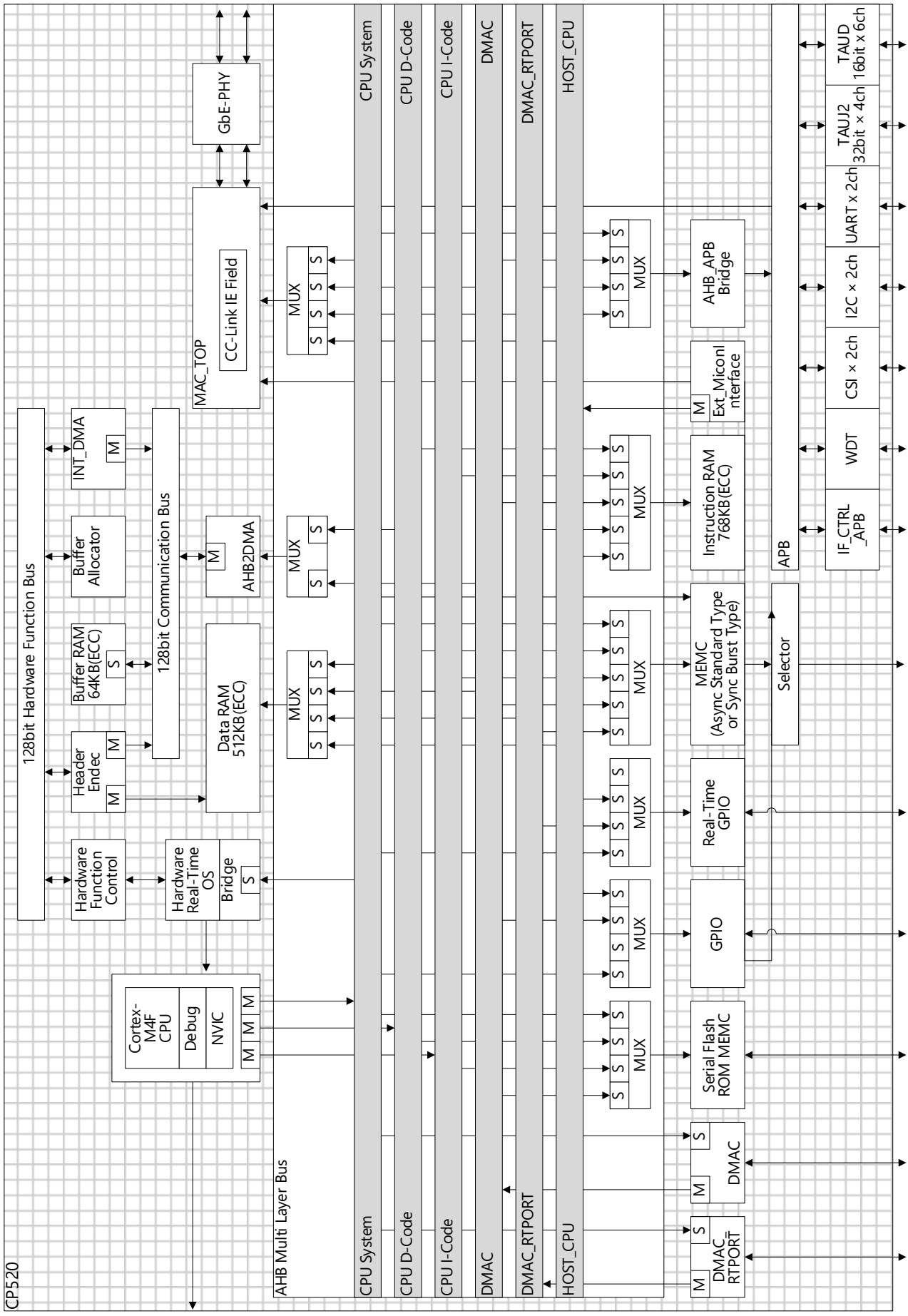
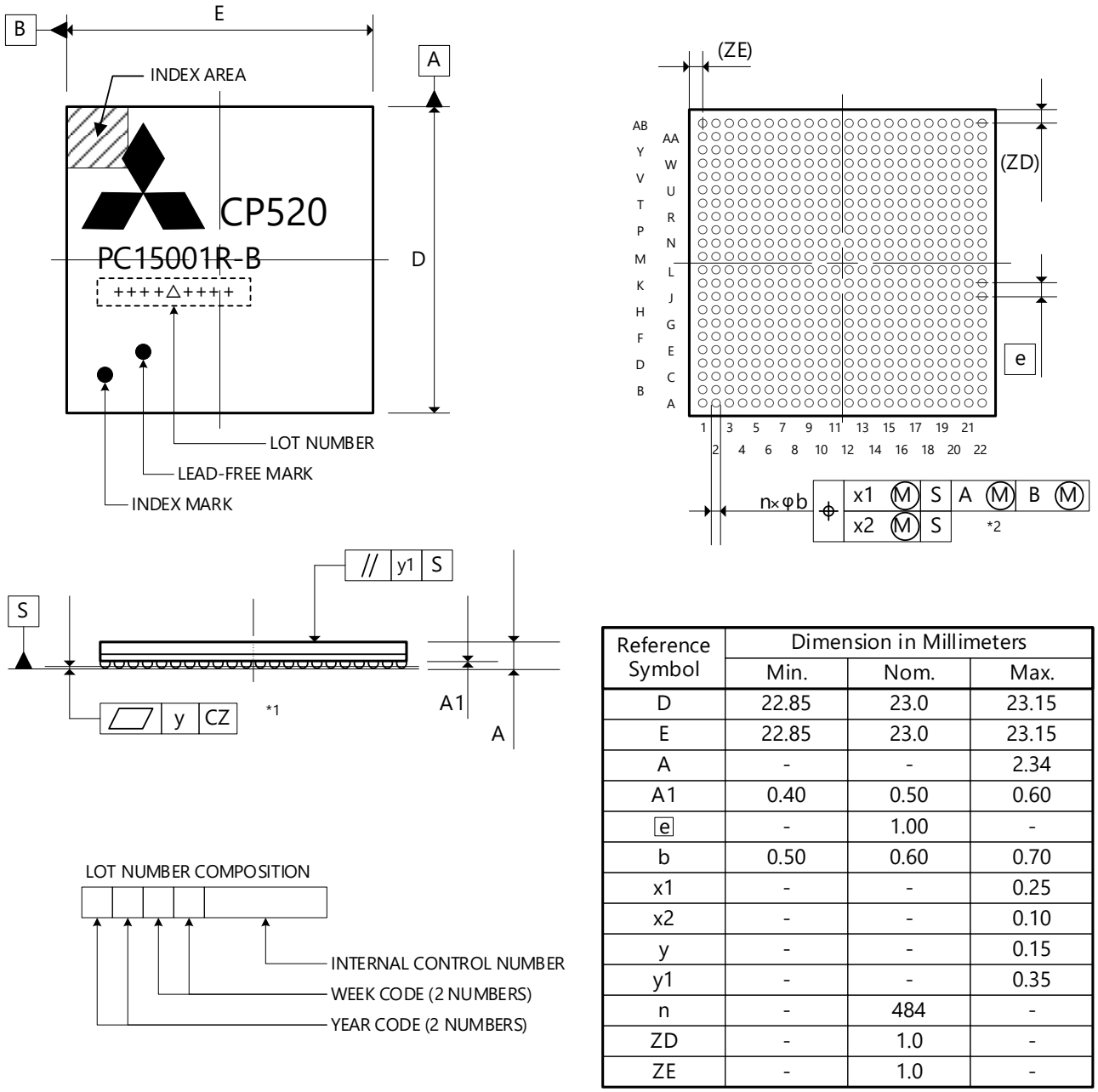


Figure 4.2-1 Function Block Configuration Diagram



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	22.85	23.0	23.15
E	22.85	23.0	23.15
A	-	-	2.34
A1	0.40	0.50	0.60
e	-	1.00	-
b	0.50	0.60	0.70
x1	-	-	0.25
x2	-	-	0.10
y	-	-	0.15
y1	-	-	0.35
n	-	484	-
ZD	-	1.0	-
ZE	-	1.0	-

Figure 4.3-1 External Appearance

*1: y CZ indicates the distance from the S plane to the common plane (Common Zone).
The S plane is the lowest plane of the solder ball taking into consideration solder ball size variance and warping.
The common plane is a virtual plane used to ground all solder balls with variance on the same surface and is drawn parallel from the S plane.

*2: x1 and x2 indicate the permissible values of the pin center position.
x1: Tolerance of the pin center position based on external appearance standards
x2: Tolerance of the relative pin center position. The value does not include external appearance standards.

4.4 Pin Assignments

The following are the pin assignments.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	
22	GND	GND	RP21	RP23	RP25	RP27	RP02	RP00	RESERVED	RESERVED	RESERVED	P20	P22	P25	RESERVED	P67	P65	P63	P60	P30	GND	GND	22
21	GND	RP20	RP22	RP24	RP26	RP04	RP03	RP01	RESERVED	RESERVED	RESERVED	P21	P23	P26	P27	P66	P64	P62	P61	P31	P32	GND	21
20	RP30	RP32	RP10	RP11	RP12	RP13	RP07	RP05	RESERVED	RESERVED	RESERVED	RESERVED	P24	EXTP0	EXTP1	EXTP2	EXTP3	HWRZSEL	HOTRESETZ	PONRZ	P33	RESETZ	20
19	RP31	RP33	RP37	RP14	RP15	RP16	RP17	RP06	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VDD33	MEMCSEL	ADMUXMODE	BUS32EN	RSTOUTZ	P35	P34	19
18	BUSCLK	RP34	RP36	D15	GND	VDD33	GND	VDD33	GND	VDD33	VDD33	GND	GND	PLL_VDD	PLL_GND	GND	VDD33	ETHTEST	MEMIFSEL	BOOT0	GND	CCI_CLK2_097M	18
17	D6	RP35	D13	D14	CTRSTBYB	VDD33	GND	VDD10	VDD10	VDD10	VDD10	VDD10	VDD10	VDD10	VDD10	GND	VDD33	PLL_VDD	HIFSYNC	BOOT1	P36	RESERVED	17
16	D4	D5	D11	D12	GND	VDD33	GND	VDD10	GND	GND	GND	GND	GND	GND	VDD10	GND	VDD33	PLL_GND	EXTP9	EXTP8	P37	GND	16
15	D2	D3	D9	D10	GND	GND	GND	VDD10	GND	GND	GND	GND	GND	GND	VDD10	GND	GND	GND	EXTP7	EXTP6	P70	XT2	15
14	D0	D1	D7	D8	GND	VDD33	GND	VDD10	GND	GND	GND	GND	GND	GND	VDD10	GND	GND	GND	EXTP5	EXTP4	P71	XT1	14
13	RDZ	WRSTBZ	CSZ0	A20	GND	GND	GND	VDD10	VDD10	VDD10	VDD10	VDD10	VDD10	VDD10	VDD10	GND	VDD33	GND	OSCTH	NMIZ	P73	P72	13
12	P10	P12	WRZ0	A19	GND	VDD33	VDD33	GND	VDD33	GND	VDD33	VDD33	GND	VDD33	GND	VDD33	VDD33	GND	GND	TRACECLK	P75	P74	12
11	P11	P13	WRZ1	A18	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	TRACEDATA1	TRACEDATA0	P77	P76	11
10	P14	P15	A17	GND	GND	GND	GND	GND	GND	GND	RESERVED	GND	GND	GND	GND	GND	GND	GND	GND	TRACEDATA2	P01	P00	10
9	P16	P17	A15	A16	GND	GND	GND	GND	VDD33_GPHY	VDD33_GPHY	VDD33_GPHY	VDD33_GPHY	VDD33_GPHY	VDD33_GPHY	GND	GND	GND	GND	TRSTZ	TRACEDATA3	P03	P02	9
8	P47	P44	A13	A14	GND	GND	GND	GND	VDD33_GPHY	GND	GND	GND	GND	VDD33_GPHY	GND	GND	GND	GND	TDO	JTAGSEL	P05	P04	8
7	P45	P46	A11	A12	GND	GND	GND	GND	VDD1	GND	GND	GND	GND	VDD1	GND	GND	GND	GND	TCK	RESERVED	P07	P06	7
6	P43	P41	A9	A10	GND	GND	GND	GND	VDD1	GND	GND	GND	GND	VDD1	GND	GND	RESERVED	GND	TDI	RESERVED	P51	P50	6
5	P42	A7	A8	PHYADD1	GND	RESERVED	RESERVED	RESERVED	RESERVED	GND	GND	GND	GND	RESERVED	RESERVED	RESERVED	RESERVED	GND	TMS	RESERVED	P53	P52	5
4	P40	A5	A6	PHYADD2	GND	RESERVED	RESERVED	RESERVED	GND	GND	GND	GND	GND	GND	RESERVED	RESERVED	RESERVED	GND	RESERVED	RESERVED	P55	P54	4
3	A2	A3	A4	PHYADD3	GND	GND	GND	GND	GND	VDD1A	VDD1A	GND	VDD25A	VDD25A	VDD25A	GND	GND	GND	GND	GND	P57	P56	3
2	GND	PHY0_LED0	PHYADD4	GND	GND	GND	P0_D3N	P0_D2N	P0_D1N	P0_D0N	GND	REF_FILT	GND	P1_D3N	P1_D2N	P1_D1N	P1_D0N	GND	GND	GND	PHY1_LED0	GND	2
1	GND	GND	GND	GND	GND	GND	P0_D3P	P0_D2P	P0_D1P	P0_D0P	GND	REF_REXT	GND	P1_D3P	P1_D2P	P1_D1P	P1_D0P	GND	GND	GND	GND	GND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	

Legend : GND pin : VDD*** pin

Figure 4.4-1 Pin Assignments

4.5 Base Addresses

The stated address of each register in the following is the relative address from the base address.

- When access is from the CPU and the DMA controller: Base address (BASE) = 4001_0000H
- When access is from an external MCU interface: Base address (BASE) = D_0000H

4.6 Memory Maps

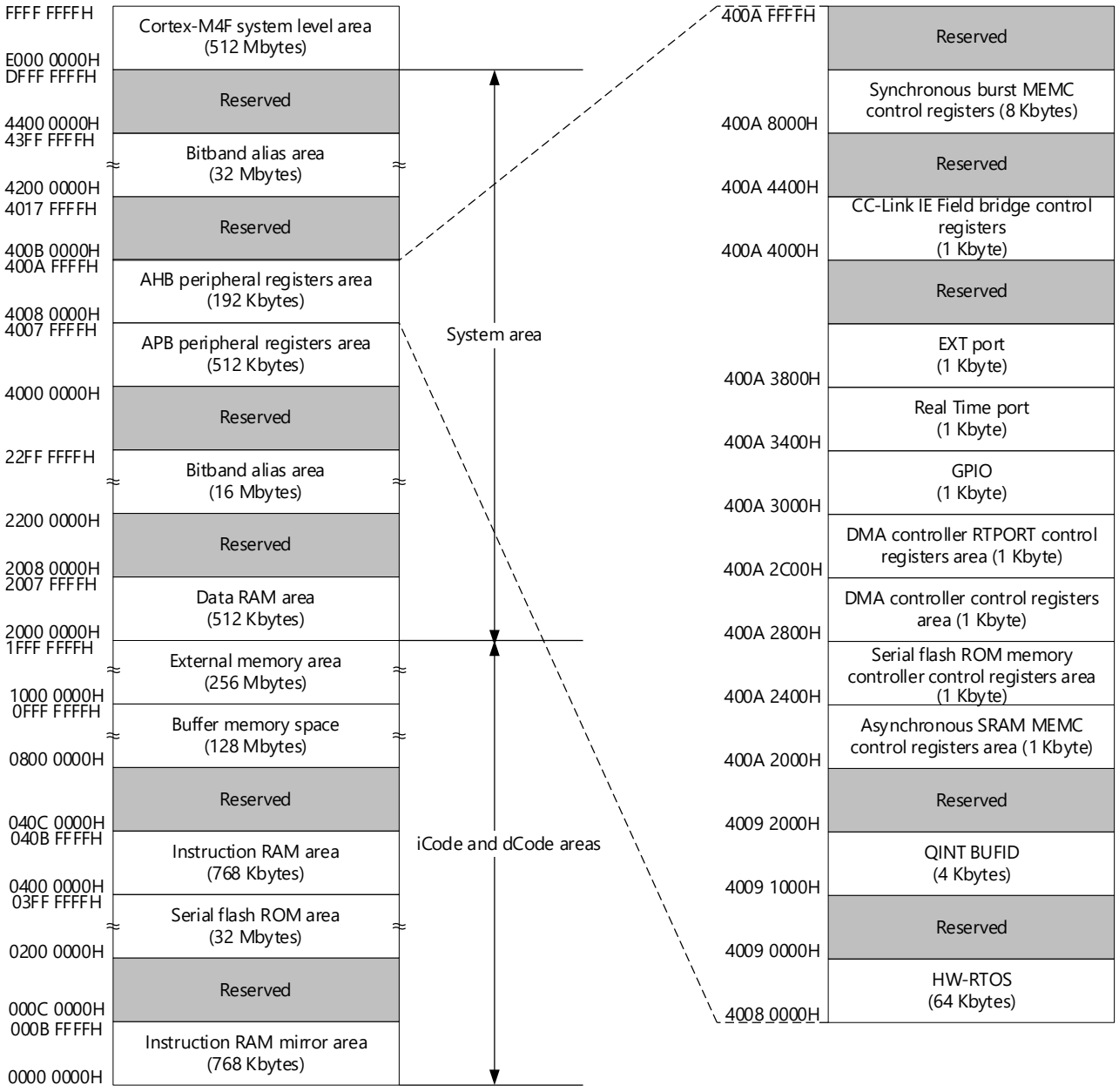


Figure 4.6-1 Entire Memory Map

The instruction RAM mirror area (768 Kbytes) differ depending on the selected boot mode. For details, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

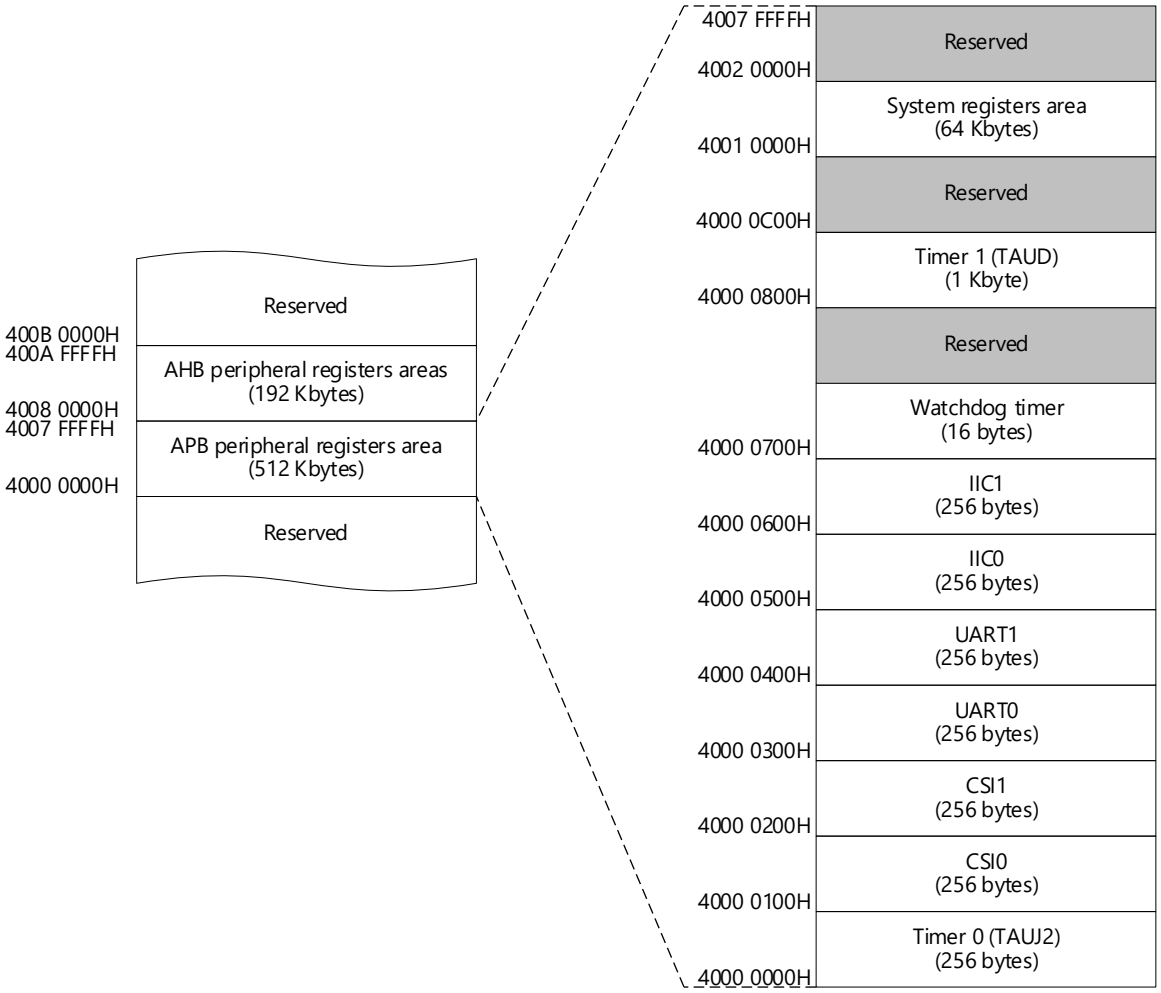


Figure 4.6-2 Memory Map (APB Peripheral Register Area)

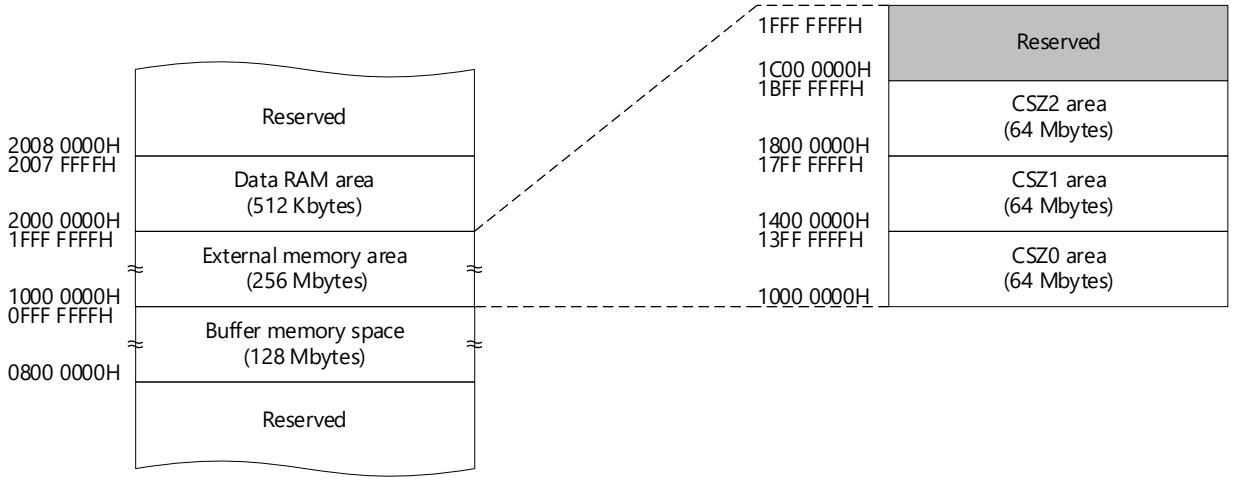


Figure 4.6-3 Memory Map (External Memory Area)

The upper 52 Kbytes of the AHB peripheral registers area covers the range from the GPIO area to the synchronous burst memory controller control registers.
For details, refer to "Figure 4.6-1 Entire Memory Map".
The instruction RAM mirror area (768 Kbytes) differ depending on the selected boot mode as follows. For details, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

BOOT1	BOOT0	Boot Mode	Access Area	Remarks
0	0	External memory boot	-	The external MCU interface is not available.
	1	External serial flash ROM boot	Reserved	Not accessible
1	0	External MCU boot	Instruction RAM area	-
	1	Instruction RAM boot		For debugging only

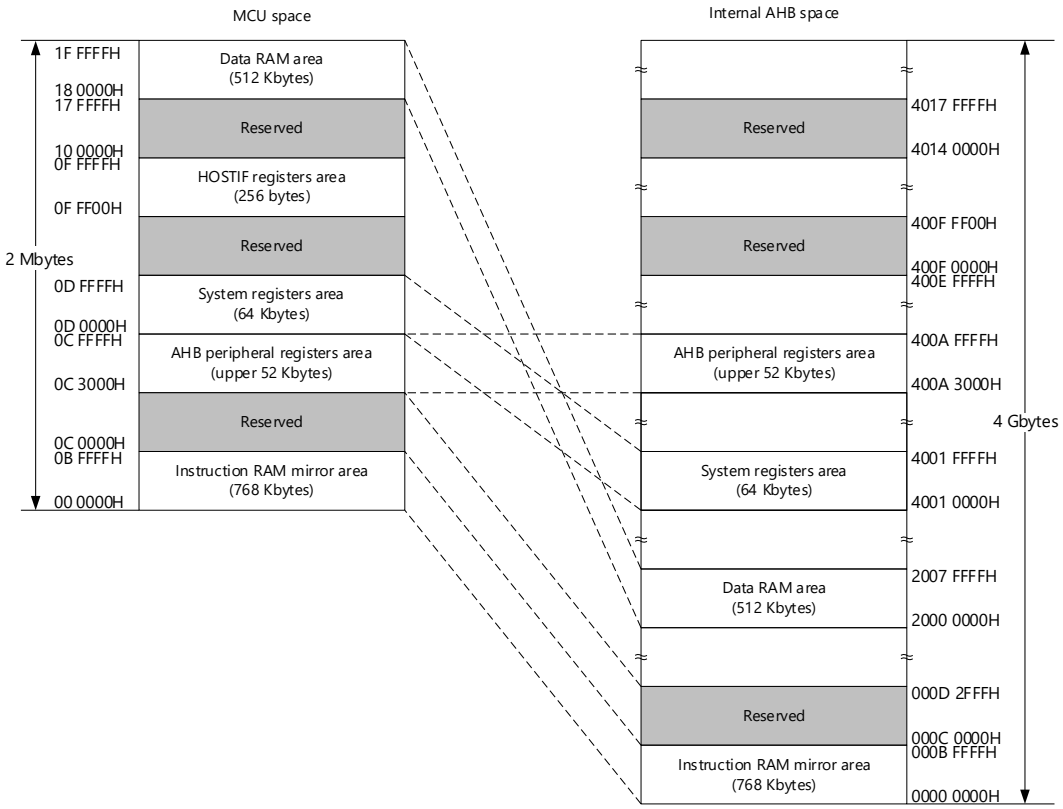


Figure 4.6-4 Memory Maps (External MCU Interface Space)

4.7 Exception Handling

Cortex-M4F exception handling refers to the process of responding to a sudden request for a different task during a process that involves program execution. Among the different exceptions, a general-purpose exception without a defined application is referred to as an "interrupt".

Exception numbers 1 to 15 are the system exception for the Cortex-M4F CPU. Interrupts from the CP520 internal hardware and external pins are assigned to exception number 16 and higher exception numbers. The following table lists the exceptions.

Note that "CP520 internal hardware" hereinafter refers to the areas other than the Cortex-M4F CPU area.

Table 4.7-1 List of Exceptions

Exception No.	Exception Type	Priority	Description
1	Reset	-3 (highest)	・ Input on the reset pins (RESETZ, PONRZ, HOTRESETZ) ・ Reset by the watchdog timer ・ Setting the SYSRESETREQ bit in NVIC of the Cortex-M4F CPU to 1 ・ Reset by the SYSRESET register
2	NMI	-2	・ Input on the NMI pin ・ Generation of NMI by the watchdog timer
3	Hard fault	-1	All classes of exceptions that no other exception handler can handle. Used to call up a response to a fault.
4	Memory management fault	Programmable	Exception from the CPU
5	Bus fault	Programmable	Bus error in access through the bus to the area outside the scope of management by the CPU
6	Usage fault	Programmable	Error in instruction execution, including the execution of an undefined instruction
7 to 10	Reserved	-	-
11	SVCall	Programmable	System service call by an SVC instruction
12	Debug monitor	Programmable	Debug monitor
13	Reserved	-	-
14	PendSV	Programmable	Request for system service that can be kept pending
15	SysTick	Programmable	Indication from the system timer
16 to 143	CP520 specific interrupt	Programmable	Interrupt from the CP520 internal hardware and external pins. For details, refer to Section 4.7.1 "List of interrupts".

CP520 uses the interrupt controller of Cortex-M4F.
For Cortex-M4F exception handling operations, visit the following Arm Limited website.
http://infocenter.arm.com/help/topic/com.arm.doc.set.cortexm/index.html

4.7.1 List of interrupts

Interrupts from the CP520 internal hardware and external pins are connected not only to the NVIC of the Cortex-M4F but also to the internal hardware real-time OS (HW-RTOS), trigger for starting the internal DMA controllers (common to both the general-purpose DMAC and real-time port DMAC), and timers.
CP520 supports the following interrupts.

Table 4.7.1-1 List of Interrupts

○: Connection, -: Not used

Exception No.	Name	Cause	Connected to				
			NVIC	HW-RTOS	DMAC	Real Time PORT	Timer TAUJ2/TAUD
16	INTTAUJ2I0	TAUJ2 channel 0 interrupt	○	○	○	○	○
17	INTTAUJ2I1	TAUJ2 channel 1 interrupt	○	○	○	○	○
18	INTTAUJ2I2	TAUJ2 channel 2 interrupt	○	○	○	○	○
19	INTTAUJ2I3	TAUJ2 channel 3 interrupt	○	○	○	○	○
20	INTUAJ0TIT	UARTJ0 send interrupt	○	○	○	○	○
21	INTUAJ0TIR	UARTJ0 reception interrupt	○	○	○	○	○
22	INTUAJ1TIT	UARTJ1 send interrupt	○	○	○	○	○
23	INTUAJ1TIR	UARTJ1 reception interrupt	○	○	○	○	○
24	INTCSIH0IC	CSIH0 communication status interrupt	○	○	○	○	○
25	INTCSIH0IR	CSIH0 reception status interrupt	○	○	○	○	○
26	INTCSIH0IJC	CSIH0 job completion interrupt	○	○	○	○	○
27	INTCSIH1IC	CSIH1 communication status interrupt	○	○	○	○	○
28	INTCSIH1IR	CSIH1 reception status interrupt	○	○	○	○	○
29	INTCSIH1IJC	CSIH1 job completion interrupt	○	○	○	○	○
30	INTIICB0TIA	IICB0 data send/receive interrupt	○	○	○	○	○
31	INTIICB1TIA	IICB1 data send/receive interrupt	○	○	○	○	○
32 - 37	-	Reserved	-	-	-	-	-
38	INTDMA00	General DMAC channel 0 transfer completion interrupt	○	○	○	○	○
39	INTDMA01	General DMAC channel 1 transfer completion interrupt	○	○	○	○	○
40	INTDMA02	General DMAC channel 2 transfer completion interrupt	○	○	○	○	○
41	INTDMA03	General DMAC channel 3 transfer completion interrupt	○	○	○	○	○
42	INTRTDMA	Real-time port DMAC transfer completion interrupt	○	○	○	○	○
43	INTTAUDI0	TAUD channel 0 interrupt	○	○	○	○	○
44	INTTAUDI1	TAUD channel 1 interrupt	○	○	○	○	○
45	INTTAUDI2	TAUD channel 2 interrupt	○	○	○	○	○
46	INTTAUDI3	TAUD channel 3 interrupt	○	○	○	○	○
47	INTTAUDI4	TAUD channel 4 interrupt	○	○	○	○	○
48	INTBUFDMA	Inter-buffer DMA transfer completion interrupt	○	○	○	○	○
49	INTETHPHY0	GbE-PHY PORT0 interrupt	○	○	○	○	○
50	INTETHPHY1	GbE-PHY PORT1 interrupt	○	○	○	○	○
51 - 62	-	Reserved	-	-	-	-	-
63	INTPZ0	INTPZ0 input	○	○	○	○	○
64	INTPZ1	INTPZ1 input	○	○	○	○	○
65	INTPZ2	INTPZ2 input	○	○	○	○	○
66	INTPZ3	INTPZ3 input	○	○	○	○	○
67	INTPZ4	INTPZ4 input	○	○	○	○	○
68	INTPZ5	INTPZ5 input	○	○	○	○	○
69	INTPZ6	INTPZ6 input	○	○	○	○	○

Exception No.	Name	Cause	Connected to				
			NVIC	HW-RTOS	DMAC	Real Time PORT	Timer TAUJ2/TAUD
70	INTPZ7	INTPZ7 input	○	○	○	○	○
71	INTPZ8	INTPZ8 input	○	○	○	○	○
72	INTPZ9	INTPZ9 input	○	○	○	○	○
73	INTPZ10	INTPZ10 input	○	○	○	○	○
74	INTPZ11	INTPZ11 input/TAUD channel 5 interrupt*1	○	○	○	○	○
75	INTPZ12	INTPZ12 input/TAUD channel 6 interrupt*1	○	○	○	○	○
76	INTPZ13	INTPZ13 input/TAUD channel 7 interrupt*1	○	○	○	○	○
77	INTPZ14	INTPZ14 input/TAUD channel 8 interrupt*1	○	○	○	○	○
78	INTPZ15	INTPZ15 input/TAUD channel 9 interrupt*1	○	○	○	○	○
79	INTPZ16	INTPZ16 input/TAUD channel 10 interrupt*1	○	○	○	○	○
80	INTPZ17	INTPZ17 input/TAUD channel 11 interrupt*1	○	○	○	○	○
81	INTPZ18	INTPZ18 input/TAUD channel 12 interrupt*1	○	○	○	○	○
82	INTPZ19	INTPZ19 input/TAUD channel 13 interrupt*1	○	○	○	○	○
83	INTPZ20	INTPZ20 input/TAUD channel 14 interrupt*1	○	○	○	○	○
84	INTPZ21	INTPZ21 input/TAUD channel 15 interrupt*1	○	○	○	○	○
85	INTPZ22	INTPZ22 input*1	○	○	○	○	○
86	INTPZ23	INTPZ23 input*1	○	○	○	○	○
87	INTPZ24	INTPZ24 input	○	○	○	○	○
88	INTPZ25	INTPZ25 input	○	○	○	○	○
89	INTPZ26	INTPZ26 input	○	○	○	○	○
90	INTPZ27	INTPZ27 input	○	○	○	○	○
91	INTPZ28	INTPZ28 input	○	○	○	○	○
92	INTHWRTOS	HW-RTOS interrupt	○	-	-	-	-
93	INTBRAMERR	Buffer RAM area access error interrupt	○	○	-	-	-
94	INTIICB0TIS	IICB0 status interrupt	○	○	-	-	-
95	INTIICB1TIS	IICB1 status interrupt	○	○	-	-	-
96	INTWDTAL	WDT alarm interrupt (including the 75% of timeout interrupt)	○	○	-	-	-
97	INTSFLASH	Serial flash ROM controller error interrupt	○	○	-	-	-
98	INTUAJ0TIS	UARTJ0 status interrupt	○	○	-	-	-
99	INTUAJ1TIS	UARTJ1 status interrupt	○	○	-	-	-
100	INTCSIH0IRE	CSIH0 communication error interrupt	○	○	-	-	-
101	INTCSIH1IRE	CSIH1 communication error interrupt	○	○	-	-	-
102	-	Reserved	-	-	-	-	-
103	-	Reserved	-	-	-	-	-
104	INTDERR0	General DMAC error response interrupt	○	○	-	-	-
105	INTDERR1	Real-time port DMAC error response interrupt	○	○	-	-	-
106 - 109	-	Reserved	-	-	-	-	-
110	INTBUFDMAERR	Internal buffer DMA error interrupt	○	○	-	-	-
111	INTLED0PHY0	GbE-PHY LED0_PHY0 input interrupt	○	○	○	○	○
112	INTLED0PHY1	GbE-PHY LED0_PHY1 input interrupt	○	○	○	○	○
113 - 122	-	Reserved	-	-	-	-	-
123	INTCCINMIZ	CC-Link IE Field NMIZ interrupt	○	○	○	○	○
124	INTCCIWDTZ	CC-Link IE Field WDTZ interrupt*2	○	○	○	○	○
125	INTCCIINTZ	CC-Link IE Field INTZ interrupt	○	○	○	○	○
126 - 136	-	Reserved	-	-	-	-	-
137	INTGBEPHYFLF	GbE-PHY FASTLINK_FAIL interrupt	○	○	-	-	-

Exception No.	Name	Cause	Connected to				
			NVIC	HW-RTOS	DMAC	Real Time PORT	Timer TAUJ2/TAUD
138	INTLED1PHY0	GbE-PHY LED1_PHY0 input interrupt	○	○	○	○	○
139	INTLED1PHY1	GbE-PHY LED1_PHY1 input interrupt	○	○	○	○	○
140	INTLED2PHY0	GbE-PHY LED2_PHY0 input interrupt	○	○	-	-	-
141	INTLED2PHY1	GbE-PHY LED2_PHY1 input interrupt	○	○	-	-	-
142	INTFPU	FPU interrupt	○	○	-	-	-
143	-	Reserved	-	-	-	-	-

*1: INTPZ/TAUD interrupts are selected using the INTSEL register.
For details, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

*2: The CC-Link IE Field WDTZ interrupt uses a WDTIL signal having an inverted CCI_WDTIZ pin.

4.8 Peripheral Modules

For details of the following peripheral modules, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

- Clock/Reset function
- CPU
- Bus structure
- Boot procedure
- Hardware real-time OS
- Gigabit Ethernet PHY
- Asynchronous SRAM memory controller (ROM/SRAM)
- Synchronous burst access memory controller
- External MCU interface
- Serial flash ROM memory controller
- DMA function
- 32-bit timer array unit (TAUJ2)
- 16-bit timer array unit (TAUD)
- Window watchdog timer A (WDTA)
- Asynchronous serial interface J (UARTJn)
- Clocked serial interface H (CSIH)
- I2C bus (IICB)
- Debugging

4.9 I/O Standby Function

The CP520 port implements a standby function designed to prevent undefined external output and I/O through current (device destruction countermeasure) when the I/O power supply (VDD33) is ON and the core power supply (VDD10) is OFF.

The external pins of each port during standby can be set to H (output), L (output), or Hi-Z by dedicated pin CTRSTBYB (Active: Low) setup.
The state cannot be selected by software.

Table 4.9-1 Operation of I/O with Standby Function

Mode	VDD10	VDD33	CTRSTBYB	Y0 Output (External)	Y1 Output (Internal)	Pull-up/Pull-down Resistance
Standby	OFF	ON	0	L*1, H*1, Hi-Z	L	Disabled
Normal	ON		1	Normal operation		Enabled

*1: The target I/O pin outputs High or Low.

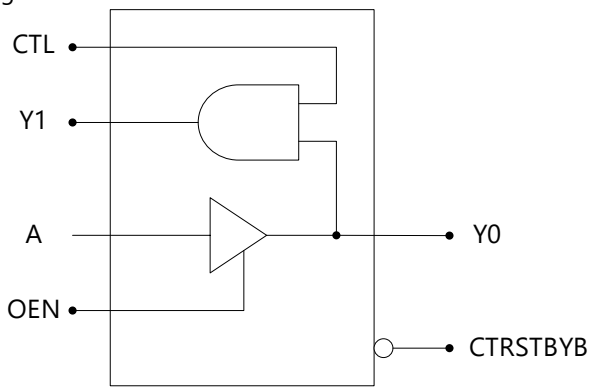


Figure 4.9-1 Block Diagram of I/O with Standby Function

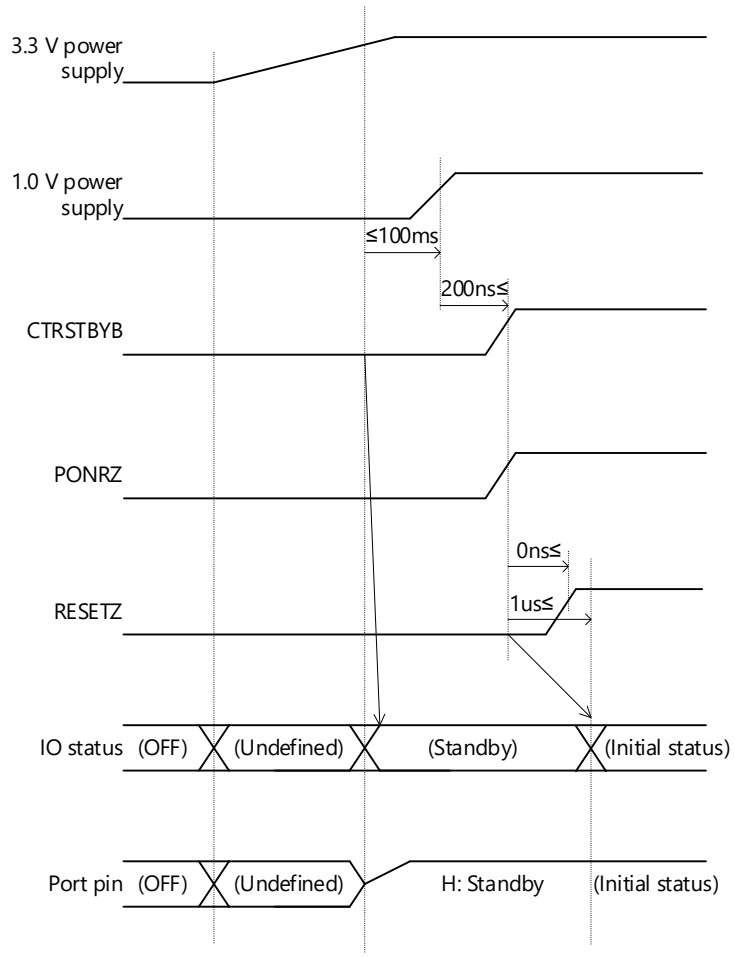


Figure 4.9-2 Power Supply ON Timing Chart (Standby H Type): 3.3 V Power Supply → 1.0 V Power Supply Startup

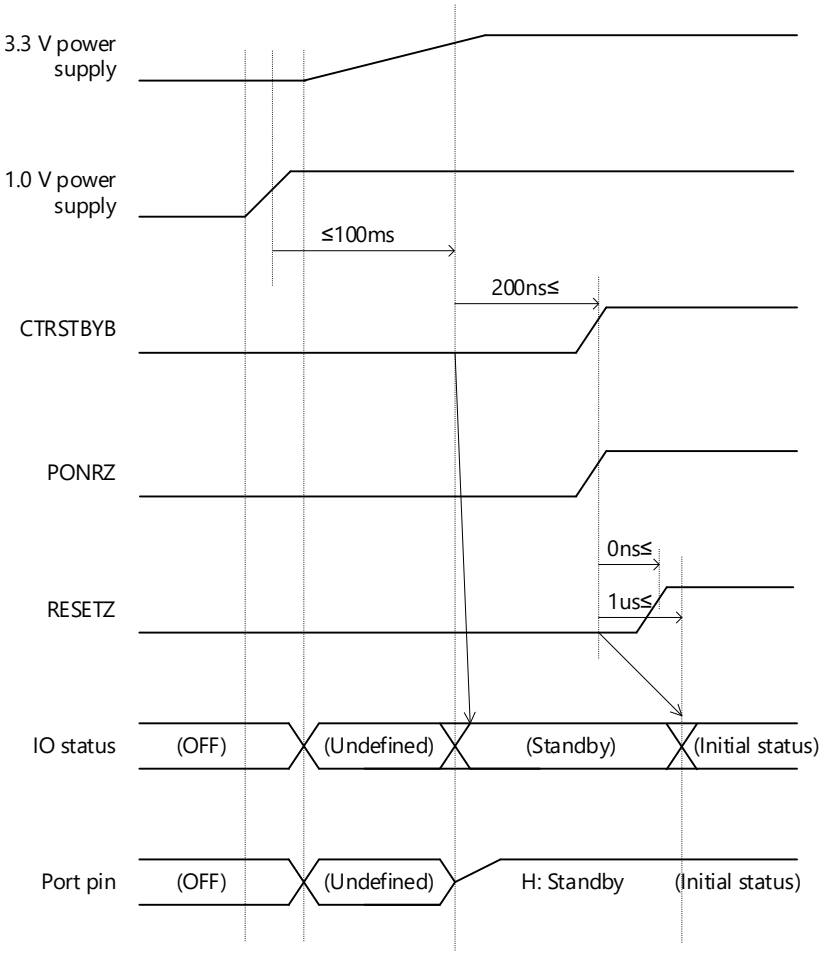


Figure 4.9-3 Power Supply ON Timing Chart (Standby H Type): 1.0 V Power Supply → 3.3 V Power Supply Startup

5 PIN FUNCTIONS

This chapter describes the function of each CP520 pin.

The meanings of the items, symbols, and abbreviations used in each table in this section are given below.

Table 5-1 Meanings of the Items in the Tables

Item	Meaning
Function Name	Name of a function of the pin when the pin has a multiplexed function
Pin Name	Name of the pin (For the pins, refer to Section 4.4 "Pin Assignments".)
I/O	I/O direction of the given pin
Description	Summary of the given pin function
Active	Active level of the given pin
Level during Reset	Indicates the pin state while RSTOUTZ=Low. For details on the reset specifications, refer to "R-IN32M4-CL2 User's Manual: Peripheral Modules".
I/O Standby	Indicates the pin state during I/O standby of the given pin. For details, refer to Section 4.9 "I/O Standby Function".

Table 5-2 Meanings of the Symbols and Abbreviations in the Tables

Target	Symbol and Abbreviation	Meaning
I/O	-	The pin does not have an I/O direction, such as a power supply or ground pin.
Active Level	-	There is no active level (clock pin, data pin, address pin, etc).
	High	The active level is High.
	Low	The active level is Low.
Level during Reset	-	The pin has no initial level or state following a reset. (Input-dedicated pin)
	High	The pin state during a reset is High.
	Low	The pin state during a reset is Low.
	Hi-Z (High)	The pin state during a reset is Hi-Z with the internal pull-up resistor pulling it to the High level.
	Hi-Z (Low)	The pin state during a reset is Hi-Z with the internal pull-down resistor pulling it to the Low level.
I/O Standby	-	There is no I/O standby function.
	High	The pin state during standby is High.
	Low	The pin state during standby is Low.
	Hi-Z	The pin state during standby is Hi-Z.

5.1 Pin List

The following table lists the pins in order of the pin number.

Table 5.1-1 Pin List (Pin Number Order)

"I"=Input, "O"=Output

Pin No.	Pin ID	Pin Name	I/O	Pin No.	Pin ID	Pin Name	I/O	Pin No.	Pin ID	Pin Name	I/O	Pin No.	Pin ID	Pin Name	I/O	Pin No.	Pin ID	Pin Name	I/O
1	A1	GND	-	59	F22	RP27	I/O	117	AA15	P70	I/O	175	U3	GND	-	233	H4	RESERVED_H4	-
2	B1	GND	-	60	E22	RP25	I/O	118	AA16	P37	I/O	176	V3	GND	-	234	J4	GND	-
3	C1	GND	-	61	D22	RP23	I/O	119	AA17	P36	I/O	177	W3	GND	-	235	K4	GND	-
4	D1	GND	-	62	C22	RP21	I/O	120	AA18	GND	-	178	Y3	GND	-	236	L4	GND	-
5	E1	GND	-	63	B22	GND	-	121	AA19	P35	I/O	179	Y4	RESERVED_Y4	I/O	237	M4	GND	-
6	F1	GND	-	64	A22	GND	-	122	AA20	P33	I/O	180	Y5	RESERVED_Y5	I	238	N4	GND	-
7	G1	P0_D3P	I/O	65	A21	GND	-	123	AA21	P32	I/O	181	Y6	RESERVED_Y6	I	239	P4	GND	-
8	H1	P0_D2P	I/O	66	A20	RP30	I/O	124	Y21	P31	I/O	182	Y7	RESERVED_Y7	I	240	R4	RESERVED_R4	-
9	J1	P0_D1P	I/O	67	A19	RP31	I/O	125	W21	P61	I/O	183	Y8	JTAGSEL	I	241	T4	RESERVED_T4	-
10	K1	P0_D0P	I/O	68	A18	BUSCLK	O	126	V21	P62	I/O	184	Y9	TRACEDATA3	I/O	242	U4	RESERVED_U4	-
11	L1	GND	-	69	A17	D6	I/O	127	U21	P64	I/O	185	Y10	TRACEDATA2	I/O	243	V4	GND	-
12	M1	REF_REXT	I/O	70	A16	D4	I/O	128	T21	P66	I/O	186	Y11	TRACEDATA0	I/O	244	W4	RESERVED_W4	I/O
13	N1	GND	-	71	A15	D2	I/O	129	R21	P27	I/O	187	Y12	TRACECLK	O	245	W5	TMS	I/O
14	P1	P1_D3P	I/O	72	A14	D0	I/O	130	P21	P26	I/O	188	Y13	NMIZ	I	246	W6	TDI	I
15	R1	P1_D2P	I/O	73	A13	RDZ	I/O	131	N21	P23	I/O	189	Y14	EXTP4	I/O	247	W7	TCK	I
16	T1	P1_D1P	I/O	74	A12	P10	I/O	132	M21	P21	I/O	190	Y15	EXTP6	I/O	248	W8	TDO	O
17	U1	P1_D0P	I/O	75	A11	P11	I/O	133	L21	RESERVED_L21	I	191	Y16	EXTP8	I/O	249	W9	TRSTZ	I
18	V1	GND	-	76	A10	P14	I/O	134	K21	RESERVED_K21	I	192	Y17	BOOT1	I	250	W10	GND	-
19	W1	GND	-	77	A9	P16	I/O	135	J21	RESERVED_J21	I	193	Y18	BOOT0	I	251	W11	TRACEDATA1	I/O
20	Y1	GND	-	78	A8	P47	I/O	136	H21	RP01	I/O	194	Y19	RSTOUTZ	O	252	W12	GND	-
21	AA1	GND	-	79	A7	P45	I/O	137	G21	RP03	I/O	195	Y20	PONRZ	I	253	W13	OSCTH	I
22	AB1	GND	-	80	A6	P43	I/O	138	F21	RP04	I/O	196	W20	HOTRESETZ	I	254	W14	EXTP5	I/O
23	AB2	GND	-	81	A5	P42	I/O	139	E21	RP26	I/O	197	V20	HWRZSEL	I	255	W15	EXTP7	I/O
24	AB3	P56	I/O	82	A4	P40	I/O	140	D21	RP24	I/O	198	U20	EXTP3	I/O	256	W16	EXTP9	I/O
25	AB4	P54	I/O	83	A3	A2	I/O	141	C21	RP22	I/O	199	T20	EXTP2	I/O	257	W17	HIFSYNC	I
26	AB5	P52	I/O	84	A2	GND	-	142	B21	RP20	I/O	200	R20	EXTP1	I/O	258	W18	MEMIFSEL	I
27	AB6	P50	I/O	85	B2	PHY0_LED0	O	143	B20	RP32	I/O	201	P20	EXTP0	I/O	259	W19	BUS32EN	I
28	AB7	P06	I/O	86	C2	PHYADD4	I	144	B19	RP33	I/O	202	N20	P24	I/O	260	V19	ADMUXMODE	I
29	AB8	P04	I/O	87	D2	GND	-	145	B18	RP34	I/O	203	M20	RESERVED_M20	O	261	U19	MEMCSEL	I
30	AB9	P02	I/O	88	E2	GND	-	146	B17	RP35	I/O	204	L20	RESERVED_L20	I	262	T19	VDD33	-
31	AB10	P00	I/O	89	F2	GND	-	147	B16	D5	I/O	205	K20	RESERVED_K20	I	263	R19	RESERVED_R19	I
32	AB11	P76	I/O	90	G2	P0_D3N	I/O	148	B15	D3	I/O	206	J20	RESERVED_J20	O	264	P19	RESERVED_P19	I
33	AB12	P74	I/O	91	H2	P0_D2N	I/O	149	B14	D1	I/O	207	H20	RP05	I/O	265	N19	RESERVED_N19	I
34	AB13	P72	I/O	92	J2	P0_D1N	I/O	150	B13	WRSTBZ	I/O	208	G20	RP07	I/O	266	M19	RESERVED_M19	O
35	AB14	XT1	I	93	K2	P0_D0N	I/O	151	B12	P12	I/O	209	F20	RP13	I/O	267	L19	RESERVED_L19	I
36	AB15	XT2	I/O	94	L2	GND	-	152	B11	P13	I/O	210	E20	RP12	I/O	268	K19	RESERVED_K19	I
37	AB16	GND	-	95	M2	REF_FILT	I/O	153	B10	P15	I/O	211	D20	RP11	I/O	269	J19	RESERVED_J19	O
38	AB17	RESERVED_AB17	I	96	N2	GND	-	154	B9	P17	I/O	212	C20	RP10	I/O	270	H19	RP06	I/O
39	AB18	CCI_CLK2_097M	I	97	P2	P1_D3N	I/O	155	B8	P44	I/O	213	C19	RP37	I/O	271	G19	RP17	I/O
40	AB19	P34	I/O	98	R2	P1_D2N	I/O	156	B7	P46	I/O	214	C18	RP36	I/O	272	F19	RP16	I/O
41	AB20	RESETZ	I	99	T2	P1_D1N	I/O	157	B6	P41	I/O	215	C17	D13	I/O	273	E19	RP15	I/O
42	AB21	GND	-	100	U2	P1_D0N	I/O	158	B5	A7	I/O	216	C16	D11	I/O	274	D19	RP14	I/O
43	AB22	GND	-	101	V2	GND	-	159	B4	A5	I/O	217	C15	D9	I/O	275	D18	D15	I/O
44	AA22	GND	-	102	W2	GND	-	160	B3	A3	I/O	218	C14	D7	I/O	276	D17	D14	I/O
45	Y22	P30	I/O	103	Y2	GND	-	161	C3	A4	I/O	219	C13	CSZ0	I/O	277	D16	D12	I/O
46	W22	P60	I/O	104	AA2	PHY1_LED0	O	162	D3	PHYADD3	I	220	C12	WRZ0	I/O	278	D15	D10	I/O
47	V22	P63	I/O	105	AA3	P57	I/O	163	E3	GND	-	221	C11	WRZ1	I/O	279	D14	D8	I/O
48	U22	P65	I/O	106	AA4	P55	I/O	164	F3	GND	-	222	C10	A17	I/O	280	D13	A20	I/O
49	T22	P67	I/O	107	AA5	P53	I/O	165	G3	GND	-	223	C9	A15	I/O	281	D12	A19	I/O

Pin No.	Pin ID	Pin Name	I/O	Pin No.	Pin ID	Pin Name	I/O	Pin No.	Pin ID	Pin Name	I/O	Pin No.	Pin ID	Pin Name	I/O	Pin No.	Pin ID	Pin Name	I/O
50	R22	RESERVED_R22	I	108	AA6	P51	I/O	166	H3	GND	-	224	C8	A13	I/O	282	D11	A18	I/O
51	P22	P25	I/O	109	AA7	P07	I/O	167	J3	GND	-	225	C7	A11	I/O	283	D10	GND	-
52	N22	P22	I/O	110	AA8	P05	I/O	168	K3	VDD1A	-	226	C6	A9	I/O	284	D9	A16	I/O
53	M22	P20	I/O	111	AA9	P03	I/O	169	L3	VDD1A	-	227	C5	A8	I/O	285	D8	A14	I/O
54	L22	RESERVED_L22	I	112	AA10	P01	I/O	170	M3	GND	-	228	C4	A6	I/O	286	D7	A12	I/O
55	K22	RESERVED_K22	I	113	AA11	P77	I/O	171	N3	VDD25A	-	229	D4	PHYADD2	I	287	D6	A10	I/O
56	J22	RESERVED_J22	I	114	AA12	P75	I/O	172	P3	VDD25A	-	230	E4	GND	-	288	D5	PHYADD1	I
57	H22	RP00	I/O	115	AA13	P73	I/O	173	R3	VDD25A	-	231	F4	RESERVED_F4	-	289	E5	GND	-
58	G22	RP02	I/O	116	AA14	P71	I/O	174	T3	GND	-	232	G4	RESERVED_G4	-	290	F5	RESERVED_F5	-
291	G5	RESERVED_G5	I	330	E16	GND	-	369	L17	VDD10	-	408	L16	GND	-	447	H10	GND	-
292	H5	RESERVED_H5	-	331	E15	GND	-	370	K17	VDD10	-	409	K16	GND	-	448	H9	GND	-
293	J5	RESERVED_J5	-	332	E14	GND	-	371	J17	VDD10	-	410	J16	GND	-	449	J9	VDD33_GPHY	-
294	K5	GND	-	333	E13	GND	-	372	H17	VDD10	-	411	H16	VDD10	-	450	K9	VDD33_GPHY	-
295	L5	GND	-	334	E12	GND	-	373	G17	GND	-	412	G16	GND	-	451	L9	VDD33_GPHY	-
296	M5	GND	-	335	E11	GND	-	374	F17	VDD33	-	413	G15	GND	-	452	M9	VDD33_GPHY	-
297	N5	GND	-	336	E10	GND	-	375	F16	VDD33	-	414	G14	GND	-	453	N9	VDD33_GPHY	-
298	P5	RESERVED_P5	-	337	E9	GND	-	376	F15	GND	-	415	G13	GND	-	454	P9	VDD33_GPHY	-
299	R5	RESERVED_R5	-	338	E8	GND	-	377	F14	VDD33	-	416	G12	VDD33	-	455	P10	GND	-
300	T5	RESERVED_T5	I	339	E7	GND	-	378	F13	GND	-	417	G11	GND	-	456	P11	GND	-
301	U5	RESERVED_U5	-	340	E6	GND	-	379	F12	VDD33	-	418	G10	GND	-	457	P12	VDD33	-
302	V5	GND	-	341	F6	GND	-	380	F11	GND	-	419	G9	GND	-	458	P13	VDD10	-
303	V6	GND	-	342	G6	GND	-	381	F10	GND	-	420	G8	GND	-	459	P14	GND	-
304	V7	GND	-	343	H6	GND	-	382	F9	GND	-	421	H8	GND	-	460	N14	GND	-
305	V8	GND	-	344	J6	VDD1	-	383	F8	GND	-	422	J8	VDD33_GPHY	-	461	M14	GND	-
306	V9	GND	-	345	K6	GND	-	384	F7	GND	-	423	K8	GND	-	462	L14	GND	-
307	V10	GND	-	346	L6	GND	-	385	G7	GND	-	424	L8	GND	-	463	K14	GND	-
308	V11	GND	-	347	M6	GND	-	386	H7	GND	-	425	M8	GND	-	464	J14	GND	-
309	V12	GND	-	348	N6	GND	-	387	J7	VDD1	-	426	N8	GND	-	465	J13	VDD10	-
310	V13	GND	-	349	P6	VDD1	-	388	K7	GND	-	427	P8	VDD33_GPHY	-	466	J12	VDD33	-
311	V14	GND	-	350	R6	GND	-	389	L7	GND	-	428	R8	GND	-	467	J11	GND	-
312	V15	GND	-	351	T6	GND	-	390	M7	GND	-	429	R9	GND	-	468	J10	GND	-
313	V16	PLL_GND	-	352	U6	RESERVED_U6	I	391	N7	GND	-	430	R10	GND	-	469	K10	GND	-
314	V17	PLL_VDD	-	353	U7	GND	-	392	P7	VDD1	-	431	R11	GND	-	470	L10	RESERVED_L10	I/O
315	V18	ETHTEST	I	354	U8	GND	-	393	R7	GND	-	432	R12	GND	-	471	M10	GND	-
316	U18	VDD33	-	355	U9	GND	-	394	T7	GND	-	433	R13	VDD10	-	472	N10	GND	-
317	T18	GND	-	356	U10	GND	-	395	T8	GND	-	434	R14	VDD10	-	473	N11	GND	-
318	R18	PLL_GND	-	357	U11	GND	-	396	T9	GND	-	435	R15	VDD10	-	474	N12	GND	-
319	P18	PLL_VDD	-	358	U12	VDD33	-	397	T10	GND	-	436	P15	GND	-	475	N13	VDD10	-
320	N18	GND	-	359	U13	VDD33	-	398	T11	GND	-	437	N15	GND	-	476	M13	VDD10	-
321	M18	GND	-	360	U14	GND	-	399	T12	VDD33	-	438	M15	GND	-	477	L13	VDD10	-
322	L18	VDD33	-	361	U15	GND	-	400	T13	GND	-	439	L15	GND	-	478	K13	VDD10	-
323	K18	VDD33	-	362	U16	VDD33	-	401	T14	GND	-	440	K15	GND	-	479	K12	GND	-
324	J18	GND	-	363	U17	VDD33	-	402	T15	GND	-	441	J15	GND	-	480	K11	GND	-
325	H18	VDD33	-	364	T17	GND	-	403	T16	GND	-	442	H15	VDD10	-	481	L11	GND	-
326	G18	GND	-	365	R17	VDD10	-	404	R16	VDD10	-	443	H14	VDD10	-	482	M11	GND	-
327	F18	VDD33	-	366	P17	VDD10	-	405	P16	GND	-	444	H13	VDD10	-	483	M12	VDD33	-
328	E18	GND	-	367	N17	VDD10	-	406	N16	GND	-	445	H12	GND	-	484	L12	VDD33	-
329	E17	CTRSTBYB	I	368	M17	VDD10	-	407	M16	GND	-	446	H11	GND	-	-	-	-	

5.2.1 Port pins and real-time port pins

The pins described in Section 5.2.1 are multiplexed with port pins described in Section 5.2.2 "Ethernet pins" to Section 5.2.16 "Operating mode setting pins".

The chip has 13 ports and real-time ports for the 3.3-V interface, all of which are 8-bit ports except for EXTP, which has 10 bits.
Grouping them into sets of four ports allows 32-bit access: i.e., through ports 0 to 3 (P00 to P37), ports 4 to 7 (P40 to P77), and real-time ports 0 to 3 (RP00 to RP37).

Ports RP0x to RP3x (x: 0 to 7) operate as real-time ports. Together, they are able to handle input and output in 32-bit units in synchronization with the DMA transfer trigger from the dedicated DMA controller for the real-time ports.

Port 5 (P53 to P56) is 5V-Tolerant compatible. For the tolerant buffer, refer to the following:
- Section 5.6.1 "Port pins, real-time port pin buffer types, and handling of unused pins".
- Section 6.1 "Absolute Maximum Ratings", Section 6.2 "Recommended Operating Conditions", Section 6.3 "DC Characteristics", and Section 6.4 "Pull-Up/Pull-Down Resistor Values".

Table 5.2.1-1 Port Pins and Real-Time Port Pins

Pin ID	Pin Name	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function 4	Level during Reset	I/O Standby
AB10	P00	INTPZ0	-	CCI_RUNLEDZ	P00_RESERVED4		
AA10	P01	INTPZ1	-	CCI_USER1LEDZ	P01_RESERVED4		
AB9	P02	INTPZ2	-	CCI_DLINKLEDZ	P02_RESERVED4		
AA9	P03	INTPZ3	-	CCI_ERRLEDZ	P03_RESERVED4		
AB8	P04	INTPZ4	-	CCI_LERR0LEDZ	P04_RESERVED4		
AA8	P05	INTPZ5	-	CCI_LERR1LEDZ	P05_RESERVED4		
AB7	P06	-	-	CCI_SDLEDZ	P06_RESERVED4		
AA7	P07	-	-	CCI_RDLEDZ	P07_RESERVED4		
A12	P10	SMIO2	-	-	P10_RESERVED4		
A11	P11	SMIO3	-	-	P11_RESERVED4		
B12	P12	CSZ3	-	CCI_WDTIZ	P12_RESERVED4		
B11	P13	CSZ2	-	P13_RESERVED3	P13_RESERVED4		
A10	P14	SMSCK	-	-	P14_RESERVED4		
B10	P15	SMIO0	-	-	P15_RESERVED4		
A9	P16	SMIO1	-	-	P16_RESERVED4	Hi-Z (High)	High
B9	P17	SMCSZ	-	-	P17_RESERVED4		
M22	P20	RXD0	-	P20_RESERVED3	P20_RESERVED4		
M21	P21	TXD0	-	P21_RESERVED3	P21_RESERVED4		
N22	P22	INTPZ8	-	P22_RESERVED3	P22_RESERVED4		
N21	P23	INTPZ9	-	P23_RESERVED3	P23_RESERVED4		
N20	P24	INTPZ10	P24_RESERVED2	P24_RESERVED3	P24_RESERVED4		
P22	P25	WDTOUTZ	-	P25_RESERVED3	P25_RESERVED4		
P21	P26	TINJ1 / TIND5[*1]	TOUTJ1 / TOUTD5[*1]	P26_RESERVED3	P26_RESERVED4		
R21	P27	TINJ0 / TIND4[*1]	TOUTJ0 / TOUTD4[*1]	-	P27_RESERVED4		
Y22	P30	RXD1	-	-	P30_RESERVED4		
Y21	P31	TXD1	-	-	P31_RESERVED4		
AA21	P32	DMAREQZ1	P32_RESERVED2	P32_RESERVED3	P32_RESERVED4		
AA20	P33	DMAACKZ1	-	P33_RESERVED3	P33_RESERVED4		
AB19	P34	DMATCZ1	-	-	P34_RESERVED4		
AA19	P35	CSISCK1	INTPZ22	-	P35_RESERVED4	Hi-Z (Low)	Hi-Z
AA17	P36	CSISI1	INTPZ23	-	P36_RESERVED4	Hi-Z (High)	High
AA16	P37	CSISO1	INTPZ24	-	P37_RESERVED4	Hi-Z (Low)	Hi-Z
A4	P40	A1/MA0	HA1	-	-		
B6	P41	WAITZ	HWAITZ	-	-		
A5	P42	CSICS00	HERROUTZ	P42_RESERVED3	-		
A6	P43	CSICS01	HBUSCLK	P43_RESERVED3	-	Hi-Z (High)	High
B8	P44	CSZ1	HPGCSZ	-	P44_RESERVED4		
A7	P45	CSISCK0	WAITZ1	-	-		
B7	P46	CSISI0	WAITZ2	-	-		
A8	P47	CSISO0	WAITZ3	-	-		

Pin ID	Pin Name	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function 4	Level during Reset	I/O Standby
AB6	P50	INTPZ6	-	CCI_USER2LEDZ	P50_RESERVED4		
AA6	P51	INTPZ7	-	P51_RESERVED3	P51_RESERVED4	Hi-Z (Low)	Hi-Z
AB5	P52	TINJ3 / TIND7[*1]	TOUTJ3 / TOUTD7[*1]	CCI_NMIZ	P52_RESERVED4	Hi-Z (High)	High
AA5	P53	P53_RESERVED1	CCI_INTZ	-	-	Hi-Z (High)	-
AB4	P54	P54_RESERVED1	P54_RESERVED2	P54_RESERVED3	P54_RESERVED4		
AA4	P55	P55_RESERVED1	P55_RESERVED2	P55_RESERVED3	P55_RESERVED4		
AB3	P56	P56_RESERVED1	P56_RESERVED2	P56_RESERVED3	-		
AA3	P57	TINJ2 / TIND6[*1]	TOUTJ2 / TOUTD6[*1]	P57_RESERVED3	P57_RESERVED4	Hi-Z (High)	High
W22	P60	SCL0	-	-	P60_RESERVED4		
W21	P61	SDA0	-	-	P61_RESERVED4		
V21	P62	RTDMAREQZ	ETH_MDC	P62_RESERVED3	P62_RESERVED4		
V22	P63	RTDMAACKZ	ETH_MDIO	P63_RESERVED3	P63_RESERVED4		
U21	P64	RTDMATCZ	NRESET_OUT	P64_RESERVED3	P64_RESERVED4		
U22	P65	DMAREQZ0	FASTLINK_FAIL	P65_RESERVED3	P65_RESERVED4		
T21	P66	DMAACKZ0	-	P66_RESERVED3	P66_RESERVED4		
T22	P67	DMATCZ0	-	P67_RESERVED3	P67_RESERVED4		
AA15	P70	CSICS10	P70_RESERVED2	P70_RESERVED3	P70_RESERVED4		
AA14	P71	CSICS11	P71_RESERVED2	P71_RESERVED3	P71_RESERVED4		
AB13	P72	SLEEPING	P72_RESERVED2	P72_RESERVED3	P72_RESERVED4		
AA13	P73	INTPZ11	P73_RESERVED2	P73_RESERVED3	P73_RESERVED4		
AB12	P74	INTPZ12	P74_RESERVED2	P74_RESERVED3	P74_RESERVED4		
AA12	P75	INTPZ13	XCLK1	P75_RESERVED3	P75_RESERVED4		
AB11	P76	INTPZ14	-	P76_RESERVED3	P76_RESERVED4		
AA11	P77	INTPZ15	-	P77_RESERVED3	P77_RESERVED4		
P20	EXTP0	EXTP0_RESERVED1	TOUTD0	EXTP0_RESERVED3	TIND0		
R20	EXTP1	EXTP1_RESERVED1	TOUTD1	EXTP1_RESERVED3[*2]	TIND1		
T20	EXTP2	EXTP2_RESERVED1	TOUTD2	EXTP2_RESERVED3[*2]	TIND2		
U20	EXTP3	WDTOUTZ	TOUTD3	EXTP3_RESERVED3[*2]	TIND3		
Y14	EXTP4	EXTP4_RESERVED1	EXTP4_RESERVED2	EXTP4_RESERVED3[*2]	EXTP4_RESERVED4		
W14	EXTP5	EXTP5_RESERVED1	EXTP5_RESERVED2	EXTP5_RESERVED3	EXTP5_RESERVED4		
Y15	EXTP6	EXTP6_RESERVED1	EXTP6_RESERVED2	EXTP6_RESERVED3	EXTP6_RESERVED4	Hi-Z (Low)	Hi-Z
W15	EXTP7	EXTP7_RESERVED1	EXTP7_RESERVED2	EXTP7_RESERVED3	EXTP7_RESERVED4	Hi-Z (High)	High
Y16	EXTP8	EXTP8_RESERVED1	EXTP8_RESERVED2	EXTP8_RESERVED3	EXTP8_RESERVED4		
W16	EXTP9	EXTP9_RESERVED1	EXTP9_RESERVED2	EXTP9_RESERVED3	EXTP9_RESERVED4		
H22	RP00	INTPZ16	SCL1	RP00_RESERVED3	RP00_RESERVED4	Hi-Z (High)	High
H21	RP01	INTPZ17	SDA1	RP01_RESERVED3	RP01_RESERVED4		
G22	RP02	INTPZ18	-	RP02_RESERVED3	RP02_RESERVED4		
G21	RP03	INTPZ19	-	RP03_RESERVED3	RP03_RESERVED4		
F21	RP04	INTPZ20	-	RP04_RESERVED3	RP04_RESERVED4		
H20	RP05	INTPZ21	-	RP05_RESERVED3	RP05_RESERVED4		
H19	RP06	WRZ2/BENZ2	HWRZ2/HBENZ2	-	-		
G20	RP07	WRZ3/BENZ3	HWRZ3/HBENZ3	RP07_RESERVED3[*3]	-		
C20	RP10	D24/MD24/HD24	LED0_PHY0	RP10_RESERVED3	-		
D20	RP11	D25/MD25/HD25	LED1_PHY0	RP11_RESERVED3[*3]	-		
E20	RP12	D26/MD26/HD26	LED2_PHY0	RP12_RESERVED3	-		
F20	RP13	D27/MD27/HD27	LED3_PHY0	RP13_RESERVED3[*3]	-		
D19	RP14	D28/MD28/HD28	LED0_PHY1	RP14_RESERVED3[*3]	-		
E19	RP15	D29/MD29/HD29	LED1_PHY1	RP15_RESERVED3[*3]	-		
F19	RP16	D30/MD30/HD30	LED2_PHY1	RP16_RESERVED3	-		
G19	RP17	D31/MD31/HD31	LED3_PHY1	RP17_RESERVED3	RP17_RESERVED4		
B21	RP20	BCYSTZ/ ADVZ	HBCYSTZ	RP20_RESERVED3	RP20_RESERVED4		
C22	RP21	A21/MA20	-	RP21_RESERVED3	RP21_RESERVED4		
C21	RP22	A22/MA21	-	RP22_RESERVED3[*2]	RP22_RESERVED4		
D22	RP23	A23/MA22	-	RP23_RESERVED3	RP23_RESERVED4		
D21	RP24	A24/MA23	INTPZ25	RP24_RESERVED3	RP24_RESERVED4		
E22	RP25	A25/MA24	INTPZ26	RP25_RESERVED3	RP25_RESERVED4		
E21	RP26	A26/MA25	INTPZ27	RP26_RESERVED3	RP26_RESERVED4		

Pin ID	Pin Name	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function 4	Level during Reset	I/O Standby
F22	RP27	A27/MA26	INTPZ28	-	RP27_RESERVED4		
A20	RP30	D16/MD16/HD16	TOUTD8	TIND8	RP30_RESERVED4		
A19	RP31	D17/MD17/HD17	TOUTD9	TIND9	RP31_RESERVED4		
B20	RP32	D18/MD18/HD18	TOUTD10	TIND10	RP32_RESERVED4		
B19	RP33	D19/MD19/HD19	TOUTD11	TIND11	RP33_RESERVED4		
B18	RP34	D20/MD20/HD20	TOUTD12	TIND12	RP34_RESERVED4		
B17	RP35	D21/MD21/HD21	TOUTD13	TIND13	RP35_RESERVED4		
C18	RP36	D22/MD22/HD22	TOUTD14	TIND14	RP36_RESERVED4		
C19	RP37	D23/HD23	TOUTD15	TIND15	RP37_RESERVED4		

*1: Enabling the TAUJ2 or TAUD pin functions is selectable by using the TMISEL register.
For details, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

*2: The multiplexed function is enabled while BUS32EN=1.

*3: The multiplexed function is enabled while BUS32EN=0.

5.2.2 Ethernet pins

Table 5.2.2-1 Ethernet Pins

Pin ID	Function Name	Pin Name	I/O	Description	Active	Level during Reset	I/O Standby
K2	P0_D0N	P0_D0N	I/O	PHY 0 Tx/Rx channel A negative signal	-	-	-
K1	P0_D0P	P0_D0P	I/O	PHY 0 Tx/Rx channel A positive signal	-	-	-
J2	P0_D1N	P0_D1N	I/O	PHY 0 Tx/Rx channel B negative signal	-	-	-
J1	P0_D1P	P0_D1P	I/O	PHY 0 Tx/Rx channel B positive signal	-	-	-
H2	P0_D2N	P0_D2N	I/O	PHY 0 Tx/Rx channel C negative signal	-	-	-
H1	P0_D2P	P0_D2P	I/O	PHY 0 Tx/Rx channel C positive signal	-	-	-
G2	P0_D3N	P0_D3N	I/O	PHY 0 Tx/Rx channel D negative signal	-	-	-
G1	P0_D3P	P0_D3P	I/O	PHY 0 Tx/Rx channel D positive signal	-	-	-
U2	P1_D0N	P1_D0N	I/O	PHY 1 Tx/Rx channel A negative signal	-	-	-
U1	P1_D0P	P1_D0P	I/O	PHY 1 Tx/Rx channel A positive signal	-	-	-
T2	P1_D1N	P1_D1N	I/O	PHY 1 Tx/Rx channel B negative signal	-	-	-
T1	P1_D1P	P1_D1P	I/O	PHY 1 Tx/Rx channel B positive signal	-	-	-
R2	P1_D2N	P1_D2N	I/O	PHY 1 Tx/Rx channel C negative signal	-	-	-
R1	P1_D2P	P1_D2P	I/O	PHY 1 Tx/Rx channel C positive signal	-	-	-
P2	P1_D3N	P1_D3N	I/O	PHY 1 Tx/Rx channel D negative signal	-	-	-
P1	P1_D3P	P1_D3P	I/O	PHY 1 Tx/Rx channel D positive signal	-	-	-
D5	PHYADD1	PHYADD1	I	PHY address bit 1	-	-	-
D4	PHYADD2	PHYADD2	I	PHY address bit 2	-	-	-
D3	PHYADD3	PHYADD3	I	PHY address bit 3	-	-	-
C2	PHYADD4	PHYADD4	I	PHY address bit 4	-	-	-
M2	REF_FILT	REF_FILT	I/O	Reference voltage setting for differential transmission system (external connection to 1μF capacitor)	-	-	-
M1	REF_REXT	REF_REXT	I/O	Reference voltage setting for differential transmission system (external connection to 2kΩ resistor)	-	-	-
J6, J7, P6, P7	VDD1	VDD1	-	PHY 1.0-V digital power supply	-	-	-
K3, L3	VDD1A	VDD1A	-	PHY 1.0-V analog power supply	-	-	-
N3, P3, R3	VDD25A	VDD25A	-	PHY 2.5-V analog power supply	-	-	-
J8, P8, J9, K9, L9, M9, N9, P9	VDD33_ GPHY	VDD33_ GPHY	-	PHY 3.3-V I/O power supply	-	-	-
B2	PHY0_ LED0	PHY0_ LED0	O	GbE-PHY LED0_PHY0 output signal	Low	High	-
AA2	PHY1_ LED0	PHY1_ LED0	O	GbE-PHY LED0_PHY1 output signal	Low	High	-

5.2.3 External SRAM interface pins

Usage of the external SRAM interface pins is exclusive. This is selected by the level on the MEMIFSEL pin (Setting value: Low level for the external SRAM interface pins and High level for the external MCU interface pins).

(1) When the asynchronous SRAM memory controller is selected (MEMCSEL = 0)
The external memory interface pins other than BUSCLK are inputs as long as the internal reset signal (HRESETZ) is active.

Table 5.2.3-1 External SRAM Interface Pins
(When Asynchronous SRAM Memory Controller is Selected (MEMCSEL = 0))

Pin ID	Function Name	Pin Name	I/O	Description	Active	Level during Reset	I/O Standby
A18	BUSCLK	BUSCLK	O	Bus clock output	-	Clock output	Hi-Z
C13	CSZ0	CSZ0	O	Chip select signal output	Low	Hi-Z (High)	High
B8	CSZ1	P44	O	Chip select signal output	Low	Hi-Z (High)	*2
B11	CSZ2	P13	O				
B12	CSZ3	P12	O				
A4	A1	P40	O	Address output	-	Hi-Z (High)	*2
A3, B3, C3, B4, C4, B5, C5, C6, D6, C7, D7, C8, D8, C9, D9, C10, D11, D12, D13	A2-A20	A2-A20	O	Address output	-	Hi-Z (Low)	Hi-Z
C22, C21, D22, D21, E22, E21, F22	A21-A27	RP21-RP27	O	Address output		Hi-Z (High)	*2
A14, B14, A15, B15, A16, B16, A17, C14, D14, C15, D15, C16, D16, C17, D17, D18	D0-D15	D0-D15	I/O	Data bus		Hi-Z (Low)	Hi-Z
A20, A19, B20, B19, B18, B17, C18, C19, C20, D20, E20, F20, D19, E19, F19, G19	D16-D31	RP30-RP37, RP10-RP17	I/O	Data bus		Hi-Z (High)	*2
A13	RDZ	RDZ	O	Read strobe output	Low	Hi-Z (High)	High
B13	WRSTBZ	WRSTBZ	O	Write strobe output			
C11	WRZ0 / BENZ0*1	WRZ0	O	Valid byte lane strobe output			
C12	WRZ1 / BENZ1*1	WRZ1	O				
H19	WRZ2 / BENZ2*1	RP06	O				*2
G20	WRZ3 / BENZ3*1	RP07	O				
B6	WAITZ	P41	I	Wait signal input			*2
B21	BCYSTZ	RP20	O	Bus cycle start status output			

*1: The WREN register is used to switch pin functions between WRZ3 to WRZ0 and BENZ3 to BENZ0.
For details, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

*2: For the state during I/O standby, refer to Section 5.2.1 "Port pins and real-time port pins".

(2) When the synchronous burst access memory controller is selected (MEMCSEL = 1)
The external memory interface pins other than BUSCLK are inputs as long as the internal reset signal (HRESETZ) is active.

Table 5.2.3-2 External SRAM Interface Pins
(When Synchronous Burst Access Memory Controller is Selected (MEMCSEL = 1))

Pin ID	Function Name	Pin Name	I/O	Description	Active	Level during Reset	I/O Standby
A18	BUSCLK	BUSCLK	O	Bus clock output	-	Clock output	Hi-Z
C13	CSZ0	CSZ0	O	Chip select signal output	Low	Hi-Z (High)	High
B8	CSZ1	P44	O	Chip select signal output	Low	Hi-Z (High)	*3
B11	CSZ2	P13	O				
B12	CSZ3	P12	O				
A4	MA0	P40	O	Address output	-	Hi-Z (High)	*3
A3, B3, C3, B4, C4, B5, C5, C6, D6, C7, D7, C8, D8, C9, D9, C10, D11, D12, D13	MA1-MA19	A2-A20	O	Address output	-	Hi-Z (Low)	Hi-Z
C22, C21, D22, D21, E22, E21, F22	MA20-MA26	RP21-RP27	O	Address output		Hi-Z (High)	*3
A14, B14, A15, B15, A16, B16, A17, C14, D14, C15, D15, C16, D16, C17, D17, D18	MD0-MD15 / MA0-MA15*1	D0-D15	I/O	Data bus		Hi-Z (Low)	Hi-Z
A20, A19, B20, B19, B18, B17, C18, C19, C20, D20, E20, F20, D19, E19, F19, G19	MD16-MD31 / MA16-MA31*1	RP30-RP37, RP10-RP17	I/O	Data bus		Hi-Z (High)	*3
A13	RDZ	RDZ	O	Read strobe output	Low	Hi-Z (High)	High
B13	WRSTBZ	WRSTBZ	O	Write strobe output			
C11	WRZ0 / BENZ0*2	WRZ0	O	Valid byte lane strobe output			
C12	WRZ1 / BENZ1*2	WRZ1	O				
H19	WRZ2 / BENZ2*2	RP06	O				*3
G20	WRZ3 / BENZ3*2	RP07	O				
B6	WAITZ	P41	I	Wait signal input			*3
A7, B7, A8	WAITZ1-WAITZ3	P45-P47	I	Wait signal input			
B21	ADVZ	RP20	O	Bus cycle start status output			

*1: If the ADMUXMODE pin is at the High level, these pin functions are multiplexed with address pin functions.
ADMUXMODE = 0: MD0-MD31 (separated address and data lines)
ADMUXMODE = 1: MD0-MD31/MA0-MA31 (multiplexed address and data lines)
*2: The SET_OPMODE register is used to switch pin functions between WRZ3 to WRZ0 and BENZ3 to BENZ0.
For details, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".
*3: For the state during I/O standby, refer to Section 5.2.1 "Port pins and real-time port pins".

5.2.4 External MCU interface pins

Usage of the external MCU interface pins is exclusive. This is selected by the level on the MEMIFSEL pin (Setting value: Low level for the external SRAM interface pins and High level for the external MCU interface pins).

(1) When the asynchronous SRAM memory controller is selected (MEMCSEL = 0)
The external MCU interface pins continue to operate even during a reset.

Table 5.2.4-1 External MCU Interface Pins
(When Asynchronous SRAM Memory Controller is Selected (MEMCSEL = 0))

Pin ID	Function Name	Pin Name	I/O	Description	Active	Level during Reset	I/O Standby
A6	HBUSCLK*1	P43	I	Bus clock input	-	Hi-Z (High)	High
C13	HCSZ	CSZ0	I	Chip select signal input	Low		
B8	HPGCSZ	P44	I	Page ROM mode chip select signal input	Low	Hi-Z (High)	*3
B6	HWAITZ	P41	O	Wait signal output			
A4	HA1	P40	I	Address signal input	-	Hi-Z (High)	*3
A3, B3, C3, B4, C4, B5, C5, C6, D6, C7, D7, C8, D8, C9, D9, C10, D11, D12, D13	HA2-HA20	A2-A20	I	Address signal input	-	Hi-Z (Low)	Hi-Z
A14, B14, A15, B15, A16, B16, A17, C14, D14, C15, D15, C16, D16, C17, D17, D18	HD0-HD15	D0-D15	I/O	Data bus			
A20, A19, B20, B19, B18, B17, C18, C19, C20, D20, E20, F20, D19, E19, F19, G19	HD16-HD31	RP30-RP37, RP10-RP17	I/O	Data bus	-	Hi-Z (High)	*3
A13	HRDZ	RDZ	I	Read strobe input	Low	Hi-Z (High)	High
B13	HWRSTBZ	WRSTBZ	I	Write strobe input			
C11	HWRZ0 / HBENZ0*2	WRZ0	I	Valid byte lane strobe input	Low	Hi-Z (High)	High
C12	HWRZ1 / HBENZ1*2	WRZ1	I				
H19	HWRZ2 / HBENZ2*2	RP06	I				*3
G20	HWRZ3 / HBENZ3*2	RP07	I				
A5	HERROUTZ	P42	O	Error interrupt output	Low	High	*3
B21	HBCYSTZ	RP20	I	Bus cycle input		Hi-Z (High)	

*1: HBUSCLK is used in case of Synchronous SRAM supported MCU connection mode (HIFSYNC pin is High).
The HBUSCLK pin is not used in case of asynchronous SRAM supported MCU connection mode (HIFSYNC pin is Low).
Further, the other signal connection is common in each mode.
For details on the connection example, refer to the "R-IN32M4-CL2 User's Manual: Board Design".

*2: The level being input on the HWRZSEL pin controls switching between the HWRZ3 to HWRZ0 and HBENZ3 to HBENZ0 signals.

*3: For the state during I/O standby, refer to Section 5.2.1 "Port pins and real-time port pins".

(2) When the synchronous burst access memory controller is selected (MEMCSEL = 1)
The external MCU interface pins continue to operate even during a reset.

Table 5.2.4-2 External MCU Interface Pins
(When Synchronous Burst Access Memory Controller is Selected (MEMCSEL = 1))

Pin ID	Function Name	Pin Name	I/O	Description	Active	Level during Reset	I/O Standby
A6	HBUSCLK	P43	I	Bus clock input	-	Hi-Z (High)	High
C13	HCSZ	CSZ0	I	Chip select signal input	Low		
B8	HPGCSZ	P44	I	Page ROM mode chip select signal input	Low	Hi-Z (High)	*3
B6	HWAITZ	P41	O	Wait signal output			
A4	HA1*1	P40	I	Address signal input	-	Hi-Z (High)	*3
A3, B3, C3, B4, C4, B5, C5, C6, D6, C7, D7, C8, D8, C9, D9, C10, D11, D12, D13	HA2-HA20*1	A2-A20	I	Address signal input	-	Hi-Z (Low)	Hi-Z
A14, B14, A15, B15, A16, B16, A17, C14, D14, C15, D15, C16, D16, C17, D17, D18	HD0-HD15*1	D0-D15	I/O	Data bus			
A20, A19, B20, B19, B18, B17, C18, C19, C20, D20, E20, F20, D19, E19, F19, G19	HD16-HD31*1	RP30-RP37, RP10-RP17	I/O	Data bus	-	Hi-Z (High)	*3
A13	HRDZ	RDZ	I	Read strobe input	Low	Hi-Z (High)	High
B13	HWRSTBZ	WRSTBZ	I	Write strobe input			
C11	HWRZ0 / HBENZ0*2	WRZ0	I	Valid byte lane strobe input	Low	Hi-Z (High)	High
C12	HWRZ1 / HBENZ1*2	WRZ1	I				
H19	HWRZ2 / HBENZ2*2	RP06	I				*2
G20	HWRZ3 / HBENZ3*2	RP07	I				
A5	HERROUTZ	P42	O	Error interrupt output	Low	High	*2
B21	HBCYSTZ	RP20	I	Bus cycle input		Hi-Z (High)	

*1: The address/data pin connection is dependent on address/data multiplex mode ADMUXMODE pin is High) or address/data separate mode (ADMUXMODE pin is Low). For details on the connection example, refer to the "R-IN32M4-CL2 User's Manual: Board Design".
*2: Setting the HWRZSEL pin to 1 is prohibited while the setting of the MEMCSEL pin is 1.
*3: For the state during I/O standby, refer to Section 5.2.1 "Port pins and real-time port pins".

5.2.5 Serial flash ROM interface pins

The serial flash ROM interface pins are pins of the serial flash ROM memory controller. These pins support the following modes:

- Fast Read
- Fast Read Dual Output
- Fast Read Dual I/O
- Fast Read Quad Output
- Fast Read Quad I/O

Table 5.2.5-1 Serial Flash ROM Interface Pins

Pin ID	Function Name	Pin Name	I/O	Description	Active	Level during Reset	I/O Standby
A10	SMSCK	P14	O	Serial clock output signal for serial flash ROM	-	Hi-Z (High)	*1
B10	SMIO0	P15	I/O	Serial data I/O signal for serial flash ROM (Connected to the IO0 pin of serial flash ROM)			
A9	SMIO1	P16	I/O	Serial data I/O signal for serial flash ROM (Connected to the IO1 pin of serial flash ROM)			
A12	SMIO2	P10	I/O	Serial data I/O signal for serial flash ROM (Connected to the /WP(IO2) pin of serial flash ROM)			
A11	SMIO3	P11	I/O	Serial data I/O signal for serial flash ROM (Connected to the /HOLD(IO3) pin of serial flash ROM)			
B9	SMCSZ	P17	O	Chip select signal output for serial flash ROM	Low		

*1: For the state during I/O standby, refer to Section 5.2.1 "Port pins and real-time port pins".

5.2.6 DMA interface pins

"DMA interface pins" refers to the interface pins of the DMA controllers for the internal AHB bus.
There are two DMA controllers:
one with four internal channels and pins for two external interfaces,
and one with one internal channel and pins for one external interface.
*: Each interface is fixed to a specific channel and cannot be assigned to a desired channel.

Table 5.2.6-1 DMA Interface Pins

Pin ID	Function Name	Pin Name	I/O	Description	Active	Level during Reset	I/O Standby
V21	RTDMAREQZ	P62	I	RTDMAC DMA transfer request input	Low	Hi-Z (High)	*1
V22	RTDMAACKZ	P63	O	RTDMAC DMA acknowledge output			
U21	RTDMATCZ	P64	O	RTDMAC terminal count output			
U22	DMAREQZ0	P65	I	DMA transfer request input 0			
T21	DMAACKZ0	P66	O	DMA acknowledge output 0			
T22	DMATCZ0	P67	O	Terminal count output 0			
AA21	DMAREQZ1	P32	I	DMA transfer request input 1			
AA20	DMAACKZ1	P33	O	DMA acknowledge output 1			
AB19	DMATCZ1	P34	O	Terminal count output 1			

*1: For the state during I/O standby, refer to Section 5.2.1 "Port pins and real-time port pins".

5.2.7 External interrupt input pins

The chip has one non-maskable interrupt and 29 maskable interrupt input pins.

Table 5.2.7-1 External Interrupt Input Pins

Pin ID	Function Name	Pin Name	I/O	Description	Active	Level during Reset	I/O Standby
Y13	NMIZ	NMIZ	I	Non-maskable external	Low	Hi-Z (High)	High
AB10, AA10, AB9, AA9, AB8, AA8	INTPZ0-INTPZ5	P00-P05	I	Maskable external interrupt input	Low	Hi-Z (High)	*1
AB6	INTPZ6	P50					
AA6	INTPZ7	P51				Hi-Z (Low)	
AA19	INTPZ22	P35					
AA16	INTPZ24	P37					
N22, N21, N20	INTPZ8-INTPZ10	P22-P24				Hi-Z (High)	
AA13, AB12, AA12, AB11, AA11	INTPZ11-INTPZ15	P73-P77					
H22, H21, G22, G21, F21, H20	INTPZ16-INTPZ21	RP00-RP05					
AA17	INTPZ23	P36					
D21, E22, E21, F22	INTPZ25-INTPZ28	RP24-					

*1: For the state during I/O standby, refer to Section 5.2.1 "Port pins and real-time port pins".

5.2.8 Timer I/O pins

Table 5.2.8-1 Timer I/O Pins

Pin ID	Function Name	Pin Name	I/O	Description	Active	Level during Reset	I/O Standby
R21	TINJ0 / TOUTJ0*1	P27	I/O	Timer TAUJ2 I/O pin	-	Hi-Z (High)	*2
P21	TINJ1 / TOUTJ1*1	P26					
AA3	TINJ2 / TOUTJ2*1	P57					
AB5	TINJ3 / TOUTJ3*1	P52					
P20	TIND0 / TOUTD0	EXTP0	I/O	Timer TAUD I/O pin			
R20	TIND1 / TOUTD1	EXTP1					
T20	TIND2 / TOUTD2	EXTP2					
U20	TIND3 / TOUTD3	EXTP3					
R21	TIND4 / TOUTD4*1	P27					
P21	TIND5 / TOUTD5*1	P26					
AA3	TIND6 / TOUTD6*1	P57					
AB5	TIND7 / TOUTD7*1	P52					
A20	TIND8 / TOUTD8	RP30					
A19	TIND9 / TOUTD9	RP31					
B20	TIND10 / TOUTD10	RP32					
B19	TIND11 / TOUTD11	RP33					
B18	TIND12 / TOUTD12	RP34					
B17	TIND13 / TOUTD13	RP35					
C18	TIND14 / TOUTD14	RP36					
C19	TIND15 / TOUTD15	RP37					

*1: TINJ0-TINJ3 and TIND4-TIND7, and TOUTJ0-TOUTJ3 and TOUTD4-TOUTD7 are assigned as multiplexed functions of the same pins.
Use the TMISEL register to select the pin functions to be used.
For details, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules". If you are not using external pin functions such as the interval timer function of the internal clock, both TAUJ2 and TAUD can be used at the same time.

*2: For the state during I/O standby, refer to Section 5.2.1 "Port pins and real-time port pins".

Table 5.2.9-1 Watchdog Timer Output Pin

Pin ID	Function Name	Pin Name	I/O	Description	Active	Level during Reset	I/O Standby
P22, U20	WDTOUTZ	P25, EXTP3	O	Watchdog timer output pin	Low	Hi-Z (High)	*1

*1: For the state during I/O standby, refer to Section 5.2.1 "Port pins and real-time port pins".

(1) Watchdog timer connection information
The output configuration diagram of the watchdog timer is shown below.
When a pin is not used, refer to Section 5.6 "Buffer Type of Pins and Handling of Unused Pins", and handle the pin accordingly.

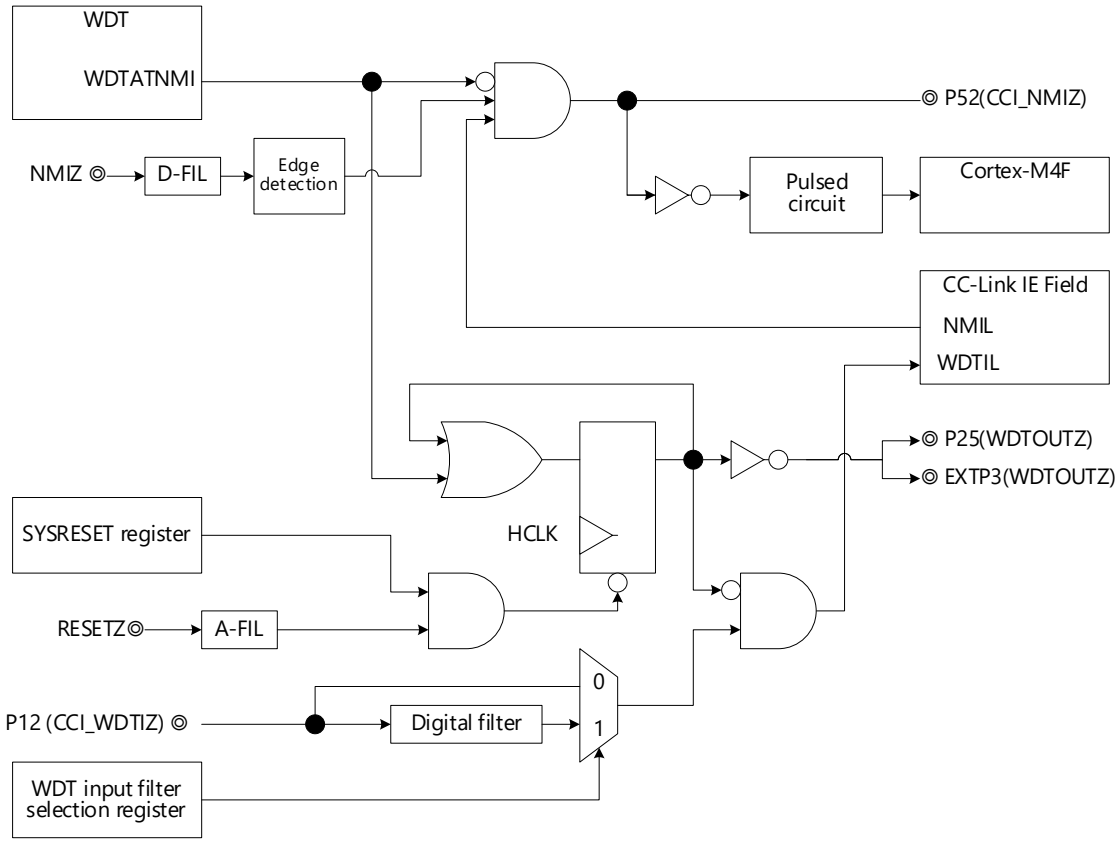


Figure 5.2.9-1 WDT Output (WDTARES/WDTATNMI) Configuration Diagram

Table 5.2.10-1 Serial Interface Pins

Pin ID	Function Name	Pin Name	I/O	Description	Active	Level during Reset	I/O Standby
M21	TXD0	P21	O	UART0 serial data output	-	Hi-Z (High)	*1
M22	RXD0	P20	I	UART0 serial data input			
Y21	TXD1	P31	O	UART1 serial data output			
Y22	RXD1	P30	I	UART1 serial data input			
A7	CSISCK0	P45	I/O	CSI0 serial clock input/output			
B7	CSISI0	P46	I	CSI0 serial data input			
A8	CSISO0	P47	O	CSI0 serial data output			
A5	CSICS00	P42	O	CSI0 chip select signal output 0	Low		
A6	CSICS01	P43	O	CSI0 chip select signal output 1			
AA19	CSISCK1	P35	I/O	CSI1 serial clock input/output	-	Hi-Z (Low)	
AA17	CSISI1	P36	I	CSI1 serial data input		Hi-Z (High)	
AA16	CSISO1	P37	O	CSI1 serial data output		Hi-Z (Low)	
AA15	CSICS10	P70	O	CSI1 chip select signal output 0	Low	Hi-Z (High)	
AA14	CSICS11	P71	O	CSI1 chip select signal output 1			
W22	SCL0	P60	I/O	I2C0 serial clock	-		
W21	SDA0	P61	I/O	I2C0 serial data			
H22	SCL1	RP00	I/O	I2C1 serial clock			
H21	SDA1	RP01	I/O	I2C1 serial data			

*1: For the state during I/O standby, refer to Section 5.2.1 "Port pins and real-time port pins".

5.2.11 CC-Link IE Field pins

Table 5.2.11-1 CC-Link IE Field Pins

Pin ID	Function Name	Pin Name	I/O	Description	Active	Level during Reset	I/O Standby
AB10	CCI_RUNLEDZ	P00	O	RUN LED output	Low	Hi-Z (High)	*1
AA10	CCI_USER1LEDZ	P01	O	USER LED1 output			
AB9	CCI_DLINKLEDZ	P02	O	D LINK LED output			
AA9	CCI_ERRLEDZ	P03	O	ERR.LED output			
AB8	CCI_LERR0LEDZ	P04	O	L ER1 LED output			
AA8	CCI_LERR1LEDZ	P05	O	L ER2 LED output			
AB7	CCI_SDLEDZ	P06	O	SD LED output			
AA7	CCI_RDLEDZ	P07	O	RD LED output			
AB6	CCI_USER2LEDZ	P50	O	USER LED2 output			
AB5	CCI_NMIZ	P52	O	Output NMI interrupt to external MCU	Low	Hi-Z (High)	
B12	CCI_WDTIZ	P12	I	Input from external WDT			
AA5	CCI_INTZ	P53	O	Output interrupt signal to external MCU	Low	Hi-Z (High)	
AB18	CCI_CLK2_097M	CCI_CLK2_097M	I	2.097152MHz clock (crystal oscillator)	-	-	Hi-Z

*1: For the state during I/O standby, refer to Section 5.2.1 "Port pins and real-time port pins".

Table 5.2.12-1 System Pins

Pin ID	Pin Name	I/O	Description	Active	Level during Reset	I/O Standby
AB14	XT1	I	Clock input pin ・ OSCTH = 1: Oscillator is in use. XT1 and XT2 are respectively connected to GND and oscillator. ・ OSCTH = 0: Resonator is in use. XT1 and XT2 are connected to resonator.	-	-	-
AB15	XT2	I/O		-	-	
AB20	RESETZ	I	Reset input	Low	-	
Y20	PONRZ	I	Internal RAM power-on reset input	Low	-	
W20	HOTRESETZ	I	Hot reset input	Low	-	
W13	OSCTH	I	External clock input mode setting 0: Resonator connection mode 1: External clock input mode	High	-	Hi-Z
Y8	JTAGSEL	I	JTAG pin operating mode setting 0: Cortex-M4F JTAG mode 1: B-SCAN JTAG mode	-	-	
Y19	RSTOUTZ	O	External reset output	Low	Low	
P18, V17	PLL_VDD	-	PLL power supply (1.0V)	-	-	-
R18, V16	PLL_GND	-	PLL GND	-	-	
K18, L18, F12, F14, F16, F17, F18, G12, H18, J12, L12, M12, P12, T12, T19, U12, U13, U16, U17, U18	VDD33	-	I/O power supply (3.3V)	-	-	
H13, H14, H15, H16, H17, J13, J17, K13, K17, L13, L17, M13, M17, N13, N17, P13, P17, R13, R14, R15, R16, R17	VDD10	-	Internal power supply (1.0V)	-	-	

Pin ID	Pin Name	I/O	Description	Active	Level during Reset	I/O Standby
A1, A2, A21, A22, B1, B22, C1, D1, D2, D10, E1, E2, E3, E4, E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, E16, E18, F1, F2, F3, F6, F7, F8, F9, F10, F11, F13, F15, G3, G6, G7, G8, G9, G10, G11, G13, G14, G15, G16, G17, G18, H3, H6, H7, H8, H9, H10, H11, H12, J3, J4, J10, J11, J14, J15, J16, J18, K4, K5, K6, K7, K8, K10, K11, K12, K14, K15, K16, L1, L2, L4, L5, L6, L7, L8, L11, L14, L15, L16, M3, M4, M5, M6, M7, M8, M10, M11, M14, M15, M16, M18, N1, N2, N4, N5, N6, N7, N8, N10, N11, N12, N14, N15, N16, N18, P4, P10, P11, P14, P15, P16, R6, R7, R8, R9, R10, R11, R12, T3, T6, T7, T8, T9, T10, T11, T13, T14, T15, T16, T17, T18, U3, U7, U8, U9, U10, U11, U14, U15, V1, V2, V3, V4, V5, V6, V7, V8, V9, V10, V11, V12, V13, V14, V15, W1, W2, W3, W10, W12, Y1, Y2, Y3, AA1, AA18, AA22, AB1, AB2, AB16, AB21, AB22	GND	-	Power supply ground voltage (GND)	-	-	
E17	CTRSTBYB*1	I	I/O standby control	Low	-	
V18	ETHTEST	I	Connect the pin to GND.	-	-	

*1: Deassert the CTRSYBYB pin simultaneously with PONRZ. For details, refer to Section 4.9 "I/O Standby Function".

5.2.13 Trace pins

Table 5.2.13-1 Trace Pins

Pin ID	Function Name	Pin Name	I/O	Description	Active	Level during Reset	I/O Standby
Y12	TRACECLK	TRACECLK	O	Trace port clock output	-	-	Hi-Z
Y9	TRACEDATA3*1	TRACEDATA3	O	Trace port data output	-	Hi-Z (High)	High
Y10	TRACEDATA2*1	TRACEDATA2	O				
W11	TRACEDATA1*1	TRACEDATA1	O				
Y11	TRACEDATA0*1	TRACEDATA0	O				

*1: The initial setting is for input and the pin is switched from input to output in 20 BUSCLK cycles after the RSTOUTZ pin has been deasserted in response to release from the reset state.

5.2.14 CPU power control pin

Table 5.2.14-1 CPU Power Control Pin

Pin ID	Function Name	Pin Name	I/O	Description	Active	Level during Reset	I/O Standby
AB13	SLEEPING	P72	O	CPU core sleep mode output	High	Hi-Z (High)	*1

*1: For the state during I/O standby, refer to Section 5.2.1 "Port pins and real-time port pins".

5.2.15 Test pins

Table 5.2.15-1 Test Pins

Pin ID	Function Name	Pin Name	I/O	Description	Active	Level during Reset	I/O Standby
W5	TMS	TMS	I/O	Mode select signal	-	-	-
W6	TDI	TDI	I	Serial data input	-	-	-
W8	TDO	TDO	O	Serial data output	-	-	-
W9	TRSTZ	TRSTZ	I	Reset signal	Low	-	-
W7	TCK	TCK	I	Clock signal (JTAG clock)	-	-	-

5.2.16 Operating mode setting pins

The operating mode setting pins set the CP520 boot mode as well as operating modes such as those of the external memory interface and memory controller.

Table 5.2.16-1 Operating Mode Setting Pins

Pin ID	Function Name	Pin Name	I/O	Description	Active	Level during Reset	I/O Standby
Y17	BOOT1	BOOT1	I	Boot mode selection 00: External memory boot 01: External serial flash ROM boot 10: External MCU boot 11: Instruction RAM boot (only available for debugging)	-	-	-
Y18	BOOT0	BOOT0	I		-	-	-
W18	MEMIFSEL	MEMIFSEL	I	External memory interface selection 0: Slave memory interface 1: External MCU interface	-	-	-
U19	MEMCSEL	MEMCSEL	I	Internal memory controller selection 0: Asynchronous SRAM memory controller 1: Synchronous burst access memory controller	-	-	-
W19	BUS32EN	BUS32EN	I	External memory interface bus width selection 0: 16-bit bus 1: 32-bit bus	-	-	-
W17	HIFSYNC	HIFSYNC	I	External MCU interface operating mode selection 0: Asynchronous SRAM interface 1: Synchronous SRAM interface	-	-	-
V20	HWRZSEL	HWRZSEL	I	External MCU interface HWRZ/HBENZ selection 0: Used as HBENZ 1: Used as HWRZ	-	-	-
V19	ADMUXMODE	ADMUXMODE	I	Multiplexing of address and data lines 0: Separate address and data lines 1: Multiplexed address and data lines	-	-	-

The setting state can be confirmed using the operating mode monitor register (MDMNT).
For details on the operating mode monitor register, refer to Section 9.9 "Operating Mode Monitor Register (MDMNT)".

The combinations of available operating mode setting pins in CP520 are as follows.
Do not set any combination of operating mode setting pins other than the below.

Table 5.2.16-2 Combinations of Operating Mode Setting Pins

Boot Mode	External Memory Boot				External MCU Boot				External Serial Flash ROM Boot							
External memory interface	Slave memory interface				External MCU interface				Slave memory interface				External MCU interface			
Memory controller type	Asynchronous		Synchronous		Asynchronous		Synchronous		Asynchronous		Synchronous		Asynchronous		Synchronous	
External bus width	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit
BOOT1-0	00	00	00	00	10	10	10	10	01	01	01	01	01	01	01	01
MEMIFSEL	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
MEMCSEL	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
BUS32EN	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HIFSYNC	0	0	0	0	*1	*1	1	1	0	0	0	0	*1	*1	1	1
HWRZSEL	0	0	0	0	*2	*2	0	0	0	0	0	0	*2	*2	0	0
ADMUXMODE	0	0	*3	*3	0	0	*3	*3	0	0	*3	*3	0	0	*3	*3

*1: The external MCU interface function is selectable by the level on the HIFSYNC pin.
HIFSYNC = 0: Asynchronous SRAM supported MCU connection mode
HIFSYNC = 1: Synchronous SRAM supported MCU connection mode
For details, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

*2: The external MCU interface HWRZ or HBENZ is selectable by the level on the HWRZSEL pin.
For details, refer to Section 5.2.4 "External MCU interface pins", (1) When the asynchronous SRAM memory controller is selected (MEMCSEL = 0).

*3: Multiplexing of address and data lines is selectable by the level on the ADMUXMODE pin.
For details, refer to Section 5.2.3 "External SRAM interface pins",(2) When the synchronous burst access memory controller is selected (MEMCSEL = 1).

Remarks

The combination of operating mode setting pins used to select booting for instruction RAM (BOOT1-0 = 11) is the same as that for booting from external memory (BOOT1-0 = 00).
Asynchronous: asynchronous SRAM memory controller (MEMCSEL = 0)
Synchronous: synchronous burst access memory controller (MEMCSEL = 1)

5.3 Pin States

The initial state of the port functions after release from the reset state differs depending on the state of the operating mode setting pins.
For the state of the operating mode setting pins in each boot mode and the supported combinations, refer to Section 5.2.16 "Operating mode setting pins".

5.3.1 Pin states when booting is from external memory

The list of pin states is given below.
Entries in shaded cells shaded indicate multiplexed pin functions that are enabled in the initial state.
The initial state of booting for instruction RAM is the same as that for booting from external memory.

Table 5.3.1-1 Pin States when Booting is from External Memory

Pin Name	External Memory Boot (BOOT1-0 = 00)			
	Slave Memory Interface (MEMIFSEL = 0)			
	Asynchronous SRAM memory controller (MEMCSEL = 0)		Synchronous burst access memory controller (MEMCSEL = 1)	
	16bit (BUS32EN = 0)	32bit (BUS32EN = 1)	16bit (BUS32EN = 0)	32bit (BUS32EN = 1)
P00	P00	P00	P00	P00
P01	P01	P01	P01	P01
P02	P02	P02	P02	P02
P03	P03	P03	P03	P03
P04	P04	P04	P04	P04
P05	P05	P05	P05	P05
P06	P06	P06	P06	P06
P07	P07	P07	P07	P07
P10	P10	P10	P10	P10
P11	P11	P11	P11	P11
P12	P12	P12	P12	P12
P13	P13	P13	P13	P13
P14	P14	P14	P14	P14
P15	P15	P15	P15	P15
P16	P16	P16	P16	P16
P17	P17	P17	P17	P17
P20	P20	P20	P20	P20
P21	P21	P21	P21	P21
P22	P22	P22	P22	P22
P23	P23	P23	P23	P23
P24	P24	P24	P24	P24
P25	P25	P25	P25	P25
P26	P26	P26	P26	P26
P27	P27	P27	P27	P27
P30	P30	P30	P30	P30
P31	P31	P31	P31	P31
P32	P32	P32	P32	P32
P33	P33	P33	P33	P33
P34	P34	P34	P34	P34
P35	P35	P35	P35	P35
P36	P36	P36	P36	P36
P37	P37	P37	P37	P37
P40	A1	P40	MA0	MA0
P41	P41	P41	P41	P41
P42	P42	P42	P42	P42
P43	P43	P43	P43	P43
P44	P44	P44	P44	P44
P45	P45	P45	P45	P45
P46	P46	P46	P46	P46
P47	P47	P47	P47	P47
P50	P50	P50	P50	P50
P51	P51	P51	P51	P51
P52	P52	P52	P52	P52
P53	P53	P53	P53	P53

Pin Name	External Memory Boot (BOOT1-0 = 00)			
	Slave Memory Interface (MEMIFSEL = 0)			
	Asynchronous SRAM memory controller (MEMCSEL = 0)		Synchronous burst access memory controller (MEMCSEL = 1)	
	16bit (BUS32EN = 0)	32bit (BUS32EN = 1)	16bit (BUS32EN = 0)	32bit (BUS32EN = 1)
P54	P54	P54	P54	P54
P55	P55	P55	P55	P55
P56	P56	P56	P56	P56
P57	P57	P57	P57	P57
P60	P60	P60	P60	P60
P61	P61	P61	P61	P61
P62	P62	P62	P62	P62
P63	P63	P63	P63	P63
P64	P64	P64	P64	P64
P65	P65	P65	P65	P65
P66	P66	P66	P66	P66
P67	P67	P67	P67	P67
P70	P70	P70	P70	P70
P71	P71	P71	P71	P71
P72	P72	P72	P72	P72
P73	P73	P73	P73	P73
P74	P74	P74	P74	P74
P75	P75	P75	P75	P75
P76	P76	P76	P76	P76
P77	P77	P77	P77	P77
EXTP0	EXTP0_RESERVED1	EXTP0_RESERVED1	EXTP0_RESERVED1	EXTP0_RESERVED1
EXTP1	EXTP1_RESERVED1	EXTP1_RESERVED1	EXTP1_RESERVED1	EXTP1_RESERVED1
EXTP2	EXTP2_RESERVED1	EXTP2_RESERVED1	EXTP2_RESERVED1	EXTP2_RESERVED1
EXTP3	EXTP3	EXTP3	EXTP3	EXTP3
EXTP4	EXTP4_RESERVED1	EXTP4_RESERVED1	EXTP4_RESERVED1	EXTP4_RESERVED1
EXTP5	EXTP5	EXTP5	EXTP5	EXTP5
EXTP6	EXTP6	EXTP6	EXTP6	EXTP6
EXTP7	EXTP7	EXTP7	EXTP7	EXTP7
EXTP8	EXTP8_RESERVED1	EXTP8_RESERVED1	EXTP8_RESERVED1	EXTP8_RESERVED1
EXTP9	EXTP9_RESERVED1	EXTP9_RESERVED1	EXTP9_RESERVED1	EXTP9_RESERVED1
RP00	RP00	RP00	RP00	RP00
RP01	RP01	RP01	RP01	RP01
RP02	RP02	RP02	RP02	RP02
RP03	RP03	RP03	RP03	RP03
RP04	RP04	RP04	RP04	RP04
RP05	RP05_RESERVED4	RP05_RESERVED4	RP05_RESERVED4	RP05_RESERVED4
RP06	RP06	WRZ2	RP06	WRZ2
RP07	RP07	WRZ3	RP07	WRZ3
RP10	RP10	D24	RP10	MD24
RP11	RP11	D25	RP11	MD25
RP12	RP12	D26	RP12	MD26
RP13	RP13	D27	RP13	MD27
RP14	RP14	D28	RP14	MD28
RP15	RP15	D29	RP15	MD29
RP16	RP16	D30	RP16	MD30
RP17	RP17	D31	RP17	MD31
RP20	RP20	RP20	ADVZ	ADVZ
RP21	RP21	RP21	RP21	RP21
RP22	RP22	RP22	RP22	RP22
RP23	RP23	RP23	RP23	RP23
RP24	RP24	RP24	RP24	RP24
RP25	RP25	RP25	RP25	RP25
RP26	RP26	RP26	RP26	RP26
RP27	RP27	RP27	RP27	RP27
RP30	RP30	D16	RP30	MD16
RP31	RP31	D17	RP31	MD17

Pin Name	External Memory Boot (BOOT1-0 = 00)			
	Slave Memory Interface (MEMIFSEL = 0)			
	Asynchronous SRAM memory controller (MEMCSEL = 0)		Synchronous burst access memory controller (MEMCSEL = 1)	
	16bit (BUS32EN = 0)	32bit (BUS32EN = 1)	16bit (BUS32EN = 0)	32bit (BUS32EN = 1)
RP32	RP32	D18	RP32	MD18
RP33	RP33	D19	RP33	MD19
RP34	RP34	D20	RP34	MD20
RP35	RP35	D21	RP35	MD21
RP36	RP36	D22	RP36	MD22
RP37	RP37	D23	RP37	MD23

5.3.2 Pin states when booting is from external serial flash ROM

The list of pin states is given below.
Entries in shaded cells shaded indicate multiplexed pin functions that are enabled in the initial state.
The initial state of booting for instruction RAM is the same as that for booting from external memory.

Remarks
Asynchronous type: asynchronous SRAM memory controller (MEMCSEL = 0)
Synchronous type: synchronous burst access memory controller (MEMCSEL = 1)
16 bit: 16-bit bus width of the external memory interface (BUS32EN = 0)
32 bit: 32-bit bus width of the external memory interface (BUS32EN = 1)

Table 5.3.2-1 Pin States when Booting is from External Serial Flash ROM

Pin Name	External Serial Flash ROM Boot (BOOT1-0 = 01)							
	Slave Memory Interface (MEMIFSEL = 0)				External MCU Interface (MEMIFSEL = 1)			
	Asynchronous type		Synchronous type		Asynchronous type		Synchronous type	
	16bit	32bit	16bit	32bit	16bit	32bit	16bit	32bit
P00	P00	P00	P00	P00	P00	P00	P00	P00
P01	P01	P01	P01	P01	P01	P01	P01	P01
P02	P02	P02	P02	P02	P02	P02	P02	P02
P03	P03	P03	P03	P03	P03	P03	P03	P03
P04	P04	P04	P04	P04	P04	P04	P04	P04
P05	P05	P05	P05	P05	P05	P05	P05	P05
P06	P06	P06	P06	P06	P06	P06	P06	P06
P07	P07	P07	P07	P07	P07	P07	P07	P07
P10	P10	P10	P10	P10	P10	P10	P10	P10
P11	P11	P11	P11	P11	P11	P11	P11	P11
P12	P12	P12	P12	P12	P12	P12	P12	P12
P13	P13	P13	P13	P13	P13	P13	P13	P13
P14	SMSCK	SMSCK	SMSCK	SMSCK	SMSCK	SMSCK	SMSCK	SMSCK
P15	SMIO0	SMIO0	SMIO0	SMIO0	SMIO0	SMIO0	SMIO0	SMIO0
P16	SMIO1	SMIO1	SMIO1	SMIO1	SMIO1	SMIO1	SMIO1	SMIO1
P17	SMCSZ	SMCSZ	SMCSZ	SMCSZ	SMCSZ	SMCSZ	SMCSZ	SMCSZ
P20	P20	P20	P20	P20	P20	P20	P20	P20
P21	P21	P21	P21	P21	P21	P21	P21	P21
P22	P22	P22	P22	P22	P22	P22	P22	P22
P23	P23	P23	P23	P23	P23	P23	P23	P23
P24	P24	P24	P24	P24	P24	P24	P24	P24
P25	P25	P25	P25	P25	P25	P25	P25	P25
P26	P26	P26	P26	P26	P26	P26	P26	P26
P27	P27	P27	P27	P27	P27	P27	P27	P27
P30	P30	P30	P30	P30	P30	P30	P30	P30
P31	P31	P31	P31	P31	P31	P31	P31	P31
P32	P32	P32	P32	P32	P32	P32	P32	P32
P33	P33	P33	P33	P33	P33	P33	P33	P33
P34	P34	P34	P34	P34	P34	P34	P34	P34
P35	P35	P35	P35	P35	P35	P35	P35	P35
P36	P36	P36	P36	P36	P36	P36	P36	P36
P37	P37	P37	P37	P37	P37	P37	P37	P37
P40	A1	P40	MA0	MA0	HA1	HA1	HA1	HA1
P41	P41	P41	P41	P41	HWAITZ	HWAITZ	HWAITZ	HWAITZ
P42	P42	P42	P42	P42	HERROUTZ	HERROUTZ	HERROUTZ	HERROUTZ
P43	P43	P43	P43	P43	HBUSCLK	HBUSCLK	HBUSCLK	HBUSCLK
P44	P44	P44	P44	P44	HPGCSZ	HPGCSZ	HPGCSZ	HPGCSZ
P45	P45	P45	P45	P45	P45	P45	P45	P45
P46	P46	P46	P46	P46	P46	P46	P46	P46
P47	P47	P47	P47	P47	P47	P47	P47	P47
P50	P50	P50	P50	P50	P50	P50	P50	P50
P51	P51	P51	P51	P51	P51	P51	P51	P51
P52	P52	P52	P52	P52	P52	P52	P52	P52
P53	P53	P53	P53	P53	P53	P53	P53	P53
P54	P54	P54	P54	P54	P54	P54	P54	P54

Pin Name	External Serial Flash ROM Boot (BOOT1-0 = 01)							
	Slave Memory Interface (MEMIFSEL = 0)				External MCU Interface (MEMIFSEL = 1)			
	Asynchronous type		Synchronous type		Asynchronous type		Synchronous type	
	16bit	32bit	16bit	32bit	16bit	32bit	16bit	32bit
P55	P55	P55	P55	P55	P55	P55	P55	P55
P56	P56	P56	P56	P56	P56	P56	P56	P56
P57	P57	P57	P57	P57	P57	P57	P57	P57
P60	P60	P60	P60	P60	P60	P60	P60	P60
P61	P61	P61	P61	P61	P61	P61	P61	P61
P62	P62	P62	P62	P62	P62	P62	P62	P62
P63	P63	P63	P63	P63	P63	P63	P63	P63
P64	P64	P64	P64	P64	P64	P64	P64	P64
P65	P65	P65	P65	P65	P65	P65	P65	P65
P66	P66	P66	P66	P66	P66	P66	P66	P66
P67	P67	P67	P67	P67	P67	P67	P67	P67
P70	P70	P70	P70	P70	P70	P70	P70	P70
P71	P71	P71	P71	P71	P71	P71	P71	P71
P72	P72	P72	P72	P72	P72	P72	P72	P72
P73	P73	P73	P73	P73	P73	P73	P73	P73
P74	P74	P74	P74	P74	P74	P74	P74	P74
P75	P75	P75	P75	P75	P75	P75	P75	P75
P76	P76	P76	P76	P76	P76	P76	P76	P76
P77	P77	P77	P77	P77	P77	P77	P77	P77
EXTP0	EXTP0_ RESERVED1	EXTP0_ RESERVED1	EXTP0_ RESERVED1	EXTP0_ RESERVED1	EXTP0_ RESERVED1	EXTP0_ RESERVED1	EXTP0_ RESERVED1	EXTP0_ RESERVED1
EXTP1	EXTP1_ RESERVED1	EXTP1_ RESERVED1	EXTP1_ RESERVED1	EXTP1_ RESERVED1	EXTP1_ RESERVED1	EXTP1_ RESERVED1	EXTP1_ RESERVED1	EXTP1_ RESERVED1
EXTP2	EXTP2_ RESERVED1	EXTP2_ RESERVED1	EXTP2_ RESERVED1	EXTP2_ RESERVED1	EXTP2_ RESERVED1	EXTP2_ RESERVED1	EXTP2_ RESERVED1	EXTP2_ RESERVED1
EXTP3	EXTP3	EXTP3	EXTP3	EXTP3	EXTP3	EXTP3	EXTP3	EXTP3
EXTP4	EXTP4_ RESERVED1	EXTP4_ RESERVED1	EXTP4_ RESERVED1	EXTP4_ RESERVED1	EXTP4_ RESERVED1	EXTP4_ RESERVED1	EXTP4_ RESERVED1	EXTP4_ RESERVED1
EXTP5	EXTP5	EXTP5	EXTP5	EXTP5	EXTP5	EXTP5	EXTP5	EXTP5
EXTP6	EXTP6	EXTP6	EXTP6	EXTP6	EXTP6	EXTP6	EXTP6	EXTP6
EXTP7	EXTP7	EXTP7	EXTP7	EXTP7	EXTP7	EXTP7	EXTP7	EXTP7
EXTP8	EXTP8_ RESERVED1	EXTP8_ RESERVED1	EXTP8_ RESERVED1	EXTP8_ RESERVED1	EXTP8_ RESERVED1	EXTP8_ RESERVED1	EXTP8_ RESERVED1	EXTP8_ RESERVED1
EXTP9	EXTP9_ RESERVED1	EXTP9_ RESERVED1	EXTP9_ RESERVED1	EXTP9_ RESERVED1	EXTP9_ RESERVED1	EXTP9_ RESERVED1	EXTP9_ RESERVED1	EXTP9_ RESERVED1
RP00	RP00	RP00	RP00	RP00	RP00	RP00	RP00	RP00
RP01	RP01	RP01	RP01	RP01	RP01	RP01	RP01	RP01
RP02	RP02	RP02	RP02	RP02	RP02	RP02	RP02	RP02
RP03	RP03	RP03	RP03	RP03	RP03	RP03	RP03	RP03
RP04	RP04	RP04	RP04	RP04	RP04	RP04	RP04	RP04
RP05	RP05_ RESERVED4	RP05_ RESERVED4	RP05_ RESERVED4	RP05_ RESERVED4	RP05_ RESERVED4	RP05_ RESERVED4	RP05_ RESERVED4	RP05_ RESERVED4
RP06	RP06	WRZ2	RP06	WRZ2	RP06	HWRZ2	RP06	HWRZ2
RP07	RP07	WRZ3	RP07	WRZ3	RP07	HWRZ3	RP07	HWRZ3
RP10	RP10	D24	RP10	MD24	RP10	HD24	RP10	HD24
RP11	RP11	D25	RP11	MD25	RP11	HD25	RP11	HD25
RP12	RP12	D26	RP12	MD26	RP12	HD26	RP12	HD26
RP13	RP13	D27	RP13	MD27	RP13	HD27	RP13	HD27
RP14	RP14	D28	RP14	MD28	RP14	HD28	RP14	HD28
RP15	RP15	D29	RP15	MD29	RP15	HD29	RP15	HD29
RP16	RP16	D30	RP16	MD30	RP16	HD30	RP16	HD30
RP17	RP17	D31	RP17	MD31	RP17	HD31	RP17	HD31
RP20	RP20	RP20	ADVZ	ADVZ	HBCYSTZ	HBCYSTZ	HBCYSTZ	HBCYSTZ
RP21	RP21	RP21	RP21	RP21	RP21	RP21	RP21	RP21
RP22	RP22	RP22	RP22	RP22	RP22	RP22	RP22	RP22
RP23	RP23	RP23	RP23	RP23	RP23	RP23	RP23	RP23
RP24	RP24	RP24	RP24	RP24	RP24	RP24	RP24	RP24

Pin Name	External Serial Flash ROM Boot (BOOT1-0 = 01)							
	Slave Memory Interface (MEMIFSEL = 0)				External MCU Interface (MEMIFSEL = 1)			
	Asynchronous type		Synchronous type		Asynchronous type		Synchronous type	
	16bit	32bit	16bit	32bit	16bit	32bit	16bit	32bit
RP25	RP25	RP25	RP25	RP25	RP25	RP25	RP25	RP25
RP26	RP26	RP26	RP26	RP26	RP26	RP26	RP26	RP26
RP27	RP27	RP27	RP27	RP27	RP27	RP27	RP27	RP27
RP30	RP30	D16	RP30	MD16	RP30	HD16	RP30	HD16
RP31	RP31	D17	RP31	MD17	RP31	HD17	RP31	HD17
RP32	RP32	D18	RP32	MD18	RP32	HD18	RP32	HD18
RP33	RP33	D19	RP33	MD19	RP33	HD19	RP33	HD19
RP34	RP34	D20	RP34	MD20	RP34	HD20	RP34	HD20
RP35	RP35	D21	RP35	MD21	RP35	HD21	RP35	HD21
RP36	RP36	D22	RP36	MD22	RP36	HD22	RP36	HD22
RP37	RP37	D23	RP37	MD23	RP37	HD23	RP37	HD23

5.3.3 Pin states when booting is for external MCU

The list of pin states is given below.
Entries in shaded cells shaded indicate multiplexed pin functions that are enabled in the initial state.
The initial state of booting for instruction RAM is the same as that for booting from external memory.

Remarks
Asynchronous type: asynchronous SRAM memory controller (MEMCSEL = 0)
Synchronous type: synchronous burst access memory controller (MEMCSEL = 1)
16 bit: 16-bit bus width of the external memory interface (BUS32EN = 0)
32 bit: 32-bit bus width of the external memory interface (BUS32EN = 1)

Table 5.3.3-1 Pin States when Booting is for External MCU

Pin Name	External MCU Boot (BOOT1-0 = 10)			
	External MCU Interface (MEMIFSEL = 1)			
	Asynchronous SRAM memory controller (MEMCSEL = 0)		Synchronous burst access memory controller (MEMCSEL = 1)	
	16bit (BUS32EN = 0)	32bit (BUS32EN = 1)	16bit (BUS32EN = 0)	32bit (BUS32EN = 1)
P00	P00	P00	P00	P00
P01	P01	P01	P01	P01
P02	P02	P02	P02	P02
P03	P03	P03	P03	P03
P04	P04	P04	P04	P04
P05	P05	P05	P05	P05
P06	P06	P06	P06	P06
P07	P07	P07	P07	P07
P10	P10	P10	P10	P10
P11	P11	P11	P11	P11
P12	P12	P12	P12	P12
P13	P13	P13	P13	P13
P14	P14	P14	P14	P14
P15	P15	P15	P15	P15
P16	P16	P16	P16	P16
P17	P17	P17	P17	P17
P20	P20	P20	P20	P20
P21	P21	P21	P21	P21
P22	P22	P22	P22	P22
P23	P23	P23	P23	P23
P24	P24	P24	P24	P24
P25	P25	P25	P25	P25
P26	P26	P26	P26	P26
P27	P27	P27	P27	P27
P30	P30	P30	P30	P30
P31	P31	P31	P31	P31
P32	P32	P32	P32	P32
P33	P33	P33	P33	P33
P34	P34	P34	P34	P34
P35	P35	P35	P35	P35
P36	P36	P36	P36	P36
P37	P37	P37	P37	P37
P40	HA1	HA1	HA1	HA1
P41	HWAITZ	HWAITZ	HWAITZ	HWAITZ
P42	HERROUTZ	HERROUTZ	HERROUTZ	HERROUTZ
P43	HBUSCLK	HBUSCLK	HBUSCLK	HBUSCLK
P44	HPGCSZ	HPGCSZ	HPGCSZ	HPGCSZ
P45	P45	P45	P45	P45
P46	P46	P46	P46	P46
P47	P47	P47	P47	P47
P50	P50	P50	P50	P50
P51	P51	P51	P51	P51
P52	P52	P52	P52	P52
P53	P53	P53	P53	P53

Pin Name	External MCU Boot (BOOT1-0 = 10) External MCU Interface (MEMIFSEL = 1) Asynchronous SRAM memory controller (MEMCSEL = 0)		Synchronous burst access memory controller (MEMCSEL = 1)	
	16bit (BUS32EN = 0)	32bit (BUS32EN = 1)	16bit (BUS32EN = 0)	32bit (BUS32EN = 1)
P54	P54	P54	P54	P54
P55	P55	P55	P55	P55
P56	P56	P56	P56	P56
P57	P57	P57	P57	P57
P60	P60	P60	P60	P60
P61	P61	P61	P61	P61
P62	P62	P62	P62	P62
P63	P63	P63	P63	P63
P64	P64	P64	P64	P64
P65	P65	P65	P65	P65
P66	P66	P66	P66	P66
P67	P67	P67	P67	P67
P70	P70	P70	P70	P70
P71	P71	P71	P71	P71
P72	P72	P72	P72	P72
P73	P73	P73	P73	P73
P74	P74	P74	P74	P74
P75	P75	P75	P75	P75
P76	P76	P76	P76	P76
P77	P77	P77	P77	P77
EXTP0	EXTP0_RESERVED1	EXTP0_RESERVED1	EXTP0_RESERVED1	EXTP0_RESERVED1
EXTP1	EXTP1_RESERVED1	EXTP1_RESERVED1	EXTP1_RESERVED1	EXTP1_RESERVED1
EXTP2	EXTP2_RESERVED1	EXTP2_RESERVED1	EXTP2_RESERVED1	EXTP2_RESERVED1
EXTP3	EXTP3	EXTP3	EXTP3	EXTP3
EXTP4	EXTP4_RESERVED1	EXTP4_RESERVED1	EXTP4_RESERVED1	EXTP4_RESERVED1
EXTP5	EXTP5	EXTP5	EXTP5	EXTP5
EXTP6	EXTP6	EXTP6	EXTP6	EXTP6
EXTP7	EXTP7	EXTP7	EXTP7	EXTP7
EXTP8	EXTP8_RESERVED1	EXTP8_RESERVED1	EXTP8_RESERVED1	EXTP8_RESERVED1
EXTP9	EXTP9_RESERVED1	EXTP9_RESERVED1	EXTP9_RESERVED1	EXTP9_RESERVED1
RP00	RP00	RP00	RP00	RP00
RP01	RP01	RP01	RP01	RP01
RP02	RP02	RP02	RP02	RP02
RP03	RP03	RP03	RP03	RP03
RP04	RP04	RP04	RP04	RP04
RP05	RP05_RESERVED4	RP05_RESERVED4	RP05_RESERVED4	RP05_RESERVED4
RP06	RP06	HWRZ2	RP06	HWRZ2
RP07	RP07	HWRZ3	RP07	HWRZ3
RP10	RP10	HD24	RP10	HD24
RP11	RP11	HD25	RP11	HD25
RP12	RP12	HD26	RP12	HD26
RP13	RP13	HD27	RP13	HD27
RP14	RP14	HD28	RP14	HD28
RP15	RP15	HD29	RP15	HD29
RP16	RP16	HD30	RP16	HD30
RP17	RP17	HD31	RP17	HD31
RP20	HBCYSTZ	HBCYSTZ	HBCYSTZ	HBCYSTZ
RP21	RP21	RP21	RP21	RP21
RP22	RP22	RP22	RP22	RP22
RP23	RP23	RP23	RP23	RP23
RP24	RP24	RP24	RP24	RP24
RP25	RP25	RP25	RP25	RP25
RP26	RP26	RP26	RP26	RP26
RP27	RP27	RP27	RP27	RP27
RP30	RP30	HD16	RP30	HD16
RP31	RP31	HD17	RP31	HD17

Pin Name	External MCU Boot (BOOT1-0 = 10) External MCU Interface (MEMIFSEL = 1) Asynchronous SRAM memory controller (MEMCSEL = 0)		Synchronous burst access memory controller (MEMCSEL = 1)	
	16bit (BUS32EN = 0)	32bit (BUS32EN = 1)	16bit (BUS32EN = 0)	32bit (BUS32EN = 1)
RP32	RP32	HD18	RP32	HD18
RP33	RP33	HD19	RP33	HD19
RP34	RP34	HD20	RP34	HD20
RP35	RP35	HD21	RP35	HD21
RP36	RP36	HD22	RP36	HD22
RP37	RP37	HD23	RP37	HD23

5.4 Operating Mode Monitoring

The levels on the operating mode setting pins listed in the following table can be confirmed by using the operating mode monitoring register.
For the operating mode setting pins, refer to Section 5.2.16 "Operating mode setting pins".
For the operating mode monitoring register, refer to Section 9.9 "Operating Mode Monitor Register (MDMNT)".

Table 5.4-1 Operating Mode Setting Pins for which the Settings can be Checked

Pin ID	Pin Name	Function
W19	BUS32EN	Selects the bus width when the external memory interface is started.
W18	MEMIFSEL	Selects the type of external memory interface.
W17	HIFSYNC	Sets the operating mode of the external MCU interface.
V20	HWRZSEL	Selects HWRZ or HBENZ of the external MCU interface.
Y8	JTAGSEL	Sets the operating mode of JTAG pins.
W13	OSCTH	Inputs High level in external clock input mode.
Y18, Y17	BOOT0, BOOT1	Selects boot mode.
U19	MEMCSEL	Selects the internal memory controller.
V19	ADMUXMODE	Multiplexing of address and data lines

5.5 Buffer Switching

The driving ability and use of a pull-up or pull-down resistor is programmable for real-time and general-purpose port pins (with some exceptions).

This function provides stable operation in systems with large loads by providing the ability to raise the driving ability.
The buffer switching register (DRCTL; Appendix 2.6) is used to switch the buffer function.

5.6 Buffer Type of Pins and Handling of Unused Pins

5.6.1 Port pins, real-time port pin buffer types, and handling of unused pins

Table 5.6.1-1 Port Pins, Real-time Port Pin Buffer Types, and Handling of Unused Pins

Pin ID	Pin Name	I/O	Interface	Recommended Connection when Not in Use
AB10, AA10, AB9, AA9, AB8, AA8, AB7, AA7 M22, M21, N22, N21, P22, P21, R21 Y22, Y21, AA21, AA20, AB19, AA19, AA16 B8 AB6 W22, W21, V21, V22, U21, U22, T21, T22 AA15, AA14, AB13, AA13, AB12, AA12, AB11, AA11 H22, H21, G22, G21, F21 C20, D20, E20, F20, D19, E19, F19, G19 B21, C22, C21, D22, D21, E22, E21, F22 B19, B18 P20, Y15, W15	P00-P07, P20-P23, P25-P27, P30-P35, P37, P44, P50, P60-P67, P70-P77, RP00-RP04, RP10-RP17, RP20-RP27, RP33, RP34, EXTP0, EXTP6, EXTP7	I/O	Programmable I/O buffer (3.3V) Driving ability selection (6mA, 12mA) Resistor selection (pull-up or pull-down or less)	Open
A12, A11, B12, B11, A10, B10, A9, B9 N20 AA17 A4, B6, A5, A6, A7, B7, A8 AA6, AB5, AA3 H20, H19, G20 A20, A19, B20, B17, C18, C19 R20, T20, U20, Y14, W14 Y16, W16	P10-P17, P24, P36, P40-P43, P45-P47, P51, P52, P57, RP05-RP07, RP30-RP32, RP35-RP37, EXTP1-EXTP5, EXTP8, EXTP9	I/O	Programmable I/O buffer (3.3V, 6mA) Resistor selection (pull-up or pull-down or less)	
AA5, AB4, AA4, AB3	P53-P56	I/O	5V-tolerant I/O buffer 4mA 50kΩ pull-up	

5.6.2 Buffer types of Ethernet pins and handling of unused pins

Table 5.6.2-1 Buffer Types of Ethernet Pins and Handling of Unused Pins

Pin ID	Pin Name	I/O	Interface	Recommended Connection when Not in Use
K2	P0_D0N	I/O	Management data Interface (analog)	Open
K1	P0_D0P	I/O	Management data Interface (analog)	Open
J2	P0_D1N	I/O	Management data Interface (analog)	Open
J1	P0_D1P	I/O	Management data Interface (analog)	Open
H2	P0_D2N	I/O	Management data Interface (analog)	Open
H1	P0_D2P	I/O	Management data Interface (analog)	Open
G2	P0_D3N	I/O	Management data Interface (analog)	Open
G1	P0_D3P	I/O	Management data Interface (analog)	Open
U2	P1_D0N	I/O	Management data Interface (analog)	Open
U1	P1_D0P	I/O	Management data Interface (analog)	Open
T2	P1_D1N	I/O	Management data Interface (analog)	Open
T1	P1_D1P	I/O	Management data Interface (analog)	Open
R2	P1_D2N	I/O	Management data Interface (analog)	Open
R1	P1_D2P	I/O	Management data Interface (analog)	Open
P2	P1_D3N	I/O	Management data Interface (analog)	Open
P1	P1_D3P	I/O	Management data Interface (analog)	Open
D5	PHYADD1	I	Device SMI Address bit 1. (with pull-down resistor)	Open
D4	PHYADD2	I	Device SMI Address bit 2. (with pull-down resistor)	Open
D3	PHYADD3	I	Device SMI Address bit 3. (with pull-down resistor)	Open
C2	PHYADD4	I	Device SMI Address bit 4. (with pull-down resistor)	Open
M2	REF_FILT	I/O	Copper media reference filter pin	Connect the pin to GND via an external 1uF capacitor.
M1	REF_REXT	I/O	Copper media reference external pin	Connect the pin to GND via an external 2.0kΩ (1%) resistor.
J6, J7, P6, P7	VDD1	-	1.0 V internal power supply	Connect the pin to VDD (1.0V).
K3, L3	VDD1A	-	1.0 V analog power requiring additional PCB power supply filtering	Connect the pin to VDD (1.0V).
N3, P3, R3	VDD25A	-	2.5-V general analog power supply	Connect the pin to VDD (2.5V).
J8, J9, K9, L9, M9, N9, P8, P9	VDD33_GPHY	-	3.3 V general I/O power supply	Connect the pin to VDD (3.3V).
B2	PHY0_LED0	O	GbE-PHY LED0_PHY0 output signal Output buffer (3.3V) 3mA	Open
AA2	PHY1_LED0	O	GbE-PHY LED0_PHY1 output signal Output buffer (3.3V) 3mA	Open

5.6.3 Buffer types of external SRAM / external MCU interface pins and handling of unused pins

Table 5.6.3-1 Buffer Types of External SRAM / External MCU Interface Pins and Handling of Unused Pins

Pin ID	Pin Name	I/O	Interface	Recommended Connection when Not in Use
A18	BUSCLK	O	Output buffer (3.3V) 9mA	Open
C13	CSZ0	I/O	I/O buffer (3.3V) 6mA 50kΩ Pull-up	Open
A3, B3, C3, B4, C4, B5, C5, C6, D6, C7, D7, C8, D8, C9, D9, C10, D11, D12, D13	A2-A20	I/O	I/O buffer (3.3V) 6mA 50kΩ Pull-down	Open
A14, B14, A15, B15, A16, B16, A17, C14, D14, C15, D15, C16, D16, C17, D17, D18	D0-D15			
A13	RDZ	I/O	I/O buffer (3.3V) 6mA 50kΩ Pull-up	Open
B13	WRSTBZ / HWRSTBZ			
C12, C11	WRZ0, WRZ1			

5.6.4 Buffer types of external interrupt input pin and handling of unused pin

Table 5.6.4-1 Buffer Types of External Interrupt Input Pin and Handling of Unused Pin

Pin ID	Pin Name	I/O	Interface	Recommended Connection when Not in Use
Y13	NMIZ	I	Input buffer (3.3V) Schmitt in 50kΩ Pull-up	Connect the pin to VDD (3.3V).

5.6.5 Buffer types of CC-Link IE Field pin and handling of unused pin

Table 5.6.5-1 Buffer Types of CC-Link IE Field Pin and Handling of Unused Pin

Pin ID	Pin Name	I/O	Interface	Recommended Connection when Not in Use
AB18	CCI_CLK2_097M	I	Input buffer (3.3V)	Connect the 2.097152MHz crystal oscillator.

Table 5.6.6-1 Buffer Types of System Pins and Handling of Unused Pins

Pin ID	Pin Name	I/O	Interface	Recommended Connection when Not in Use
AB14	XT1	I	Oscillator with EN	*1
AB15	XT2	I/O		*1
Y19	RSTOUTZ	O	Output buffer (3.3V) 6mA	Open
AB20	RESETZ	I	Input buffer (3.3V) Schmitt in	Connect a reset signal since these pins are always used.
Y20	PONRZ			
W20	HOTRESETZ			Connect the pin to VDD (3.3V).
W13	OSCTH	I	Input buffer (3.3V) Schmitt in 50kΩ pull-down	Set these pins in accordance with the operating mode.
Y8	JTAGSEL			
V18	ETHTEST	I	Input buffer (3.3V) 50kΩ pull-down	Connect the pin to GND.
E17	CTRSTBYB	I	Input buffer (3.3V) Schmitt in STBY-INPUT	Connect the pin to VDD (3.3V).
P18, V17	PLL_VDD	-	PLL power supply (1.0V)	Connect the pin to VDD (1.0V).
R18, V16	PLL_GND	-	PLL GND	Connect the pin to GND.
K18, L18, F12, F14, F16-F18, G12, H18, J12, L12, M12, P12, T12, T19, U12, U13, U16-U18	VDD33	-	I/O power supply (3.3V)	Connect the pin to VDD (3.3V).
H13-H17, J13, J17, K13, K17, L13, L17, M13, M17, N13, N17, P13, P17, R13-R17	VDD10	-	Internal power supply (1.0V)	Connect the pin to VDD (1.0V).
A1, A2, A21, A22, B1, B22, C1, D1, D2, D10, E1-E16, E18, F1-F3, F6-F11, F13, F15, G3, G6-G11, G13-G18, H3, H6-H12, J3, J4, J10, J11, J14-J16, J18, K4-K8, K11-K12, K14-K16, L1, L2, L4-L8, L11, L14-L16, M3-M8, M10, M11, M14-M16, M18, N1, N2, N4-N8, N10-N12, N14-N16, N18, P4, P10, P11, P14-P16, R6-R12, T3, T6-T11, T13-T18, U3, U7-U11, U14, U15, V1-V15, W1-W3, W10, W12, Y1-Y3, AA1, AA18, AA22, AB1, AB2, AB16, AB21, AB22	GND	-	Power supply ground voltage (GND)	Connect the pin to GND.

*1: The pin connection differs depending on the setting of the OSCTH pin. For details, refer to "R-IN32M4-CL2 Series User's Manual: Board Design".

5.6.7 Buffer types of trace pins and handling of unused pins

Table 5.6.7-1 Buffer Types of Trace Pins and Handling of Unused Pins

Pin ID	Pin Name	I/O	Interface	Recommended Connection when Not in Use
Y12	TRACECLK	O	Output buffer (3.3V) 6mA	Open
Y9, Y10, W11, Y11	TRACEDATA3-0	I/O	Programmable I/O buffer (3.3V, 6mA), 50kΩ Pull-up	

5.6.8 Buffer types of test pins and handling of unused pins

Table 5.6.8-1 Buffer Types of Test Pins and Handling of Unused Pins

Pin ID	Pin Name	I/O	Interface	Recommended Connection when Not in Use (Required)
W5	TMS	I/O	I/O buffer (3.3V) 6mA Pull-up	Open
W6	TDI	I	Input buffer (3.3V) 25kΩ Pull-up	Open
W8	TDO	O	3-state Output buffer (3.3V) 6mA	Open
W9	TRSTZ	I	Input buffer (3.3V) Schmitt in, 50kΩ Pull-up	Open
W7	TCK	I	Input buffer (3.3V) 25kΩ Pull-up	Open

5.6.9 Buffer types of operating mode setting pins and handling of unused pins

Table 5.6.9-1 Buffer Types of Operating Mode Setting Pins and Handling of Unused Pins

Pin ID	Pin Name	I/O	Interface	Recommended Connection when Not in Use
Y17, Y18	BOOT0, BOOT1	I	Input buffer (3.3V) Schmitt in	Set these pins in accordance with the operating mode.
W18	MEMIFSEL			
W19	BUS32EN			
W17	HIFSYNC			
V20	HWRZSEL			
U19	MEMCSEL			
V19	ADMUXMODE			

Table 5.6.10-1 Buffer Types of Reserved Pins and Pin Handling

Pin ID	Pin Name	I/O	Interface	Recommended Connection when Not in Use
L10	RESERVED_L10	I/O	-	Open
J20	RESERVED_J20	O	-	Open
J19	RESERVED_J19	O	-	Open
M20	RESERVED_M20	O	-	Open
M19	RESERVED_M19	O	-	Open
J22	RESERVED_J22	I	-	Connect the pin to GND.
J21	RESERVED_J21	I	-	Connect the pin to GND.
K22	RESERVED_K22	I	-	Connect the pin to GND.
K21	RESERVED_K21	I	-	Connect the pin to GND.
L22	RESERVED_L22	I	-	Connect the pin to GND.
L21	RESERVED_L21	I	-	Connect the pin to GND.
K20	RESERVED_K20	I	-	Connect the pin to GND.
K19	RESERVED_K19	I	-	Connect the pin to GND.
L20	RESERVED_L20	I	-	Connect the pin to GND.
L19	RESERVED_L19	I	-	Connect the pin to GND.
R22	RESERVED_R22	I	-	Connect the pin to GND.
U6	RESERVED_U6	I	-	Connect the pin to GND.
Y5	RESERVED_Y5	I	-	Connect the pin to GND via 47Ω resistor.
Y6	RESERVED_Y6	I	-	Connect the pin to GND via 47Ω resistor.
Y7	RESERVED_Y7	I	-	Connect the pin to GND via 47Ω resistor.
R19	RESERVED_R19	I	-	Connect the pin to GND via 47Ω resistor.
P19	RESERVED_P19	I	-	Connect the pin to GND via 47Ω resistor.
AB17	RESERVED_AB17	I	-	Connect the pin to GND.
G5	RESERVED_G5	I	-	Connect the pin to GND.
H5	RESERVED_H5	-	-	Connect the pin to GND.
P5	RESERVED_P5	-	-	Connect the pin to GND.
R5	RESERVED_R5	-	-	Connect the pin to GND.
J5	RESERVED_J5	-	-	Connect the pin to GND.
T5	RESERVED_T5	I	-	Connect the pin to GND.
F5	RESERVED_F5	-	-	Open
F4	RESERVED_F4	-	-	Open
G4	RESERVED_G4	-	-	Open
H4	RESERVED_H4	-	-	Open
U5	RESERVED_U5	-	-	Open
R4	RESERVED_R4	-	-	Open
T4	RESERVED_T4	-	-	Open
U4	RESERVED_U4	-	-	Open
Y4	RESERVED_Y4	I/O	-	Open
W4	RESERVED_W4	I/O	-	Open
N19	RESERVED_N19	I	-	Connect the pin to GND.

6 ELECTRICAL CHARACTERISTICS

This chapter describes the CP520 electrical characteristics and access timing.
The terminology used in electrical characteristics and access timing is given in the table below.

Table 6-1 Terminology Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin.
Input voltage	V_I	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates the absolute tolerance value for DC current to prevent damage or reduced reliability when a current flows out of or into an output pin.
Operating ambient temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	$T_{.Sgt.}$	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current is being applied to the device.

Table 6-2 Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates the voltage range for normal logic operations that occur when V_{SS} = 0V.
High-level input voltage	V_{IH}	A voltage, which is applied to the input pins of CP520, indicating the voltage of the High-level state for normal operation of the input buffer. If a voltage that is equal to or greater than the minimum value is applied, the input voltage is guaranteed as a High-level voltage.
Low-level input voltage	V_{IL}	A voltage, which is applied to the input pins of CP520, indicating the voltage of the Low-level state for normal operation of the input buffer. If a voltage that is equal to or less than the maximum value is applied, the input voltage is guaranteed as a Low-level voltage.
Positive trigger voltage	V_P	Indicates the input level at which the output level is inverted when the input to CP520 is changed from the Low-level side to the High-level side.
Negative trigger voltage	V_N	Indicates the input level at which the output level is inverted when the input to CP520 is changed from the High-level side to the Low-level side.
Hysteresis voltage	V_H	Indicates the differential between the positive trigger voltage and the negative trigger voltage.
Input rising time	t_{ried}, t_{ric}, t_{ris}	Indicates the limit value for the time period when an input voltage applied to CP520 rises from 10% to 90%. t_{ried}, t_{ric}, and t_{ris} each indicate the input rising time for the data clock and Schmitt buffer.
Input falling time	t_{fid}, t_{fic}, t_{fis}	Indicates the limit value for the time period when an input voltage applied to CP520 falls from 90% to 10%. t_{fid}, t_{fic}, and t_{fis} each indicate the input falling time for the data clock and Schmitt buffer.

Table 6-3 Terms Used for DC Characteristics

Parameter	Symbol	Meaning
Operating current consumption	I_{DD}	Indicates the current that flows from the power supply pin when the rated power supply voltage is applied each time the voltage of the input and output pins changes.
Off-state output current	I_{OZ}	Indicates the current that flows via an output pin when the rated voltage is applied when a 3-state output has high impedance.
Output short circuit current	I_{OS}	Indicates the current that flows when the output pins are shorted to the ground when output is at High level.
Input leakage current	I_{LI}	Indicates the current that flows via an input pin when a voltage is applied to that pin.
Low-level output current	I_{OL}	Indicates the current that flows to the output pins when the rated Low-level output voltage is being applied.
High-level output current	I_{OH}	Indicates the current that flows from the output pins when the rated High-level output voltage is being applied.
Low-level output voltage	V_{OL}	Indicates the output voltage at Low level and when the output pin is open.
High-level output voltage	V_{OH}	Indicates the output voltage at High level and when the output pin is open.

6.1 Absolute Maximum Ratings

Take precautions to ensure that the absolute maximum ratings defined for each item are not exceeded.
Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter.
3.3V must be applied to the I/O pins only after applying the power supply voltage.

Table 6.1-1 Absolute Maximum Ratings

Parameter	Symbol	Conditions		Ratings	Unit
Power supply voltage	V_{DD}	1.0V system		-0.3 to +1.10	V
		2.5V system		-0.3 to +2.75	V
		3.3V system		-0.3 to +3.60	V
I/O voltage	V_I / V_O	2.5V buffer*1	-	-0.3 to +2.75	V
		3.3V buffer*2	-	-0.3 to +3.6	V
		3.3V buffer*3	V_I / V_O < V_{DD} +0.5V	-0.5 to +4.1	V
		5V-tolerant buffer	V_I / V_O < V_{DD} +3.0V	-0.5 to +6.6	V
Output current (3.3V buffer)	I_O	6mA type		15	mA
		12mA type		25	mA
Output current (5V-tolerant buffer)	I_O	4mA type		10.35	mA
Operating ambient temperature	T_A	-		-40 to +85	°C
Storage temperature	$T_{.Sgt.}$	-		-65 to +125	°C

*1: This applies to the PHYADD3 and PHYADD4 pins.
*2: This applies to the PHYADD1, PHYADD2, TDI, TMS, and TCK pins.
*3: This applies to the pins other than PHYADD1, PHYADD2, TDI, TMS, and TCK pins.

6.2 Recommended Operating Conditions

Table 6.2-1 Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}	1.0V power supply	0.95	1.0	1.05	V
		2.5V power supply	2.375	2.5	2.625	V
		3.3V power supply	3.135	3.3	3.465	V
Negative trigger voltage	V_N	3.3V buffer	0.6	-	1.8	V
		5V-tolerant buffer	0.8	-	1.1	V
Positive trigger voltage	V_P	3.3V buffer	1.2	-	2.4	V
		5V-tolerant buffer	1.7	-	2.2	V
Hysteresis voltage	V_H	3.3V buffer	0.3	-	1.5	V
		5V-tolerant buffer	0.9	-	1.1	V
Low-level input voltage	V_{IL}	3.3V buffer	-0.3	-	0.8	V
		5V-tolerant buffer	0	-	0.8	V
High-level input voltage	V_{IH}	3.3V buffer	2.0	-	V_{DD} + 0.3	V
		5V-tolerant buffer	2.0	-	5.5	V
Input rising/falling time	t_{ried}	-	0	-	200	ns
	t_{fid}	-	0	-	200	ns
Input rising/falling time (clock)	t_{ric}	-	0	-	4	ns
	t_{fic}	-	0	-	4	ns
Input rising/falling time (Schmitt input)	t_{ris}	-	0	-	1	ms
	t_{fis}	-	0	-	1	ms
Operating ambient temperature	T_A	-	-40	-	85	°C

6.3 DC Characteristics

The (+) and (–) signs in the table indicate the current direction. Current flowing to the device is indicated by (+) and current flowing out is indicated by (–).

Table 6.3-1 DC Characteristics (V_{DD} = 3.3±0.165V, T_A = –40 to +85°C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Operating current consumption	I_{DD}	V_I = V_{DD} or GND	1.0V	-	-	1540	mA
			2.5V	-	-	305	mA
			3.3V	-	-	75	mA
Off-state current	I_{OZ}	V_I = V_{DD} or GND	3.3V output	-	-	±10	µA
			5V-tolerant buffer	-	-	±10	µA
Output short circuit current[*1]	I_{OS}	V_O = GND	-	-	-	-250	mA
Input leakage current (3.3V buffer)	I_I	V_I = V_{DD} or GND	Normal input	-	-	±10	µA
		V_I = GND	With pull-up resistor (50kΩ)	-28.9	-65.7	-129.8	µA
			With pull-up resistor (25kΩ)	-85.0	-160.0	-280.0	µA
		V_I = V_{DD}	With pull-down resistor (50kΩ)	10.2	43.4	83.9	µA
Input leakage current (5V-tolerant buffer)	I_I	V_I = GND	With pull-up resistor (50kΩ)	39.0	-	100.9	µA
Low-level output current (3.3V buffer)	I_{OL}	V_{OL} = 0.4V	6mA type	6.0	-	-	mA
			12mA type	12.0	-	-	mA
Low-level output current (5V-tolerant buffer)	I_{OL}	V_{OL} = 0.4V	4mA type	4.0	-	-	mA
High-level output current (3.3V buffer)	I_{OH}	V_{OH} = 2.4V	6mA type	-6.0	-	-	mA
			12mA type	-12.0	-	-	mA
High-level output current (5V-tolerant buffer)	I_{OH}	V_{OH} = 2.4V	4mA type	-4.0	-	-	mA
Low-level output voltage	V_{OL}	I_{OL} = 0mA	3.3V buffer	-	-	0.1	V
			5V-tolerant buffer	-	-	0.1	V
High-level output voltage	V_{OL}	I_{OL} = 0mA	3.3V buffer	V_{DD} - 0.1	-	-	V
			5V-tolerant buffer	V_{DD} - 0.1	-	-	V

*1: The output short circuit time is no more than one second and is only for one pin.

6.4 Pull-Up/Pull-Down Resistor Values

Table 6.4-1 Pull-Up/Pull-Down Resistor Values (V_{DD} = 3.3±0.165V, T_A = –40 to +85°C)

Parameter	Library Specification[*1]	MIN.	TYP.	MAX.	Unit
Pull-up resistor (3.3V buffer)	50kΩ	24	45	78	kΩ
Pull-up resistor (3.3V buffer) (TCK, TMS, TDI)	25kΩ	10	21	40	kΩ
Pull-down resistor (3.3V buffer)	50kΩ	24	45	78	kΩ
Pull-up resistor (5V-tolerant buffer)	50kΩ	35.7	51.2	77.0	kΩ

*1: The pull-up and pull-down resistance values in this document are described using library specification. The actual ranges of the resistance values are within the MIN and MAX values in the table above.

6.5 Pin Capacitance

Table 6.5-1 Pin Capacitance

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Input buffer	C_B	5.0	-	7.0	pF
Output buffer		5.0	-	7.0	pF
I/O buffer		5.0	-	7.0	pF

6.6 Power-On/Off Sequence

Table 6.6-1 lists external power supplies to the CPU area and GbE-PHY area.
Figure 6.6-1 shows the power-on/off sequence.

We recommend supplying external power voltage VDD10 and then supplying external power voltage VDD33.
If VDD33 is supplied first, note that the I/O modes of the I/O buffers are not fixed and outputs become undefined over the period between VDD33 and VDD10 rising to their thresholds.
3.3V must be applied to the I/O pins only after the power supply voltages have been applied.

When turning off the power, disconnect VDD33, then VDD10.

Table 6.6-1 External Power Supplies

External Power Supply	Voltage [V]	Supplied to	External Pin Name
VDD33	3.3±0.165*1	CPU	VDD33
		GbE-PHY	VDD33_GPHY
VDD25	2.5±0.125*1	GbE-PHY	VDD25A
VDD10	1.0±0.05*1	CPU	VDD10, PLL_VDD
		GbE-PHY	VDD1, VDD1A

*1: Ripple incorporated value. As a target value, set the DC component to within ±3% and the ripple component to within ±2%.

(1) Supplying power voltages

Supply power voltages so that the following two conditions are both satisfied.

1) The time from the first power voltage among VDD33, VDD25, or VDD10 to reach 10% of VDD to all VDDs at least having reached 90% of VDD is within 100ms.
2) The time from the first power voltage among VDD33, VDD25, or VDD10 to reach 95% of VDD to all VDDs at least having reached 95% of VDD is within 50ms.

(2) Turning off power voltages

Turn off power voltages so that the following two conditions are both satisfied.

1) The time from the first power voltage among VDD33, VDD25, or VDD10 to reach 90% of VDD to all VDDs at least having reached 10% of VDD is within 100ms.
2) The time from the first power voltage among VDD33, VDD25, or VDD10 to reach 95% of VDD to all VDDs at least having reached 95% of VDD is within 50ms.

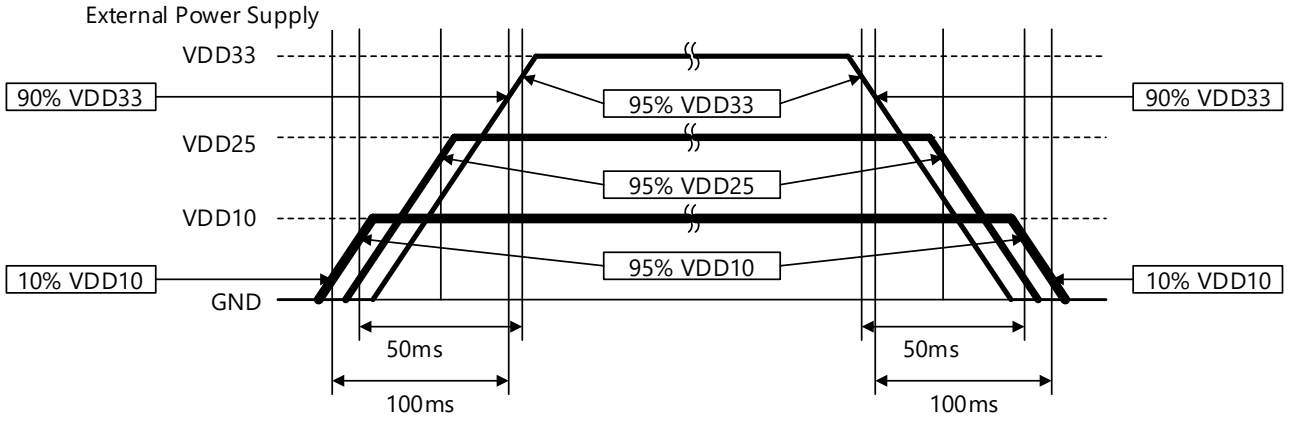


Figure 6.6-1 Power-On/Off Sequence

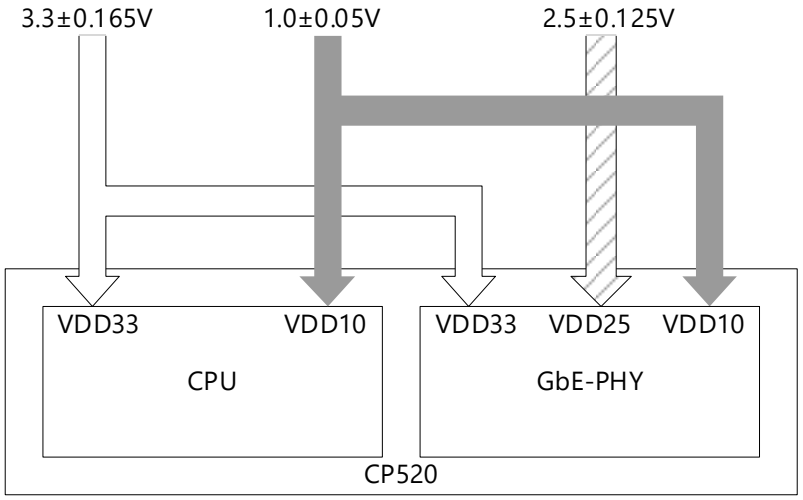


Figure 6.6-2 Power Supply Path to CPU Area and GbE-PHY Area

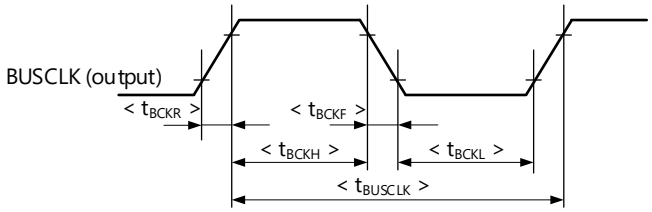
6.7.1 Clock pins

(1) Input clocks

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
XT1, XT2	t_{SYSCLK}	-	25±50ppm, 5ps-rms		MHz
CLK2_097M	$t_{CCLIECLK}$	-	2.097±100ppm		MHz
HBUSCLK	$t_{HBUSCLK}$	-	-	50	MHz
CSISCK0, CSISCK1	$t_{CSISSCK}$	Slave mode	-	16.6	MHz
TCK	t_{TCK}	-	-	50	MHz

(2) Output clocks

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
BUSCLK output cycle	t_{BUSCLK}	C_L = 15pF	10	-	ns
BUSCLK High-level width	t_{BCKH}		0.5 × t_{BUSCLK} - 2.0	0.5 × t_{BUSCLK} + 2.0	ns
BUSCLK Low-level width	t_{BCKL}		0.5 × t_{BUSCLK} - 2.0	0.5 × t_{BUSCLK} + 2.0	ns
BUSCLK rising time	t_{BCKR}		-	1.2	ns
BUSCLK falling time	t_{BCKF}		-	1.2	ns
CSISCK0 and CSISCK1 output frequency	$t_{CSIMSCK}$	Master mode, C_L = 15pF	-	25	MHz
SCL0 and SCL1 output frequency	t_{SCL}	High-speed mode, C_L = 30pF	-	400	kHz
SMSCK output frequency	t_{SMSCK}	C_L = 15pF	-	50	MHz
TRACECLK output frequency	$t_{TRACECLK}$	C_L = 15pF	-	50	MHz



*: For other clocks, refer to the AC characteristics of each interface.

Figure 6.7.1-1 Output Clocks Timing

Table 6.7.2-1 Reset Pins

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
RESETZ input Low-level width	t_{WRSL}	-	1	-	µs
HOTRESETZ input Low-level width	t_{WHRSL}	-		-	µs
PONRZ input Low-level width	t_{WPRSL}	-		-	µs
PONRZ input timing (for RESETZ ↑)	t_{SKPR}	-	0	-	µs

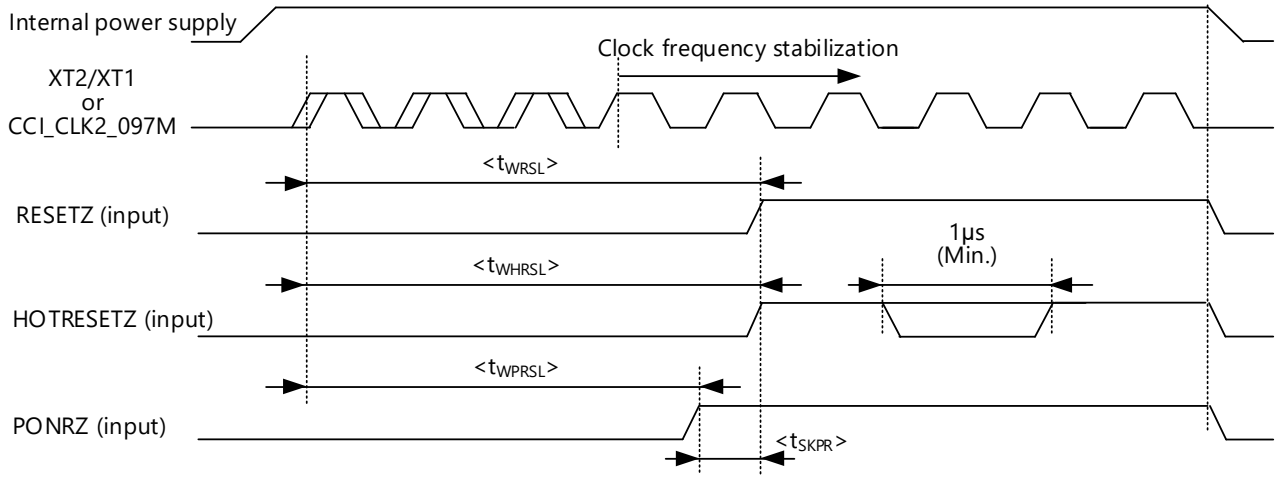


Figure 6.7.2-1 Reset Timing

6.7.3 External memory interface pins

(1) Calculating a delay value due to the external load

For the external memory interface pins of CP520, the listed values are for a load of 0pF, but the actual loads will differ with the user.

Calculate the timing according to the load conditions of the user. The user must also take the wiring delay on the board into account.

Table 6.7.3-1 Delay Value Due to External Load

Driving Ability	Delay Value per pF (ns)	
	MIN.	MAX.
6mA	0.026	0.067
12mA	0.012	0.034

[Calculation Example]

When an address pin (6-mA output buffer) has a 30-pF load, the actual delay is as follows.

However, the user must also take the wiring delay on the board into account since the wiring delay is not included.

MIN.: 1.0ns (Minimum delay value for a load of 0pF) + (0.026 × 30)ns = 1.78ns

MAX.: 7.0ns (Maximum delay value for a load of 0pF) + (0.067 × 30)ns = 9.01ns

(2) Asynchronous SRAM memory controller access timing

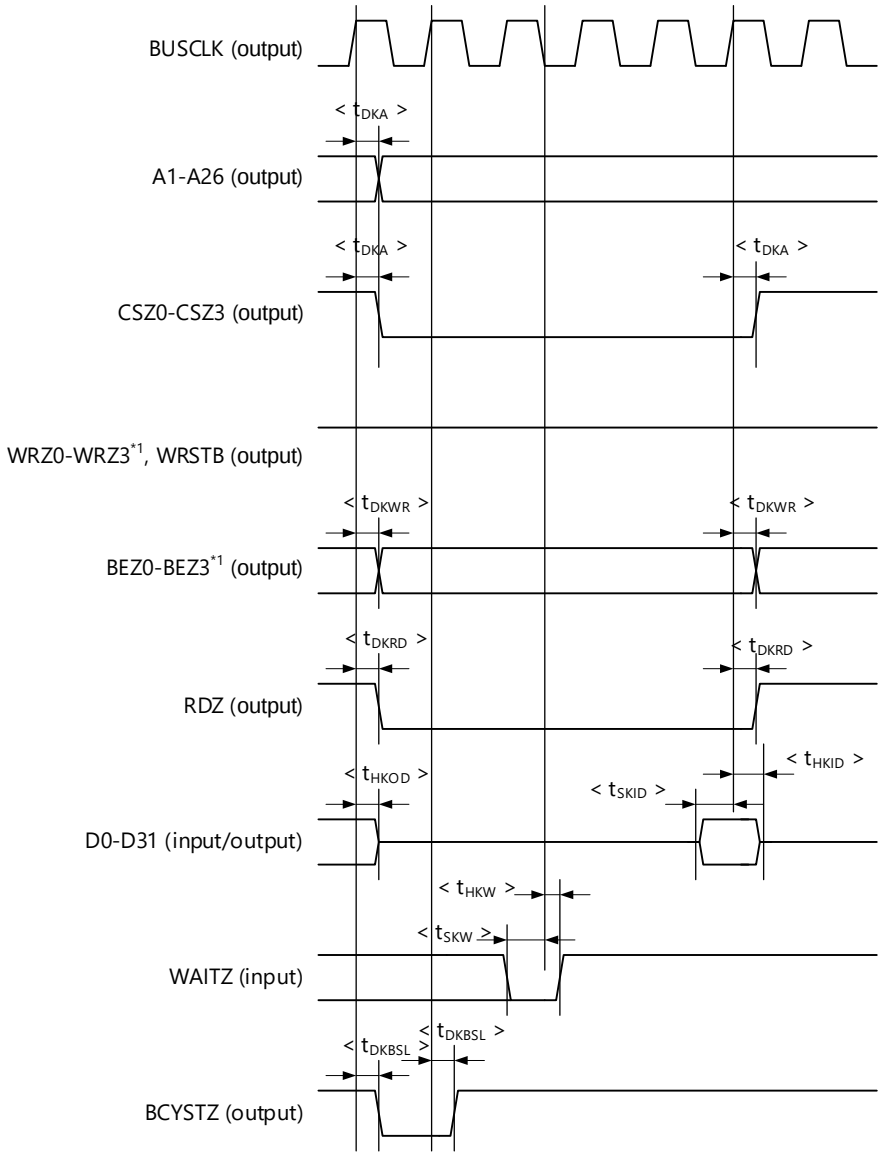
Table 6.7.3-2 Asynchronous SRAM Memory Controller Access Timing

Parameter	Symbol	MIN.	MAX.	Unit
Address and CSZ0-CSZ3 output delay time (for BUSCLK ↑)	t_{DKA}	1.0 (1.78)*1	7.0 (9.01)*1	ns
RDZ output delay time (for BUSCLK ↑)	t_{DKRD}	1.0 (1.78)*1	7.0 (9.01)*1	ns
WRZ0-WRZ3 (BENZ0-BENZ3), and WRSTBZ output delay time (for BUSCLK ↑)	t_{DKWR}	1.0 (1.78)*1	7.0 (9.01)*1	ns
BCYSTZ output delay time (for BUSCLK ↑)	t_{DKBSL}	1.0 (1.78)*1	7.0 (9.01)*1	ns
WAITZ input setup time (for BUSCLK ↓)	t_{SKW}	4.0	-	ns
WAITZ input hold time (for BUSCLK ↓)	t_{HKW}	0	-	ns
Data input setup time (for BUSCLK ↑)	t_{SKID}	4.0	-	ns
Data input hold time (for BUSCLK ↑)	t_{HKID}	0	-	ns
Data output delay time (for BUSCLK ↑)	t_{DKOD}	1.0 (1.78)*1	7.0 (9.01)*1	ns
Data float delay time (for BUSCLK ↑)	t_{HKOD}	1.0 (1.78)*1	7.0 (9.01)*1	ns

*1: Values in parenthesis are for a load of 30pF.

(a) Read timing

The following timing is for the case where the settings in the SMCn register for numbers of idle wait cycles, write recovery wait cycles, and address setting wait cycles are 0, and that for data wait cycles is 3.

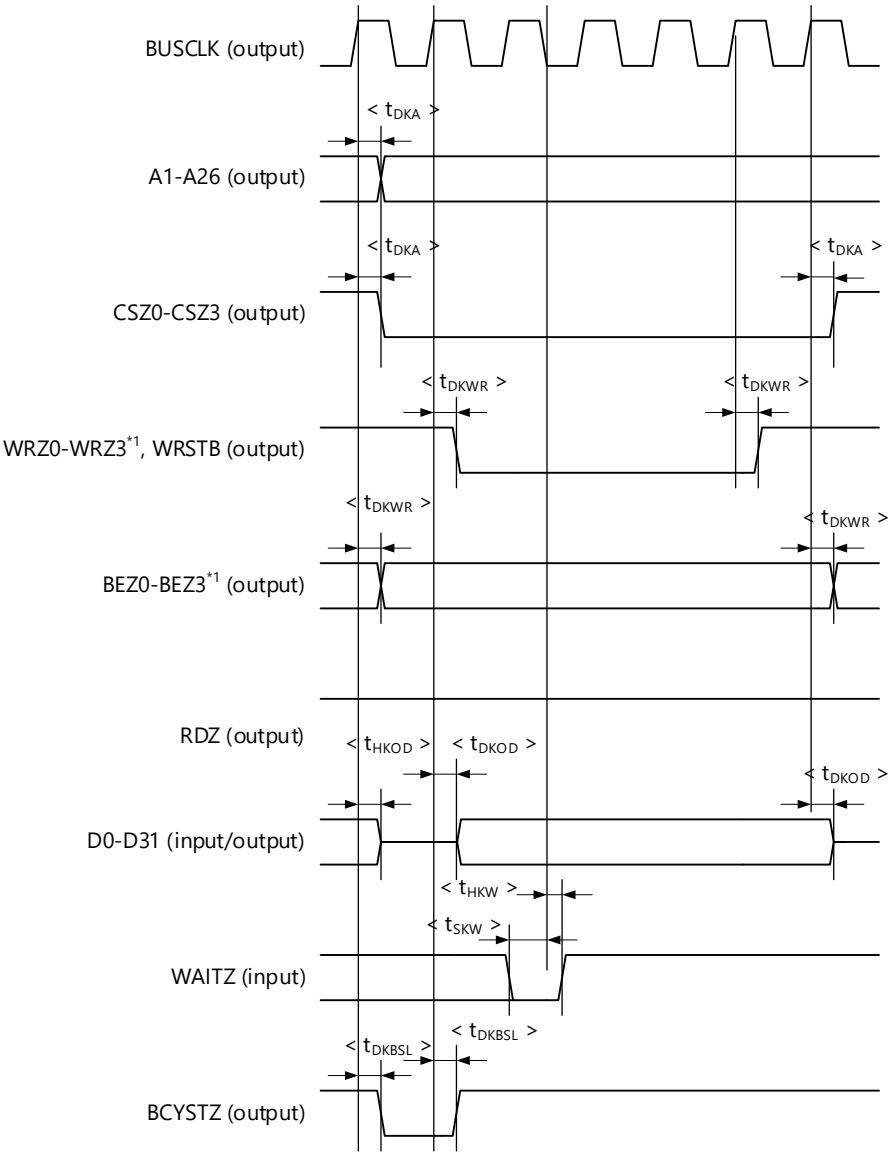


*1: The WRZ0 to WRZ3 pins are multiplexed with the BENZ0 to BENZ3 pin functions. The pin names are WRZ0 to WRZ3. The WRZ0 to WRZ3 pins are selected by default during a reset. Use the write-enable switching register (WREN) to switch the pin functions of these pins.
For details, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

Figure 6.7.3-1 Memory Controller Read Timing (Asynchronous Memory)

(b) Write timing

The following timing is for the case where the settings in the SMCn register for numbers of idle wait cycles, write recovery wait cycles, and address setting wait cycles are 0, and that for data wait cycles is 3.



*1: The WRZ0 to WRZ3 pins are multiplexed with the BENZ0 to BENZ3 pin functions. The pin names are WRZ0 to WRZ3. The WRZ0 to WRZ3 pins are selected by default during a reset. Use the write-enable switching register (WREN) to switch the pin functions of these pins.
For details, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

Figure 6.7.3-2 Memory Controller Write Timing (Asynchronous Memory)

(3) Synchronous burst access memory controller access timing

Table 6.7.3-3 Synchronous Burst Access Memory Controller Access Timing

Parameter	Symbol	MIN.	MAX.	Unit
BUSCLK output frequency	t_{BUSCLK}	-	50	MHz
Address and CSZ0-CSZ3 output delay time	t_{DKA}	1.0 (1.78)*1	7.8 (9.81)*1	ns
RDZ output delay time	t_{DKRD}	1.0 (1.78)*1	7.8 (9.81)*1	ns
WRZ0-WRZ3 (BENZ0-BENZ3) and WRSTBZ output delay time	t_{DKWR}	1.0 (1.78)*1	7.8 (9.81)*1	ns
ADVZ output delay time	t_{DKBSL}	1.0 (1.78)*1	7.8 (9.81)*1	ns
WAITZ and WAITZ1-3 input setup time	t_{SKW}	5.3	-	ns
WAITZ and WAITZ1-3 input hold time	t_{HKW}	0	-	ns
Data input setup time	t_{SKID}	5.3	-	ns
Data input hold time	t_{HKID}	0	-	ns
Data output delay time	t_{DKOD}	1.0 (1.78)*1	7.8 (9.81)*1	ns
Data float delay time	t_{HKOD}	1.0 (1.78)*1	7.8 (9.81)*1	ns

*1: Values in parenthesis are for a load of 30pF.

(a) Read timing

The following timing is for the case where t_ceoe is 2 and t_rc is 4.

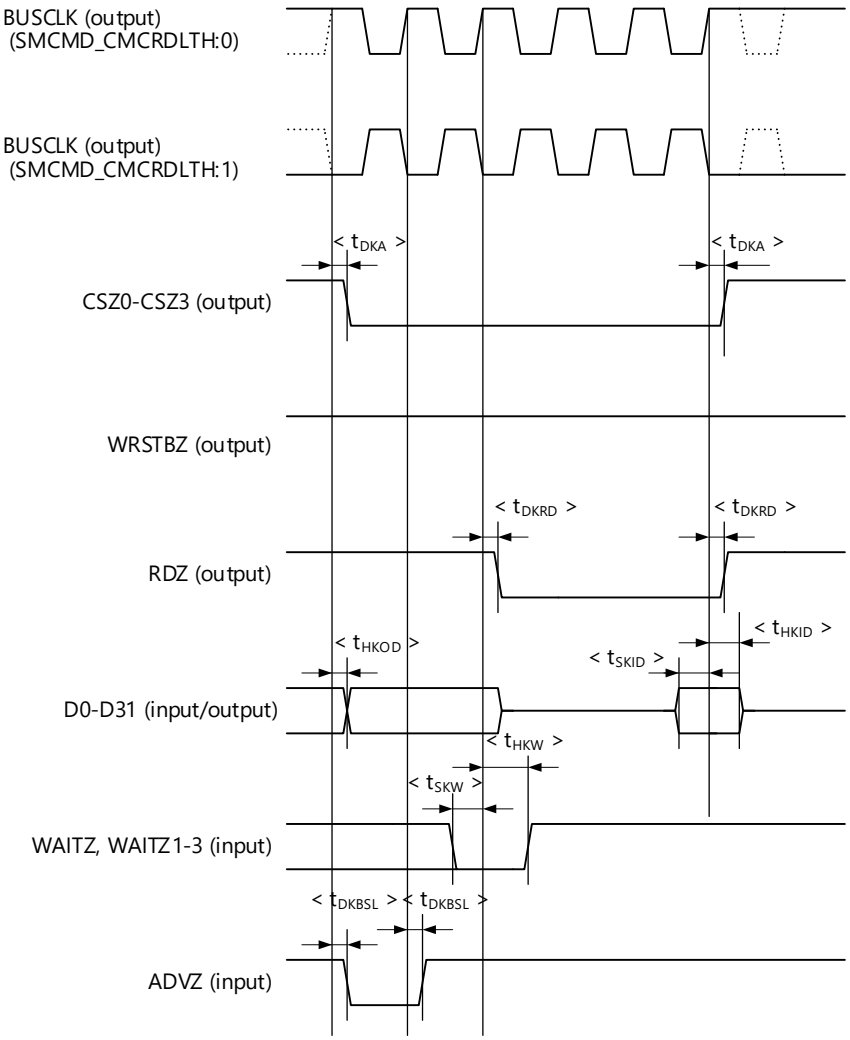


Figure 6.7.3-3 Memory Controller Read Timing (Clock Synchronous Memory)

(b) Write timing

The above timing is for the case where t_wp is 2 and t_wc is 5.

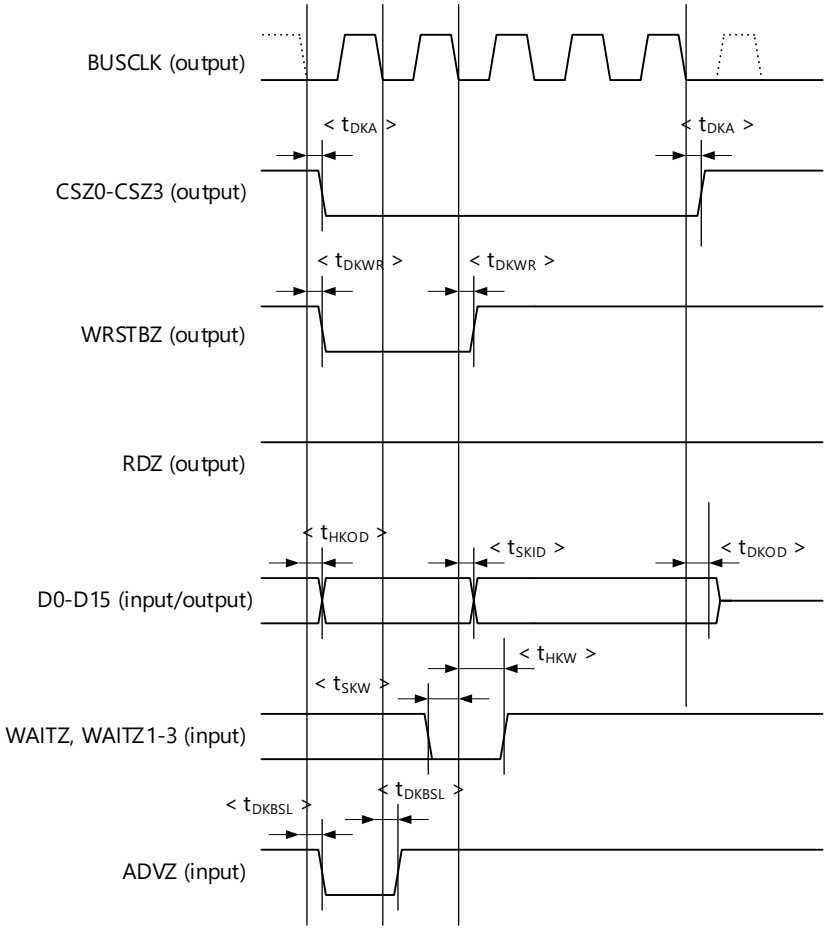


Figure 6.7.3-4 Memory Controller Write Timing (Clock Synchronous Memory)

6.7.4 External MCU interface pins

The load condition for the external MCU interface pins: 65pF (HD pin) and 35pF (HWAITZ pin)

(1) Synchronous SRAM supported MCU connection mode (during register access)

Table 6.7.4-1 Access Timing: Synchronous SRAM Supported MCU Connection Mode (During Register Access)

No.	Parameter	Symbol	MIN.	MAX.	Unit
1	HBUSCLK High-level width	t_{HBHIGH}	$0.5t_{HBUSCLK}$-2.1	$0.5t_{HBUSCLK}$+2.1	ns
2	HBUSCLK Low-level width	t_{HBLOW}	$0.5t_{HBUSCLK}$-2.1	$0.5t_{HBUSCLK}$+2.1	ns
3	HBUSCLK input cycle	$t_{HBUSCLK}$	20.0	-	ns
4	Address, HCSZ, HPGCSZ, and HRDZ input setup time (for HBUSCLK ↑)	t_{SKHA}	4.0	-	ns
5	HBENZ0-HBENZ3 (HWRZ0-HWRZ3), HWRSTBZ input setup time (for HBUSCLK ↑)	t_{SKHWR}	4.0	-	ns
6	Address, HCSZ, HPGCSZ, and HRDZ input hold time (for HBUSCLK ↑)	t_{HKHA}	1.0	-	ns
7	HBENZ0-HBENZ3 (HWRZ0-HWRZ3), HWRSTBZ input hold time (for HBUSCLK ↑)	t_{HKHWR}	1.0	-	ns
8	HWRZ0-HWRZ3, HWRSTBZ recovery time (High-level width)	t_{WHWR}	35.0	-	ns
9	Data input setup time (for HBUSCLK ↑)	t_{SKIHD}	4.0	-	ns
10	Data input hold time (for HBUSCLK ↑)	t_{HKIHD}	1.0	-	ns
11	HWAITZ output delay time (for HCSZ, HPGCSZ ↓)	t_{DKHD}	2.2	-	ns
12	HWAITZ output delay time (for HWRSTBZ, HWRZ0-HWRZ3 ↓)	t_{DKHWT}	2.2	-	ns
13	HWAITZ valid data output delay time (for HBUSCLK ↑)	t_{DKHWTV}	2.0	11.0	ns
14	HWAITZ valid data hold time (for HWRSTBZ, HWRZ0-HWRZ3 ↑)	t_{HKHWTV}	4.2	-	ns
15	HWAITZ output hold time (for HWRSTBZ, HWRZ0-HWRZ3 ↑)	t_{HKWTWR}	-	16.8	ns
16	Data and HWAITZ output hold time (for HCSZ, HPGCSZ ↑)	t_{HKWTCS}	-	16.8	ns
17	HRDZ recovery time (High-level width)	t_{WHRD}	35.0	-	ns
18	Data, HWAITZ output delay time (for HRDZ ↓)	t_{DKHDHR}	2.2	-	ns
19	Data fixing time (for HWAITZ ↑)	$t_{SKHDHWT}$	$t_{HBUSCLK}$-10.0	-	ns
20	Data and HWAITZ valid data output hold time (for HRDZ ↑)	$t_{HKHWTHR}$	2.2	-	ns
21	Data and HWAITZ output hold time (for HRDZ ↑)	t_{HKOHD}	-	16.8	ns
22	Data and HWAITZ output delay time in on-page access (for addresses)	t_{DKPON}	4.2	15.4	ns
23	Data and HWAITZ output delay time in off-page access (for addresses) (when not crossing a 16-byte boundary)	t_{DKPOFF}	4.2	15.4	ns
	Data and HWAITZ output delay time in off-page access (for addresses) (when crossing a 16-byte boundary)	t_{DKPOFF}	4.2	49.5	ns
24	HWAITZ valid data output delay time (for HCSZ, HPGCSZ ↓)	$t_{DKWTVCS}$	-	15.4	ns

(a) Write timing

Supply a stable signal to the address, data, and control lines during access.

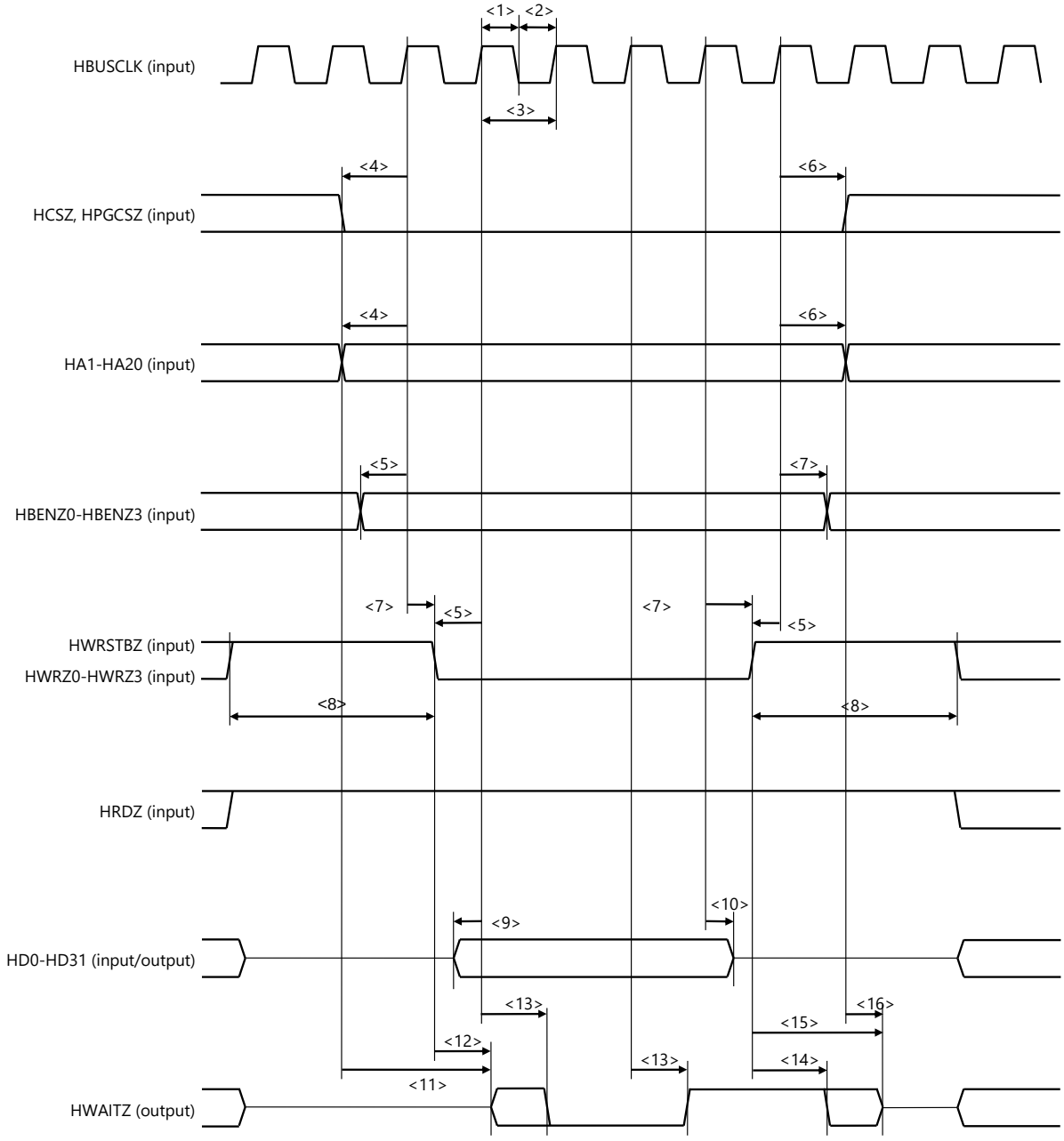


Figure 6.7.4-1 Synchronous SRAM Supported MCU Connection Mode (During Register Access) Write Timing (MEMCSEL=L, HIFSYNC=H)

(b) Read timing

Supply a stable signal to the address, data, and control lines during access.

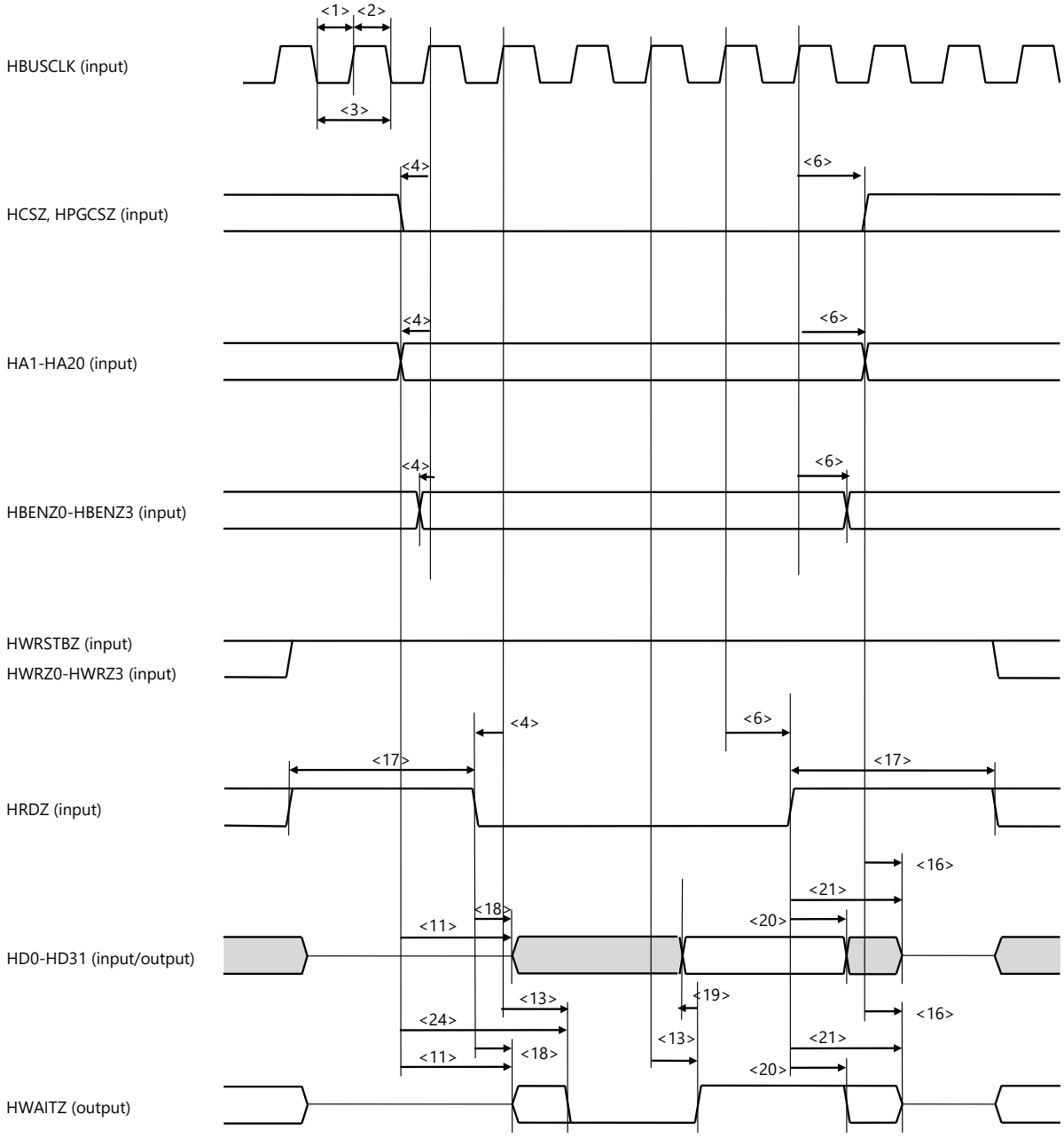


Figure 6.7.4-2 Synchronous SRAM Supported MCU Connection Mode (During Register Access) Read Timing (MEMCSEL=L, HIFSYNC=H)

(c) Page ROM read timing

Supply a stable signal to the address, data, and control lines during access.

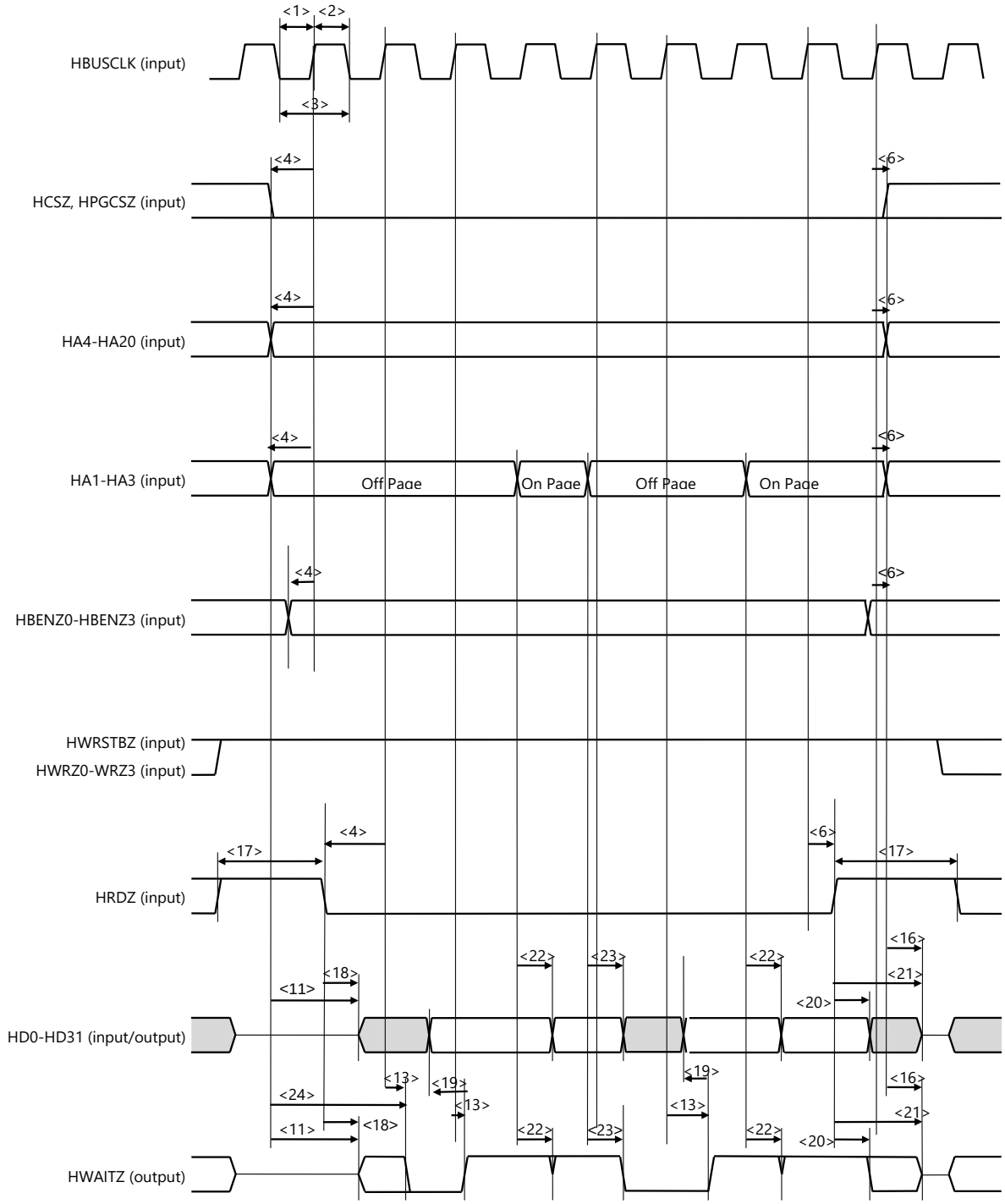


Figure 6.7.4-3 Synchronous SRAM Supported MCU Connection Mode (During Register Access) Page ROM Read Timing (MEMCSEL=L, HIFSYNC=H)

(2) Asynchronous SRAM supported MCU connection mode
For details, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

Table 6.7.4-2 Access Timing: Asynchronous SRAM Supported MCU Connection Mode

No.	Parameter	Symbol	MIN.	MAX.	Unit
1	Address, HCSZ/HPGCSZ, and HBENZ0-HBENZ3 input setup time (for HWRSTBZ, HWRZ0-HWRZ3 ↓)	t_{ADDWRS}	7.0*1 - 10×n	-	ns
2	HWRZ0-HWRZ3, HWRSTBZ recovery time (High-level width)	t_{WRW}	35.0	-	ns
3	Data input setup time (for HWRSTBZ, HWRZ0-HWRZ3 ↓)	t_{WRS}	7.0*1 - 10×n	-	ns
4	Data input hold time (for HWRSTBZ, HWRZ0-HWRZ3 ↑)	t_{WRH}	7.0	-	ns
5	HWAITZ output delay time (for HCSZ or HPGCSZ ↓)	t_{CLZ}	2.2	-	ns
6	HWAITZ output delay time (for HWRSTBZ, HWRZ0-HWRZ3 ↓)	t_{WAITD}	2.2	-	ns
7	HWAITZ valid data output delay time (for HWRSTBZ, HWRZ0-HWRZ3 ↓)	$t_{WRWAITF}$	-	15.4	ns
8	HWAITZ valid data output hold time (for HWRSTBZ, HWRZ0-HWRZ3 ↑)	t_{WAITVH}	4.2	-	ns
9	HWAITZ output hold time (for HWRZ0-3, HWRSTBZ ↑)	t_{WAITH}	-	16.8	ns
10	Address and HWAITZ output hold time (for HCSZ, HPGCSZ ↑)	t_{CHZ}	-	16.8	ns
11	Address and HCSZ, HPGCSZ input setup time (for HRDZ ↓)	t_{ADDRDS}	6.2*2 - 10 × n	-	ns
12	Address input hold time in page access (for HRDZ ↑)	t_{ADDRDH}	7.0	-	ns
13	HRDZ recovery time (High-level width)	t_{RDW}	35.0	-	ns
14	Data, HWAITZ output delay time (for HRDZ ↓)	t_{RDLZ}	2.2	-	ns
15	HWAITZ valid data output delay time (for HRDZ ↓)	$t_{RDWAITF}$	-	15.4	ns
16	Data fixing time (for HWAITZ ↑)	t_{WAITR}	-	-6.2*3 + 10×n	ns
17	Data and HWAITZ valid data output hold time (for HRDZ ↑)	t_{DATAOH}	2.2	-	ns
18	Data and HWAITZ output hold time (for HRDZ ↑)	t_{RDHZ}	-	16.8	ns
19	Data and HWAITZ output delay time in on-page access (for addresses)	$t_{PAGEOND}$	4.2	15.4	ns
20	Data and HWAITZ output delay time in off-page access (for addresses) (when not crossing a 16-byte boundary)	$t_{PAGEOFD}$	4.2	15.4	ns
	Data and HWAITZ output delay time in off-page access (for addresses) (when crossing a 16-byte boundary)	$t_{PAGEOFD}$	4.2	49.5	ns
21	HWAITZ valid data output delay time (for HCSZ, HPGCSZ ↓)	t_{WAITVD}	-	15.4	ns

*1: When the value of WRSTD2 to WRSTD0 in the HIFBTC register is 000b. (n: setting of WRSTD2 to WRSTD0)
*2: When the value of RDSTD1 to RDSTD0 in the HIFBTC register is 00b. (n: setting of RDSTD1 to RDSTD0)
*3: When the value of RDDTS1 to RDDTS0 in the HIFBTC is 00b. (n: setting of RDDTS1 to RDDTS0)

(a) Write timing

Supply a stable signal to the address, data, and control lines during access.

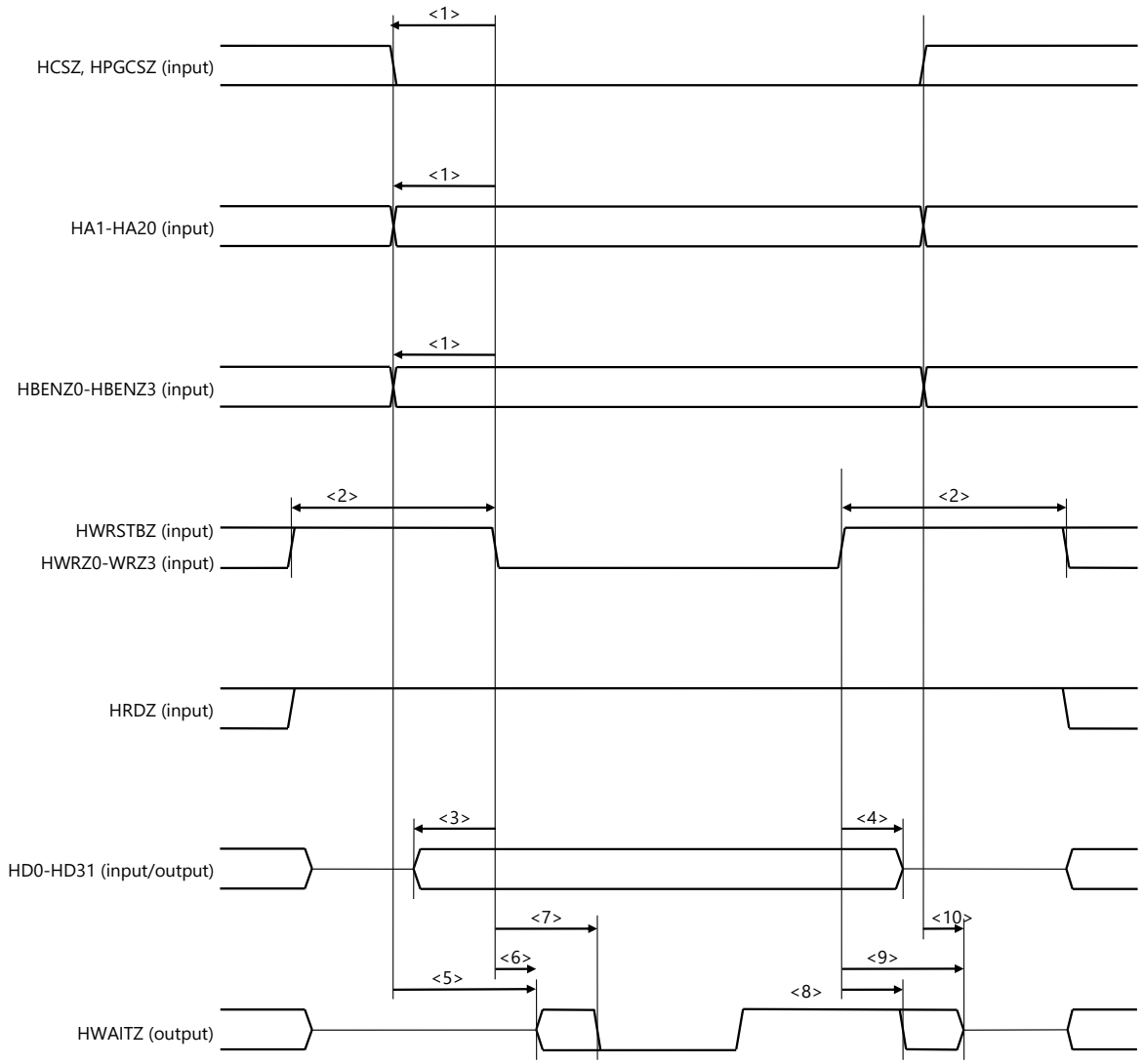


Figure 6.7.4-4 Asynchronous SRAM Supported MCU Connection Mode Write Timing (MEMCSEL=L, HIFSYNC=L)

(b) Read timing

Supply a stable signal to the address, data, and control lines during access.

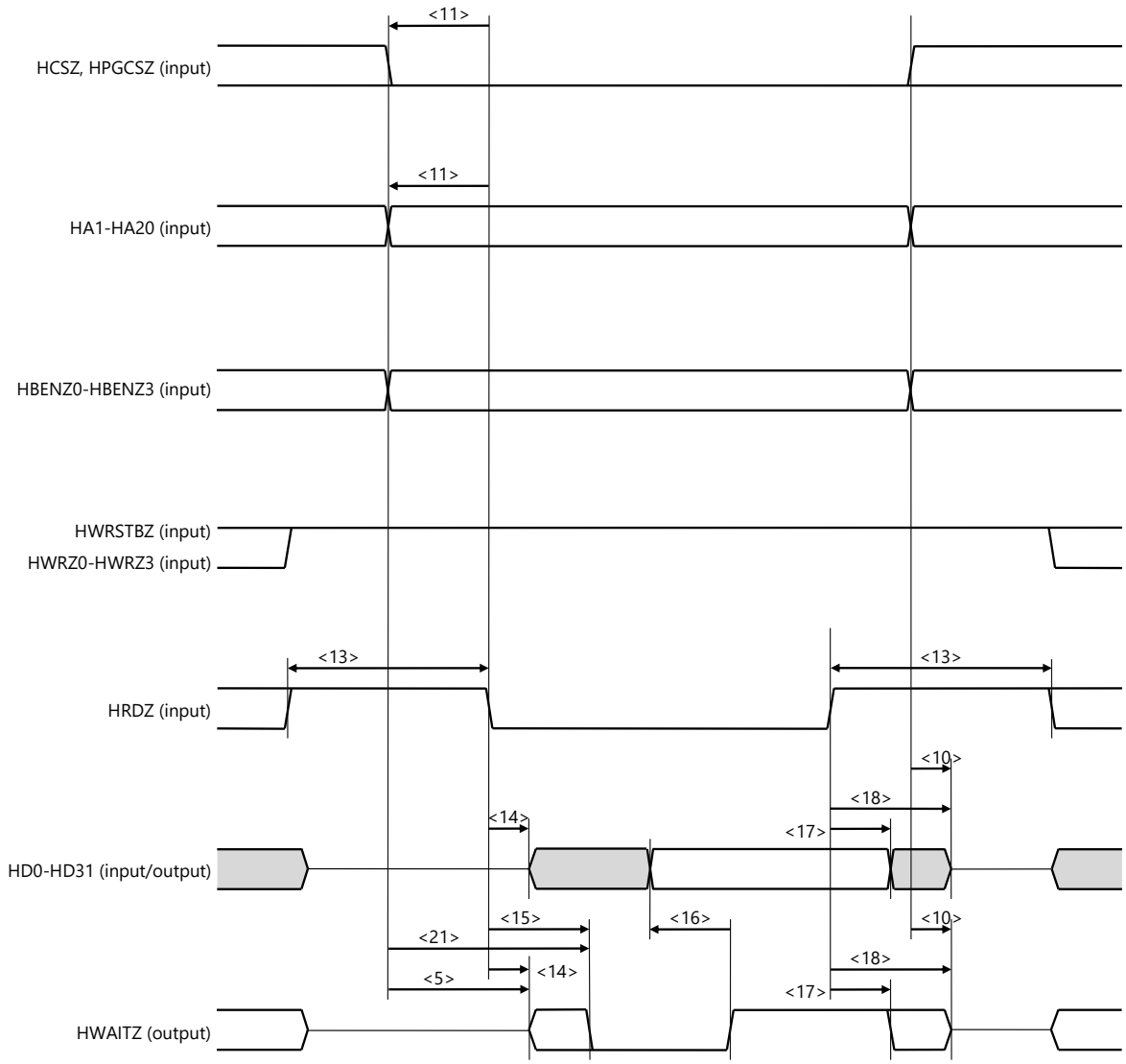


Figure 6.7.4-5 Asynchronous SRAM Supported MCU Connection Mode Read Timing (MEMCSEL=L, HIFSYNC=L)

(c) Page ROM read timing

Supply a stable signal to the address, data, and control lines during access.

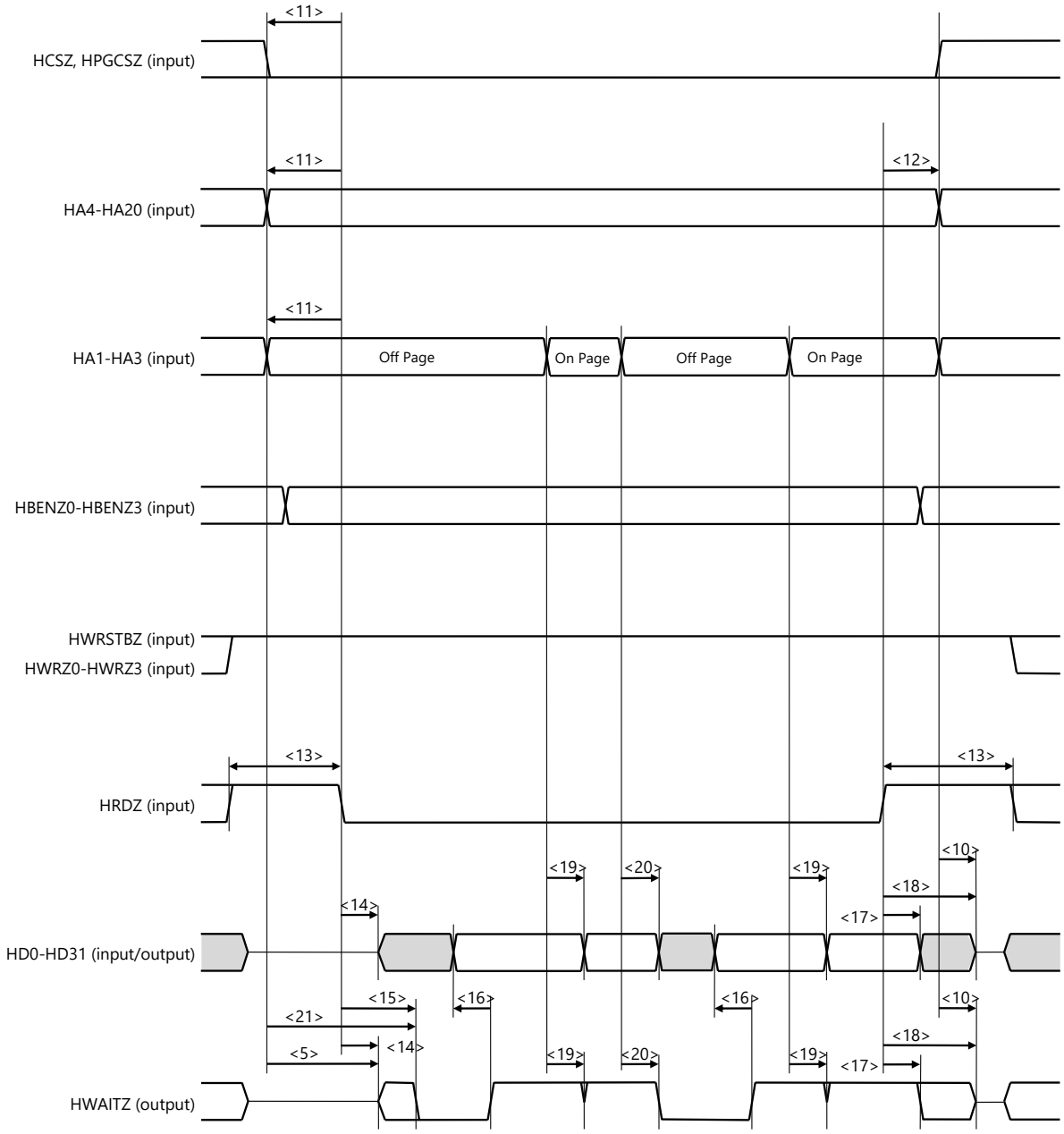


Figure 6.7.4-6 Asynchronous SRAM Supported MCU Connection Mode Page ROM Read Timing (MEMCSEL=L, HIFSYNC=L)

(3) Synchronous burst transfer supported MCU connection mode

Table 6.7.4-3 Access Timing: Synchronous Burst Transfer Supported MCU Connection Mode

No.	Parameter	Symbol	MIN.	MAX.	Unit
1	HBUSCLK High-level width	t_{HBHIGH}	$0.5t_{HBUSCLK}$-2.1	$0.5t_{HBUSCLK}$+2.1	ns
2	HBUSCLK Low-level width	t_{HBLOW}	$0.5t_{HBUSCLK}$-2.1	$0.5t_{HBUSCLK}$+2.1	ns
3	HBUSCLK input cycle	$t_{HBUSCLK}$	20	-	ns
4	Address and HCSZ/HPGCSZ input setup time (for HBUSCLK ↑)	t_{SKPHA}	4.0	-	ns
5	Address and HCSZ/HPGCSZ input hold time (for HBUSCLK ↑)	t_{HKPCS}	1.0	-	ns
6	Address and HCSZ/HPGCSZ input setup time (for HBUSCLK ↓)	t_{SKNHA}	4.0	-	ns
7	Address and HCSZ, HPGCSZ input hold time (for HBUSCLK ↓)	t_{HKNHA}	1.0	-	ns
8	HWRZ0-HWRZ3 input setup time (for HBUSCLK ↑)	t_{SKPHWR}	4.0	-	ns
9	HWRZ0-HWRZ3 input hold time (for HBUSCLK ↑)	t_{HKPHWR}	1.0	-	ns
10	HWRZ0-HWRZ3 input setup time (for HBUSCLK ↓)	t_{SKNHWR}	4.0	-	ns
11	HWRZ0-HWRZ3 input hold time (for HBUSCLK ↓)	t_{HKNHWR}	1.0	-	ns
12	HBCYSTZ and HWRSTBZ input setup time (for HBUSCLK ↑)	$t_{SKPHBCY}$	4.0	-	ns
13	HBCYSTZ and HWRSTBZ input hold time (for HBUSCLK ↑)	$t_{HKPHBCY}$	1.0	-	ns
14	HBCYSTZ and HWRSTBZ input setup time (for HBUSCLK ↓)	$t_{SKNHBCY}$	4.0	-	ns
15	HBCYSTZ and HWRSTBZ input hold time (for HBUSCLK ↓)	$t_{HKNHBCY}$	1.0	-	ns
16	HRDZ input setup time (for HBUSCLK ↑)	t_{SKPHRD}	4.0	-	ns
17	HRDZ input hold time (for HBUSCLK ↑)	t_{HKPHRD}	1.0	-	ns
18	HRDZ input setup time (for HBUSCLK ↓)	t_{SKNHRD}	4.0	-	ns
19	HRDZ input hold time (for HBUSCLK ↓)	t_{HKNHRD}	1.0	-	ns
20	Data input setup time (for HBUSCLK ↑)	t_{SKPHD}	4.0	-	ns
21	Data input hold time (for HBUSCLK ↑)	t_{HKPHD}	1.0	-	ns
22	Data input setup time (for HBUSCLK ↓)	t_{SKNHD}	4.0	-	ns
23	Data input hold time (for HBUSCLK ↓)	t_{HKNHD}	1.0	-	ns
24	Data output delay time (for HRDZ ↓)	t_{DKNHRD}	2.2	-	ns
25	Data output hold time (for HRDZ ↑)	t_{HKPHRD}	-	16.8	ns
26	Data output delay time (for HBUSCLK ↑)	t_{DKPHD}	2.0	10.0	ns
27	Data output delay time (for HBUSCLK ↓)	t_{DKNHD}	2.0	10.0	ns
28	HWAITZ output delay time (for HBUSCLK ↑)	t_{DKPHWT}	2.0	11.0	ns
29	HWAITZ output delay time (for HBUSCLK ↓)	t_{DKNHWT}	2.0	11.0	ns
30	Data output hold time (for HCSZ/HPGCSZ ↑)	t_{HKPHCS}	-	16.8	ns

(a) Write timing (separation of address and data)
Supply a stable signal to the address, data, and control lines during access.

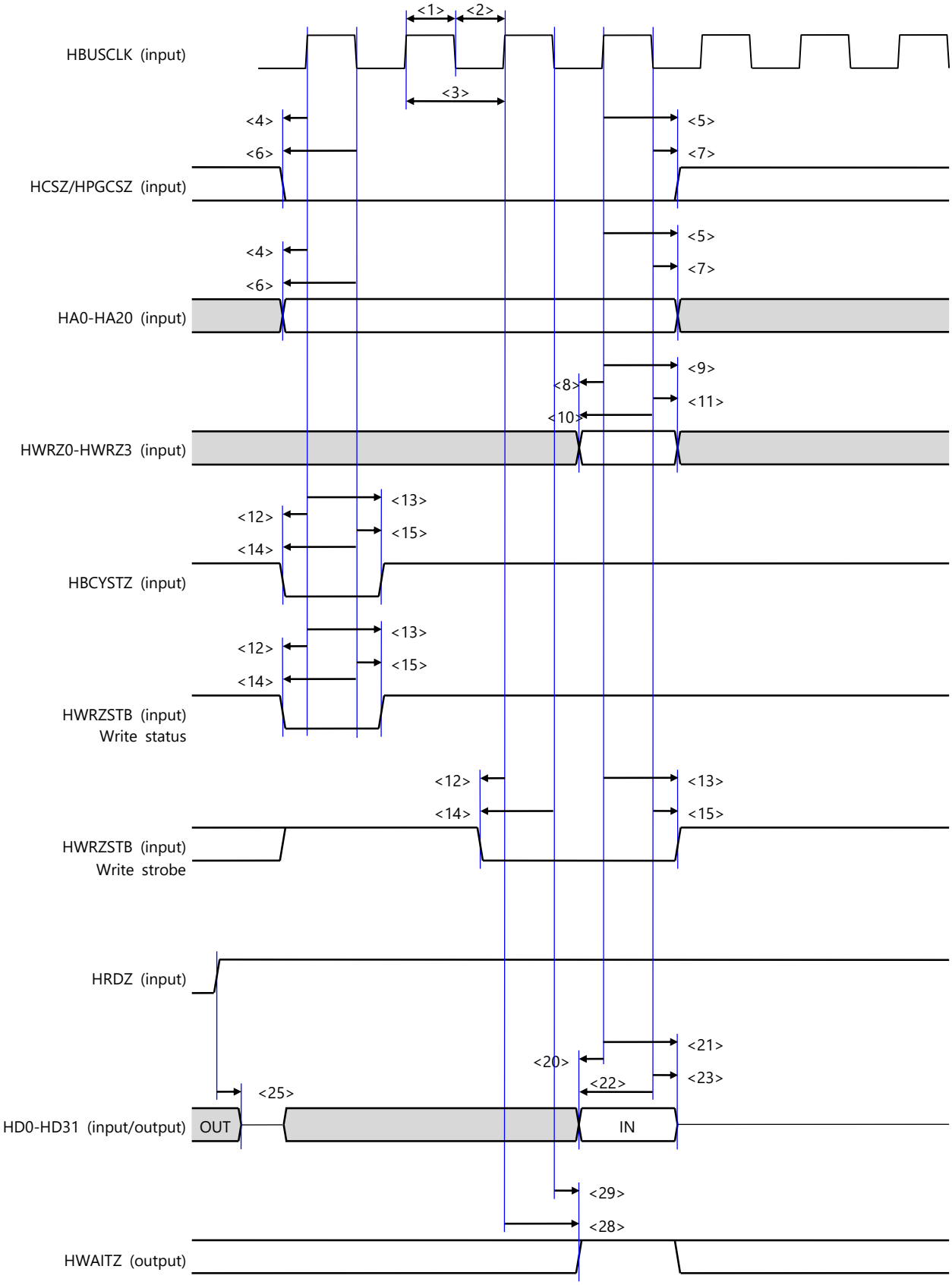


Figure 6.7.4-7 Synchronous Burst Transfer Supported MCU Connection Mode Write Timing (MEMCSEL=H, ADMUXMODE=L)

(b) Read timing (separation of address and data)
Supply a stable signal to the address, data, and control lines during access.

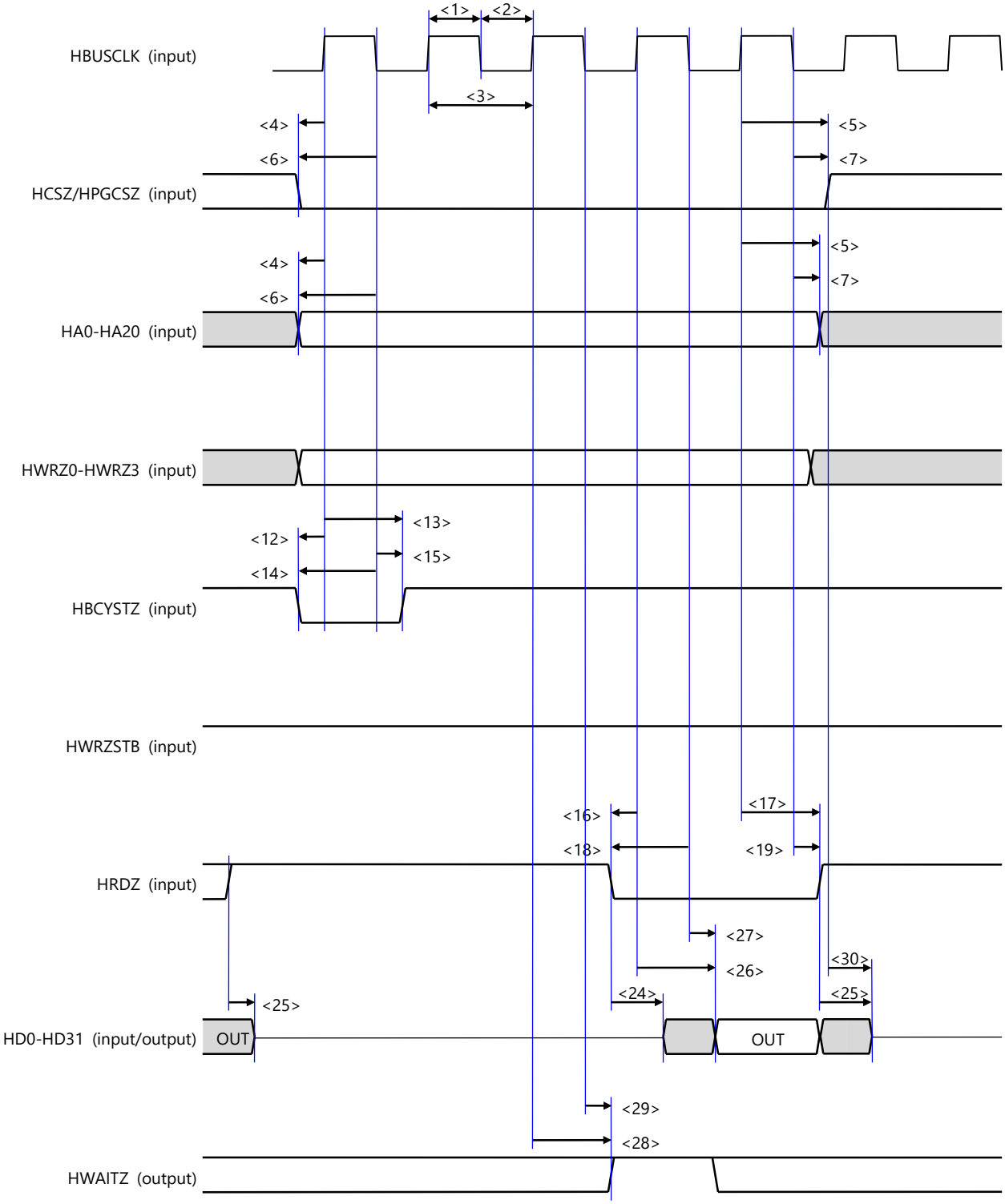


Figure 6.7.4-8 Synchronous Burst Transfer Supported MCU Connection Mode Read Timing (MEMCSEL=H, ADMUXMODE=L)

(c) Write timing (multiplexing of address and data)
Supply a stable signal to the address, data, and control lines during access.

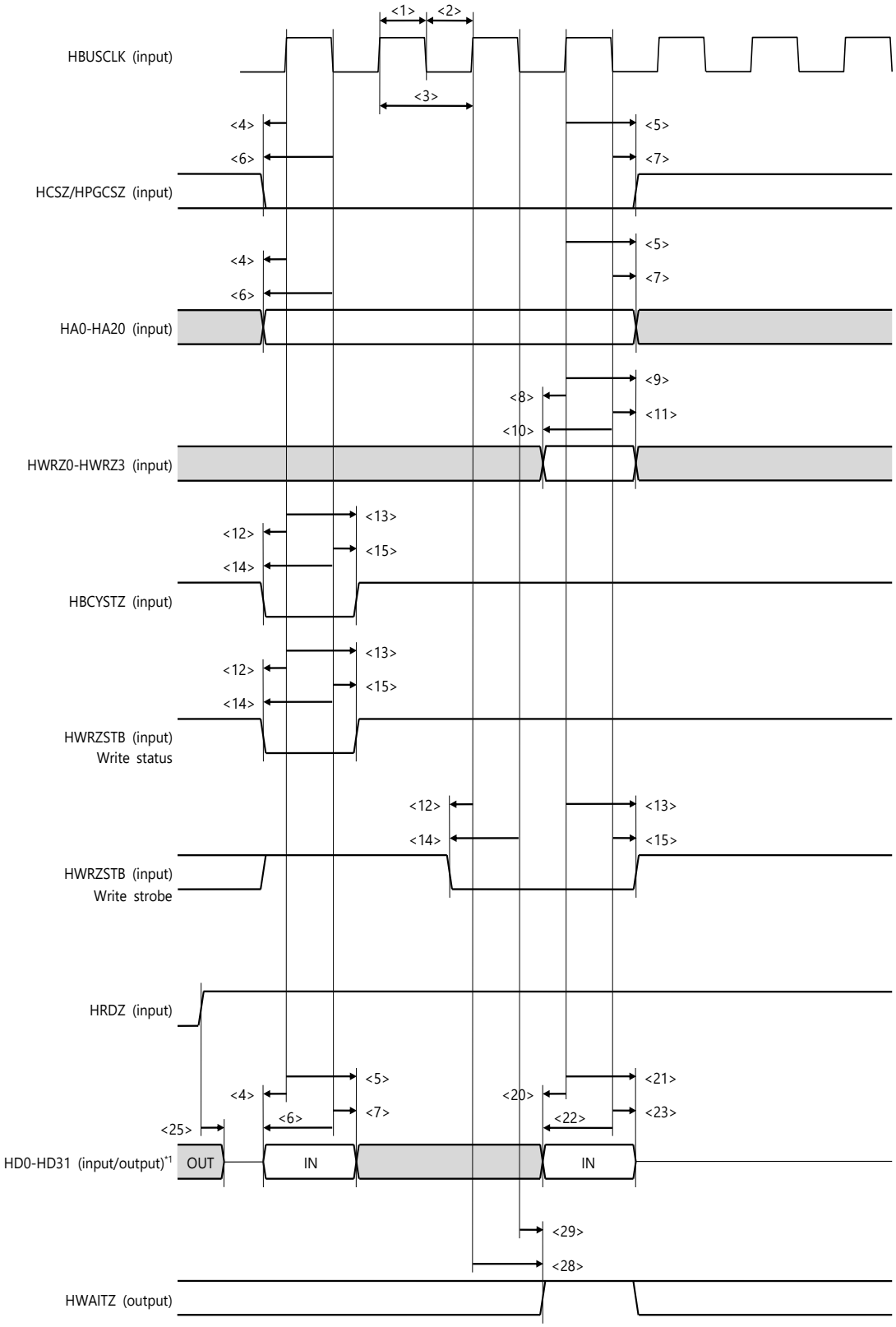


Figure 6.7.4-9 Synchronous Burst Transfer Supported MCU Connection Mode Write Timing (MEMCSEL=H, ADMUXMODE=H)

*1: The address is acquired from a different source depending on the data bus width.
16-bit data bus: Address = {HA[20:17], HWDATA[15:0], 1'b0}
32-bit data bus: Address = {HWDATA[18:0], 2'b00}

(d) Read timing (multiplexing of address and data)
Supply a stable signal to the address, data, and control lines during access.

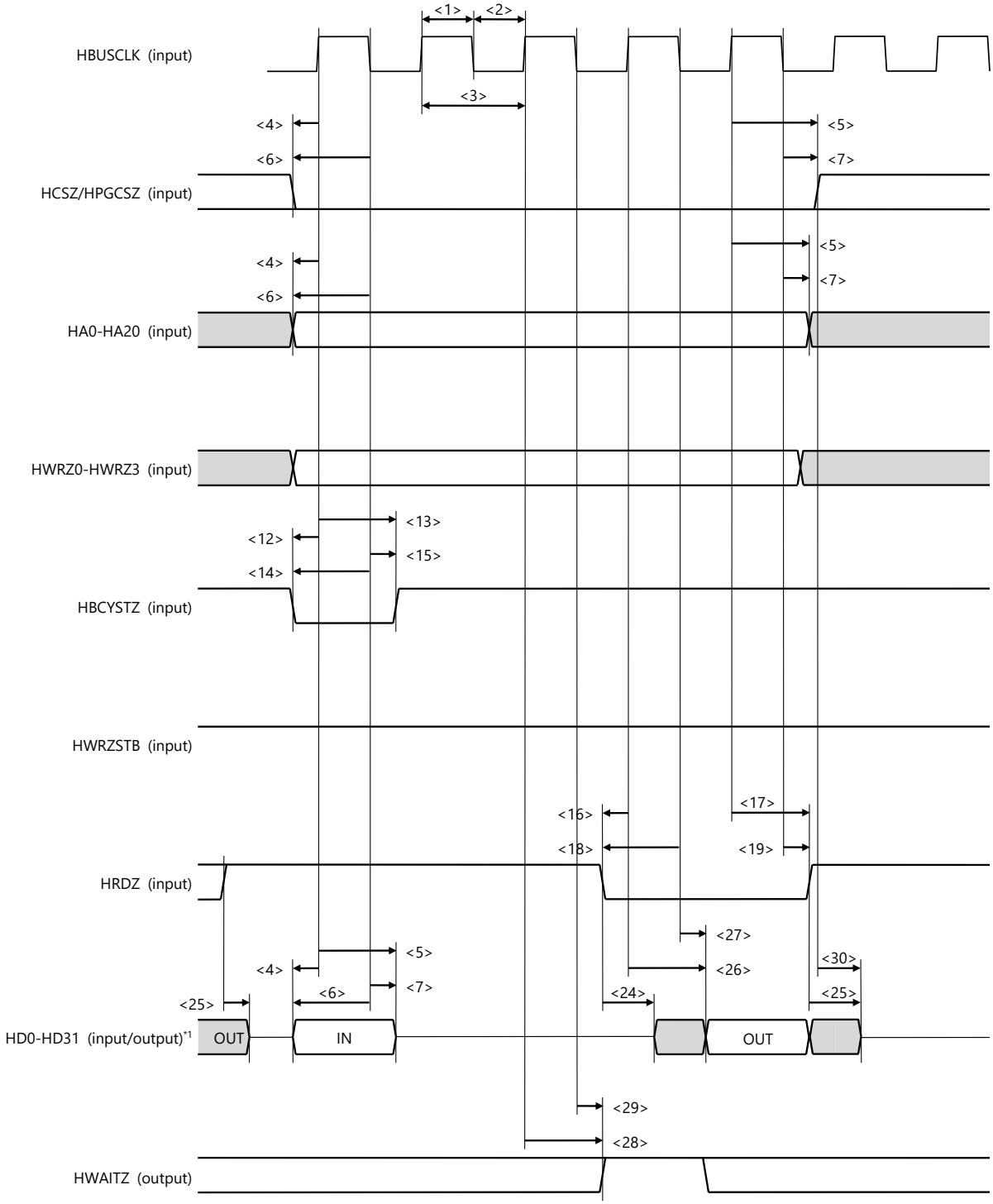


Figure 6.7.4-10 Synchronous Burst Transfer Supported MCU Connection Mode Read Timing (MEMCSEL=H, ADMUXMODE=H)

*1: The address is acquired from a different source depending on the data bus width.
16-bit data bus: Address = {HA[20:17], HWDATA[15:0], 1'b0}
32-bit data bus: Address = {HWDATA[18:0], 2'b00}

Table 6.7.5-1 Serial Flash ROM Interface

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SMSCK output cycle	t_{SFRCYC}	C_L = 15pF	20	-	ns
SMSCK High-level width	t_{SMCKH}		0.5 t_{SFRCYC} - 2.0	0.5 t_{SFRCYC} + 2.0	ns
SMSCK Low-level width	t_{SMCKL}		0.5 t_{SFRCYC} - 2.0	0.5 t_{SFRCYC} + 2.0	ns
SMSCK rising time	t_{SMCKR}		-	1.9	ns
SMSCK falling time	t_{SMCKF}		-	1.9	ns
Delay time between SMCSZ falling and SMSCK rising	$t_{DSMCSCK}$	C_L = 15pF Freq = 50MHz	6.0*1	-	ns
Hold time from SMSCK rising to SMCSZ rising	$t_{DSMCKCS}$	C_L = 15pF Freq = 50MHz	9.0*1	-	ns
SMCSZ High-level width	t_{SMCSH}	C_L = 15pF	14*1	-	ns
SMIO0-3 input setup time (for SMSCK ↓)	t_{SSMIO}	-	6.0	-	ns
SMIO0-3 input hold time (for SMSCK ↓)	t_{HSMIO}	-	0	-	ns
SMIO0-3 output delay time (for SMSCK ↓)	t_{DSMIO}	C_L = 15pF	-1.0	5.0	ns

*1: The timing can be extended by the setting of the SFMSSC register. For details, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

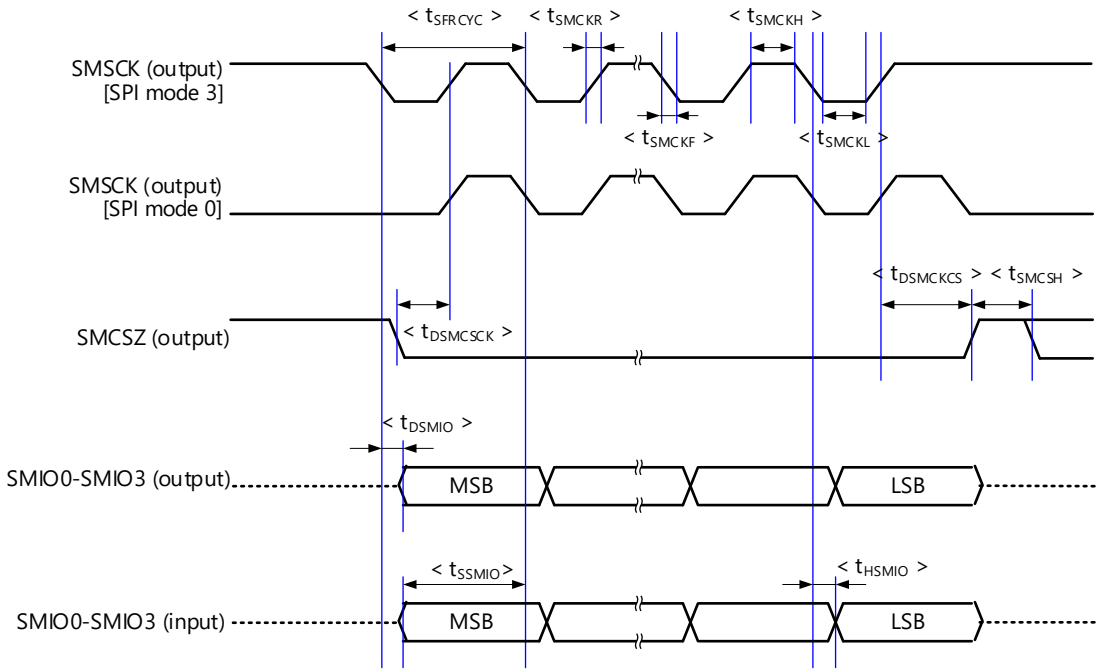


Figure 6.7.5-1 Serial Flash ROM Access Timing

Table 6.7.6-1 External DMA Interface

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
DMAREQZn and RTDMAREQZ input setup time (for BUSCLK ↑)	t_{SKDR}	-	7.0	-	ns
DMAREQZn and RTDMAREQZ input hold time 1	t_{HKDR1}	-	Until DMAACKZ↓, RTDMAACKZ↓	-	ns
DMAREQZn and REDMAREQZ input hold time 2 (for BUSCLK ↑)	t_{HKDR2}	-	-	t_{BUSCLK}*1 × m*2 - 7.0	ns
DMAACKZn and RTDMACKZ output delay time (for BUSCLK ↑)	t_{DKDA}	C_L = 30pF	2.0	10.0	ns
DMAACKZn and RTDMAACKZ output Low-level width	t_{WDAL}	-	t_{BUSCLK}*1 × m*2 - 8	t_{BUSCLK}*1 × m*2 + 8	ns
DMATCZn and RTDMATCZ output delay time (for BUSCLK ↑)	t_{DKTC}	C_L = 30pF	2.0	10.0	ns

*1: t_{BUSCLK} is one cycle (10ns) of BUSCLK.
*2: n = 0 or 1, m = 1 to 31 (DMAIFC0, DMAIFC1, and RTMDAIFC registers)

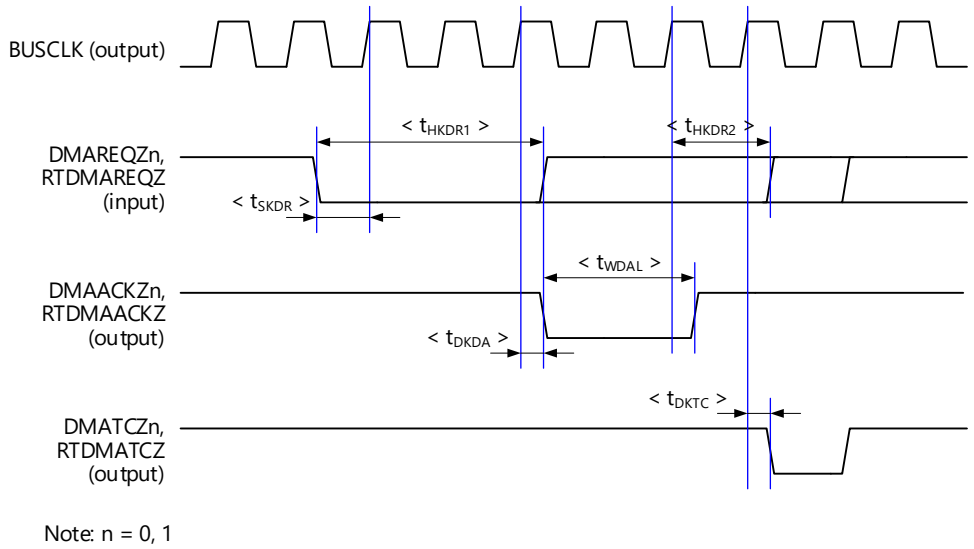


Figure 6.7.6-1 External DMA Access Timing

6.7.7 Clocked serial interface

The clocked serial interface (CSI) supports master mode and slave mode.

(1) CSI master mode

Table 6.7.7-1 CSI Master Mode

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
CSISCKn output cycle	$t_{CSIMSCK}$	C_L = 15pF	40	-	ns
CSISCKn output High-level width	t_{WSKH}	C_L = 15pF	$t_{CSIMSCK}$ × 0.5 - 5.0	-	ns
CSISCKn output Low-level width	t_{WSKL}	C_L = 15pF	$t_{CSIMSCK}$ × 0.5 - 5.0	-	ns
CSISIn input setup time (for CSISCKn ↑)	t_{SMSI}	-	8.5	-	ns
CSISIn input setup time (for CSISCKn ↓)	t_{SMSI}	-	8.5	-	ns
CSISIn input hold time (for CSISCKn ↑)	t_{HMSI}	-	7.0	-	ns
CSISIn input hold time (for CSISCKn ↓)	t_{HMSI}	-	7.0	-	ns
CSISOn output delay time (for CSISCKn ↑)	t_{DMSO}	C_L = 15pF	-	7.0	ns
CSISOn output delay time (for CSISCKn ↓)	t_{DMSO}		-	7.0	ns
CSISOn output hold time (for CSISCKn ↑)	t_{HMSO}		$t_{CSIMSCK}$ × 0.5 - 5.0	-	ns
CSISOn output hold time (for CSISCKn ↓)	t_{HMSO}		$t_{CSIMSCK}$ × 0.5 - 5.0	-	ns

*: n = 0, 1

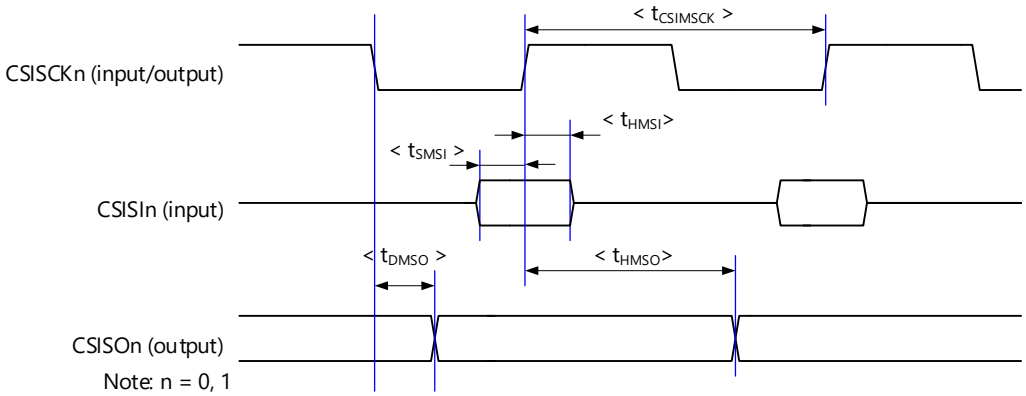


Figure 6.7.7-1 CSI Access Timing (Master Mode)

*: The above figure shows an example of the timing for data output of "for CSISCKn ↓" and data input of "for CSISCKn ↑". Read the timing for reference according to the operating mode.

(2) CSI slave mode

Table 6.7.7-2 CSI Slave Mode

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
CSISCKn input cycle	$t_{CSISSCK}$	-	60	-	ns
CSISCKn input High-level width	t_{WSKH}	-	$t_{CSISSCK}$ × 0.5 - 5.0	-	ns
CSISCKn input Low-level width	t_{WSKL}	-	$t_{CSISSCK}$ × 0.5 - 5.0	-	ns
CSISIn input setup time (for CSISCKn ↑)	t_{SSI}	-	10.0	-	ns
CSISIn input setup time (for CSISCKn ↓)	t_{SSI}	-	10.0	-	ns
CSISIn input hold time (for CSISCKn ↑)	t_{HSI}	-	15	-	ns
CSISIn input hold time (for CSISCKn ↓)	t_{HSI}	-	15	-	ns
CSISOn output delay time (for CSISCKn ↑)	t_{DSSO}	C_L = 15pF	-	10.0	ns
CSISOn output delay time (for CSISCKn ↓)	t_{DSSO}		-	10.0	ns
CSISOn output hold time (for CSISCKn ↑)	t_{HSSO}		$t_{CSISSCK}$ × 0.5 - 5.0	-	ns
CSISOn output hold time (for CSISCKn ↓)	t_{HSSO}		$t_{CSISSCK}$ × 0.5 - 5.0	-	ns

*: n = 0, 1

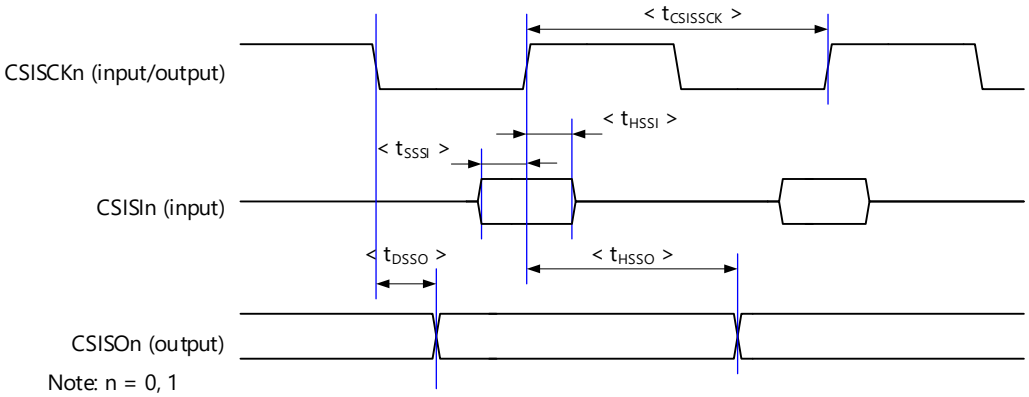


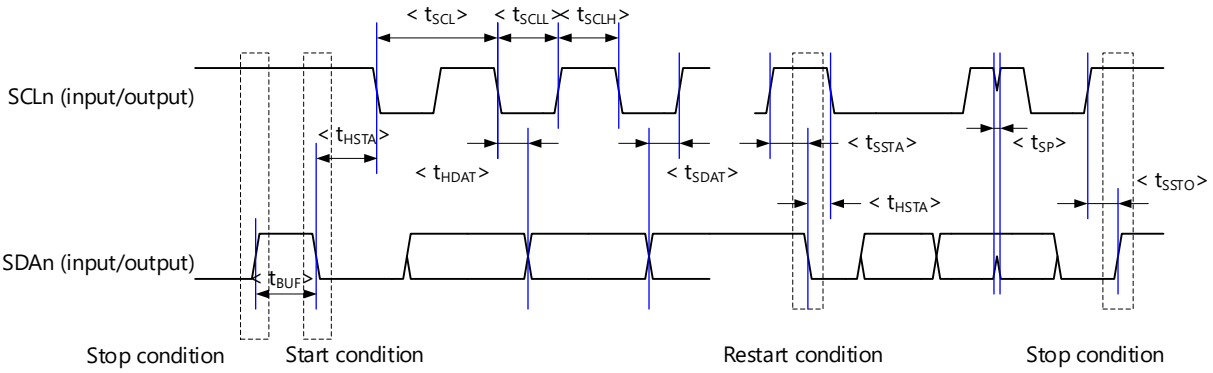
Figure 6.7.7-2 CSI Access Timing (Slave Mode)

*: The above figure shows an example of the timing for data output of "for CSISCKn ↓" and data input of "for CSISCKn ↑". Read the timing for reference according to the operating mode.

Table 6.7.8-1 I2C Interface

Parameter		Symbol	Conditions	Normal Mode		High-Speed Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLn input/output frequency		t_{SCL}	C_L = 30pF	0	100	0	400	kHz
Bus-free time between the stop condition and start condition		t_{BUF}		4.7	-	1.3	-	µs
Hold time		t_{HSTA}		4.0	-	0.6	-	µs
SCLn clock Low-level width		t_{SCLL}		4.7	-	1.3	-	µs
SCLn clock High-level width		t_{SCLH}		4.0	-	0.6	-	µs
Setup time for the start and restart conditions		t_{SSTA}		4.7	-	0.6	-	µs
Data hold time	For a CBUS compatible master	t_{HDAT}		-	-	-	-	µs
	For an I2C bus			-	-	0	0.9	µs
Data setup time		t_{SDAT}		250	-	100	-	ns
SDAn and SCLn rising time		t_{SCLR}		-	1000	20 + 0.1C_b	300	ns
SDAn and SCLn falling time		t_{SCLF}		-	300	20 + 0.1C_b	300	ns
Stop condition setup time		t_{SSTO}		4.0	-	0.6	-	µs
Pulse width of spike suppressed by input filter		t_{SP}		-	-	0	50	ns
Capacitance load of each bus line		C_b	-	-	400	-	400	pF

*: n = 0, 1



Note: n = 0, 1
The figure does not cover t_{SCLR} and t_{SCLF}.

Figure 6.7.8-1 I2C Access Timing

6.7.9 Debugging interface

(1) Debugging serial interface

Table 6.7.9-1 Debugging Serial Interface

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
TCK input cycle	t_{TCK}	-	20	-	ns
TMS input setup time (for TCK ↑)	t_{STMS}	-	6.5	-	ns
TMS input hold time (for TCK ↑)	t_{HTMS}	-	0	-	ns
TDI input setup time (for TCK ↑)	t_{STDI}	-	6.5	-	ns
TDI input hold time (for TCK ↑)	t_{HTDI}	-	0	-	ns
TDO output delay time (for TCK ↓)	t_{DTDO}	C_L = 30pF	3.0	13.0	ns

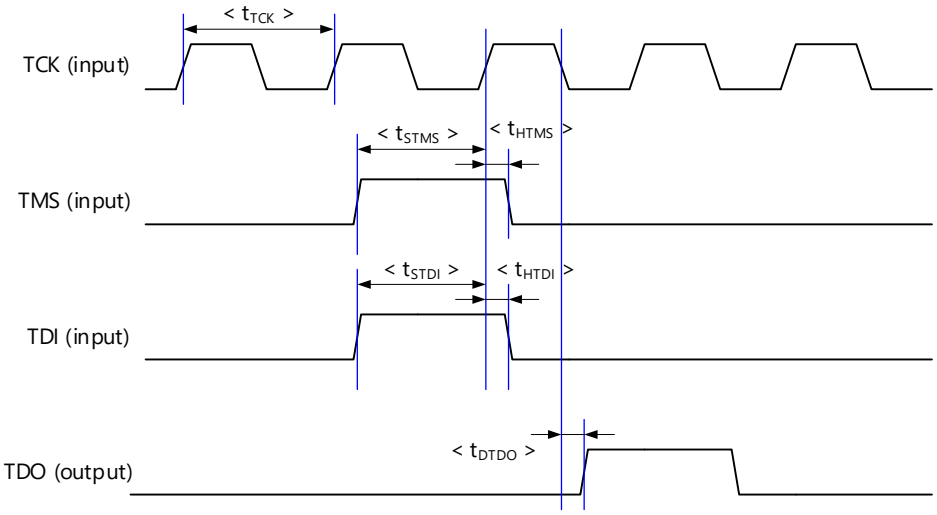


Figure 6.7.9-1 Debugging Serial Access Timing

(2) Trace interface

Table 6.7.9-2 Trace Interface

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
TRACECLK output cycle	t_{TRCCLK}	C_L = 15pF	20	-	ns
TRACEDATAn output delay time (for TRACECLK)	$t_{DTRCDAT}$	C_L = 15pF	0.26	8.43	ns

*: n = 0-3

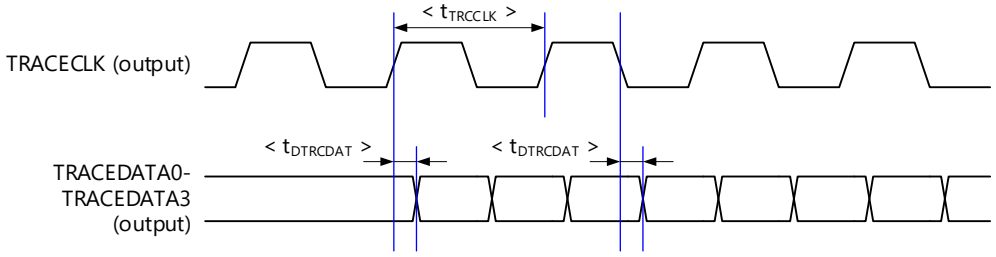


Figure 6.7.9-2 Trace Access Timing

7 DEVELOPING A CP520 APPLICATION CIRCUIT

This chapter describes how to develop a CP520 application circuit based on a CP520 application circuit diagram example (drawing_CP520.pdf).
Design a CP520 application circuit referring to the provided circuit diagram example.
Note that the components used in the example are described in Section 7.2 "Component List". Refer to this list when selecting components.

7.1 CP520 Application Circuit Diagram Example

The CP520 application circuit diagram example is provided in PDF format in the Manual folder on the provided CD-ROM. For details on the provided CD-ROM, refer to Section 1.4 "Enclosed CD-ROM".

Note
Provide single-point grounding for 2GND and GND in the power supply peripheral circuit as much as possible to separate the 2GND pattern and GND pattern.

7.2 Component List

The components shaded in the table require caution at the time of selection. Select the components while referring to Section 7.3.1 "Component selection precautions".

Note that the components are listed as reference, and not specified components. Select each component as required. For inquiries and purchasing, contact the respective manufacturers.
The component model names in the lists are subject to change without notice by the respective manufacturers.

7.2.1 Component list (CP520 peripheral circuits)

"Table 7.2.1-1 List of Components Used in CP520 Application Circuit Diagram Example (Peripheral Circuits)" and "Table 7.2.1-2 List of Components Reserved in CP520 Application Circuit Diagram Example (Peripheral Circuits)" list the components used in the CP520 application circuit diagram example (peripheral circuits).

Table 7.2.1-1 List of Components Used in CP520 Application Circuit Diagram Example (Peripheral Circuits)

No.	Symbol	Qty	Product Name	Specifications	Model Name	Manufacturer
1	C35, C37, C41	3	Capacitor	470pF, 50V	GRM155B11H471KA01D	Murata Manufacturing Co., Ltd.
2	C63, C64, C65, C66, C67, C68, C79, C80, C81, C82, C83, C84, C90, C91, C99, C100, C101, C102, C103, C104	20	Capacitor	1000pF, 50V	GRM1552C1H102JA01D	Murata Manufacturing Co., Ltd.
3	C30, C32	2	Capacitor	1000pF, 2kV	CF42X7R102K2000AT	Kyocera Crystal Device Corporation
4	C29, C31	2	Capacitor	2200pF, 2kV	CF43X7R222M2000AT	Kyocera Crystal Device Corporation
5	C40, C44, C54, C55, C56, C57, C70, C71, C72, C73	10	Capacitor	0.01µF, 25V	GRM155B11E103KA01D	Murata Manufacturing Co., Ltd.
6	C1, C2, C3, C4, C36, C38, C46, C47, C48, C49, C51, C52, C58, C59, C60, C61, C62, C74, C75, C76, C77, C78, C86, C87, C88, C89, C93, C94, C95, C96, C97, C98, C107, C108, C109, C110, C111, C112, C113, C114, C115, C116, C117	43	Capacitor	0.1µF, 10V	GRM155B11A104KA01D	Murata Manufacturing Co., Ltd.
7	C6, C9, C12, C15, C18, C21, C24, C27, C34	9	Capacitor	0.1µF, 25V	GRM155B31E104KA87D	Murata Manufacturing Co., Ltd.
8	C33	1	Capacitor	1.0µF, 25V	GRM188R71E105KA12D	Murata Manufacturing Co., Ltd.
9	C39, C45, C50, C53, C69, C85, C106	7	Capacitor	10µF, 10V	GRM21BR71A106KE51L	Murata Manufacturing Co., Ltd.
10	C42, C43, C92	3	Capacitor	10µF, 10V	GRM21BB31A106KE18L	Murata Manufacturing Co., Ltd.
11	C105	1	Capacitor	47µF, 16V	GRM32EB31C476KE15L	Murata Manufacturing Co., Ltd.
12	CON1	1	ICE connector	-	FTSH-110-01-L-DV-K	Samtec Inc.
13	CON2, CON3	2	RJ-45 connector	-	2201061-1	Tyco Electronics Japan G.K.
14	CU1	1	25MHz crystal oscillator	-	KC2520B25.0000C1GESJ	Kyocera Crystal Device Corporation
15	CU2	1	2.097152MHz crystal oscillator	-	KC2520B2.09715C1GESJ	Kyocera Crystal Device Corporation
16	IC1, IC2, IC6, IC7	4	Logic IC	-	TC7SH08FU(TE85L,JF)	Toshiba Semiconductor & Storage
17	IC5	1	Logic IC	-	TC7W125FU(TE12L)	Toshiba Semiconductor & Storage
18	IC3	1	CP520 (PC15001R-B)	-	NZ2GACP520-60 (60 units in package)	Mitsubishi Electric Corporation
19	IC4	1	Serial flash	-	MX25L8006EM2I-12G	Macronix International Co., Ltd.
20	L1, L2	2	Ferrite bead	600Ω	BLM18AG601SN1D	Murata Manufacturing Co., Ltd.
21	L3, L4, L5, L6	4	Ferrite bead	120Ω	BLM18PG121SN1D	Murata Manufacturing Co., Ltd.
22	LED1, LED2, LED3, LED7, LED8, LED9, LED10, LED11	8	LED	-	19-21SYGC/S530-E3/TR8	Everlight Electronics Co., Ltd.
23	LED4, LED5, LED6	3	LED	-	19-21/R8C-AN1P2B-3T (ELJ)	Everlight Electronics Co., Ltd.
24	R2, R3, R4, R5, R6, R7, R8, R9, R10, R45, R46, R47, R48, R65, R66, R67, R68	17	Resistor	0Ω, 1A	RPC03T0R0	Taiyosha Electric Co., Ltd.
25	R36, R37, R38, R39, R40, R41, R42, R43	8	Resistor	10kΩ, 1/10W	RK73B1JTTD750J	KOA Corporation

No.	Symbol	Qty	Product Name	Specifications	Model Name	Manufacturer
26	R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R93	12	Resistor	470Ω, 1/10W	RPC03T471J	Taiyosha Electric Co., Ltd.
27	R89, R90, R91, R92	4	Resistor	1kΩ, 1/10W	RPC03T102J	Taiyosha Electric Co., Ltd.
28	R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84	16	Resistor	1.8kΩ, 1/10W	RPC03T182J	Taiyosha Electric Co., Ltd.
29	R44	1	Resistor	2kΩ, 1/10W, 0.5%	HPC05CT202D	Taiyosha Electric Co., Ltd.
30	R18, R19, R20, R21, R22, R23, R24, R85, R86, R87, R88	11	Resistor	4.7kΩ, 1/10W	RPC03T472J	Taiyosha Electric Co., Ltd.
31	R12, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64	17	Resistor	10kΩ, 1/10W	RPC03T103J	Taiyosha Electric Co., Ltd.
32	R1, R11, R13, R14, R15, R16, R17	7	Resistor	47kΩ, 1/10W	RPC03T473J	Taiyosha Electric Co., Ltd.
33	T1, T2	2	Pulse transformer*1	-	MGF101	Sinka Japan Co., Ltd.
34	SW1	1	Rotary switch	Decimal	FR01-KR10P-ST	NKK Switches Co., Ltd.
35	SW2, SW3, SW4	3	Rotary switch	Hexadecimal	FR01-KR16P-ST	NKK Switches Co., Ltd.
36	SW5	1	DIP switch	4-bit	CHS-04TB1	NIDEC COPAL ELECTRONICS CORPORATION

*1: The product H5008FNL manufactured by Pulse Electronics Corporation may also be used.

The components in the table below are non-mounted parts. Be sure to provide a pad.

Table 7.2.1-2 List of Components Reserved in CP520 Application Circuit Diagram Example (Peripheral Circuits)

No.	Symbol	Qty	Product Name	Specifications	Model Name	Manufacturer
1	C7, C10, C13, C16, C19, C22, C25, C28	8	Capacitor	1000pF, 50V	GRM1552C1H102JA01D	Murata Manufacturing Co., Ltd.
2	C5, C8, C11, C14, C17, C20, C23, C26	8	Capacitor	0.01μF, 25V	GRM155B11E103KA01D	Murata Manufacturing Co., Ltd.
3	VAR1, VAR2, VAR3, VAR4, VAR5, VAR6, VAR7, VAR8, VAR9, VAR10, VAR11, VAR12, VAR13, VAR14, VAR15, VAR16	16	Varistor	300V	USB0005WP	Kyocera Crystal Device Corporation

7.2.2 Component list (CP520 power supply peripheral circuit)

"Table 7.2.2-1 List of Components Used in CP520 Application Circuit Diagram Example (Power Supply Peripheral Circuit)" lists the components used in the CP520 application circuit diagram example (power supply circuit).

Table 7.2.2-1 List of Components Used in CP520 Application Circuit Diagram Example (Power Supply Peripheral Circuit)

No.	Symbol	Qty	Product Name	Specifications	Model Name	Manufacturer
1	C151	1	Capacitor	47μF, 16V	GRM21BR61A476ME15L	Murata Manufacturing Co., Ltd.
2	C152, C159	2	Capacitor	10μF, 10V	GRM21BB31A106KE18L	Murata Manufacturing Co., Ltd.
3	C153, C155, C156, C158, C162	5	Capacitor	0.1μF, 10V	GRM155B11A104KA01D	Murata Manufacturing Co., Ltd.
4	C154, C160	2	Capacitor	22μF, 16V	GRM21BC81C226ME44L	Murata Manufacturing Co., Ltd.
5	C161	1	Capacitor	100pF, 50V	GRM1552C1H101JA01D	Murata Manufacturing Co., Ltd.
6	C157	1	Capacitor	1.0μF, 10V	GRM155B31A105KE15D	Murata Manufacturing Co., Ltd.
7	C163	1	Capacitor	47μF, 16V	GRM32ER61C476KE15L	Murata Manufacturing Co., Ltd.
8	IC11	1	Power management IC	-	RAA230215GSB	Renesas Electronics Corporation
9	L13	1	Inductor	2.2μH	CDRH5D28RHPNP-2R2NC	SUMIDA CORPORATION
10	R151, R152	2	Resistor	0Ω, 2A	RK73Z2ATTD	KOA Corporation
11	R153	1	Resistor	100kΩ, 1/10W	HXC05CT104D	Taiyosha Electric Co., Ltd.
12	R154	1	Resistor	47kΩ, 1/10W	HXC05CT473D	Taiyosha Electric Co., Ltd.
13	R155	1	Resistor	16kΩ, 1/10W	HXC05CT163D	Taiyosha Electric Co., Ltd.
14	R156	1	Resistor	62kΩ, 1/10W	HXC05CT623D	Taiyosha Electric Co., Ltd.

7.3 Board Design Precautions

The board design precautions are described in check sheets.

7.3.1 Component selection precautions

Table 7.3.1-1 Component Selection Check Sheet

No.	Item	Description	Components Used in Circuit Diagram Example	Check Results
1	RJ-45 connector	(1) Is the connector an 8-pin ANSI/TIA/EIA-568-B shielded connector? (2) Is the connector 1000BASE-T compatible?	2201061-1 (Tyco Electronics Japan G.K.)	
2	Pulse transformer	(1) Did you select a 1000BASE-T compatible pulse transformer? (2) Is the accuracy of the turn ratio 1.00 (±2%)? (Recommended) (3) Is the return variation between 1-40MHz flat? (Recommended)	MGF101 (Sinka Japan Co., Ltd.)	
3	25MHz crystal oscillator	(1) Did you select a crystal oscillator having a frequency deviation within ±50ppm? (2) Did you select a crystal oscillator having an RMS jitter (1-sigma) of 5ps rms or less? (3) Did you select a crystal oscillator that satisfies the contents of Chapter 6 "ELECTRICAL CHARACTERISTICS"?	KC2520B25.0000C1GESJ (Kyocera Crystal Device Corporation)	
4	2.097152MHz crystal oscillator	(1) Did you select a crystal oscillator having a frequency deviation within ±50ppm? (2) Did you select a crystal oscillator that satisfies the contents of Chapter 6 "ELECTRICAL CHARACTERISTICS"?	KC2520B2.09715C1GESJ (Kyocera Crystal Device Corporation)	
5	Station number setting switch	Can the switch set the following numerical values? Station number: 1 to 120	FR01-KR10P-ST (NKK Switches Co., Ltd.)	
6	Network number setting switch	Can the switch set the following numerical values? Network number: 1 to 239	FR01-KR16P-ST (NKK Switches Co., Ltd.)	

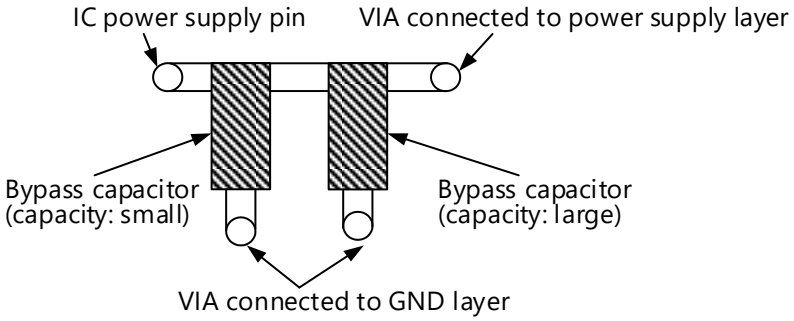
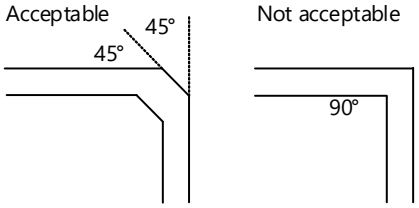
7.3.2 Circuit design precautions

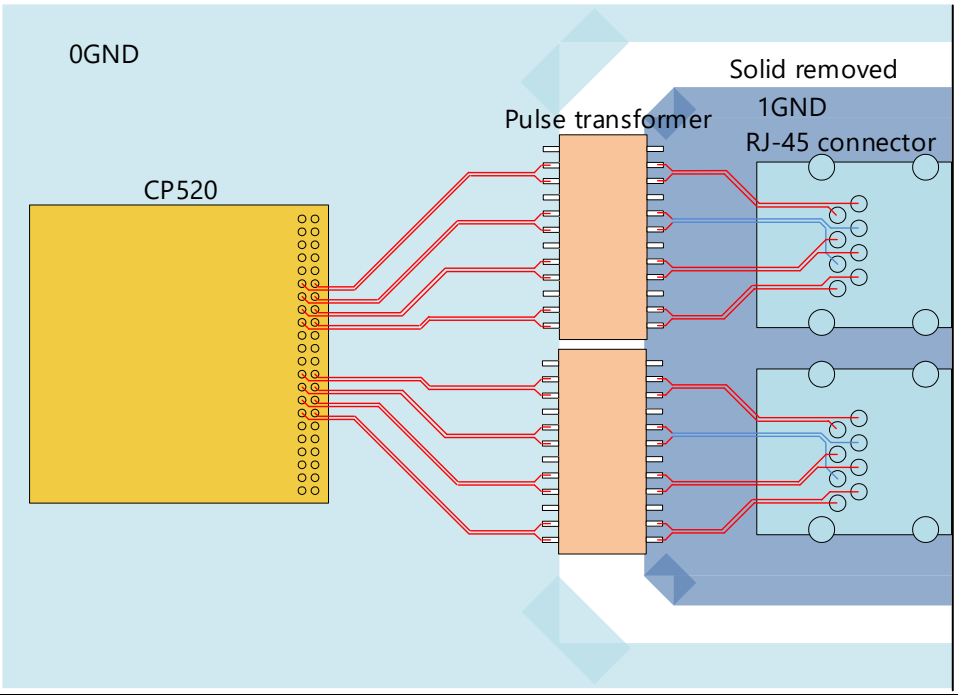
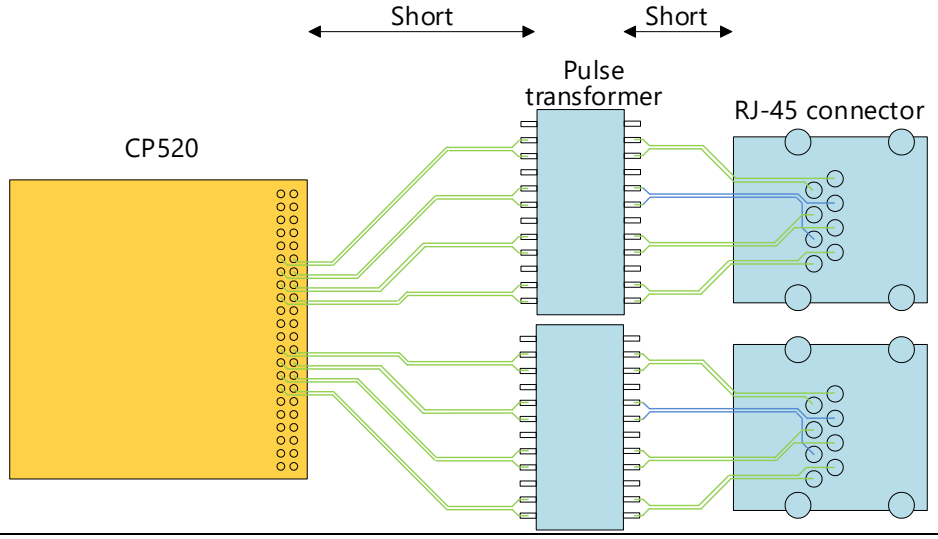
Table 7.3.2-1 Circuit Design Check Sheet

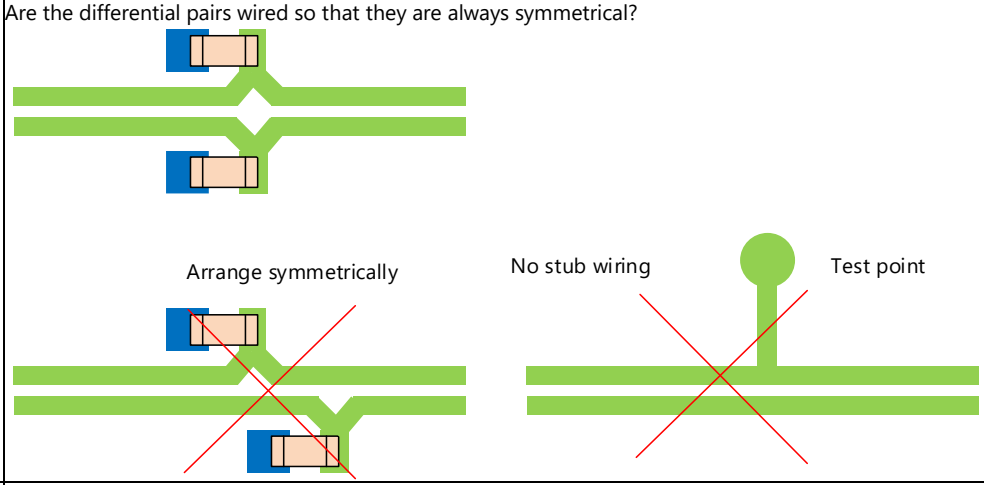
No.	Item	Description	Check Results
1	CP520 pin processing	Are the following reserved pins connected to GND via resistors? • Pin IDs: P19, R19, Y5, Y6, Y7	
2	CP520 pin processing	Are the following reserved pins directly connected to GND? • Pin IDs: G5, H5, J5, J21, J22, K19, K20, K21, K22, L19, L20, L22, L21, P5, R5, R22, T5, U6, AB17, N19	
3	Reset release	In a system where operation starts based on a clock that uses an external oscillator or an external oscillation circuit, is reset released after the clock stabilizes and starts oscillating normally?	
4	Electrical characteristics	Is the circuit designed so that the contents of Chapter 6 "ELECTRICAL CHARACTERISTICS" are satisfied?	
5	Connection from CP520 to RJ-45 connector	As for the signal lines between CP520 and pulse transformer, and between the pulse transformer and RJ-45 connector, are the positive sides of pins connected each other? And, are the negative sides of pins connected each other? (If a positive side and a negative side are connected, the system cannot pass the 1000BASE-T compliance test. In the circuit diagram examples, connect the TXVP* pin to the positive sides and the TXVN* pin to the negative sides.)	
6	External DC power supply (3.3V, 2.5V, 1.0V)	Does the power supply satisfy an output accuracy of ±5%? The target should be within ±3% for DC components, and ±2% for ripple components.	
7	PHY address	Are the PHYADD1 to PHYADD4 pins that set the upper four bits of the address set to Low (0000H)? (Set the pins to open because the pull-down resistor is built in.)	
8	In general	Have the recommended circuits of each device been checked and designed?	

7.3.3 Pattern design precautions

Table 7.3.3-1 Pattern Design Check Sheet

No.	Item	Description	Check Results
1	Board	When a board having six layers or more is used, are the high-speed signal layers and low-speed signal layers assigned as follows? Example of six-layer board L1 ——— High-speed signal layer L2 ——— High-speed signal layer L3 ——— GND L4 ——— Power supply L5 ——— Low-speed signal layer L6 ——— Low-speed signal layer Example of eight-layer board L1 ——— High-speed signal layer L2 ——— High-speed signal layer L3 ——— High-speed signal layer L4 ——— GND L5 ——— Power supply L6 ——— Low-speed signal layer L7 ——— Low-speed signal layer L8 ——— Low-speed signal layer	
2	Power management IC	Is the power management IC used in accordance with the recommended pattern wiring of the power management IC manufacturer?	
3	Wiring of bypass capacitors	Is the bypass capacitor connected in the order of IC power supply pin → bypass capacitor (capacity: small) → bypass capacitor (capacity: large) → power supply layer, as shown below? Is the GND side connected directly to the GND layer?  	
4	Power supply/GND pattern	Is the power supply/GND pattern wired as the thickest pattern possible?	
5	Signal pattern bending	When a pattern is bent, are all signal patterns bent at 45 degrees as shown below?  	
6	25MHz crystal oscillator connected to CP520	Is the 25MHz crystal oscillator connected to CP520 placed near CP520? Is the pattern to the XT2 pin designed as short as possible? Is the signal pattern shielded by GND patterns? (GND layer: 0GND if on the CP520 side and 1GND if on the RJ-45 connector side with the pulse transformer serving as a boundary)	
7	2.097152MHz crystal oscillator connected to CP520	Is the 2.097152MHz crystal oscillator connected to CP520 placed near CP520? Is the pattern to the CLK2_097M pin designed as short as possible? Is the signal pattern shielded by SG patterns? (GND layer: 0GND if on the CP520 side and 1GND if on the RJ-45 connector side with the pulse transformer serving as a boundary)	
8	Signal lines between CP520, pulse transformer, and RJ-45 connector	Are the differential signals wired so that P-side line and N-side line are balanced?	
9	Signal lines between CP520, pulse transformer, and RJ-45 connector	Are the differential signals wired so that P-side line and N-side line have the same length? Do the four pairs of signal lines have the same length?	

No.	Item	Description	Check Results
10	Signal lines between CP520, pulse transformer, and RJ-45 connector	Are the wiring layer and signal line thickness of CP520, pulse transformer, and RJ-45 connector signal lines (MDI) determined so that the differential characteristic impedance becomes 100Ω±10% (125MHz)?	
11	Signal lines between CP520, pulse transformer, and RJ-45 connector	Is the PHY side inner layer (0GND) and the RJ-45 connector side inner layer (1GND) separated using the pulse transformer as a boundary? Are the layers under the pulse transformer, including the back layer and the inner layer, free of a GND solid pattern, and is spacing of 3mm or more secured between the 0GND pattern and the 1GND pattern? 	
12	Signal lines between CP520, pulse transformer, and RJ-45 connector	To ensure that the signal lines do not become unnecessarily long, are CP520, pulse transformer, and RJ-45 connector arranged as close as possible? (In particular, the spacing between CP520 and pulse transformer should be short.) 	

No.	Item	Description	Check Results
13	Signal lines between CP520, pulse transformer, and RJ-45 connector	Are the differential pairs wired so that they are always symmetrical?  	
14	Signal lines between CP520, pulse transformer, and RJ-45 connector	When signals need to intersect, is a GND layer inserted in between? (GND layer: 0GND if on the CP520 side and 1GND if on the RJ-45 connector side with the pulse transformer serving as a boundary)	
15	RJ-45 connector	Is the RJ-45 connector shielded, and the metal casing section connected to 1GND?	

7.4 Noise Suppression Components

In the CP520 application circuit diagram example, noise suppression components are mounted in various locations. Use the following list for your reference when taking measures to reduce noise.

Table 7.4-1 Noise Suppression Component List of CP520 Application Circuit Diagram Example

No.	Circuit (Circuit Diagram)	Component (Recommended Constant)	Application	Remarks
1	CP520 PLL power supply input (Figure 5.4-1)	Ferrite bead (600Ω, 120Ω)	Separates the PLL section (analog power supply) from other power supplies and GND, and stabilizes the supplied power.	-
2	25MHz clock circuit enable input (Figure 5.4-2)	Resistor (0Ω, 1A)	Stabilizes crystal oscillation.	[Enable input] ・ Oscillates at open or High ・ Stops oscillation at Low
3	2.097MHz clock circuit enable input (Figure 5.4-2)	Resistor (0Ω, 1A)		
4	25MHz clock circuit output (Figure 5.4-2)	Resistor (0Ω, 1A)	A damping resistor. Mounted near the crystal oscillator OUT terminal to suppress signal distortion caused by line reflection, etc.	Adjust the resistance value accordingly in the course of development.
5	2.097MHz clock circuit output (Figure 5.4-2)	Resistor (0Ω, 1A)		
6	Serial flash memory interface (Figure 5.4-3)	Resistor (0Ω, 1A x4)	A damping resistor. Mounted near the signal output to suppress signal distortion caused by line reflection, etc.	
7	ICE debugger connector connection area (Figure 5.4-4)	Resistor (0Ω, 1A x9)	A damping resistor. Mounted near the signal output to suppress signal distortion caused by line reflection, etc.	
8	CP520 JTAG interface setting pin (Figure 5.4-4)	Resistor (47kΩ, 1/10W)	A pull-down resistor. Fixed to Low level for selection of JTAG debug interface.	-
9	ICE connector pin 17 processing (Figure 5.4-4)	Resistor (47kΩ, 1/10W)	A pull-down resistor. Fixed to Low level of unused pin.	-
10	Pulse transformer secondary (Figure 5.4-5)	Varistor (300V x16)	Improves the noise reduction in the MDI signal.	Reserved component
11	Pulse transformer secondary (Figure 5.4-5)	Capacitor (0.01µF, 25V x8, 1000pF, 50V x8)	Improves the noise reduction in the MDI signal.	Reserved component

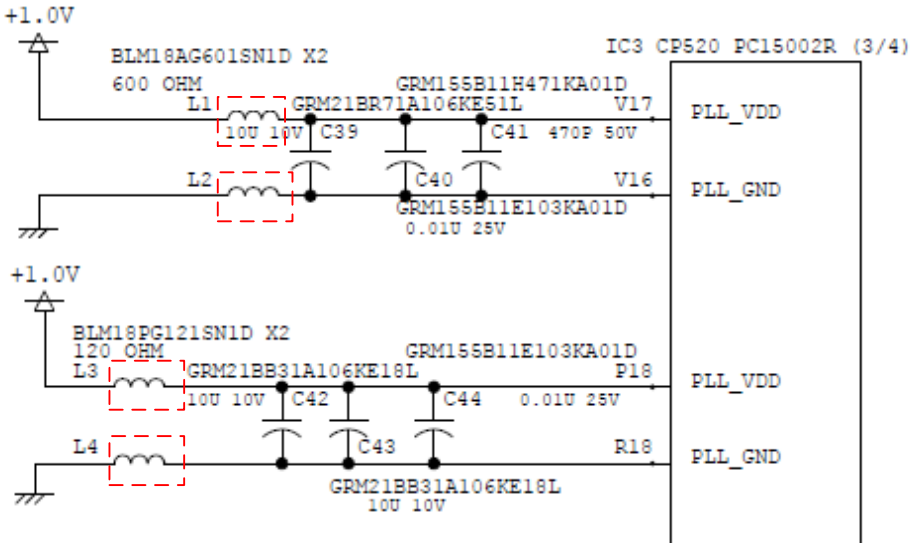


Figure 7.4-1 PLL Power Supply Input Peripheral Circuit

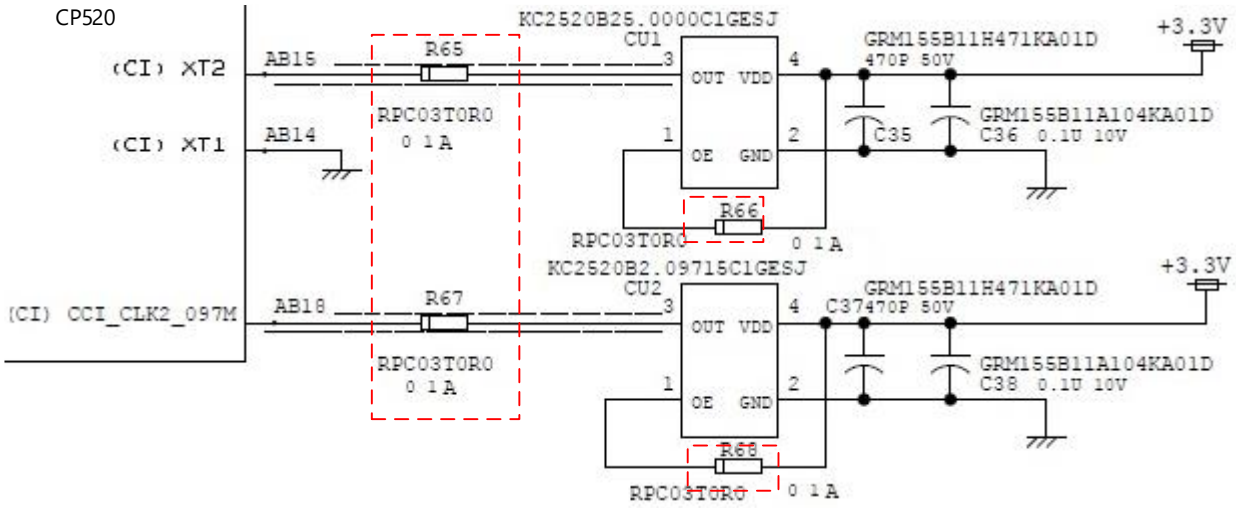


Figure 7.4-2 Clock Peripheral Circuit

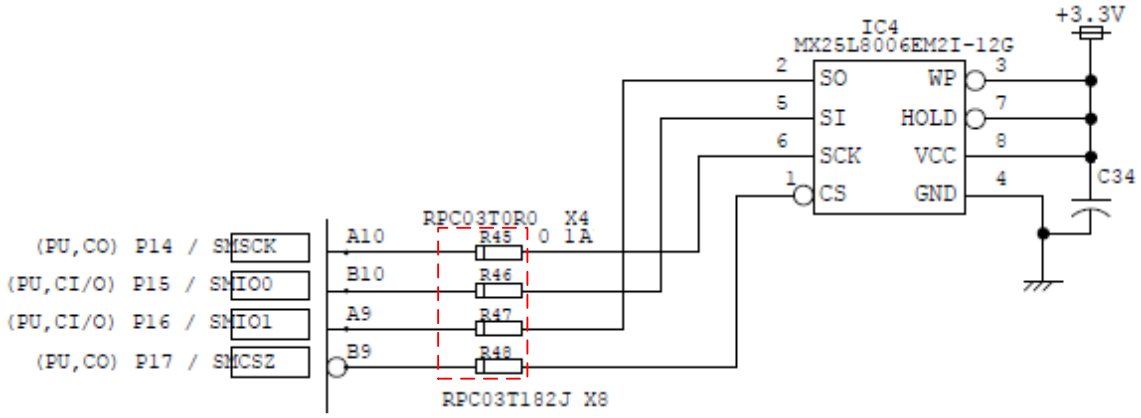


Figure 7.4-3 Serial Flash Memory Interface Peripheral Circuit

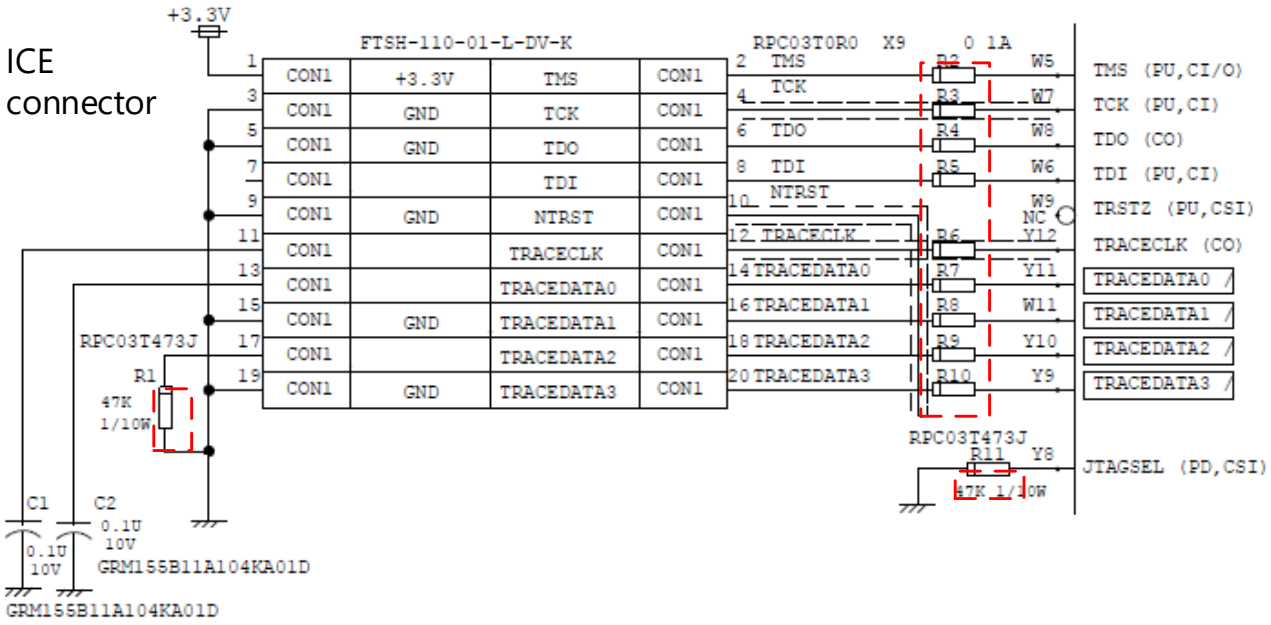


Figure 7.4-4 ICE Debugger Connector Connection Area Peripheral Circuit

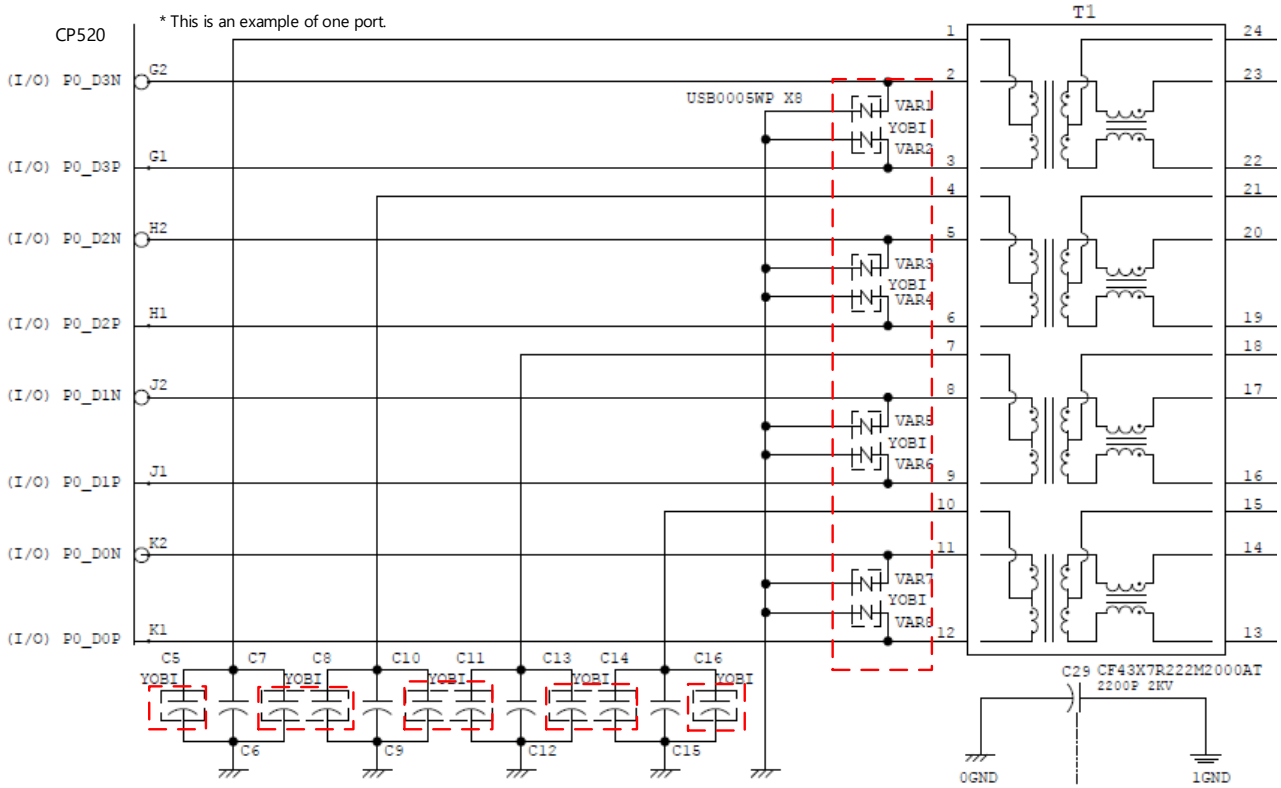


Figure 7.4-5 Pulse Transformer Peripheral Circuit

7.5 Circuits Required During Debugging

As on-chip debug functions, the Cortex-M4F built into CP520 supports debug functions, such as program download, run, and break, as well as trace functions that output program execution history.
The Cortex-M4F also supports JTAG as a basic debug interface. The following shows a connector connection example when ICE (In-Circuit Emulator) is used for the debugging tool.

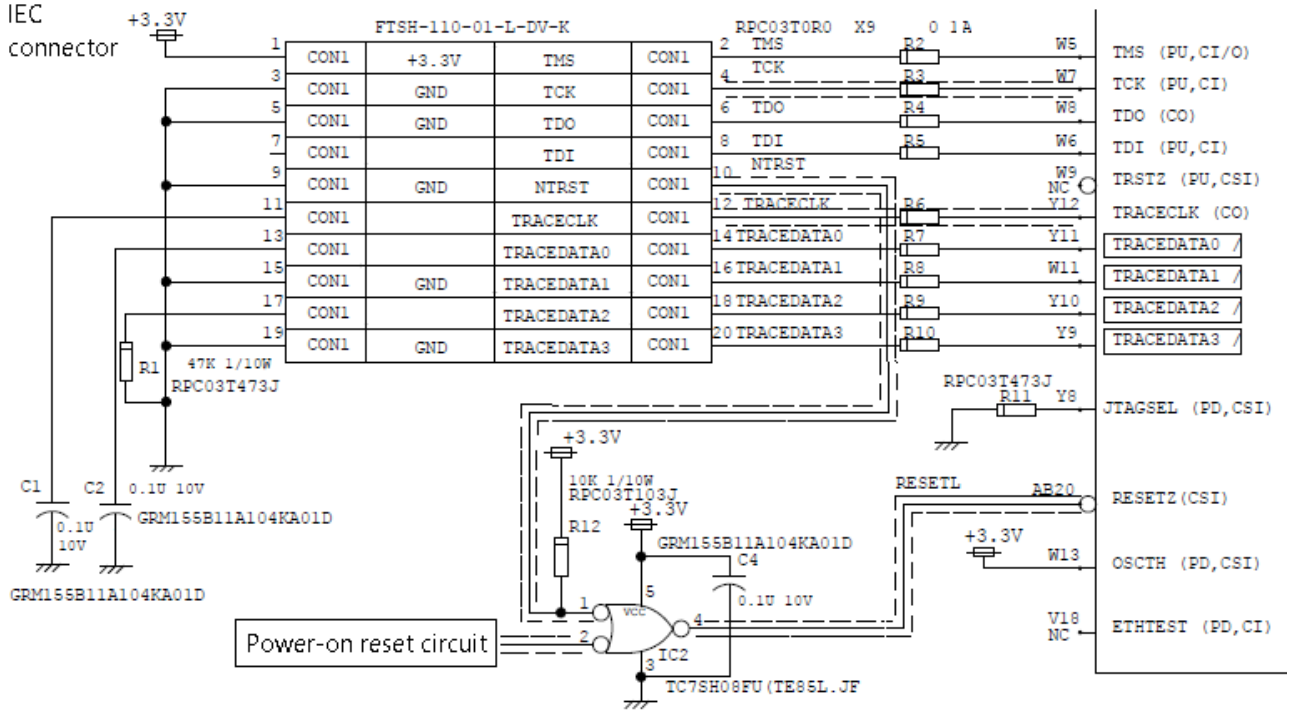


Figure 7.5-1 JTAG Interface Connection Example

If a debugger is not required during mass production, the ICE connector and damping resistors (R2 to R10) can be removed from the above circuit. At this time, CP520 vacant pin processing is not required.

7.6 Thermal Characteristics

The heat resistance value changes due to external factors such as the operating environment and power consumption. The values below, therefore, are merely for your reference.
The heat generated from the GbE-PHY area is large, and thus the GbE-PHY area is used as reference for the heat resistance value.

Table 7.6-1 Thermal Characteristics

Item	Symbol	Rated Value	Unit
Heat resistance between junction temperature (Tj) and ambient temperature (Ta)	θja	15.4	°C/W
Heat resistance between junction temperature (Tj) and LSI top surface center temperature (Tt)	Ψjt	2.4	°C/W

When GPHY_Tj is calculated from Tt and Ψjt, the LSI coordinate center is set to (0, 0), and Tt is measured using point (0, -6.58mm).

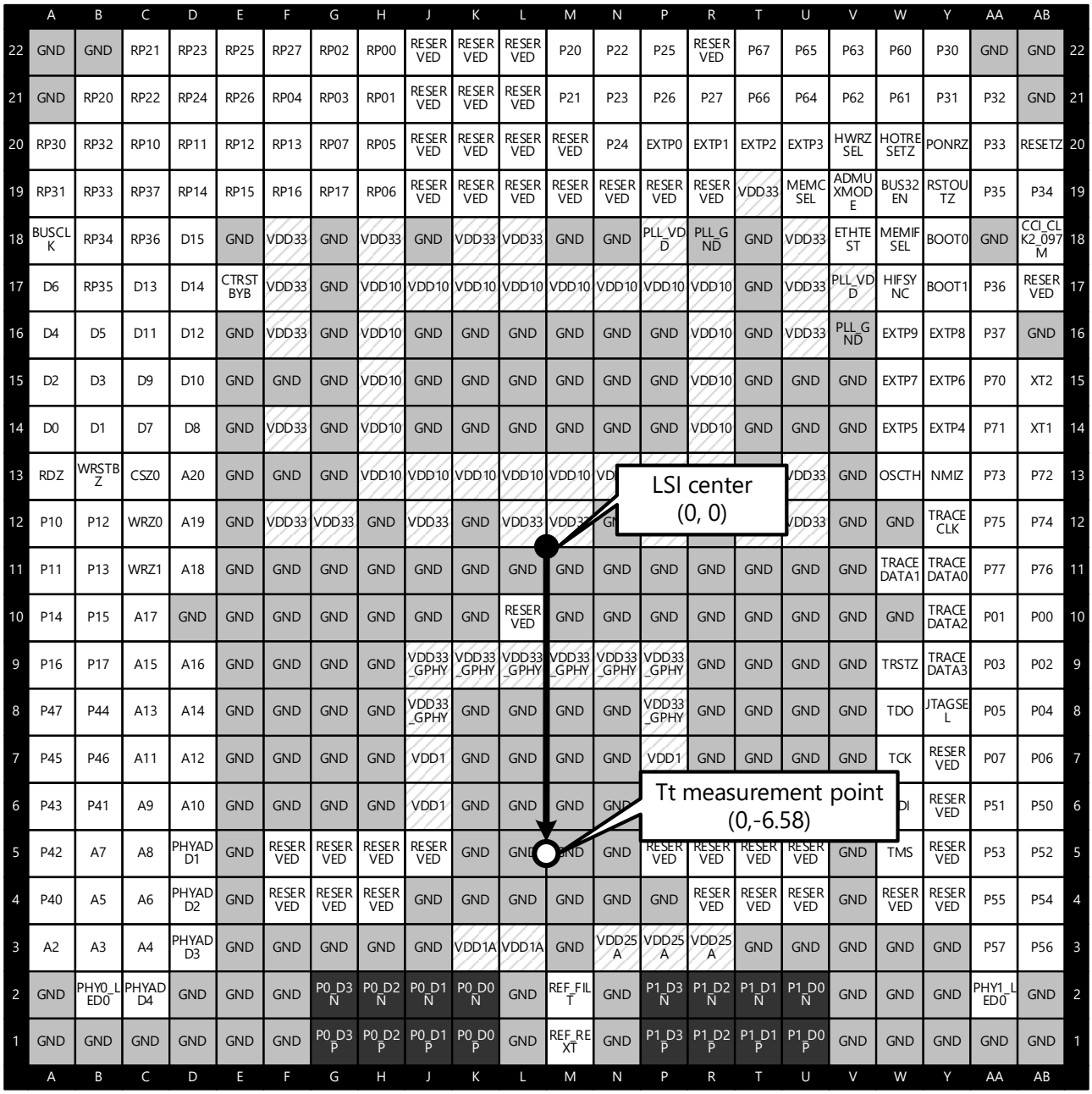


Figure 7.6-1 Tt Measurement Point

7.7 LSI Handling Precautions

7.7.1 Opening precautions

(1) This product requires moisture control. Open the package immediately before soldering.

Table 7.7.1-1 LSI Storage Conditions

No.	Item	Conditions Before Opening	Conditions After Opening
1	Temperature	5 to 35°C	5 to 30°C
2	Humidity	85% RH or less	70% RH or less
3	Life	Within 2 years	Within 168 hours*1

*1: Time from opening of the package to completion of reflow soldering

(2) In the following cases, bake the LSI and then mount it.
Note that heatproof trays must have the words "HEAT PROOF" or a maximum temperature indication. Check the indication before baking.

- When the moisture-resistant packaging is opened, the color of the 30% spot on the indicator card has been changed to pink.
- The specified storage life condition has exceeded after the moisture-resistant packaging is opened.

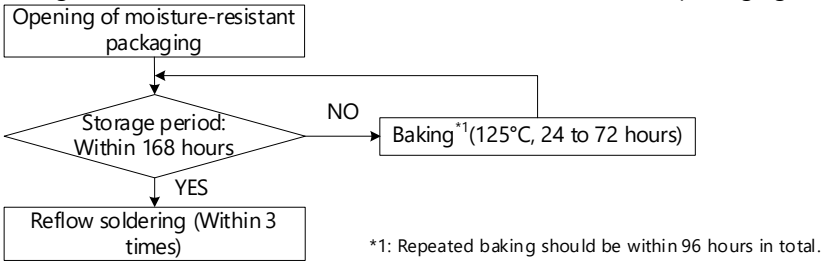


Figure 7.7.1-1 After Opening Moisture-Resistant Packaging

7.7.2 Recommended soldering conditions

The following describes the recommended reflow soldering conditions (IR reflow oven, air reflow oven, air + infrared reflow oven). To avoid re-moisture absorption after opening the moisture-resistant packaging, perform reflow soldering under the conditions below within the storage life after opening.

Table 7.7.2-1 Recommended Soldering Conditions

No.	Item		Description
1	Heat resistance	Peak temperature (package surface temperature)	250°C
2		Duration at 245°C or higher	Within 30 s
3		Duration at 217°C or higher	60 to 150 s
4		Duration at preheat temperature (150 to 200°C)	60 to 120 s
5	Reflow conditions	Maximum number of reflows	3 times or less (within the storage life after opening of moisture-resistant packaging)
6		Reflow atmosphere	Air or nitrogen (N2)
7	Chlorine content in rosin flux (percent by weight)		0.2% or less

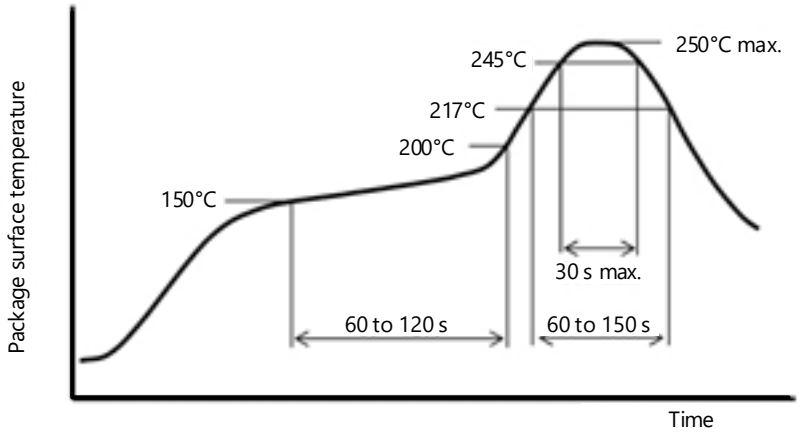


Figure 7.7.2-1 Reflow Soldering Profile

8 RESET

This function initializes the CPU and GbE-PHY areas of CP520.
"Power-on reset" and "system reset" in this manual refers to resetting from the following sources.

[Power-on reset]
・ Reset by signal input from the PONRZ pin (including initialization of CP520 internal RAM)

[System reset]
・ Reset by signal input from the HOTRESETZ pin (excluding internal PLL)
・ Reset by system reset register (SYSRESET) (equivalent to signal input from the HOTRESETZ pin)

For details, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

Table 8-1 Reset Sources and Targets to be Reset

Reset Source		Target to be Reset					RSTOUTZ Output
		Instruction RAM Data RAM Buffer RAM	PLL	CC-Link IE Field Area	CPU Debugging Unit	Other Peripheral Circuits (including GbE-PHY and CPU)	
Hardware control	PONRZ	○	○	○	-	○	○
	RESETZ	-	○	○	-	○	○
	HOTRESETZ	-	-	-	-	○	○
	TRSTZ	-	-	-	○	-	-
Software control	System reset register (SYSRESET)	-	-	-	-	○	○
	Watchdog timer (WDTARES)	-	-	-	-	○	○
	AIRCR register*1	-	-	-	-	○	○
	CP520 driver interface function*2	-	-	-	-	Valid only for GbE-PHY	-

*1: This is the Cortex-M4F internal system control register (0xE000_ED18). Setting AIRCR[2].SYSRESETREQ to "1" resets the device.
*2: Reset processing is performed in the CP520 driver interface function "gerCP52_Initialize".

(1) System reset register (SYSRESET)

This register resets CP520 (equivalent to the HOTRESETZ input pin). The registers for the PONRZ pin are not reset. When system reset is performed for this register (by writing "1b" to SYSRESET), the reset automatically released (SYSRESET will be "0b") after CP520 is reset.

This register can be read or written in 32- or 16-bit units.

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
BASE + 01C0H	15-1	-	R/W	Reserved (Write: 0 / Read: 0)	0001H
	0	SYSRST	R/W	This register performs system reset of CP520. 0b: CP520 is in the reset state. 1b: CP520 is not in the reset state.	

Note

To write to this register, the register must be released from protection by a sequence using the system protection command register (SYSPCMD).

No sequence is required to read the value of the register.

For SYSPCMD, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

(2) PHY reset register (PHYRST)

This register performs reset control of the PHY layer.

This register can be initialized only by signal input from the PONRZ pin and the RESETZ pin, which are external pins.

This register can be read or written in 32- or 16-bit units.

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
BASE + 1220H	31-1	-	R/W	Reserved (Write: 0 / Read: 0)	0000 0000H
	0	PHYRST	R/W	This register performs reset control of the PHY layer. 0b: The PHY layer is in the reset state. 1b: The PHY layer is not in the reset state.	

Note

To write to this register, the register must be released from protection by a sequence using the system protection command register (SYSPCMD).

No sequence is required to read the value of the register.

For SYSPCMD, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

(3) PHY reset switching register (PHYRSTCH)

This register performs reset switching control of the PHY layer.

This register can be read or written in 32- or 16-bit units.

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
BASE + 1224H	31-1	-	R/W	Reserved (Write: 0 / Read: 0)	0000 0000H
	0	PHYRSTCH	R/W	This register performs reset control of the PHY layer. 0b: Control by CC-Link IE Field 1b: Control by the PHYRST register	

9 REGISTERS

This chapter describes the registers in CP520, which are different from those in R-IN32M4-CL2. For the common registers, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

9.1 Register List

The following table lists the registers described in this manual.
The stated address of each register in the following is the relative address from the base address.

- When access is from the CPU and the DMA controller: Base address (BASE) = 4001_0000H
- When access is from an external MCU interface: Base address (BASE) = D_0000H

Table 9.1-1 Register List

Byte Address	Register
400A 4004H	CC-Link IE Field bus size control register
400A 4008H	CC-Link IE Field bus bridge control register
BASE + 0938H	CC-Link IE Field clock gate register
BASE + 01A4H	Clock control register 1
4001 0730H	DMA trigger factor register (DTFR0)
4001 0734H	DMA trigger factor register (DTFR1)
4001 0738H	DMA trigger factor register (DTFR2)
4001 073CH	DMA trigger factor register (DTFR3)
4001 0740H	DMA trigger factor register (RTDTFR)
BASE + 0530H	Timer trigger source register (TMTFR0)
BASE + 0534H	Timer trigger source register (TMTFR1)
BASE + 0538H	Timer trigger source register (TMTFR2)
BASE + 053CH	Timer trigger source register (TMTFR3)
BASE + 0D00H	Timer trigger source register (TMDTFR0)
BASE + 0D04H	Timer trigger source register (TMDTFR1)
BASE + 0D08H	Timer trigger source register (TMDTFR2)
BASE + 0D0CH	Timer trigger source register (TMDTFR3)
BASE + 0D10H	Timer trigger source register (TMDTFR4)
BASE + 0D14H	Timer trigger source register (TMDTFR5)
BASE + 0D18H	Timer trigger source register (TMDTFR6)
BASE + 0D1CH	Timer trigger source register (TMDTFR7)
BASE + 0710H	External interrupt mode register 0
BASE + 0A30H	Trigger synchronous port source register (RP0TFR)
BASE + 0A34H	Trigger synchronous port source register (RP1TFR)
BASE + 0A38H	Trigger synchronous port source register (RP2TFR)
BASE + 0A3CH	Trigger synchronous port source register (RP3TFR)
BASE + 0700H	Noise filter configuration register
BASE + 0000H	Operating mode monitor register

9.2 CC-Link IE Field Bus Bridge Control Registers

These control registers are used to adjust the timing for access to the CC-Link IE Field area from the CPU.

9.2.1 CC-Link IE Field bus size control register (CIEBSC)

The CIEBSC register is used to set the data bus width for access to the CC-Link IE Field area.
When using the CC-Link IE Field functions, set the bits of this register to 0000 FFFFH.

Byte Address	Access	Bit	Bit Name	R/W	Description	Initial Value
400A 4004H	32-bit units	31-0	-	R/W	Set these bits to 0000 FFFFH.	0000 FFFFH

9.2.2 CC-Link IE Field bus bridge control register (CIESMC)

The CIESMC register is used for access control of the CC-Link IE Field area.
When using the CC-Link IE Field functions, set the bits of this register to 0000 0050H.

Byte Address	Access	Bit	Bit Name	R/W	Description	Initial Value
400A 4008H	32-bit units	31-0	-	R/W	Set these bits to 0000 0050H.	0000 FFFFH

9.2.3 CC-Link IE Field clock gate register (CIECLKGTD)

The CIECLKGTD register is used to temporarily stop supply of the bus clock signal. This is to prevent the generation of a clock glitch when switching the bus clock signal of the CC-Link IE Field area.
Writing 1 to the effective bit of this register stops supply of the clock signal and writing 0 to it causes supply to resume.

Before making the setting in the SRAMBRSEL register to switch between the settings to enable the SRAM bus path from the system bus (AHB) and to enable the SRAM bus path from an external MCU, be sure to use this register to stop the bus clock signal.

Byte Address	Access	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0938H	32-bit units	31-0	CIECLKGTD	R/W	These bits stop supply of the bus clock signal in the CC-Link IE Field area. 0000 0000H: Supply 0000 0001H: Stop	0000 0000H

9.3 Clock Control Register 1 (CLKGTD1)

This register is used to stop clock supply to unused modules to save power.
Once the clock supply is stopped by using this register, it cannot be resumed. To supply the clock signal again, reset the system.
Access to stopped modules is prohibited. Operation is not guaranteed if an attempt is made to access these modules.
This register can be read or written in 32- or 16-bit units.

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
BASE + 01A4H	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 EE9FH
	15	-	R/W	Reserved (Write: 0b/Read: 1b)	
	14	GCIE	R/W	CC-Link IE Field functions 0b: Stopped 1b: Operating	
	13, 12	-	R/W	Reserved (Write: 10b / Read: 10b)	
	11	GCIE2	R/W	CC-Link IE Field functions (Write: 10b / Read: 10b) 0b: Stopped 1b: Operating	
	10-8	-	R/W	Reserved (Write: 110b / Read: 110b)	
	7	GCBCLK	R/W	BUSCLK output function 0b: Stopped 1b: Operating	
	6, 5	-	R/W	Reserved (Write: 0 / Read: 0)	
	4	GCWDT	R/W	Watchdog timer 0b: Stopped 1b: Operating	
	3, 2	-	R/W	Reserved (Write: 00b / Read: 11b)	
	1	GCCSI1	R/W	GCCSI1 function 0b: Stopped 1b: Operating	
	0	GCCSI0	R/W	GCCSI0 function 0b: Stopped 1b: Operating	

Note

To write to this register, the register must be released from protection by a sequence using the system protection command register (SYSPCMD).
No sequence is required to read the value of the register.
For SYSPCMD, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

9.4 DMA Trigger Factor Registers (DTFRn, RTDTFR)

These registers are used to select the starting trigger for DMA transfer.
The selectable factors include an interrupt request from the DMAREQZ0, DMAREQZ01, and RTDMAREQZ (DMA transfer request pin) internal peripheral modules, and an interrupt request from external interrupt pin input.

There are a total of five DTFRn and RTDFTR registers, which equals the number of system bus DMAC channels, and they are assigned to the individual DMA channels in accordance with the setting of the SEL2-SEL0 bits in the channel control registers (CHCFGn and RTCHCFG).
Note that all interrupt requests perform resynchronization processing with the internal system bus clock (HCLK).
This register can be read or written in 32-bit units.

Note
To write to this register, the register must be released from protection by a sequence using the system protection command register (SYSPCMD). No sequence is required to read the value of the register. For SYSPCMD, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

・ DTFRn

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
4001 0730H	DTFR0	31-7	-	R/W	Reserved (Write: 0 / Read: 0)	0000 0000H
		6-0	IFC6-IFC0	R/W	These bits are used to select a trigger factor for general DMA transfer channel 0. Refer to "Table 9.4-1 List of DMA Transfer Trigger Factor Selections".	
4001 0734H	DTFR1	These bits are used to select a trigger factor for general DMA transfer channel 1. (Same as DTFR0)				
4001 0738H	DTFR2	These bits are used to select a trigger factor for general DMA transfer channel 2. (Same as DTFR0)				
4001 073CH	DTFR3	These bits are used to select a trigger factor for general DMA transfer channel 3. (Same as DTFR0)				

*: When changing the setup of this register, be sure to first stop DMA operation.

・ RTDTFR

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
4001 0740H	31-7	-	R/W	Reserved (Write: 0 / Read: 0)	0000 0000H
	6-0	IFC6-IFC0	R/W	These bits are used to select a trigger factor for real-time port DMA transfer. Refer to "Table 9.4-1 List of DMA Transfer Trigger Factor Selections".	

The following triggers can be selected for DMA transfer requests.

Table 9.4-1 List of DMA Transfer Trigger Factor Selections

IFC6-IFC0	Selection of DMA Transfer Trigger Factor	IFC6-IFC0	Selection of DMA Transfer Trigger Factor	IFC6-IFC0	Selection of DMA Transfer Trigger Factor
00H	Mask DMA transfer trigger factor. (Transfer request does not occur.)	1EH	Real-time port DMAC transfer completion interrupt	42H	INTPZ15 input*1 / TAUD channel 9 interrupt
01H	DMAREQZ0 pin (DMA transfer request) input (Only DTFR0 register is enabled.)	1FH	TAUD channel 0 interrupt	43H	INTPZ16 input*1 / TAUD channel 10 interrupt
02H	DMAREQZ1 pin (DMA transfer request) input (Only DTFR1 register is enabled.)	20H	TAUD channel 1 interrupt	44H	INTPZ17 input*1 / TAUD channel 11 interrupt
03H	RTDMAREQZ pin (DMA transfer request) input (Only RTDTFR register is enabled.)	21H	TAUD channel 2 interrupt	45H	INTPZ18 input*1 / TAUD channel 12 interrupt
04H	TAUJ2 channel 0 interrupt	22H	TAUD channel 3 interrupt	46H	INTPZ19 input*1 / TAUD channel 13 interrupt
05H	TAUJ2 channel 1 interrupt	23H	TAUD channel 4 interrupt	47H	INTPZ20 input*1 / TAUD channel 14 interrupt
06H	TAUJ2 channel 2 interrupt	24H	Inter-Buffer DMA transfer completion interrupt	48H	INTPZ21 input*1 / TAUD channel 15 interrupt
07H	TAUJ2 channel 3 interrupt	25H	GbE-PHY Port 0 interrupt	49H	INTPZ22 input*1
08H	UARTJ0 send interrupt	26H	GbE-PHY Port 1 interrupt	4AH	INTPZ23 input*1
09H	UARTJ0 receive interrupt	27H-32H	Setup prohibited	4BH	INTPZ24 input*1
0AH	UARTJ1 send interrupt	33H	INTPZ0 input*1	4CH	INTPZ25 input*1
0BH	UARTJ1 receive interrupt	34H	INTPZ1 input*1	4DH	INTPZ26 input*1
0CH	CSIH0 communication status interrupt	35H	INTPZ2 input*1	4EH	INTPZ27 input*1
0DH	CSIH0 reception status interrupt	36H	INTPZ3 input*1	4FH	INTPZ28 input*1
0EH	CSIH0 end of job interrupt	37H	INTPZ4 input*1	50H-62H	Setup prohibited
0FH	CSIH1 communication status interrupt	38H	INTPZ5 input*1	63H	GbE-PHY LED0_PHY0 input interrupt
10H	CSIH1 reception status interrupt	39H	INTPZ6 input*1	64H	GbE-PHY LED0_PHY1 input interrupt
11H	CSIH1 end of job interrupt	3AH	INTPZ7 input*1	65H-6EH	Setup prohibited
12H	IICB0 data send/receive interrupt	3BH	INTPZ8 input*1	6FH	CC-Link IE Field NMIZ interrupt
13H	IICB1 data send/receive interrupt	3CH	INTPZ9 input*1	70H	CC-Link IE Field WDTZ interrupt
14H-19H	Setup prohibited	3DH	INTPZ10 input*1	71H	CC-Link IE Field INTZ interrupt
1AH	General DMAC channel 0 transfer completion interrupt	3EH	INTPZ11 input*1 / TAUD channel 5 interrupt	72H-7CH	Setup prohibited
1BH	General DMAC channel 1 transfer completion interrupt	3FH	INTPZ12 input*1 / TAUD channel 6 interrupt	7DH	GbE-PHY LED1_PHY0 input interrupt
1CH	General DMAC channel 2 transfer completion interrupt	40H	INTPZ13 input*1 / TAUD channel 7 interrupt	7EH	GbE-PHY LED1_PHY1 input interrupt
1DH	General DMAC channel 3 transfer completion interrupt	41H	INTPZ14 input*1 / TAUD channel 8 interrupt	7FH	Setup prohibited

*1: When using an external interrupt as a DMA trigger factor, be sure to specify the edge.
(Do not perform a setup of level detection.)

9.5 Timer Trigger Source Registers (TMTFR0-3, TMDTFR0-7)

These registers are used to select the interrupt request signal to be assigned to the TIN input of the timer.

- TMTFR0-3: TINJ0-3 (TAUJ2) is assigned.
- TMTDFR0-7: TIND0-7 (TAUD) is assigned. (TIND8-15 are out of scope.)

Before using these registers, set the fastest 0000B (PCLK/20) as the prescaler setting of the TAUJ2TPS register of TAUJ2.
These registers can be read or written in 32-bit units.

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0530H	TMTFR0	31-7	-	R/W	Reserved (Write: 0 / Read: 0)	0000 0000H
		6-0	IFC6-IFC0	R/W	These bits are used to select a trigger source for timer channel 0. Refer to "Table 9.5-1 List of Timer Count Trigger Source Selections".	
BASE + 0534H	TMTFR1	These bits are used to select a trigger source for timer channel 1. (Same as TMTFR0)				
BASE + 0538H	TMTFR2	These bits are used to select a trigger source for timer channel 2. (Same as TMTFR0)				
BASE + 053CH	TMTFR3	These bits are used to select a trigger source for timer channel 3. (Same as TMTFR0)				
BASE + 0D00H	TMDTFR0	These bits are used to select a trigger source for timer channel 0. (Same as TMTFR0)				
BASE + 0D04H	TMDTFR1	These bits are used to select a trigger source for timer channel 1. (Same as TMTFR0)				
BASE + 0D08H	TMDTFR2	These bits are used to select a trigger source for timer channel 2. (Same as TMTFR0)				
BASE + 0D0CH	TMDTFR3	These bits are used to select a trigger source for timer channel 3. (Same as TMTFR0)				
BASE + 0D10H	TMDTFR4	These bits are used to select a trigger source for timer channel 4. (Same as TMTFR0)				
BASE + 0D14H	TMDTFR5	These bits are used to select a trigger source for timer channel 5. (Same as TMTFR0)				
BASE + 0D18H	TMDTFR6	These bits are used to select a trigger source for timer channel 6. (Same as TMTFR0)				
BASE + 0D1CH	TMDTFR7	These bits are used to select a trigger source for timer channel 7. (Same as TMTFR0)				

Note

To write to this register, the register must be released from protection by a sequence using the system protection command register (SYSPCMD).
No sequence is required to read the value of the register.
For SYSPCMD, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

Table 9.5-1 List of Timer Count Trigger Source Selections

IFC6-IFC0	Selection of Timer Count Trigger Source	IFC6-IFC0	Selection of Timer Count Trigger Source	IFC6-IFC0	Selection of Timer Count Trigger Source
00H	Mask the timer trigger source.	20H	TAUD channel 1 interrupt	44H	INTPZ17 input*1 / TAUD channel 11 interrupt
01H-03H	Setup prohibited	21H	TAUD channel 2 interrupt	45H	INTPZ18 input*1 / TAUD channel 12 interrupt
04H	TAUJ2 channel 0 interrupt	22H	TAUD channel 3 interrupt	46H	INTPZ19 input*1 / TAUD channel 13 interrupt
05H	TAUJ2 channel 1 interrupt	23H	TAUD channel 4 interrupt	47H	INTPZ20 input*1 / TAUD channel 14 interrupt
06H	TAUJ2 channel 2 interrupt	24H	Inter-Buffer DMA transfer completion interrupt	48H	INTPZ21 input*1 / TAUD channel 15 interrupt
07H	TAUJ2 channel 3 interrupt	25H	GbE-PHY Port 0 interrupt	49H	INTPZ22 input*1
08H	UARTJ0 send interrupt	26H	GbE-PHY Port 1 interrupt	4AH	INTPZ23 input*1
09H	UARTJ0 receive interrupt	27H-32H	Setup prohibited	4BH	INTPZ24 input*1
0AH	UARTJ1 send interrupt	33H	INTPZ0 input*1	4CH	INTPZ25 input*1
0BH	UARTJ1 receive interrupt	34H	INTPZ1 input*1	4DH	INTPZ26 input*1
0CH	CSIH0 communication status interrupt	35H	INTPZ2 input*1	4EH	INTPZ27 input*1
0DH	CSIH0 reception status interrupt	36H	INTPZ3 input*1	4FH	INTPZ28 input*1
0EH	CSIH0 end of job interrupt	37H	INTPZ4 input*1	50H-62H	Setup prohibited
0FH	CSIH1 communication status interrupt	38H	INTPZ5 input*1	63H	GbE-PHY LED0_PHY0 input interrupt
10H	CSIH1 reception status interrupt	39H	INTPZ6 input*1	64H	GbE-PHY LED0_PHY1 input interrupt
11H	CSIH1 end of job interrupt	3AH	INTPZ7 input*1	65H-6EH	Setup prohibited
12H	IICB0 data send/receive interrupt	3BH	INTPZ8 input*1	6FH	CC-Link IE Field NMIZ interrupt
13H	IICB1 data send/receive interrupt	3CH	INTPZ9 input*1	70H	CC-Link IE Field WDTZ interrupt
14H-19H	Setup prohibited	3DH	INTPZ10 input*1	71H	CC-Link IE Field INTZ interrupt
1AH	General DMAC channel 0 transfer completion interrupt	3EH	INTPZ11 input*1 / TAUD channel 5 interrupt	72H-7CH	Setup prohibited
1BH	General DMAC channel 1 transfer completion interrupt	3FH	INTPZ12 input*1 / TAUD channel 6 interrupt	7DH	GbE-PHY LED1_PHY0 input interrupt
1CH	General DMAC channel 2 transfer completion interrupt	40H	INTPZ13 input*1 / TAUD channel 7 interrupt	7EH	GbE-PHY LED1_PHY1 input interrupt
1DH	General DMAC channel 3 transfer completion interrupt	41H	INTPZ14 input*1 / TAUD channel 8 interrupt	7FH	Setup prohibited
1EH	Real-time port DMAC transfer completion interrupt	42H	INTPZ15 input*1 / TAUD channel 9 interrupt	-	-
1FH	TAUD channel 0 interrupt	43H	INTPZ16 input*1 / TAUD channel 10 interrupt	-	-

*1: When using an external interrupt as a timer trigger source, be sure to specify the edge.
(Do not perform a setup of level detection.)

9.6 External Interrupt Mode Register 0 (INTM0)

This register is used to specify the trigger mode for the external interrupt requests input via external pins (NMIZ and INTPZ0-INTPZ28).

This register can be read or written in 32-bit units.

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0710H	-	31-24	-	R/W	Reserved (Write: 0 / Read: 0)	0040 0002H
	-	23, 22	-	R/W	Reserved (Write: 01b / Read: 01b)	
	LED3_PHY1	21	ESP1L31	R/W	These bits are used to specify the trigger mode for LED3_PHY1. 00b: Falling edge (initial value) 01b: Rising edge 10b: Level detection (Low detection)*1 11b: Rising and falling edges	
		20	ESP1L30			
	LED2_PHY1	19	ESP1L21	R/W	These bits are used to specify the trigger mode for LED2_PHY1. (Same as LED3_PHY1)	
		18	ESP1L20			
	LED1_PHY1	17	ESP1L11	R/W	These bits are used to specify the trigger mode for LED1_PHY1. (Same as LED3_PHY1)	
		16	ESP1L10			
	LED0_PHY1	15	ESP1L01	R/W	These bits are used to specify the trigger mode for LED0_PHY1. (Same as LED3_PHY1)	
		14	ESP1L00			
	LED3_PHY0	13	ESP0L31	R/W	These bits are used to specify the trigger mode for LED3_PHY0. (Same as LED3_PHY1)	
		12	ESP0L30			
	LED2_PHY0	11	ESP0L21	R/W	These bits are used to specify the trigger mode for LED2_PHY0. (Same as LED3_PHY1)	
		10	ESP0L20			
	LED1_PHY0	9	ESP0L11	R/W	These bits are used to specify the trigger mode for LED1_PHY0. (Same as LED3_PHY1)	
		8	ESP0L10			
	LED0_PHY0	7	ESP0L01	R/W	These bits are used to specify the trigger mode for LED0_PHY0. (Same as LED3_PHY1)	
		6	ESP0L00			
	-	5-2	-	R/W	Reserved (Write: 0 / Read: 0)	
	NMIZ	1	ESN01	R/W	These bits are used to specify the trigger mode for NMIZ. 00b: Falling edge (initial value) 01b: Rising edge 10b: Level detection (Low detection)*2 11b: Rising and falling edges	
		0	ESN00			

*1: If the active level (Low) is input to the INTPZ0-INTPZ28 pins, the input signal is judged as a successive pulse whose level toggles each time the internal system bus clock (HCLK) rises, and an interrupt request is generated.
Note that HCLK, which is used to sample external interrupts, does not stop even in standby mode.

*2: When the Low level of NMIZ is set to be detected, the signal is pulsed internally and an interrupt occurs once.

Note

To write to this register, the register must be released from protection by a sequence using the system protection command register (SYSPCMD).
No sequence is required to read the value of the register.
For SYSPCMD, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

9.7 Trigger-Synchronous Port Source Registers (RP0TFR-RP3TFR)

These registers are used to select interrupt request signals to be assigned to the trigger-synchronous signal.
The real-time ports (RP0x-RP3x) can be specified as trigger sources, in 8-bit units.
These registers can be read or written in 32-bit units.

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0A30H	RP0TFR	31-7	-	R/W	Reserved (Write: 0 / Read: 0)	0000 0000H
		6-0	IFC6-IFC0	R/W	These bits are used to select the trigger source for trigger-synchronous port 0. Refer to "Table 9.7-1 List of Trigger Synchronous Port Trigger Source Selections".	
BASE + 0A34H	RP1TFR	These bits are used to select the trigger source for trigger-synchronous port 1. (Same as RP0TFR)				
BASE + 0A38H	RP2TFR	These bits are used to select the trigger source for trigger-synchronous port 2. (Same as RP0TFR)				
BASE + 0A3CH	RP3TFR	These bits are used to select the trigger source for trigger-synchronous port 3. (Same as RP0TFR)				

Note

To write to this register, the register must be released from protection by a sequence using the system protection command register (SYSPCMD).
No sequence is required to read the value of the register.
For SYSPCMD, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

Table 9.7-1 List of Trigger Synchronous Port Trigger Source Selections

IFC6-IFC0	Selection of Trigger-Synchronous Port Trigger Source	IFC6-IFC0	Selection of Trigger-Synchronous Port Trigger Source	IFC6-IFC0	Selection of Trigger-Synchronous Port Trigger Source
00H	Timer output (TOUTJ0/TOUTD4)	1EH	Real-time port DMAC transfer completion interrupt	42H	INTPZ15 input*1 / TAUD channel 9 interrupt*2
01H	Timer output (TOUTJ1/TOUTD5)	1FH	TAUD channel 0 interrupt	43H	INTPZ16 input*1 / TAUD channel 10 interrupt*2
02H	Timer output (TOUTJ2/TOUTD6)	20H	TAUD channel 1 interrupt	44H	INTPZ17 input*1 / TAUD channel 11 interrupt*2
03H	Timer output (TOUTJ3/TOUTD7)	21H	TAUD channel 2 interrupt	45H	INTPZ18 input*1 / TAUD channel 12 interrupt*2
04H	TAUJ2 channel 0 interrupt	22H	TAUD channel 3 interrupt	46H	INTPZ19 input*1 / TAUD channel 13 interrupt*2
05H	TAUJ2 channel 1 interrupt	23H	TAUD channel 4 interrupt	47H	INTPZ20 input*1 / TAUD channel 14 interrupt*2
06H	TAUJ2 channel 2 interrupt	24H	Inter-Buffer DMA transfer completion interrupt	48H	INTPZ21 input*1 / TAUD channel 15 interrupt*2
07H	TAUJ2 channel 3 interrupt	25H	GbE-PHY Port 0 interrupt	49H	INTPZ22 input*1, *2
08H	UARTJ0 send interrupt	26H	GbE-PHY Port 1 interrupt	4AH	INTPZ23 input*1
09H	UARTJ0 receive interrupt	27H -32H	Setup prohibited	4BH	INTPZ24 input*1
0AH	UARTJ1 send interrupt	33H	INTPZ0 input*1	4CH	INTPZ25 input*1
0BH	UARTJ1 receive interrupt	34H	INTPZ1 input*1	4DH	INTPZ26 input*1
0CH	CSIH0 communication status interrupt	35H	INTPZ2 input*1	4EH	INTPZ27 input*1
0DH	CSIH0 reception status interrupt	36H	INTPZ3 input*1	4FH	INTPZ28 input*1
0EH	CSIH0 end of job interrupt	37H	INTPZ4 input*1	50H-62H	Setup prohibited
0FH	CSIH1 communication status interrupt	38H	INTPZ5 input*1	63H	GbE-PHY LED0_PHY0 input interrupt
10H	CSIH1 reception status interrupt	39H	INTPZ6 input*1	64H	GbE-PHY LED0_PHY1 input interrupt
11H	CSIH1 end of job interrupt	3AH	INTPZ7 input*1	65H -6EH	Setup prohibited
12H	IICB0 data send/receive interrupt	3BH	INTPZ8 input*1	6FH	CC-Link IE Field NMIZ interrupt
13H	IICB1 data send/receive interrupt	3CH	INTPZ9 input*1	70H	CC-Link IE Field WDTZ interrupt
14H -19H	Setup prohibited	3DH	INTPZ10 input*1	71H	CC-Link IE Field INTZ interrupt
1AH	General DMAC channel 0 transfer completion interrupt	3EH	INTPZ11 input*1 / TAUD channel 5 interrupt*2	72H -7CH	Setup prohibited
1BH	General DMAC channel 1 transfer completion interrupt	3FH	INTPZ12 input*1 / TAUD channel 6 interrupt*2	7DH	GbE-PHY LED1_PHY0 input interrupt
1CH	General DMAC channel 2 transfer completion interrupt	40H	INTPZ13 input*1 / TAUD channel 7 interrupt*2	7EH	GbE-PHY LED1_PHY1 input interrupt
1DH	General DMAC channel 3 transfer completion interrupt	41H	INTPZ14 input*1 / TAUD channel 8 interrupt*2	7FH	Setup prohibited

*1: When using an external interrupt as a trigger source for trigger-synchronous port, be sure to specify the edge. (Do not perform a setup of level detection.)

*2: INTPZ or TAUD interrupt is selected using the INTSEL register. For details, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

9.8 Noise Filter Configuration Register (NFC0)

This register is used to specify the width of the noise eliminated from the input signals shown in the table below.

Table 9.8-1 Signals Subjected to Noise Elimination

Signal	Internal Connection Area	Signal Function
NMIZ	Interrupt controller	Non-maskable external interrupt input
LED0_PHY0 - LED3_PHY0 LED0_PHY1 - LED3_PHY1	Interrupt controller, timer array, DMA, trigger-synchronous port	LED interface with GbE-PHY

This feature can only be specified for the CPU of CP520. Applications that do not use the internal CPU cannot use this feature.
For details, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".
This register can be read or written in 32-bit units.

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0700H	-	31-22	-	R/W	Reserved (Write: 0 / Read: 0)	0000 0000H
	LED3_PHY1 input	21	NFP1L31	R/W	These bits are used to set the noise filter stage of the LED3_PHY1 input with the internal system clock as a reference. 00b: 0 × HCLK 01b: 4 × HCLK 10b: 8 × HCLK 11b: 16 × HCLK	
		20	NFP1L30			
	LED2_PHY1 input	19	NFP1L21	R/W	(Same as LED3_PHY1 input)	
		18	NFP1L20			
	LED1_PHY1 input	17	NFP1L11	R/W	(Same as LED3_PHY1 input)	
		16	NFP1L10			
	LED0_PHY1 input	15	NFP1L01	R/W	(Same as LED3_PHY1 input)	
		14	NFP1L00			
	LED3_PHY0 input	13	NFP0L31	R/W	(Same as LED3_PHY1 input)	
		12	NFP0L30			
	LED2_PHY0 input	11	NFP0L21	R/W	(Same as LED3_PHY1 input)	
		10	NFP0L20			
	LED1_PHY0 input	9	NFP0L11	R/W	(Same as LED3_PHY1 input)	
		8	NFP0L10			
	LED0_PHY0 input	7	NFP0L01	R/W	(Same as LED3_PHY1 input)	
		6	NFP0L00			
	-	5-2	-	R/W	Reserved (Write: 0 / Read: 0)	
	NMI input	1	NFPNM1	R/W	These bits are used to set the noise filter stage of the NMI input with the internal system clock as a reference. 00b: 0 × HCLK 01b: 4 × HCLK 10b: 8 × HCLK 11b: 16 × HCLK	
		0	NFPNM0			

Note

To write to this register, the register must be released from protection by a sequence using the system protection command register (SYSPCMD).
No sequence is required to read the value of the register.
For SYSPCMD, refer to the "R-IN32M4-CL2 User's Manual: Peripheral Modules".

9.9 Operating Mode Monitor Register (MDMNT)

This register is used to monitor the level of the operating mode setting pins.
This register can be read in 32- or 16-bit units.

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0000H	31-12	-	R	Reserved (Read: 0)	Pin level
	11	-	R	Reserved (Read: 1b)	
	10	MEMCSEL	R	This bit is used to read the levels of the operating mode setting pins.	
	9	-	R	Reserved (Read: 0)	
	8	BOOT1	R	This bit is used to read the levels of the operating mode setting pins.	
	7	BOOT0			
	6	OSCTH			
	5	JTAGSEL			
	4	HWRZSEL			
	3	HISYNC			
	2	ADMUXMODE			
	1	MEMIFSEL			
	0	BUS32EN			

10 CREATING USER PROGRAMS

This chapter provides an overview of user program processing and customization.
The user program is sample processing for verifying the logic of the communication process of an intelligent device station or remote device station. Customize the program in accordance with user specifications.

10.1 User Program List

The following is a list of the user programs available in the "\Intelligent_Device\English\sample" or "\Remote_Device\English\sample" folders.
This list also indicates whether or not implementation in the intelligent device station (ID) or remote device station (RD) is required for each program.

Table 10.1-1 List of User Programs Related to Initial Processing and Cyclic Transmission (CP520_sample.c File)

○: Required △: Optional ×: Not required

No.	Function Name	Overview	Implementation Necessity		Reference
			ID	RD	
1	iUserMainRoutine	Main processing	○		Section 10.2.1
2	iUserInitialization	Initialization processing	○		Section 10.2.2
3	iUserStart	Communication start processing	○		Section 10.2.3
4	UserForceStop	Own station error processing	△		Section 10.2.4
5	UserStopCyclic	Cyclic transmission stop processing	△		Section 10.2.5
6	iUserExecuteMain	Event processing	○		Section 10.2.6
7	UserReceiveCyclic	MyStatus from master station and cyclic receive processing	○		Section 10.2.7
8	UserSendMyStatus	MyStatus send processing	○		Section 10.2.8
9	UserSendCyclic	Cyclic send processing	○		Section 10.2.9
10	UserUpdateStatus	Communication status update processing	○		Section 10.2.10
11	UserUpdateLed	LED update processing	○		Section 10.2.11
12	UserGetCyclicStatus	Cyclic transmission status update processing	△		Section 10.2.12
13	UserGetMIB	MIB information acquisition processing	△		Section 10.2.13
14	iUserMyStaRcvTkn	Receive processing of token frame addressed to the own station	○		Section 10.2.14

Table 10.1-2 List of User Programs Related to Transient Transmission (CP520_Transient.c File)

○: Required △: Optional ×: Not required

No.	Function Name	Overview	Implementation Necessity		Reference
			ID	RD	
1	UserReceiveTransient	Transient1, Transient2, and TransientAck receive processing	○		Section 10.3.1
2	UserHandleReceivedTransient1	Transient1 receive data processing	○		Section 10.3.2
3	UserStartMakingReceivedTransient1	Transient1 receive data reconstruction start processing	○		Section 10.3.3
4	blUserMakeReceivedTransient1	Transient1 receive data reconstruction processing	○		Section 10.3.4
5	erUserHandleReceivedMemReadRequest	SLMP memory read request frame receive processing	△		Section 10.3.5
6	erUserHandleReceivedMemWriteRequest	SLMP memory write request frame receive processing	△		Section 10.3.6
7	UserHandleReceivedTransient2	Transient2 receive data processing	△		Section 10.3.7
8	erUserCheckReceivedTransient2	Transient2 receive data check processing	△		Section 10.3.8
9	erUserHandleReceivedTransient2 _RequestSetMemory	Transient2 memory write request receive processing	△		Section 10.3.9
10	ulUserSetTransient2_Response	Transient2 response frame creation processing	△		Section 10.3.10
11	UserHandleReceivedTransientAck	TransientAck receive data processing	○		Section 10.3.11
12	blUserSetTransientAck	TransientAck frame creation processing	○		Section 10.3.12
13	UserSendTransient	Transient1, Transient2, and TransientAck send processing	○		Section 10.3.13
14	erUserSetSlmpMemRead_Request	SLMP memory read request frame creation processing	△	×	Section 10.3.14
15	pvUserJudgeTransient1Divide	Transient1 request send division determination processing	△	×	Section 10.3.15
16	erUserSetTransient1_Request	Transient1 request frame creation processing	△	×	Section 10.3.16
17	erUserHandleReceivedMemReadResponse	SLMP memory read response receive processing	△	×	Section 10.3.17
18	UserSetTransient2_Request	Transient2 request frame creation processing	△	×	Section 10.3.18
19	ulUserSetTransient2_RequestGetMemory	Transient2 memory read request frame creation processing	△	×	Section 10.3.19
20	erUserHandleReceivedTransient2_ ResponseGetMemory	Transient2 memory read response receive processing	△	×	Section 10.3.20

Caution

The CP520_Transient.c file describes Transient2 memory reading/writing and SLMP memory reading/writing as sample processing of each command.
To implement commands other than the above, add the processing for the command by referring to Appendix 1 "Frame Format" and the related manual "SLMP Reference Manual" (BAP-C3002-001).

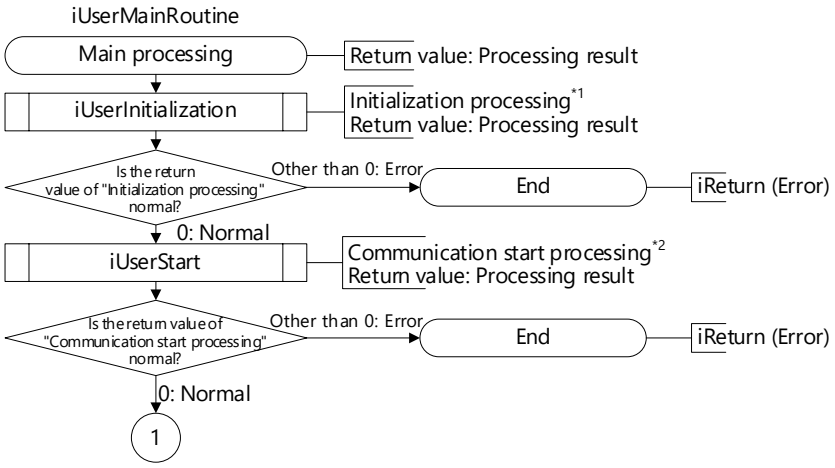
Table 10.1-3 List of User Programs Related to Hardware Test (CP520_HWTest.c File)

○: Required △: Optional ×: Not required

No.	Function Name	Overview	Implementation Necessity		Reference
			ID	RD	
1	UserIEEETest	Hardware test (IEEE 802.3ab compliance test)	○		Section 10.4.1
2	UserLoopBackTest	Hardware test (loopback communication test)	△		Section 10.4.2

10.2.1 Main processing

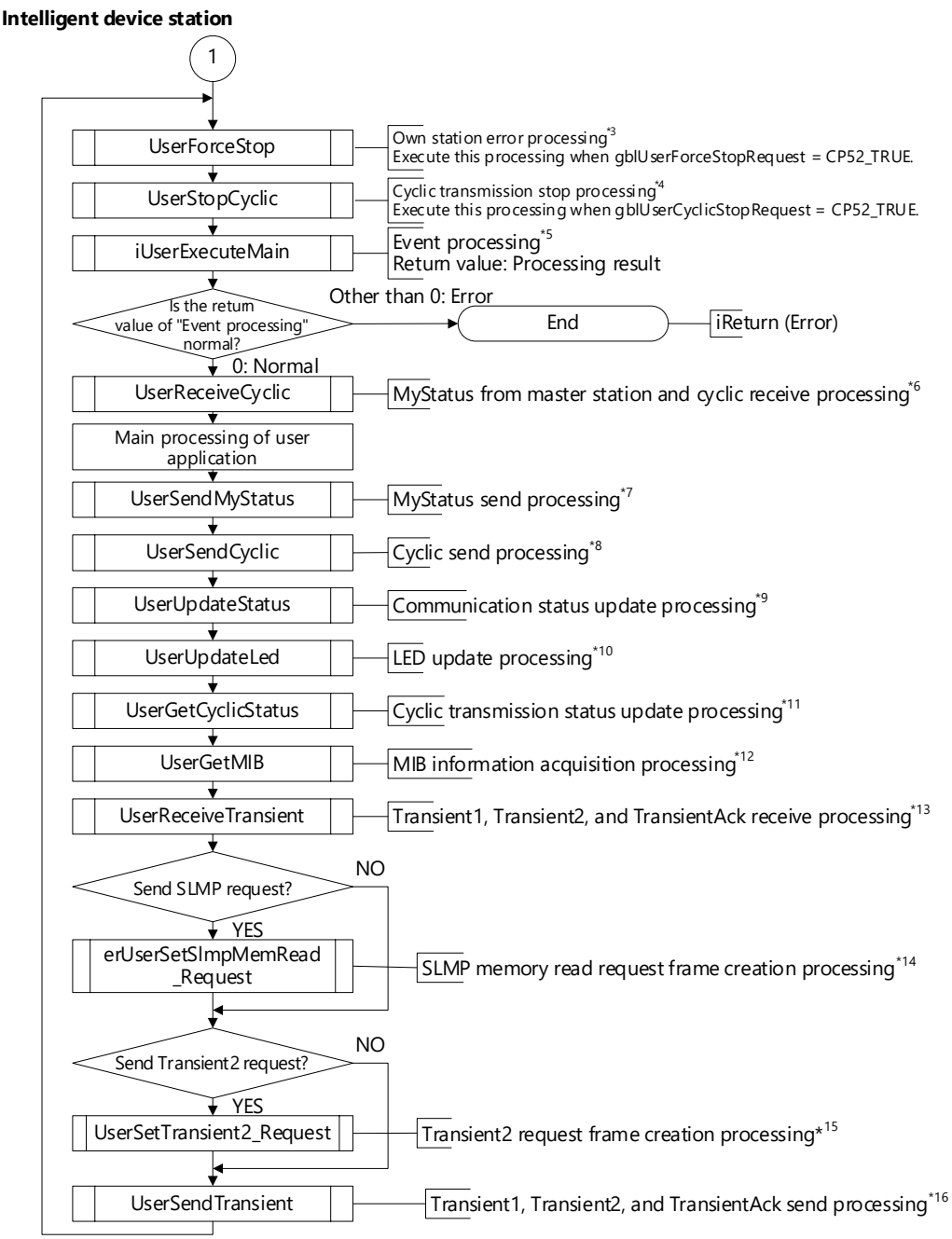
The following shows the general flow of the main processing.



*1: For details, refer to Section 10.2.2 "Initialization processing".

*2: For details, refer to Section 10.2.3 "Communication start processing".

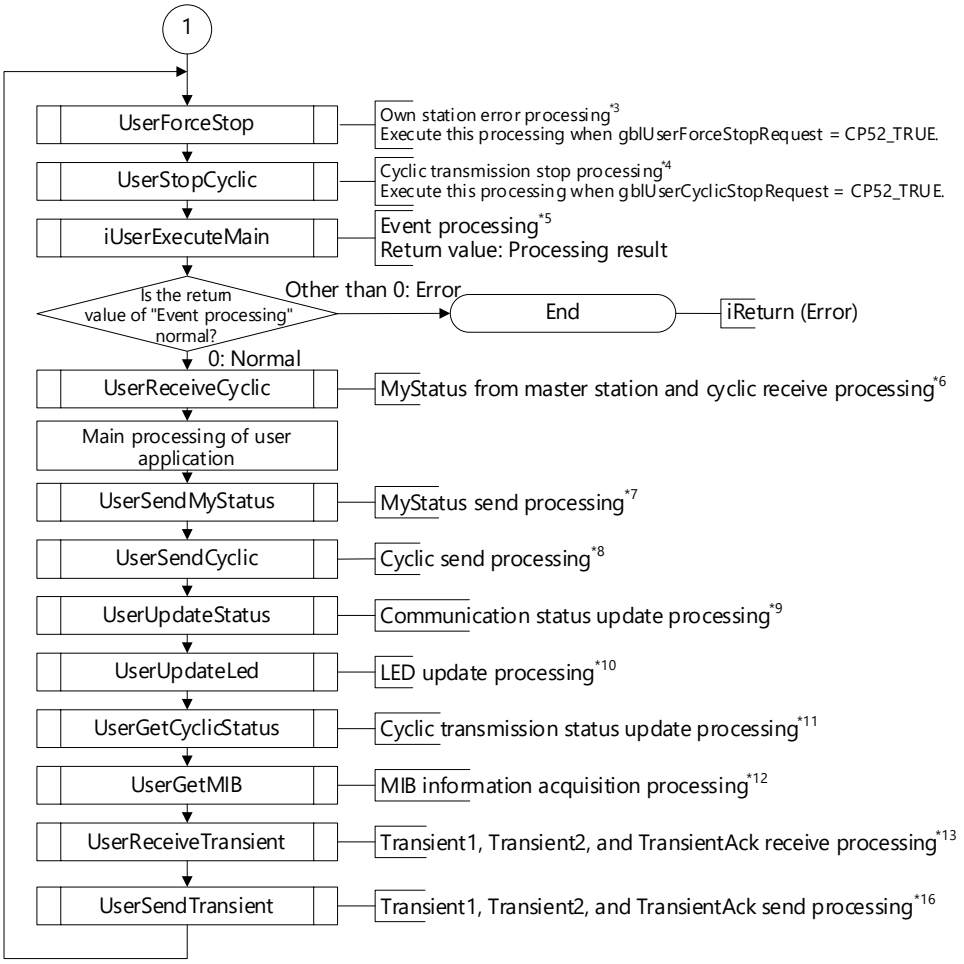
Figure 10.2.1-1 Flowchart for Main Processing (1/2)



*3: For details, refer to Section 10.2.4 "Own station error processing".
*4: For details, refer to Section 10.2.5 "Cyclic transmission stop processing".
*5: For details, refer to Section 10.2.6 "Event processing".
*6: For details, refer to Section 10.2.7 "MyStatus from master station and cyclic receive processing".
*7: For details, refer to Section 10.2.8 "MyStatus send processing".
*8: For details, refer to Section 10.2.9 "Cyclic send processing".
*9: For details, refer to Section 10.2.10 "Communication status update processing".
*10: For details, refer to Section 10.2.11 "LED update processing".
*11: For details, refer to Section 10.2.12 "Cyclic transmission status update processing".
*12: For details, refer to Section 10.2.13 "MIB information acquisition processing".
*13: For details, refer to Section 10.3.1 "Transient1, Transient2, and TransientAck receive processing".
*14: For details, refer to Section 10.3.14 "SLMP memory read request frame creation processing".
*15: For details, refer to Section 10.3.18 "Transient2 request frame creation processing".
*16: For details, refer to Section 10.3.13 "Transient1, Transient2, and TransientAck send processing".

Figure 10.2.1-2 Flowchart for Main Processing (2/3)

Remote device station

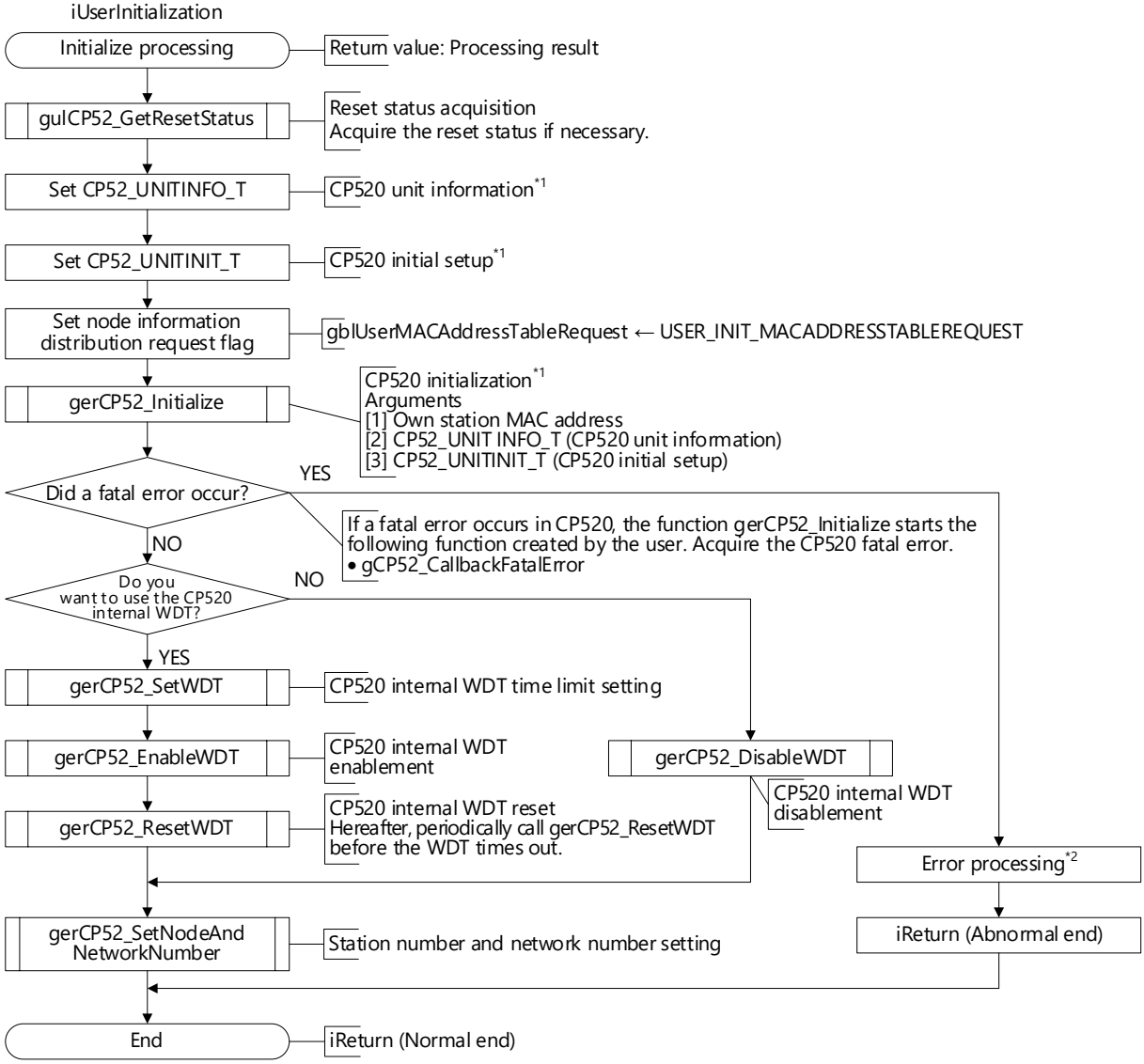


*3: For details, refer to Section 10.2.4 "Own station error processing".
*4: For details, refer to Section 10.2.5 "Cyclic transmission stop processing".
*5: For details, refer to Section 10.2.6 "Event processing".
*6: For details, refer to Section 10.2.7 "MyStatus from master station and cyclic receive processing".
*7: For details, refer to Section 10.2.8 "MyStatus send processing".
*8: For details, refer to Section 10.2.9 "Cyclic send processing".
*9: For details, refer to Section 10.2.10 "Communication status update processing".
*10: For details, refer to Section 10.2.11 "LED update processing".
*11: For details, refer to Section 10.2.12 "Cyclic transmission status update processing".
*12: For details, refer to Section 10.2.13 "MIB information acquisition processing".
*13: For details, refer to Section 10.3.1 "Transient1, Transient2, and TransientAck receive processing".
*16: For details, refer to Section 10.3.13 "Transient1, Transient2, and TransientAck send processing".

Figure 10.2.1-3 Flowchart for Main Processing (3/3)

10.2.2 Initialization processing

This function initializes CP520, enables and disables the CP520 internal WDT, and sets the station number and network number.



*1: For details, refer to Section 11.3.1 "Initial setup" (2) gerCP52_Initialize.

*2: For example, add processing such as calling UserForceStop (Own station error processing), and setting its own station to bypass mode.

Figure 10.2.2-1 Flowchart for Initialization Processing

[gblUserMACAddressTableRequest]

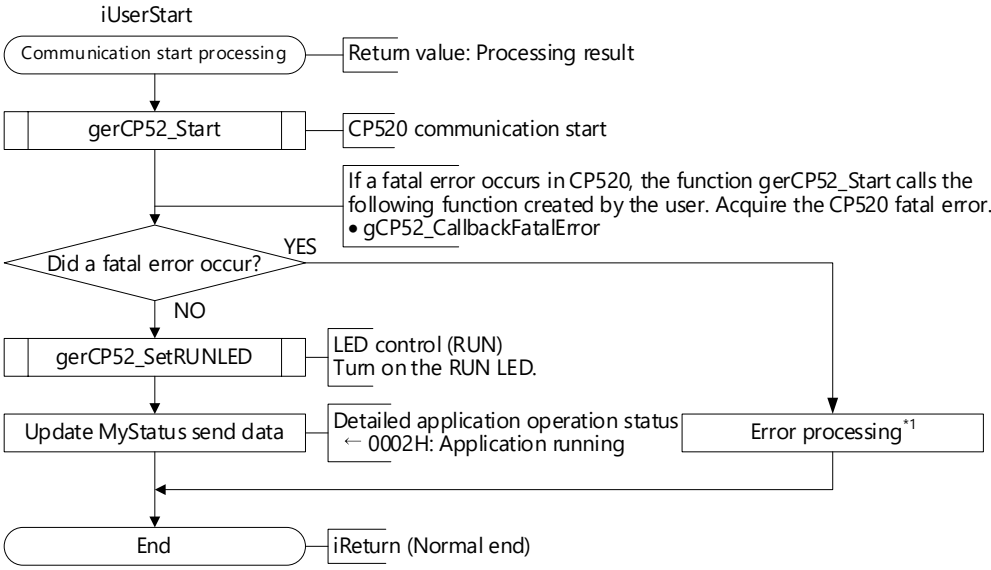
"gblUserMACAddressTableRequest" (node information distribution request flag) is used to determine whether or not the own station receives Node information distribution frame is to be received. (Refer to Section 10.3.2 "Transient1 receive data processing".)

- When own station wants to receive node information (when own station wants to send a transient request)
  Set both "blMACAddressTableRequest" (initial value of node information distribution request) and "gblUserMACAddressTableRequest" (node information distribution request flag) of CP52_UNITINIT_T to "CP52_TRUE".

- When own station does not want to receive node information (when own station does not want to send a transient request)
  Set both "blMACAddressTableRequest" (initial value of node information distribution request) and "gblUserMACAddressTableRequest" (node information distribution request flag) of CP52_UNITINIT_T to "CP52_FALSE".

10.2.3 Communication start processing

This function instructs CP520 to start communication.



*1: For example, add processing such as calling UserForceStop (Own station error processing), and setting its own station to bypass mode.

Figure 10.2.3-1 Flowchart for Communication Start Processing

10.2.4 Own station error processing

This function changes the state of its own station to an error when a (user defined) error occurs in the user program. (This processing is optional.)

When "gerCP52_ForceStop" is called, a CP520 own station enters an error state and the CP520 changes to bypass mode. In bypass mode, communication frames that have entered the port are not received by CP520 but are forwarded as is to another port.

To clear the own station error, power-on reset or system reset is required.

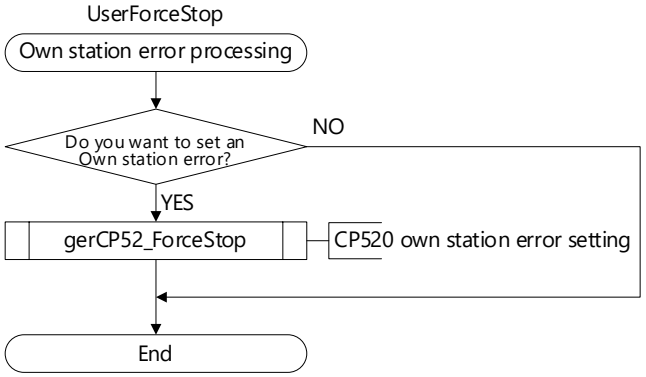


Figure 10.2.4-1 Flowchart for Own Station Error Processing

10.2.5 Cyclic transmission stop processing

This function allows you to control the stopping and restarting of cyclic transmission for user application-side reasons. (This processing is optional.)

Even if you stop cyclic transmission, transient transmission is possible. (Token passing continues.)

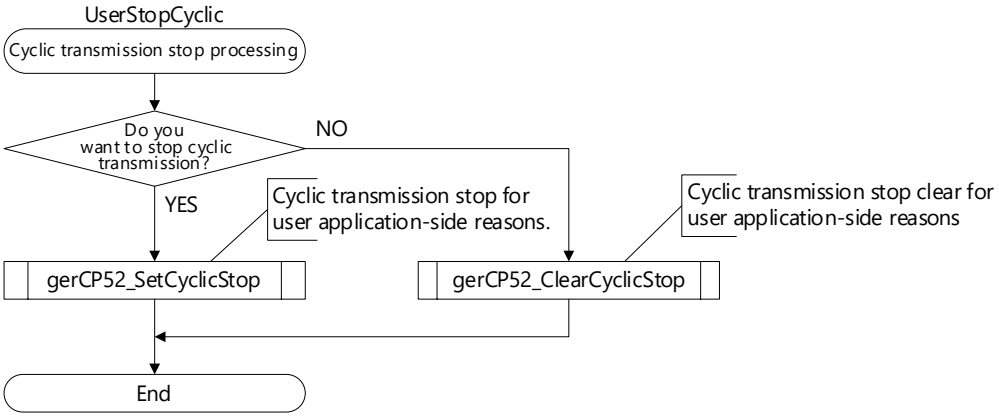
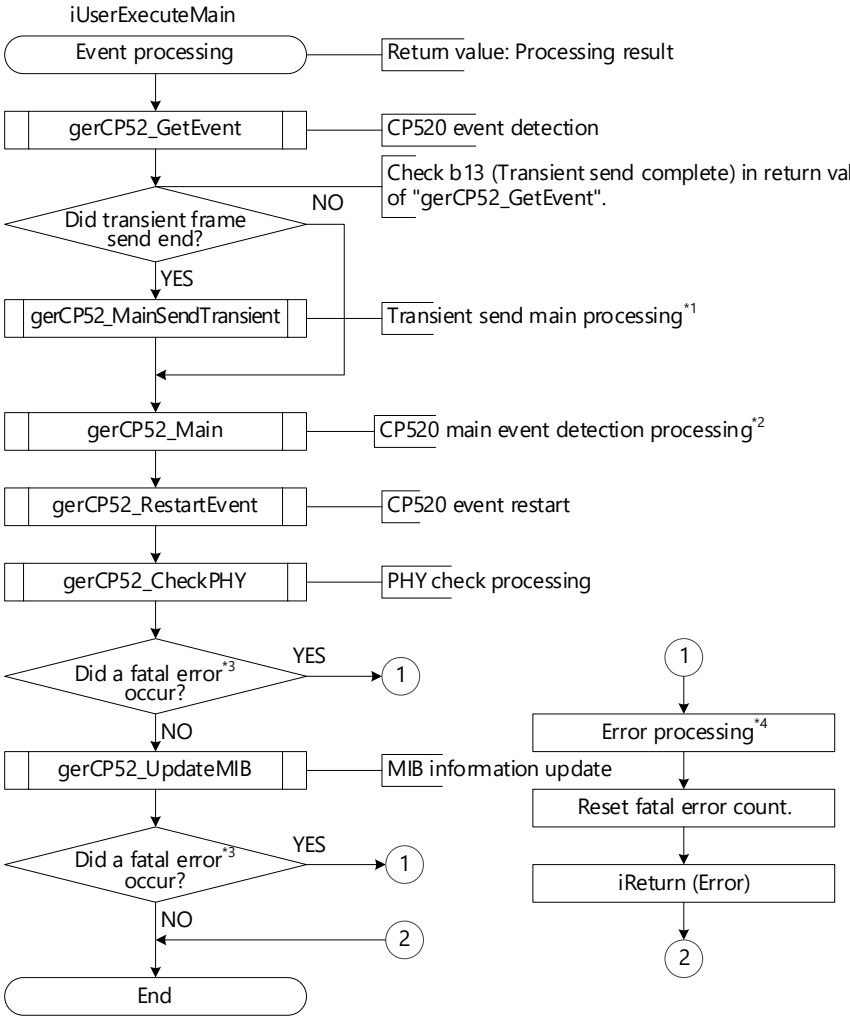


Figure 10.2.5-1 Flowchart for Cyclic Transmission Stop Processing

10.2.6 Event processing

This function detects CP520 events (interrupts causes), processes the events, and updates MIB information.



*1: This function calls the following function created by the user to report the target send descriptor status (send result).
- gerCP52_CallbackTransientSendingComplete

*2: When a command is received from the master station, the function gerCP52_Main calls the following function created by the user. Be sure to acquire the command.
- gerCP52_CallbackCommandFromMaster

*3: If a fatal error occurs in CP520, the function gerCP52_UpdateMIB calls the following function created by the user. Be sure to acquire the CP520 fatal error.
- gCP52_CallbackFatalError

*4: For example, add processing such as calling UserForceStop (Own station error processing), and setting its own station to bypass mode.

Figure 10.2.6-1 Flowchart for Event Processing

10.2.7 MyStatus from master station and cyclic receive processing

This function acquires the status of the master station from the received MyStatus frame and acquires cyclic data (RY, RWw) from the received cyclic frame. Perform "Hold/Clear processing" in accordance with the status of the master station that is acquired from the MyStatus frame (in accordance with whether the master station is stopped, an error occurred, or the like).

This function determines the output status (Hold or Clear) when the master station application has stopped or entered in an error state, or when the own station disconnects from the data link, if the CP520 application product controls external output.

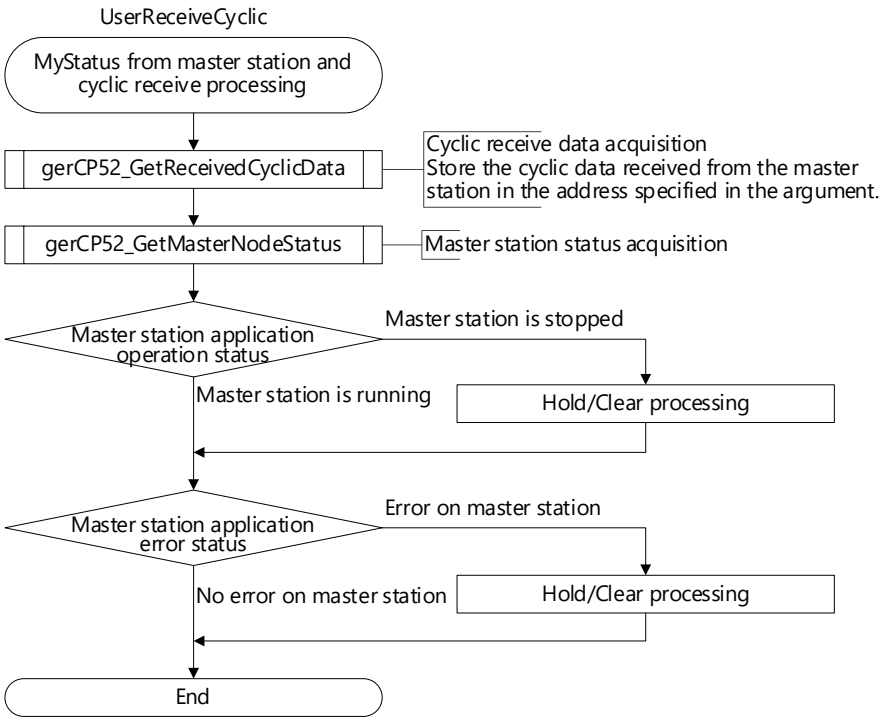


Figure 10.2.7-1 Flowchart for MyStatus from Master Station and Cyclic Receive Processing

Precautions

Consider 1) and 2) below and implement the Hold/Clear processing as a fail-safe.

1) Cyclic data (RY, RWw) sent by the master station
   When a master station application has stopped or entered an error state, cyclic data sent by the master station is held or cleared depending on the setting of the master station. (When the master station manufactured by Mitsubishi Electric is used, Hold/Clear processing is set in the "Output Setting During CPU STOP" parameter or the "Error Time Output Mode" parameter using the engineering tool.)
   There is no way for the slave station (own station) to know the status of the cyclic data sent by the master station (held data or cleared data).
2) Cyclic data (RY, RWw) acquired by the CP520 driver depending on the master station application status
   Cyclic data received in a slave station (own station) is acquired by the CP520 driver (gerCP52_GetReceivedCyclicData).
   Contents of acquired cyclic data differ depending on the operation/error status of the master station application.

Master Station Application		Cyclic Data Acquired by the CP520 Driver
Operating status	Error status	
Running	No error	Cyclic data that the master station is "currently" sending
Stopped	No error	
Running*1	Error*1	Not acquired (At the address specified by the argument, cyclic data stored in point of time before an error occurs in the master station application remains.)
Stopped	Error	

*1: When the master station manufactured by Mitsubishi Electric is used, the programmable controller CPU module cannot be in a state of "Operating" and "Error" at the same time.

10.2.8 MyStatus send processing

This function creates the MyStatus frame. The created frame is automatically sent by CP520.

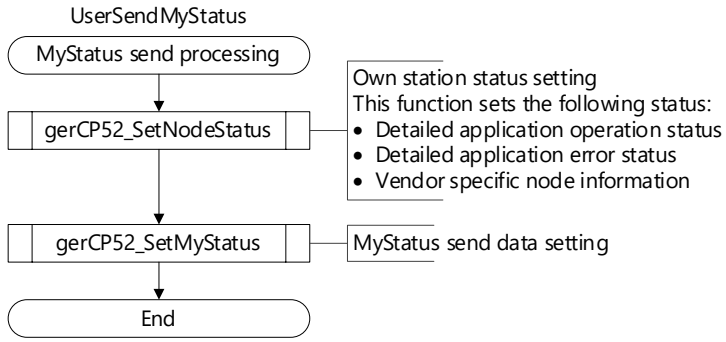


Figure 10.2.8-1 Flowchart for MyStatus Send Processing

10.2.9 Cyclic send processing

This function sends cyclic send data (RX and RWr).

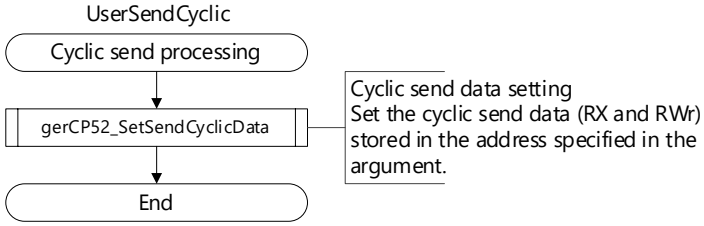


Figure 10.2.9-1 Flowchart for Cyclic Send Processing

10.2.10 Communication status update processing

This function acquires the data link status of the own station, and sets the Hold/Clear processing and the ERR. LED control flag in accordance with the data link status.

The ERR. LED control flag is used to control the ERR. LED in the LED update processing. (Refer to Section 10.2.11 "LED update processing".)
This function determines the output status (Hold or Clear) when the master station application has stopped or entered in an error state, or when the own station disconnects from the data link, if the CP520 application product controls external output.

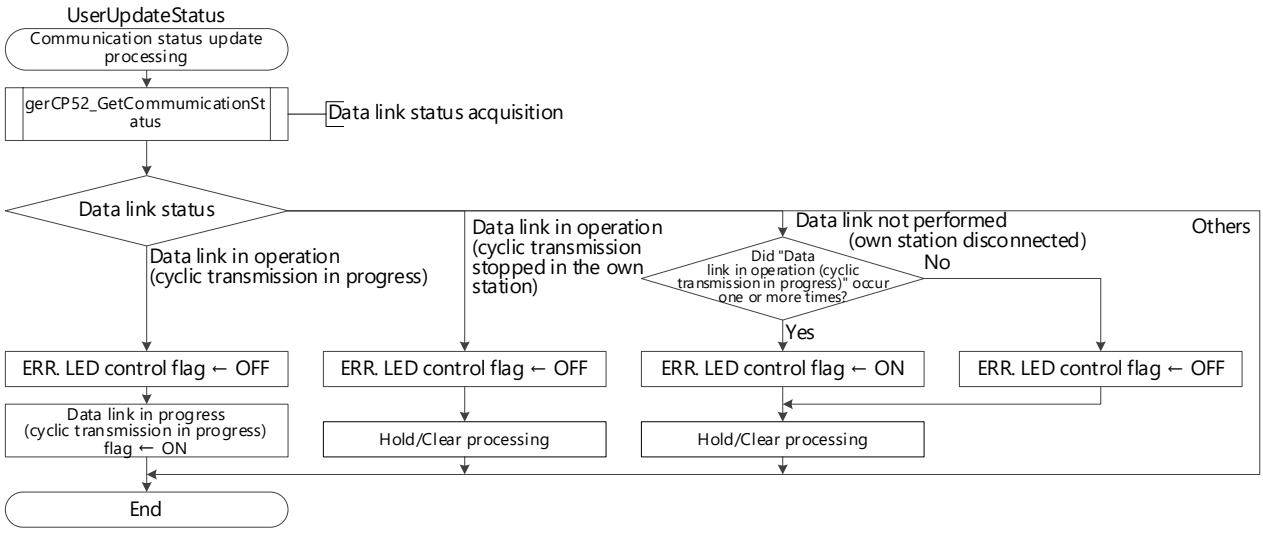


Figure 10.2.10-1 Flowchart for Communication Status Update Processing

Precautions

Consider the following, and implement the Hold/Clear processing as a fail-safe measure.

Cyclic data (RY, RWw) acquired by the CP520 driver depending on the data link status
Cyclic data received in a slave station (own station) is acquired by the CP520 driver (gerCP52_GetReceivedCyclicData).
Contents of acquired cyclic data differ depending on data link status.

Data Link Status	Cyclic Data Acquired by the CP520 Driver
Data link not performed (The own station is disconnected.)	Not acquired (At the address specified by the argument, cyclic data stored in point of time before the own station is disconnected remains.)
Data link in operation (Cyclic transmission is stopped in the own station.)*1	Cyclic data that the master station is "currently" sending

*1: The slave station receives RY, RWw and does not send RX, RWr.

10.2.11 LED update processing

This function controls the on, off, and blinking state of the D LINK LED and L ER LED in accordance with the data link status of its own station.

The ERR. LED status is controlled by the ERR. LED control flag set in Section 10.2.10 "Communication status update processing".
To control the ERR. LED status in the user application, change the value of the ERR. LED control flag within this function.

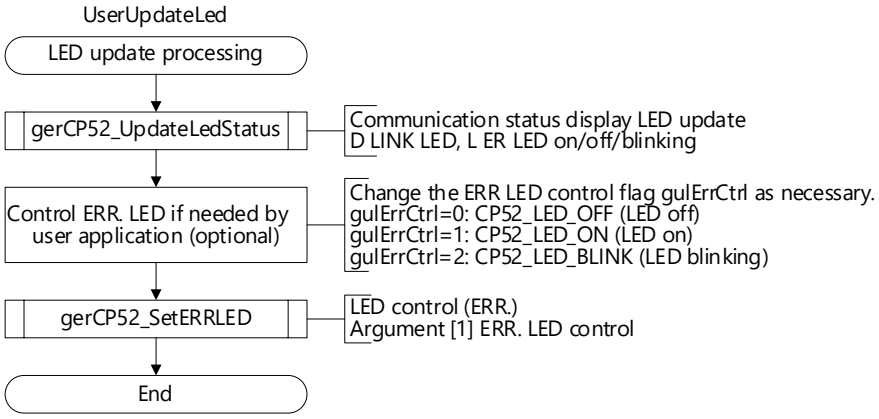
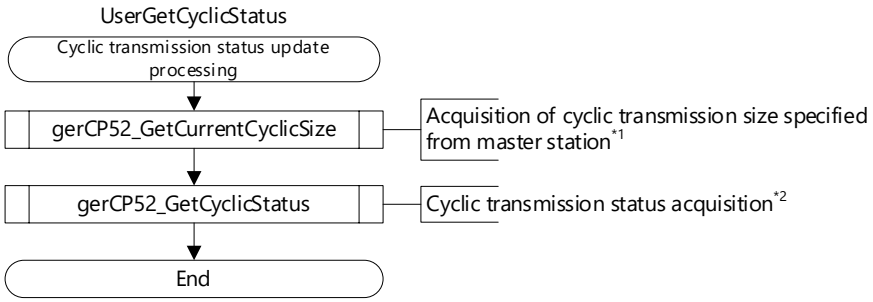


Figure 10.2.11-1 Flowchart for LED Update Processing

10.2.12 Cyclic transmission status update processing

This function acquires the cyclic transmission size specified by the master station and the cyclic transmission status. (This processing is optional.)



*1: Cyclic transmission is performed by CP520 based on the cyclic transmission size specified by the master station.
If own station wants to acquire the cyclic transmission size specified by the master station, call "gerCP52_GetCurrentCyclicSize".
For example, this processing can be used for the devices which continuously monitor the link device size of the own station and change the user application side operation according to the size change.

*2: Cyclic transmission is processed by the CP520 driver. The user program does not need to acquire the cyclic transmission status or perform processing in accordance with the status.
If own station wants to acquire the cyclic transmission status, call "gerCP52_GetCyclicStatus".
For example, this processing can be used for the devices which continuously monitor the cyclic transmission status and change the user application side operation according to the status such as disconnection.

Figure 10.2.12-1 Flowchart for Cyclic Transmission Status Update Processing

10.2.13 MIB information acquisition processing

This function acquires MIB information. (This processing is optional.)
MIB information can be used in processing such as the following:
Example: Processing in which the user program monitors the frame send/receive status and issues a report or warning in accordance with the normal state or error frequency.

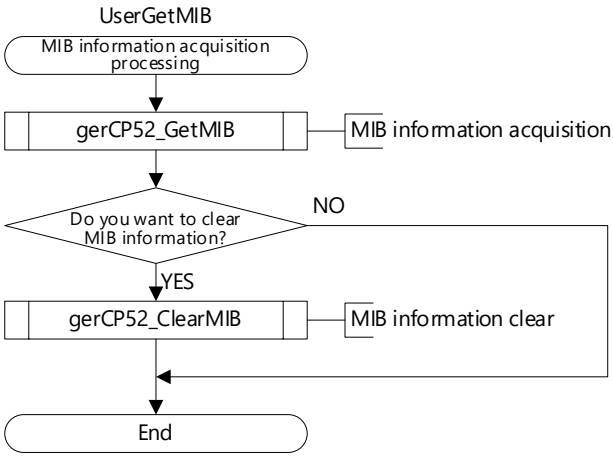


Figure 10.2.13-1 Flowchart for MIB Information Acquisition Processing

Caution
MIB information is non-disclosed information. Do not disclose the information to the end user.

(1) List of MIB information of ring control area

Table 10.2.13-1 List of MIB Information of Ring Control Area

No.	MIB Information	Description
1	Number of HEC error frames	Counts the number of HEC errors in received frames.
2	Number of DCS/FCS error frames	Counts the number of DCS/FCS errors in received frames.
3	Number of undersize error frames	Counts the number of received error frames with a size less than 28 bytes.
4	Number of forwarded frames	Counts the number of forwarded frames.
5	Number of upper layer transmission frames	Counts the number of frames transmitted to upper layers.
6	Number of discarded frames due to full forward buffer	Counts the number of frames discarded due to a full forward buffer.
7	Number of discarded frames due to full upper layer transmission buffer	Counts the number of frames discarded due to a full upper layer transmission buffer.

(2) List of MIB information of MAC IP area

Table 10.2.13-2 List of MIB Information of MAC IP Area

No.	MIB Information	Description
1	Number of received frames	Counts all frame receptions, including error frames. Error frames: FCS error, undersized, oversized frames
2	Number of sent frames	Counts the number of sent frames.
3	Number of received undersized frames	Counts the number of received frames with a size less than 64 bytes.
4	Number of received oversized frames	Counts the number of received frames with a size exceeding 1518 bytes.
5	Number of received frame FCS errors	Counts the number of received frames with an FCS error.
6	Number of received frame fragment errors	Counts the number of received frames with fragment errors. Fragment error: A frame with less than 64 bytes and an FCS error
7	Number of frames detected within minimum IFG	Counts the number of frames detected within the minimum inter-frame gap (IFG).
8	Number of received frames with SFD or less	Counts the number of received frames that ended at a field up to SFD and were not recognized as a valid frame.
9	Number of reception code errors	Counts the number of GMII reception data errors detected (RECV_*_ERR=1[*1]). Counts a RECV_*_ERR[*1] that occurred multiple times in an idle state (RECV_*_DV=1[*1]) as one error. *1: The asterisk ("*") indicates a wild character. (A: Port 0, B: Port 1)
10	Number of received invalid carrier errors	Counts the number of invalid carriers that occurred in an idle state. Counts multiple invalid carriers that occurred in an idle state as one error.
11	Number of received carrier extension errors	Counts the number of carrier extensions that occurred in an idle state. Counts multiple carrier extensions that occurred in an idle state as one error.

(3) List of other MIB information

Table 10.2.13-3 List of Other MIB Information

No.	MIB Information	Description
1	Number of link downs (port 1)	Counts the number of link downs of port 0.
2	Number of link downs (port 2)	Counts the number of link downs of port 1.
3	Number of master watch timer errors	Counts the number of timeouts of the master watch timer.
4	Number of received cyclic frames	Counts the number of cyclic frames received by CP520.
5	Number of received transient frames	Counts the number of transient frames received by CP520.
6	Number of received transient frames discarded	Counts the number of received transient frames discarded by CP520.

10.2.14 Receive processing of token frame addressed to the own station

This function receives the token frame which is addressed to the own station.

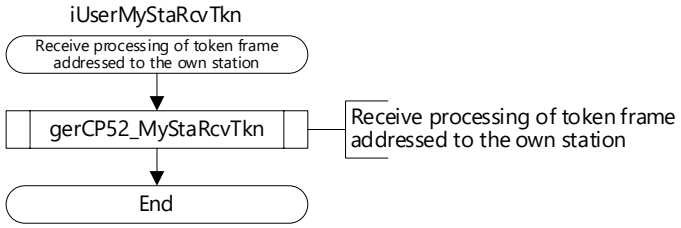


Figure 10.2.14-1 Flowchart for Receive Processing of Token Frame Addressed to the Own Station

This processing is called from "int1_task" of the main.c file[*1].
Do not change the priority of int1_task processing unless there is a special reason.
*1: This file is stored in the "...\Intelligent_Device\English" or "...\Remote_Device\English" folder.

(1) Transient transmission processing overview

[When the own station is a server]
The following shows an image of the processing procedure in which the server sends a response frame in response to a request frame from a client.

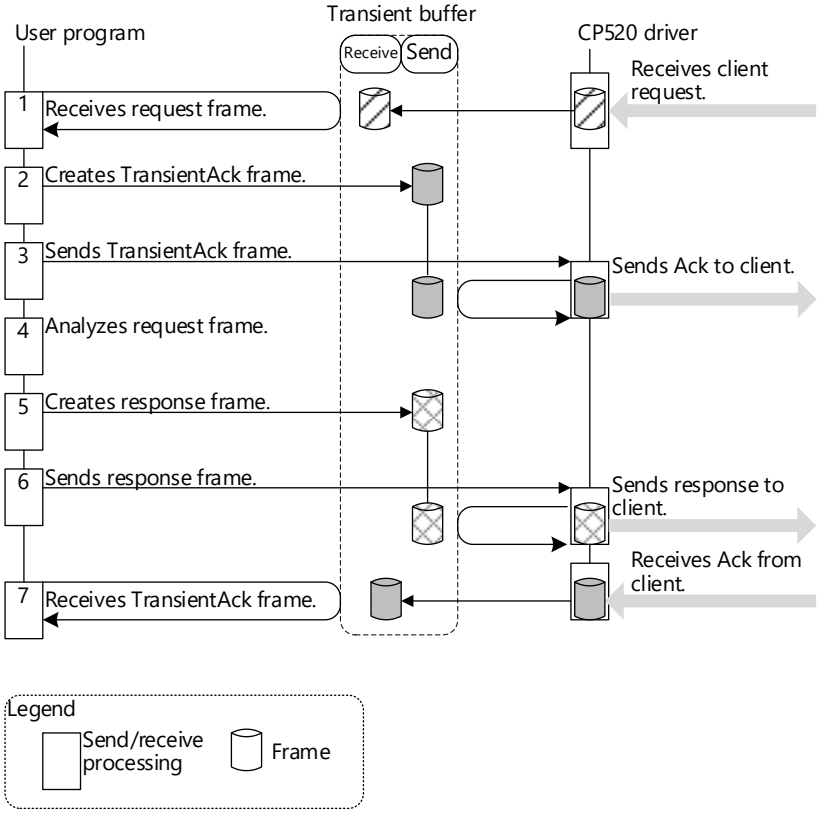


Figure 10.3-1 Server Processing Procedure

No.	Processing	Reference Section
1	Receives Transient frame.	• Section 10.3.1 "Transient1, Transient2, and TransientAck receive processing"
2	Creates TransientAck frame.	• Section 10.3.12 "TransientAck frame creation processing"
3	Sends TransientAck frame.	• Section 10.3.13 "Transient1, Transient2, and TransientAck send processing"
4	Analyzes received request frame and performs processing for each frame.	• Section 10.3.2 "Transient1 receive data processing" • Section 10.3.7 "Transient2 receive data processing"
5	Creates response frame in accordance with command.	• Section 10.3.5 "SLMP memory read request frame receive processing" • Section 10.3.6 "SLMP memory write request frame receive processing" • Section 10.3.9 "Transient2 memory write request receive processing"
6	Sends response frame.	• Section 10.3.13 "Transient1, Transient2, and TransientAck send processing"
7	Receives TransientAck frame.	• Section 10.3.11 "TransientAck receive data processing"

[When the own station is a client]
The following shows an image of the processing procedure in which the client sends a request frame and receives a response frame from the server.

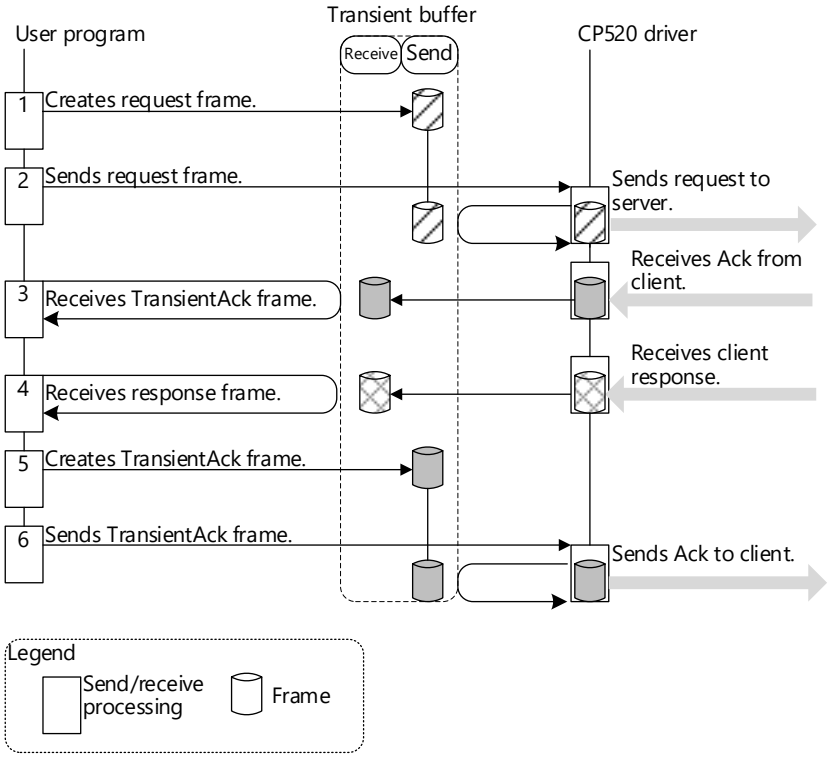


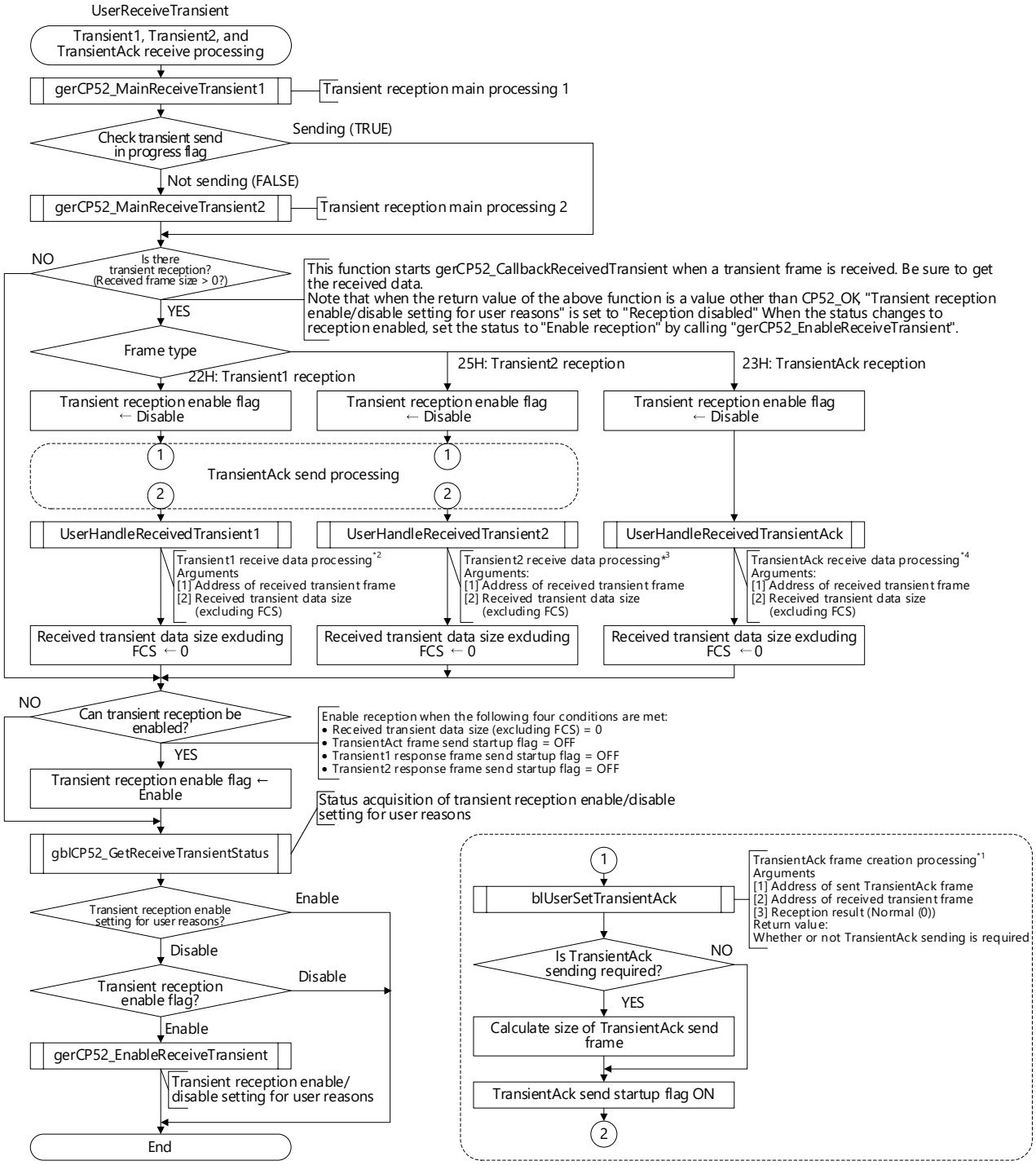
Figure 10.3-2 Client Processing Procedure

No.	Processing	Reference Section
1	Creates request frame.*1	• Section 10.3.14 "SLMP memory read request frame creation processing" • Section 10.3.18 "Transient2 request frame creation processing"
2	Sends request frame.	• Section 10.3.13 "Transient1, Transient2, and TransientAck send processing"
3	Receives TransientAck frame.	• Section 10.3.1 "Transient1, Transient2, and TransientAck receive processing" and Section 10.3.11 "TransientAck receive data processing"
4	Receives response frame.	• Section 10.3.2 "Transient1 receive data processing" and Section 10.3.17 "SLMP memory read response receive processing" • Section 10.3.7 "Transient2 receive data processing" and Section 10.3.20 "Transient2 memory read response receive processing"
5	Creates TransientAck frame.	• Section 10.3.12 "TransientAck frame creation processing"
6	Sends TransientAck frame.	• Section 10.3.13 "Transient1, Transient2, and TransientAck send processing"

*1: Transient2 memory read and SLMP memory read are described in sample code as the sample processing of each command. Implement commands other than the above by customizing the user program.

10.3.1 Transient1, Transient2, and TransientAck receive processing

This function receives Transient1, Transient2, and TransientAck frames and processes the data.



*1: For details, refer to Section 10.3.12 "TransientAck frame creation processing".

*2: For details, refer to Section 10.3.2 "Transient1 receive data processing".

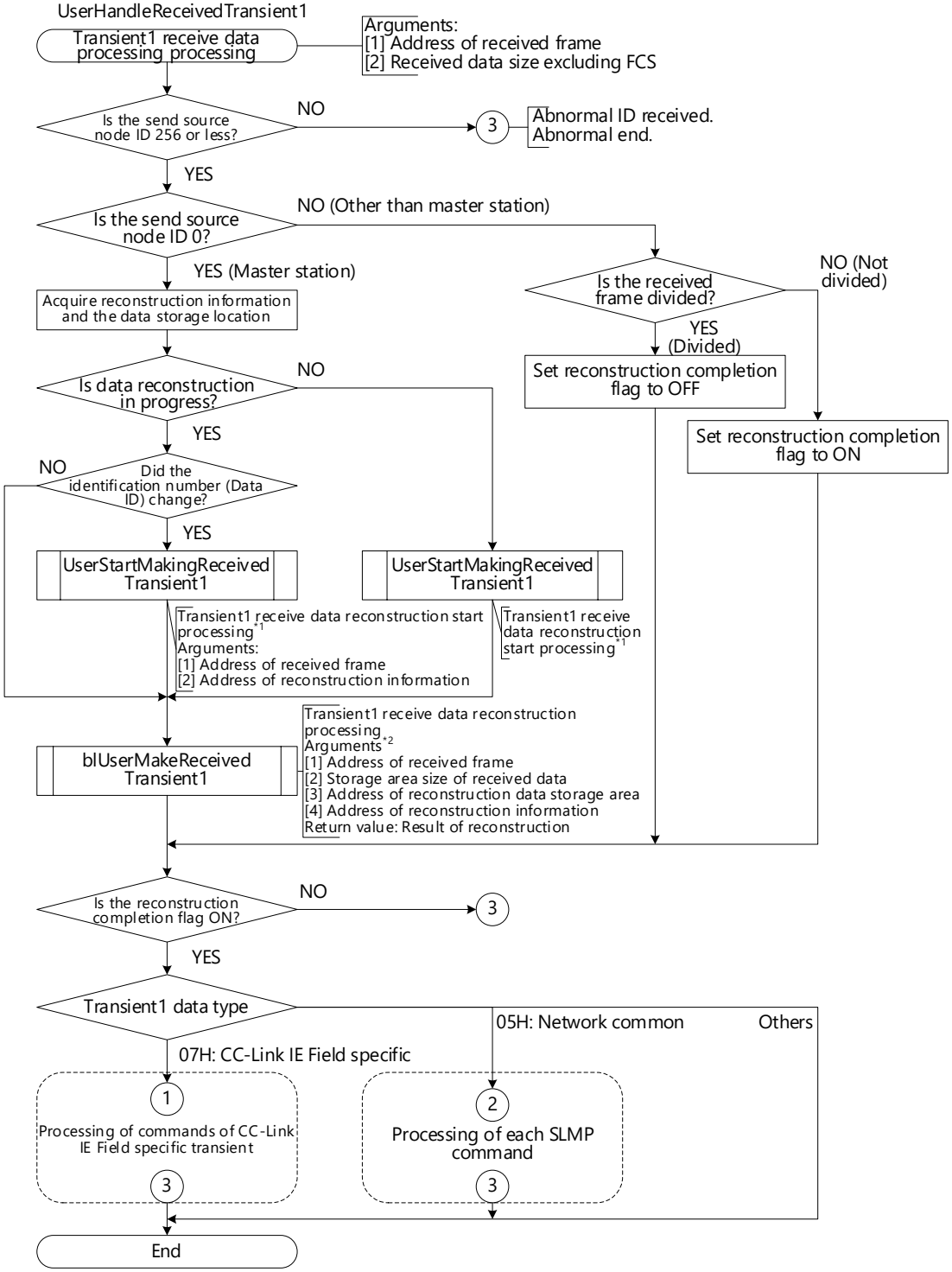
*3: For details, refer to Section 10.3.7 "Transient2 receive data processing".

*4: For details, refer to Section 10.3.11 "TransientAck receive data processing".

Figure 10.3.1-1 Flowchart for Transient1, Transient2, and TransientAck Receive Processing

10.3.2 Transient1 receive data processing

This function analyzes a received Transient1 frame and performs processing in accordance with the analysis result. In addition, this function reconstructs data when a Transient1 frame is received divided.



*1: For details, refer to Section 10.3.3 "Transient1 receive data reconstruction start processing".

*2: For details, refer to Section 10.3.4 "Transient1 receive data reconstruction processing".

Figure 10.3.2-1 Flowchart for Transient1 Receive Data Processing (1/5)

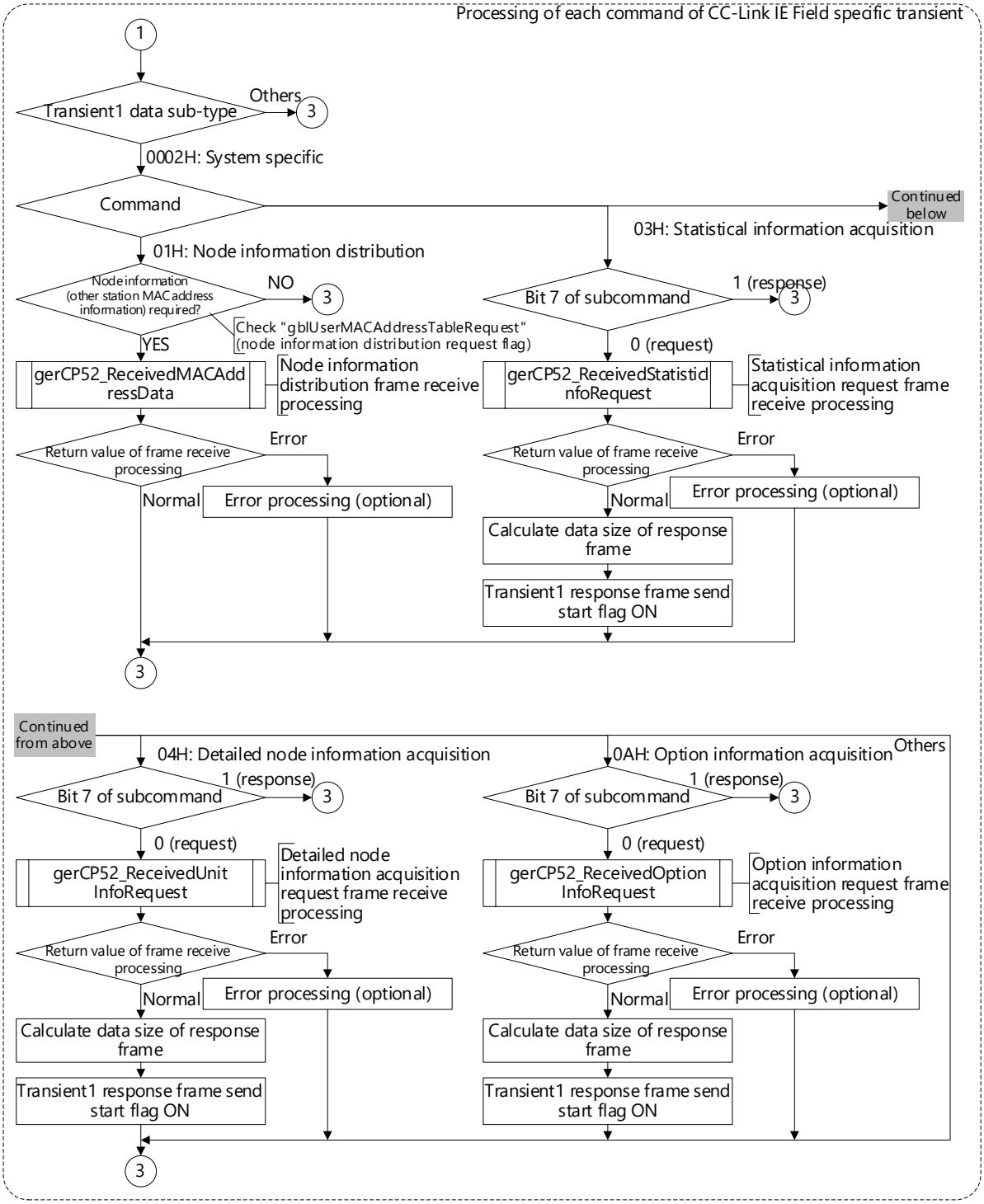
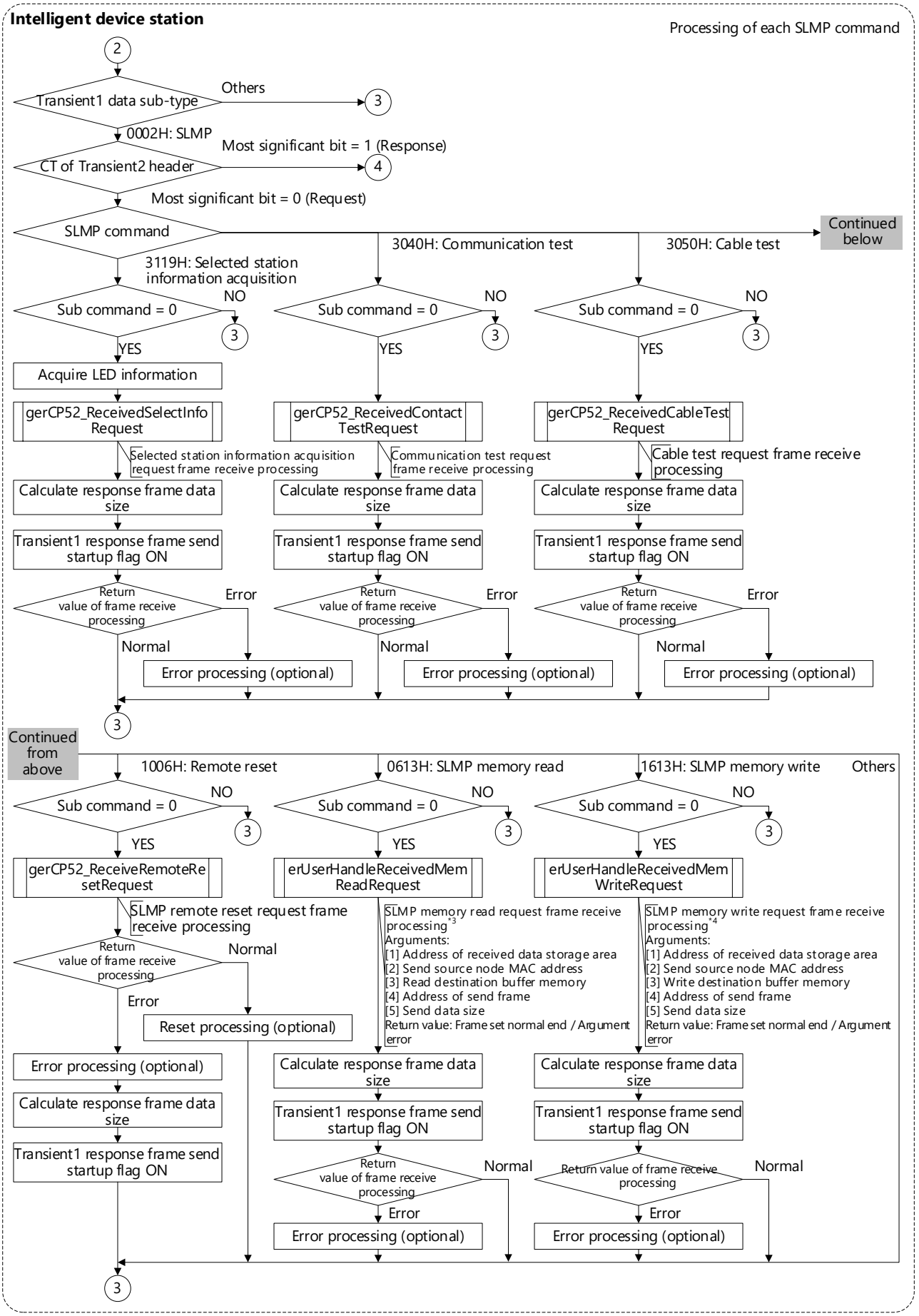


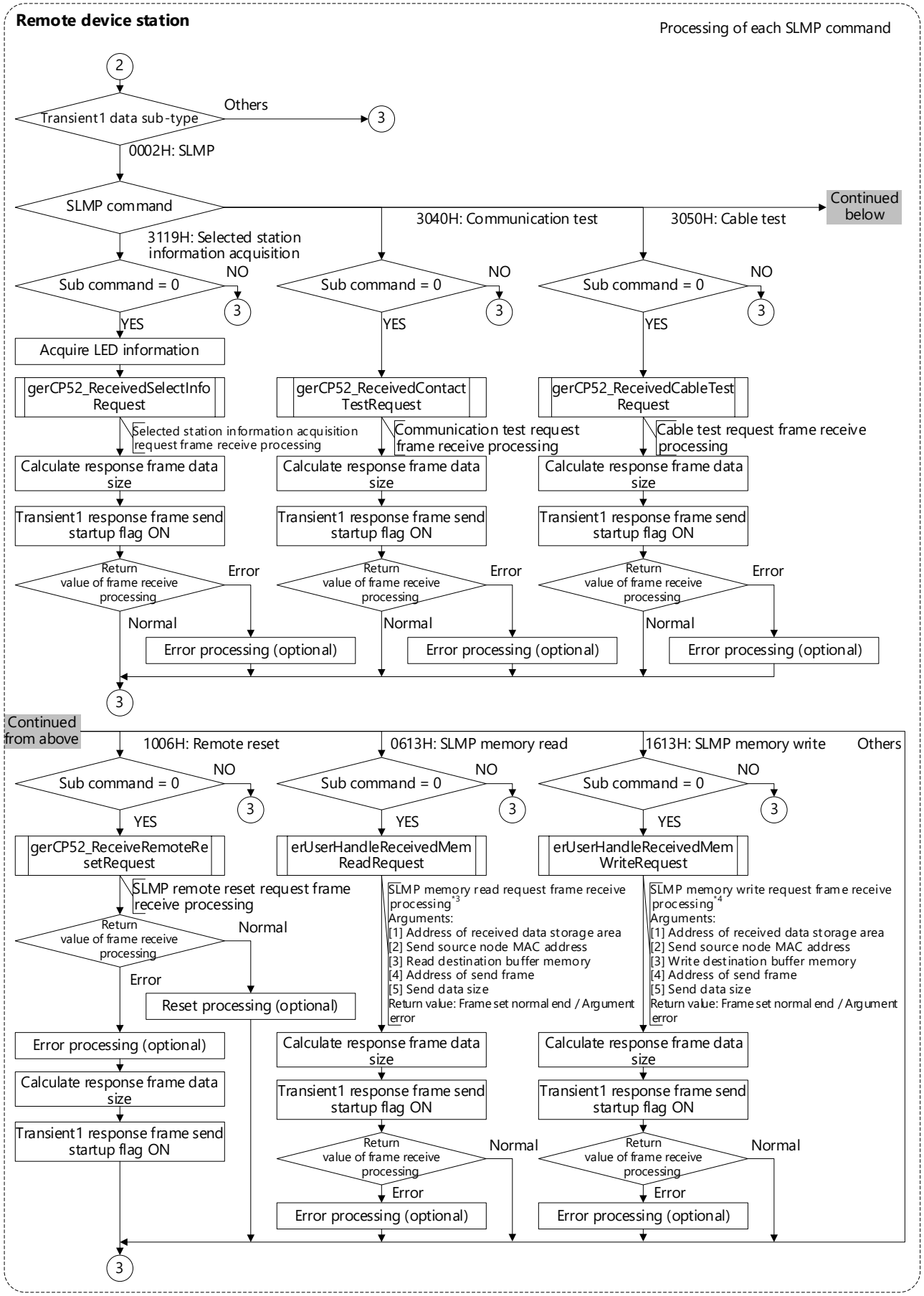
Figure 10.3.2-2 Flowchart for Transient1 Receive Data Processing (2/5)



*3: For details, refer to Section 10.3.5 "SLMP memory read request frame receive processing".

*4: For details, refer to Section 10.3.6 "SLMP memory write request frame receive processing".

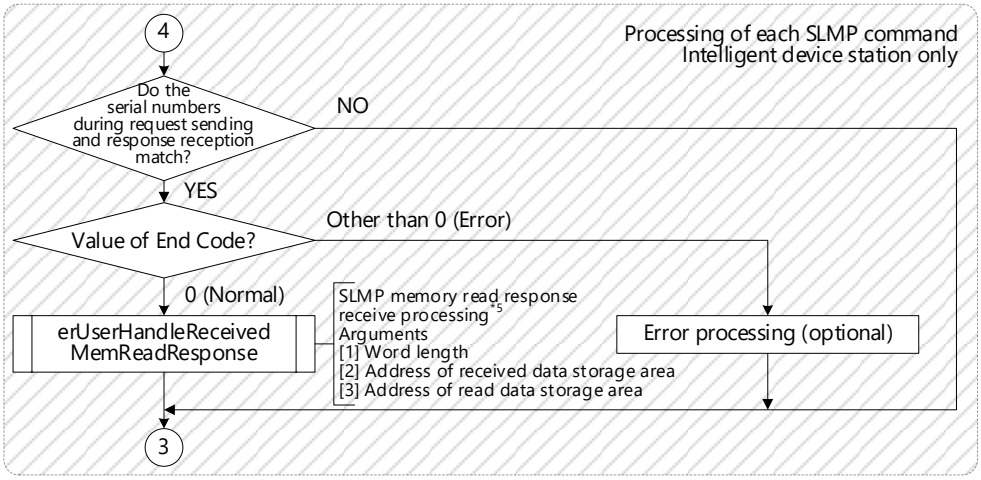
Figure 10.3.2-3 Flowchart for Transient1 Receive Data Processing (3/5)



*3: For details, refer to Section 10.3.5 "SLMP memory read request frame receive processing".

*4: For details, refer to Section 10.3.6 "SLMP memory write request frame receive processing".

Figure 10.3.2-4 Flowchart for Transient1 Receive Data Processing (4/5)



*5: For details, refer to Section 10.3.17 "SLMP memory read response receive processing".

Figure 10.3.2-5 Flowchart for Transient1 Receive Data Processing (5/5)

(1) Node information distribution

Node information is information that indicates the correspondence between other station numbers and MAC addresses.

Node information is used when an intelligent device station sends a transient request to another station (when own station is client).

- When own station wants to receive node information (when own station wants to send a transient request)
  In iUserInitialization (Section 10.2.2 "Initialization processing"), set both "blMACAddressTableRequest" (initial value of node information distribution request) and "gblUserMACAddressTableRequest" (node information distribution request flag) to "CP52_TRUE".
  Note that a TransientAck and transient response are not required for received node information distribution frames.

- When own station does not want to receive node information (when own station does not want to send a transient request)
  In iUserInitialization (Section 10.2.2 "Initialization processing"), set both "blMACAddressTableRequest" (initial value of node information distribution request) and "gblUserMACAddressTableRequest" (node information distribution request flag) to "CP52_FALSE".

(2) SLMP request reception from master station

The CC-Link IE Field Network diagnostics and parameter processing/command execution of slave stations can be performed using the engineering tool. These functions can be used by its own station responding to an SLMP request frame from the master station.

The following shows an image of the processing procedure in which the server sends SLMP response frame in response to SLMP request frame from the master station. The following figure is based on the selected station information acquisition command. The processing for sending and receiving is the same as that for the communication test, cable test, remote reset command, and the commands described in the CSP+ file.

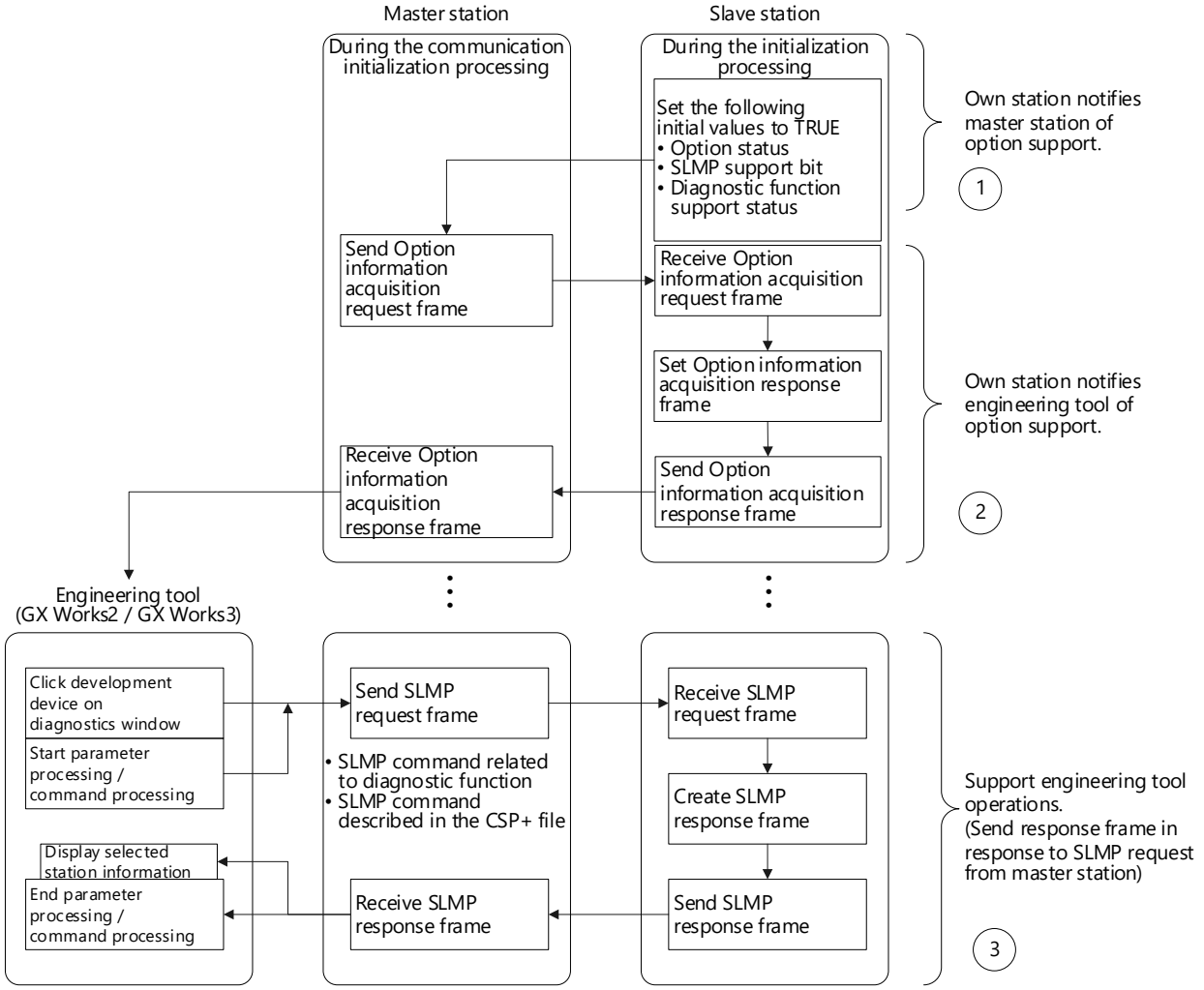


Figure 10.3.2-6 SLMP Request Reception Procedure

1) CP52_UNIT_INIT_T setup (CP520 initial setup)
Set the following members of CP52_UNITINIT_T to "CP52_TRUE". For details, refer to "Table 11.3.1-2 CP52_UNITINIT_T List".
• ulOptionSupport (Initial value of option status)
• ulSlmpSupport (Initial value of SLMP support bit)
• ulSlmpDiagnosisSupport (Initial value of diagnostic function support status)

2) Response to Option information acquisition request frame
The CP520 driver interface function "gerCP52_ReceivedOptionInfoRequest" responds to the Option information acquisition request frame from the master station.

3) Response to Selected station information acquisition request frame
The CP520 driver interface function "gerCP52_ReceivedSelectInfoRequest" responds to the Selected station information acquisition request frame from the master station.

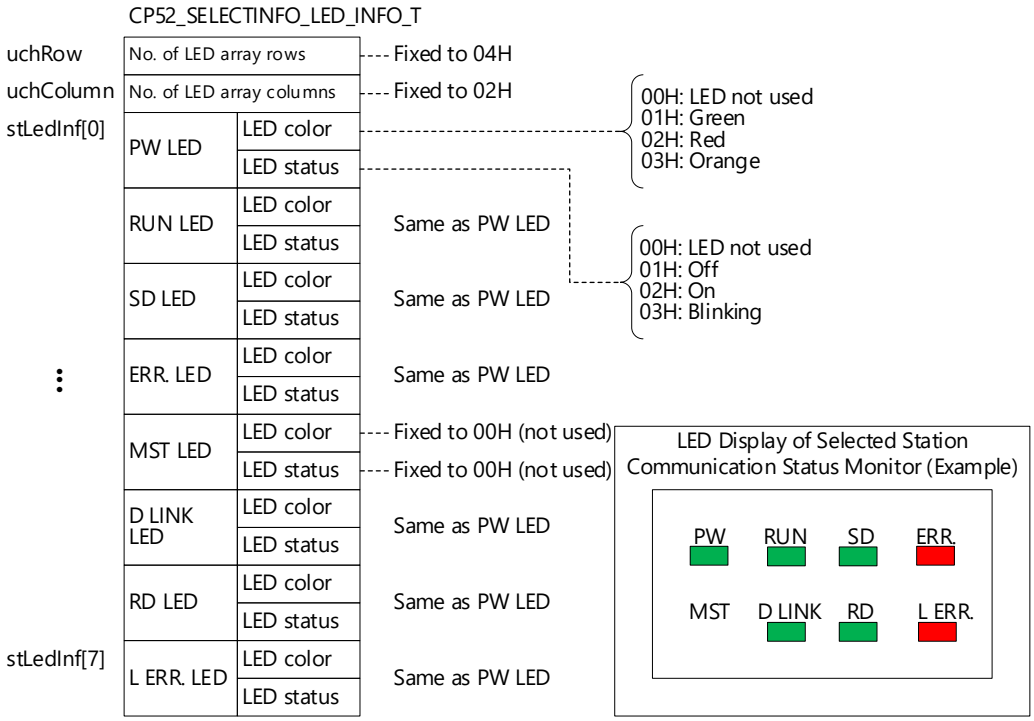
(3) Creating LED information

To display the LED status of its own station on the selected station communication status monitor, store the LED information corresponding to its own station status in "CP52_SELECTINFO_LED_INFO_T".

*: Make sure the LED information matches the status of the LEDs mounted in the CP520 application circuit.

Table 10.3.2-1 CP52_SELECTINFO_LED_INFO_T

No.	Member		Description
1	UCHAR	uchRow	Number of LED array rows (fixed to 04H)
2	UCHAR	uchColumn	Number of LED array columns (fixed to 02H)
3	CP52_LED_INFO_T	stLedInf[8]	LED information 1 to 8



Remarks
When the LED status (on/off/blinking) of the CP520 application circuit changes at an interval shorter than the communication interval of selected station information acquisition, the change in the LED status is not transmitted to the engineering tool (such as with LEDs that repeated turn on and off at high speed, such as SD and RD). When GX Works2 and GX Works3 are used, the communication interval of selected station information acquisition is approximately 5 seconds, and therefore the LED display on the diagnostics window differs from the actual LED status.

10.3.3 Transient1 receive data reconstruction start processing

This function starts reconstructing the divided Transient1 receive frame.

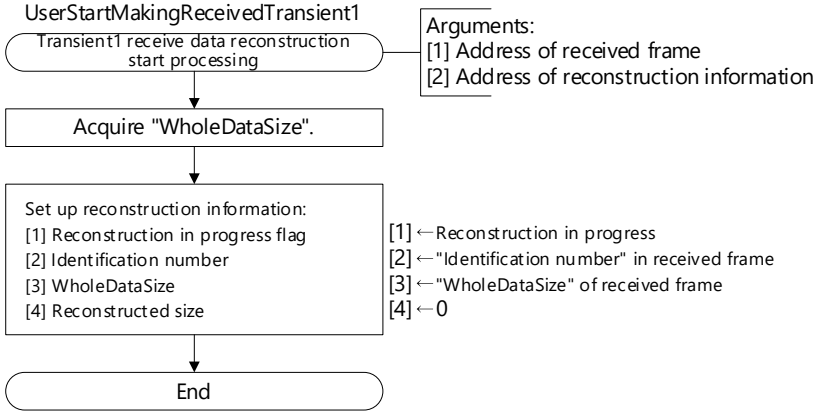


Figure 10.3.3-1 Flowchart for Transient1 Receive Data Reconstruction Start Processing

10.3.4 Transient1 receive data reconstruction processing

This function reconstructs the data of the Transient1 frame.

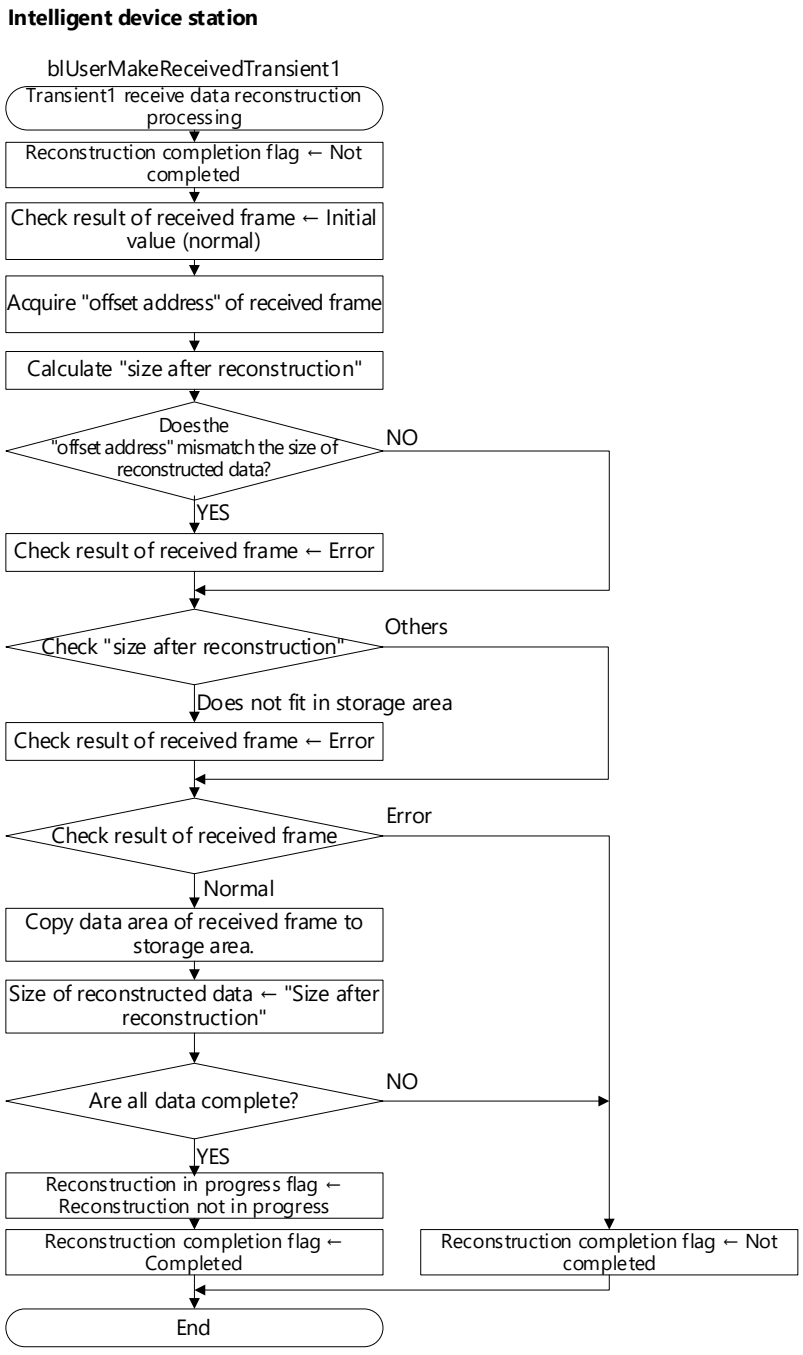


Figure 10.3.4-1 Flowchart for Transient1 Receive Data Reconstruction Processing (1/2)

Remote device station

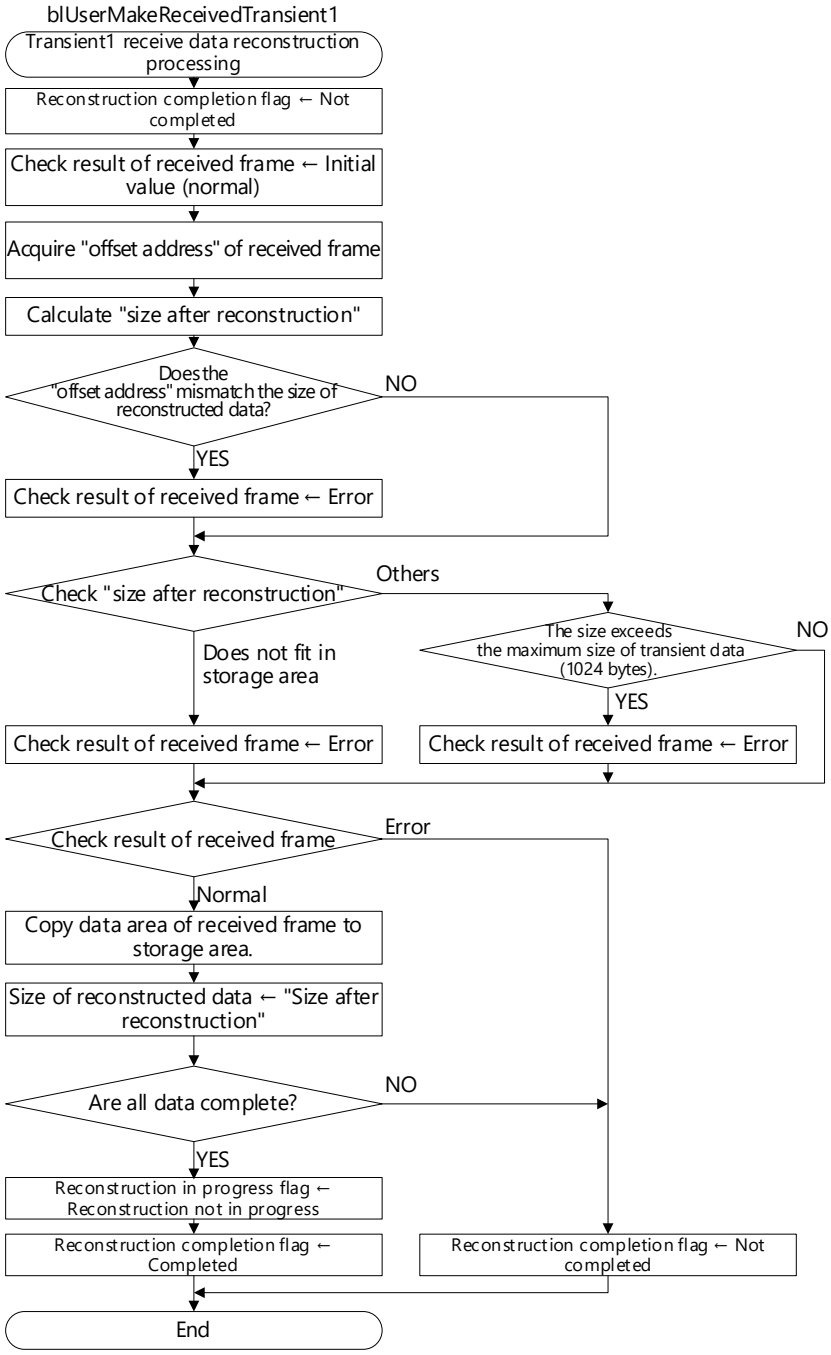


Figure 10.3.4-2 Flowchart for Transient1 Receive Data Reconstruction Processing (2/2)

10.3.5 SLMP memory read request frame receive processing

This function performs frame reception processing when SLMP memory read request frame is received in its own station from another station.

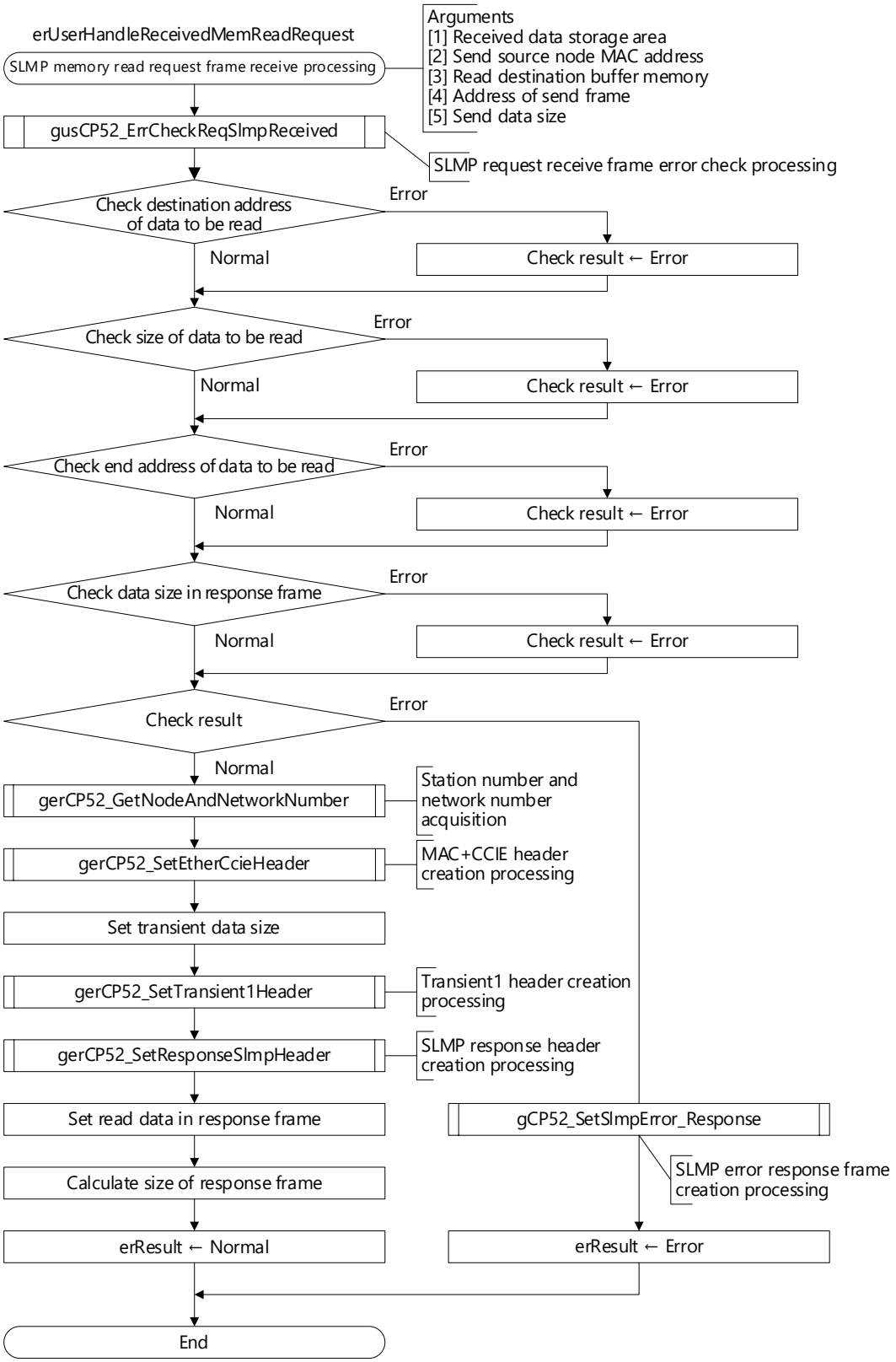


Figure 10.3.5-1 Flowchart for SLMP Memory Read Request Frame Receive Processing

10.3.6 SLMP memory write request frame receive processing

This function performs frame receive processing when SLMP memory write request frame is received in its own station from another station.

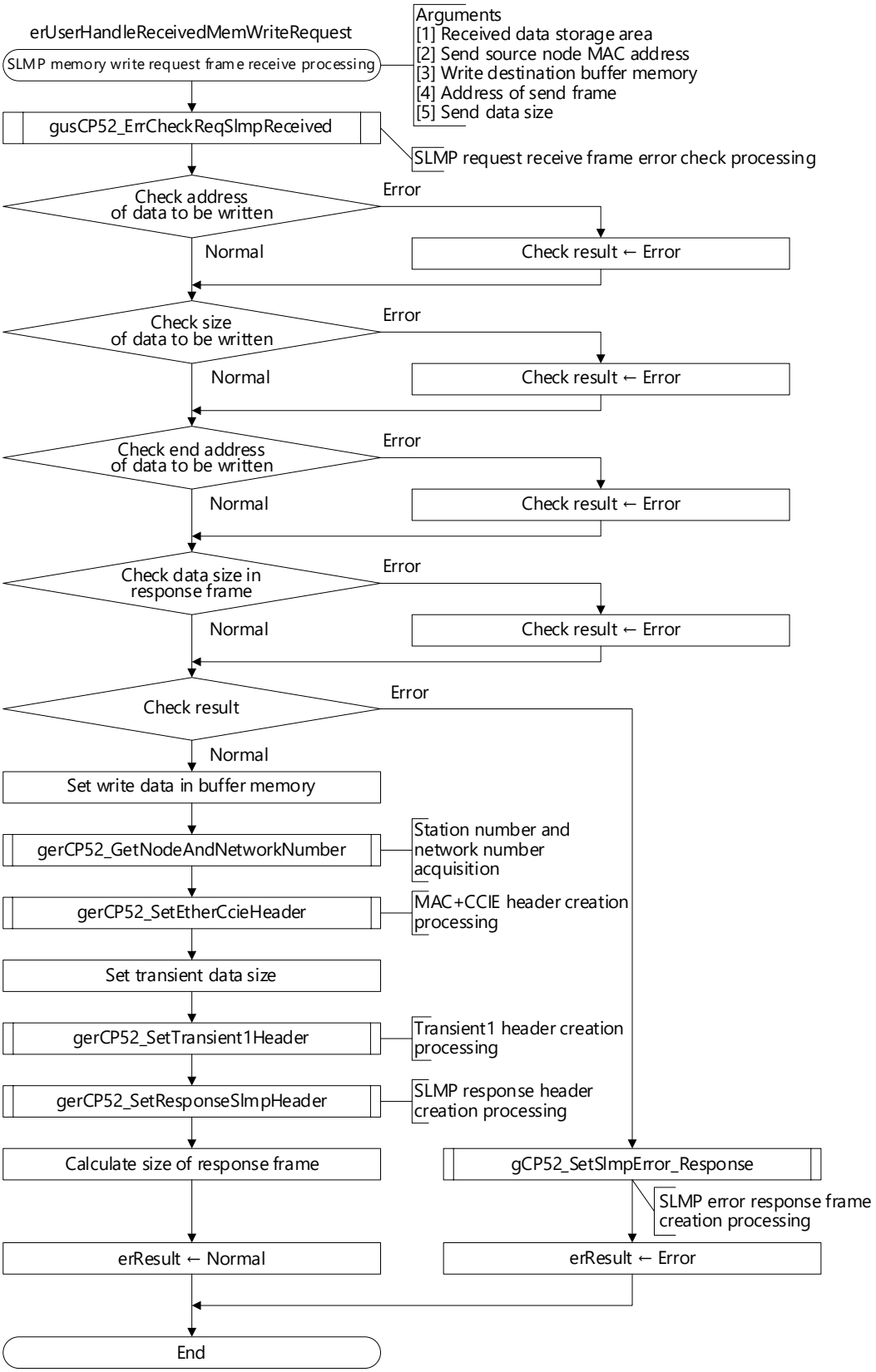
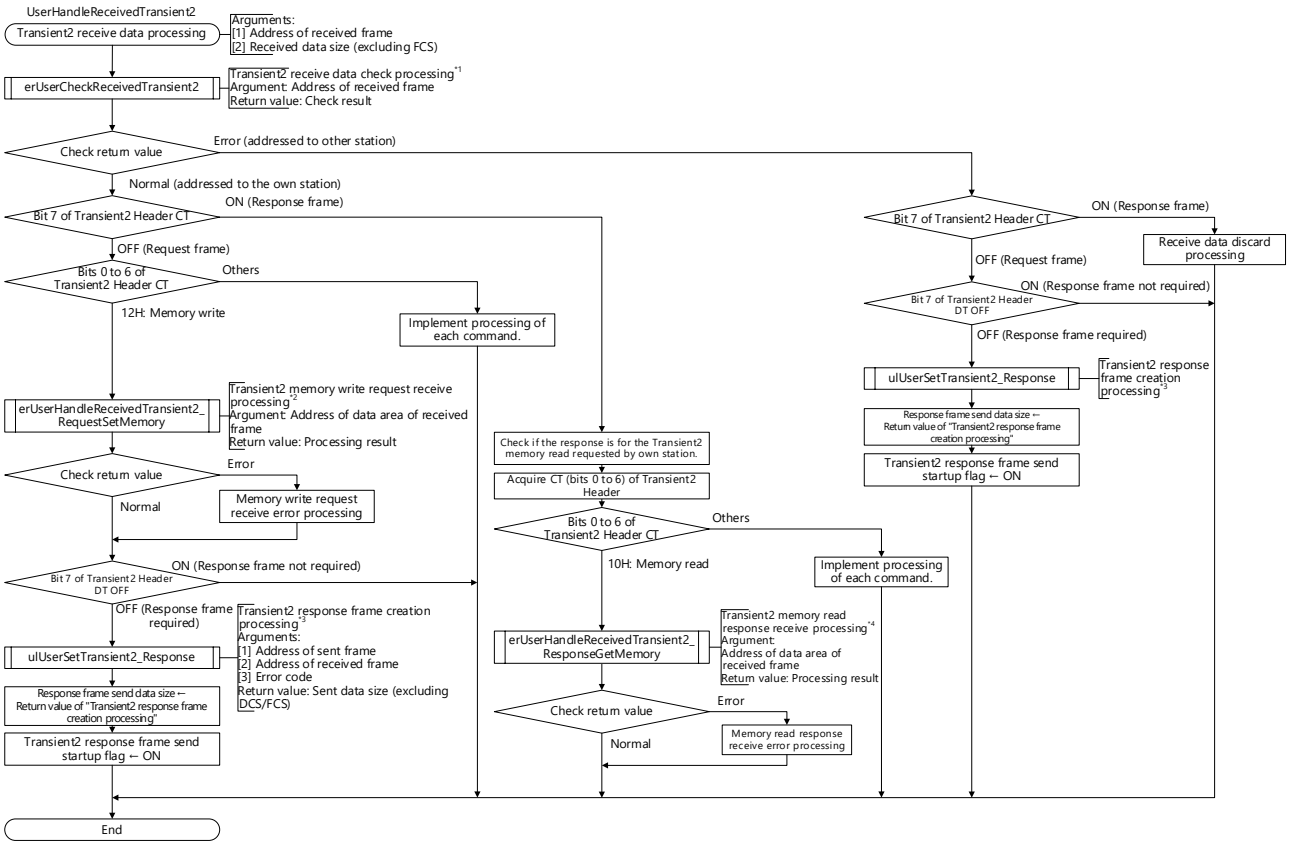


Figure 10.3.6-1 Flowchart for SLMP Memory Write Request Frame Receive Processing

10.3.7 Transient2 receive data processing

This function analyzes a received Transient2 frame and creates or receives a response frame in accordance with the analysis results.

For the intelligent device station



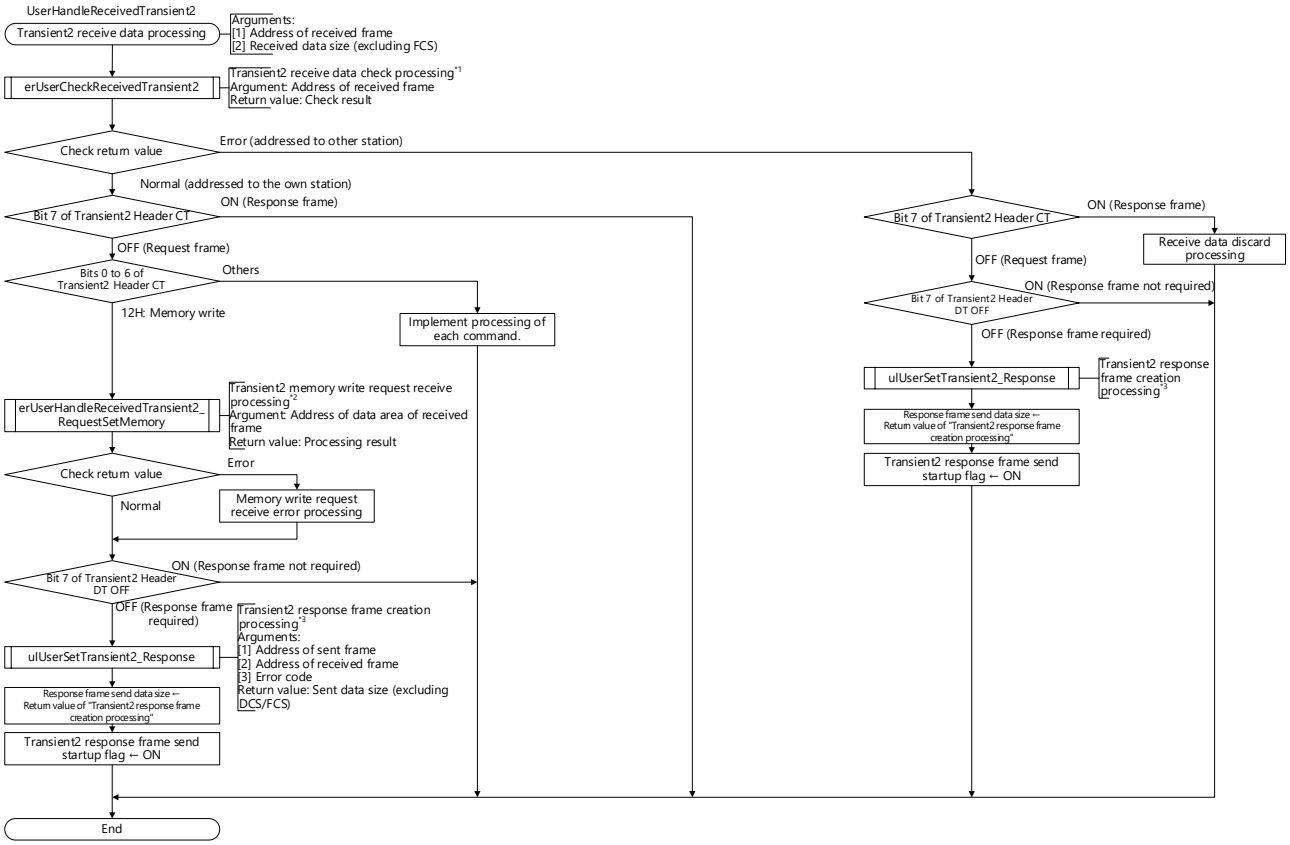
*1: For details, refer to Section 10.3.8 "Transient2 receive data check processing".

*2: For details, refer to Section 10.3.10 "Transient2 response frame creation processing".

*3: For details, refer to Section 10.3.20 "Transient2 memory read response receive processing".

Figure 10.3.7-1 Flowchart for Transient2 Receive Data Processing

For the remote device station



*1: For details, refer to Section 10.3.8 "Transient2 receive data check processing".

*2: For details, refer to Section 10.3.9 "Transient2 memory write request receive processing".

*3: For details, refer to Section 10.3.10 "Transient2 response frame creation processing".

Figure 10.3.7-2 Flowchart for Transient2 Receive Data Processing

10.3.8 Transient2 receive data check processing

This function checks if the received Transient2 frame is addressed to its own station, and checks the destination station number (DA/DS) and destination network number (DNA).

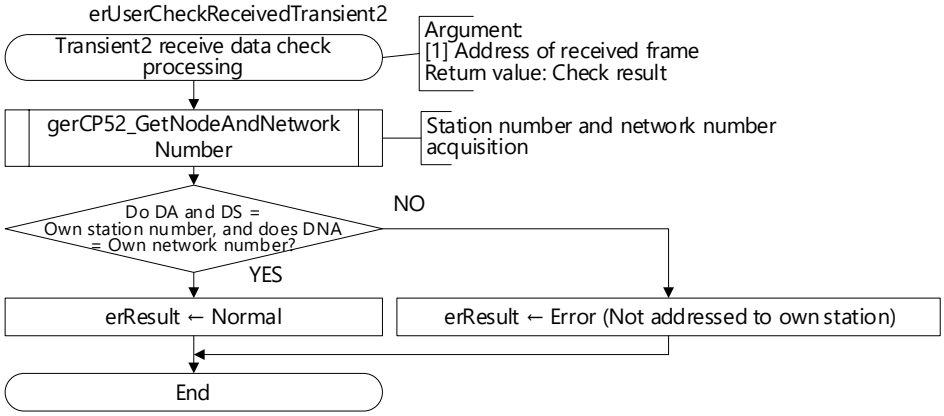


Figure 10.3.8-1 Flowchart for Transient2 Receive Data Check Processing

10.3.9 Transient2 memory write request receive processing

This function performs frame reception processing when a frame requesting to set Transient2 memory in its own station is received from another station.

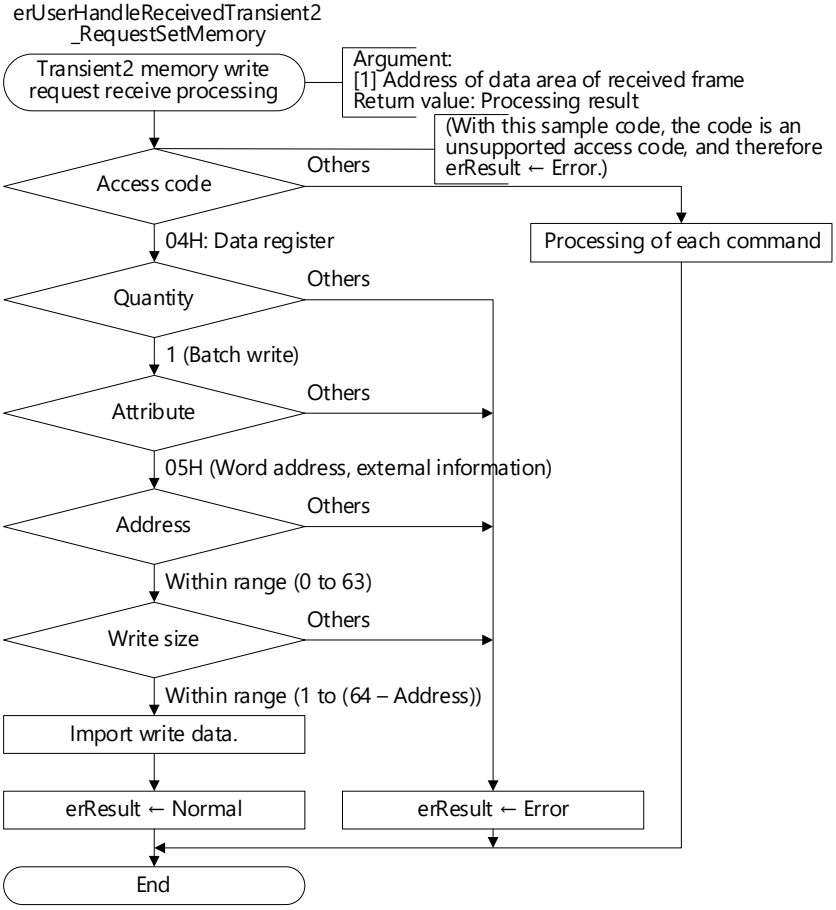


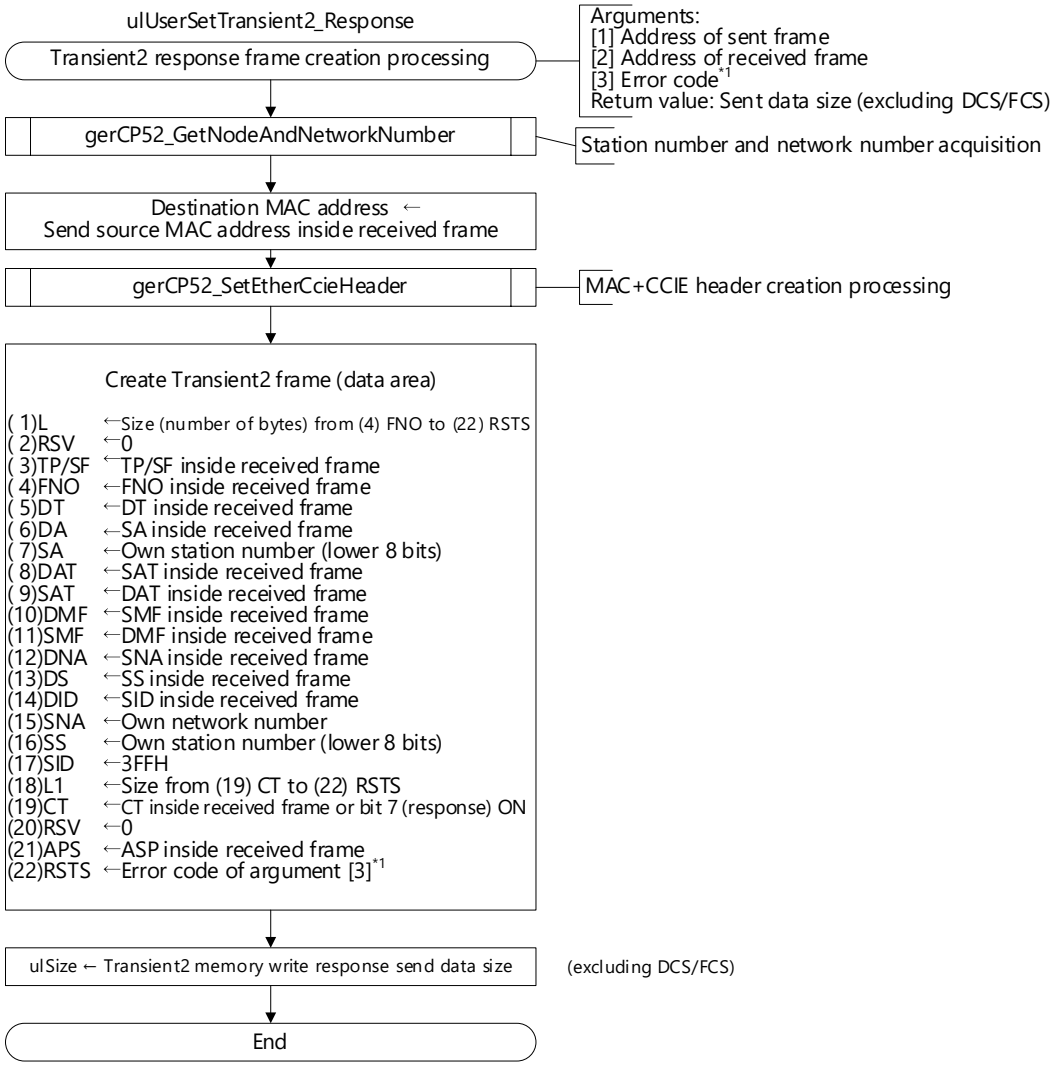
Figure 10.3.9-1 Flowchart for Transient2 Memory Write Request Receive Processing

The flow above illustrates the command processing for the settings below. Any other setup results in error.

(1) Memory write
(2) Access code: 04H (Data register)
(3) Attribute: 05H (Word access, external information)
(4) Address (start address of write destination): 0
(5) Write size: 1 to (64 – Address)

10.3.10 Transient2 response frame creation processing

This function creates a Transient2 response frame.



*1: For [3] Error Code details, refer to Details of return code (RSTS) in Appendix 1.3 "CC-Link compatible transient frame".

Figure 10.3.10-1 Flowchart for Transient2 Response Frame Creation Processing

10.3.11 TransientAck receive data processing

This function analyzes the received TransientAck frame and adds processing corresponding to the analytical results.

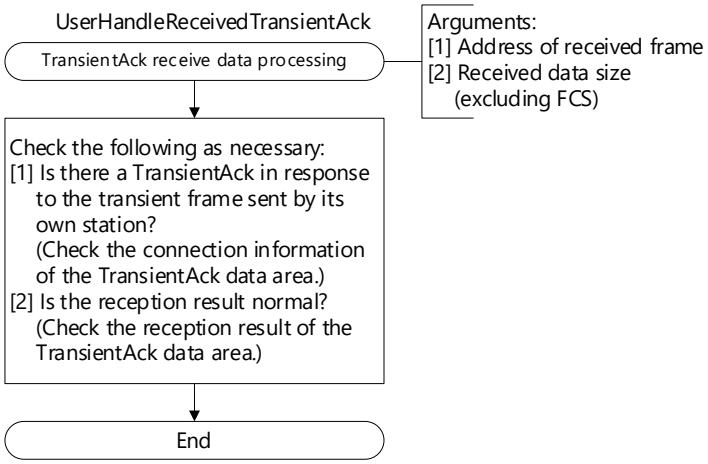


Figure 10.3.11-1 Flowchart for TransientAck Receive Data Processing

10.3.12 TransientAck frame creation processing

This function creates a TransientAck frame.

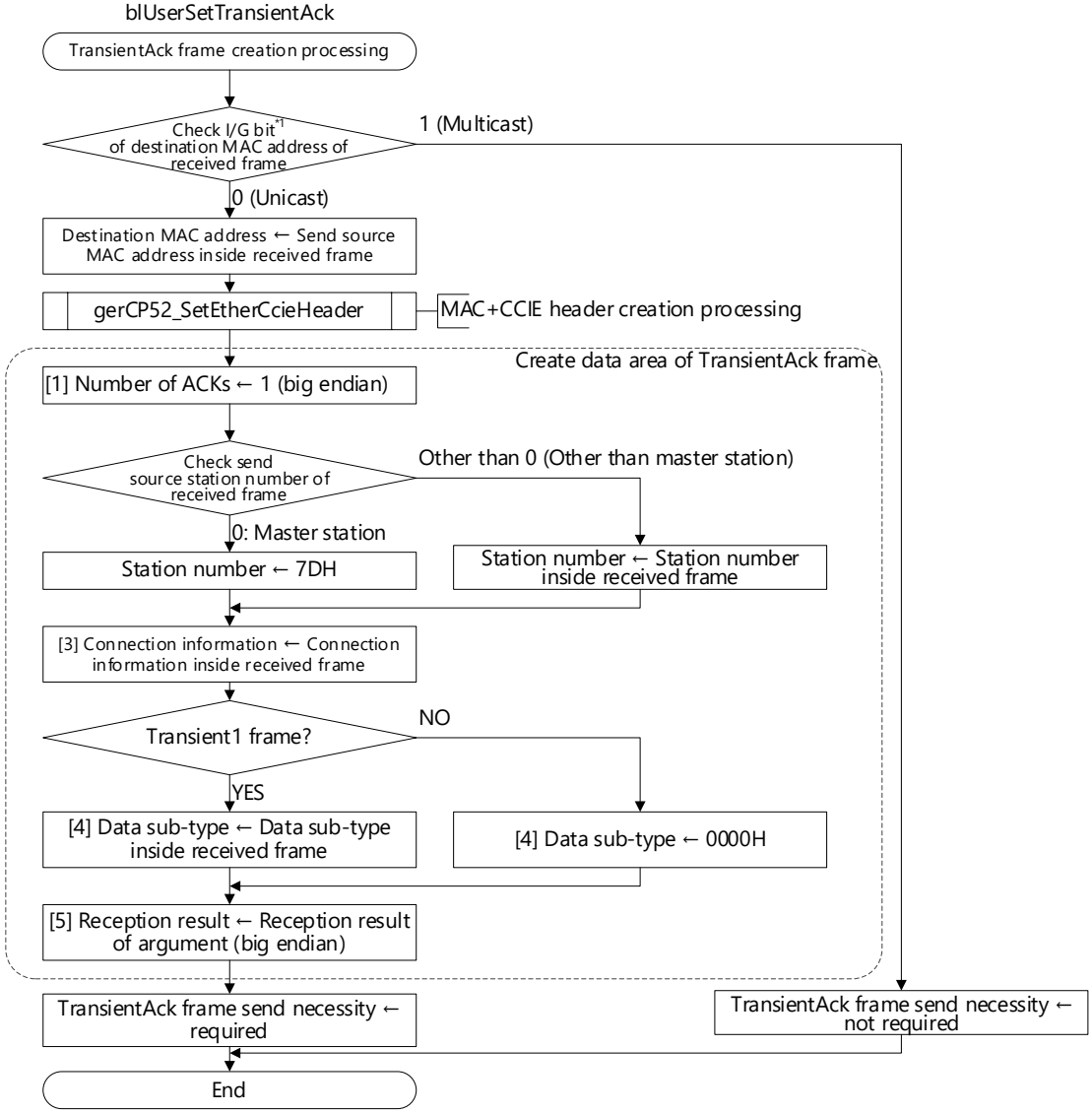
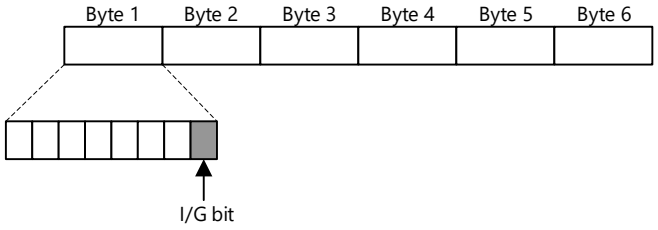


Figure 10.3.12-1 Flowchart for TransientAck Frame Creation Processing

*1: The I/G bit is the least significant bit of the first byte (octet) of the MAC address.



10.3.13 Transient1, Transient2, and TransientAck send processing

This function sends Transient1, Transient2, and TransientAck frames.

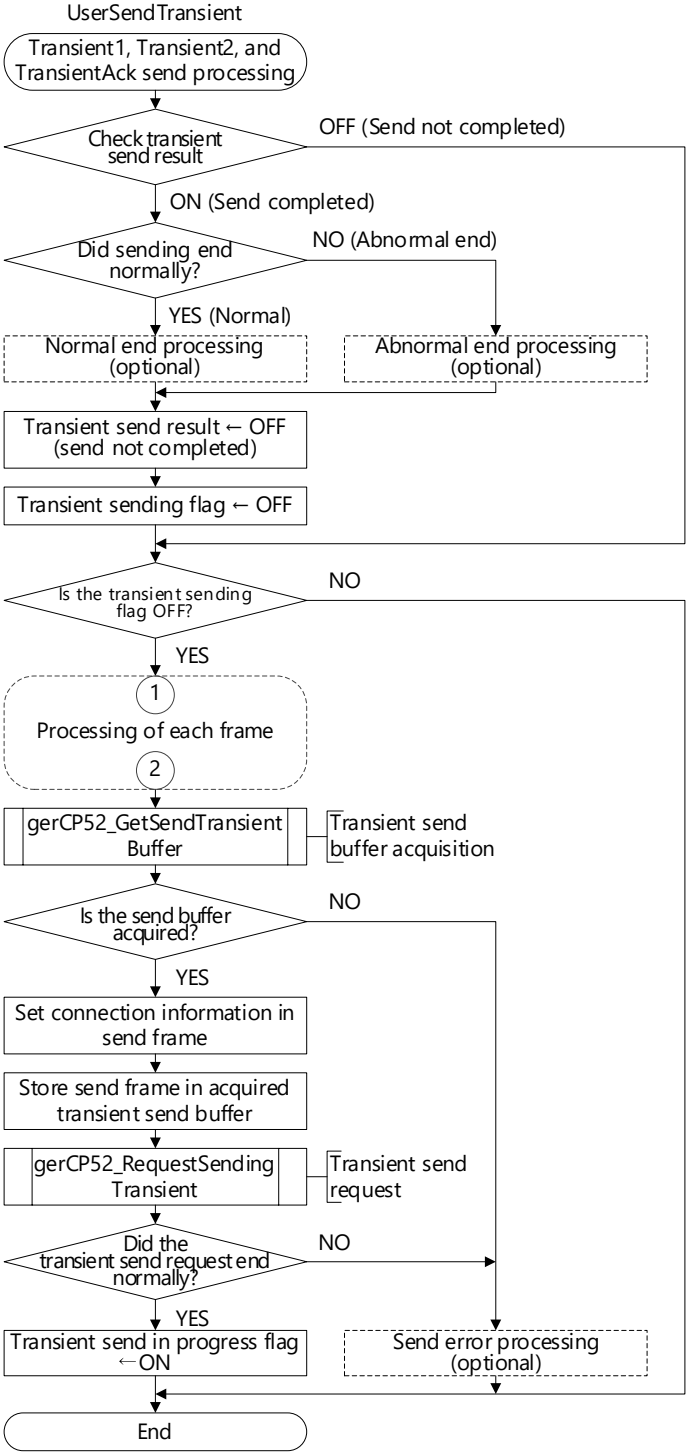


Figure 10.3.13-1 Flowchart for Transient1, Transient2, and TransientAck Send Processing (1/3)

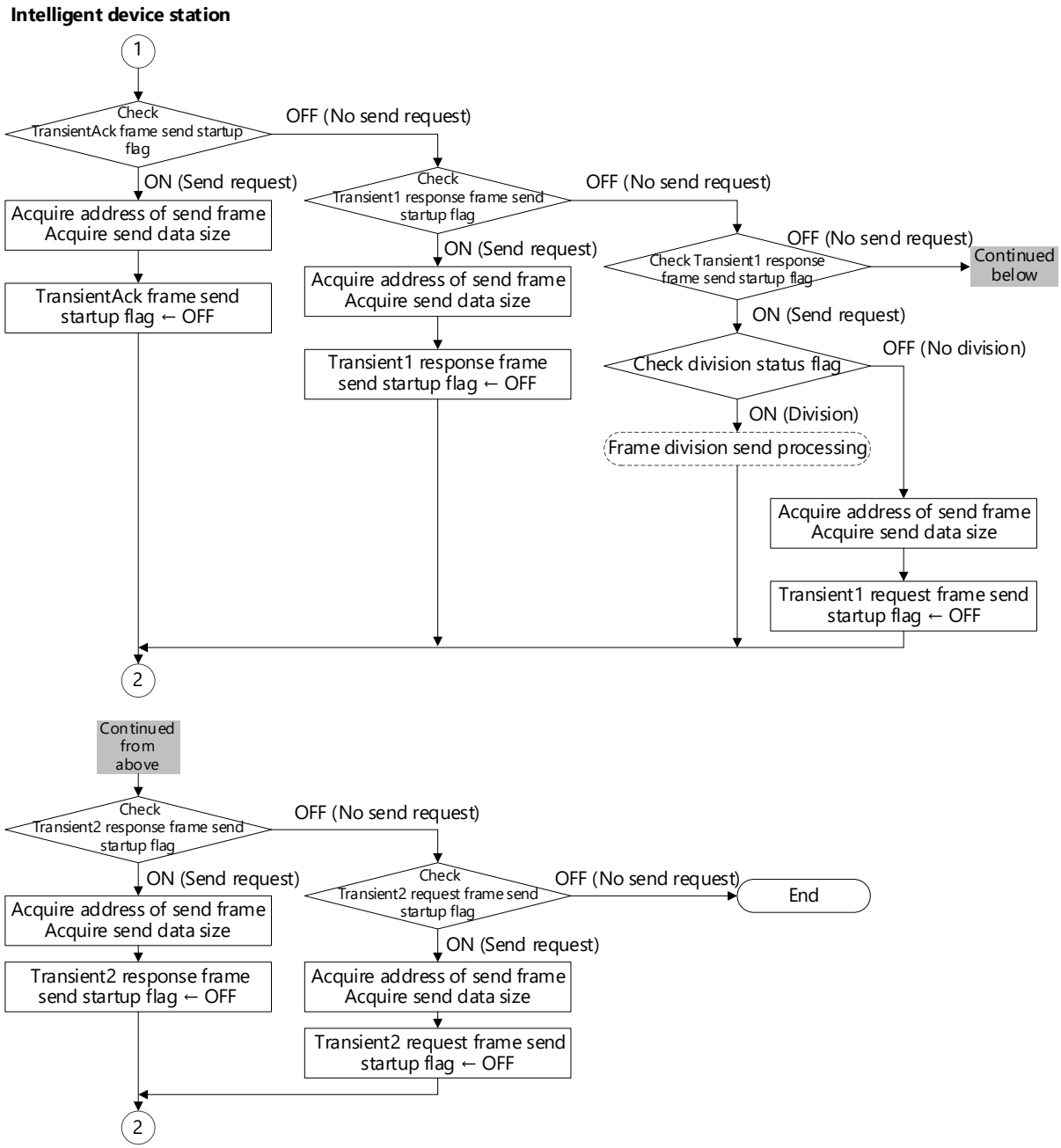


Figure 10.3.13-2 Flowchart for Transient1, Transient2, and TransientAck Send Processing (2/3)

Remote device station

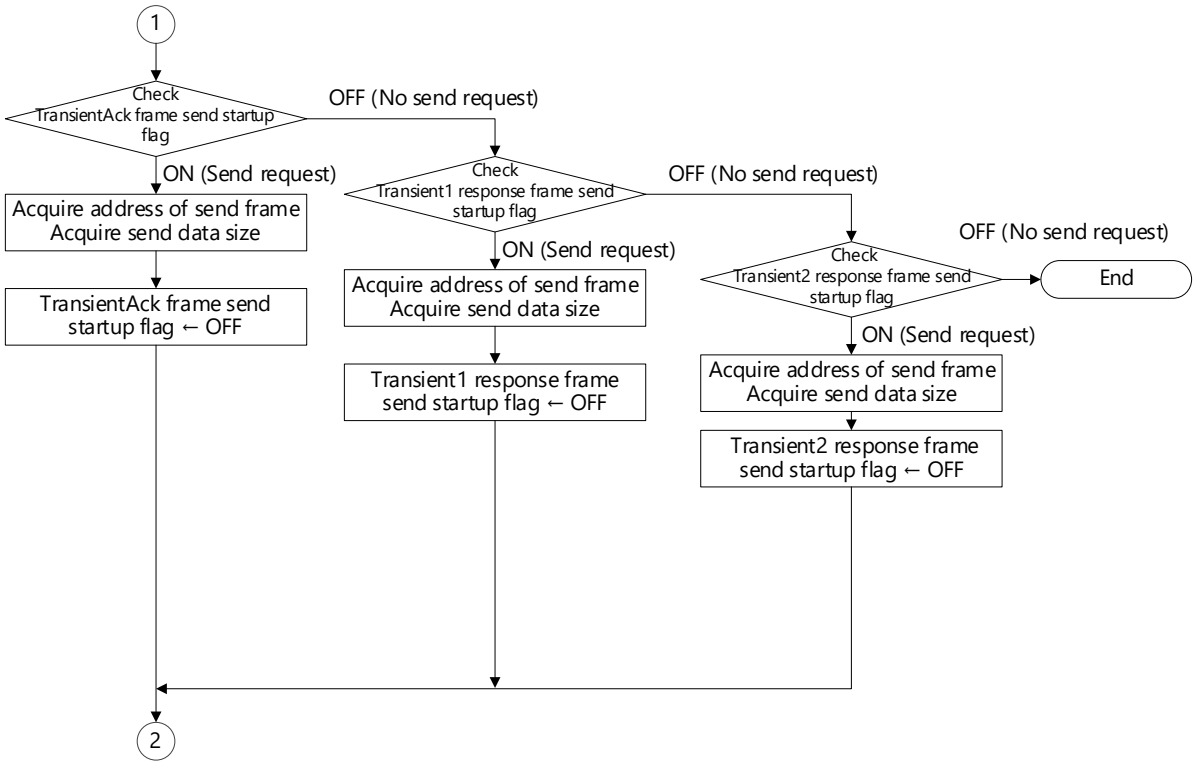
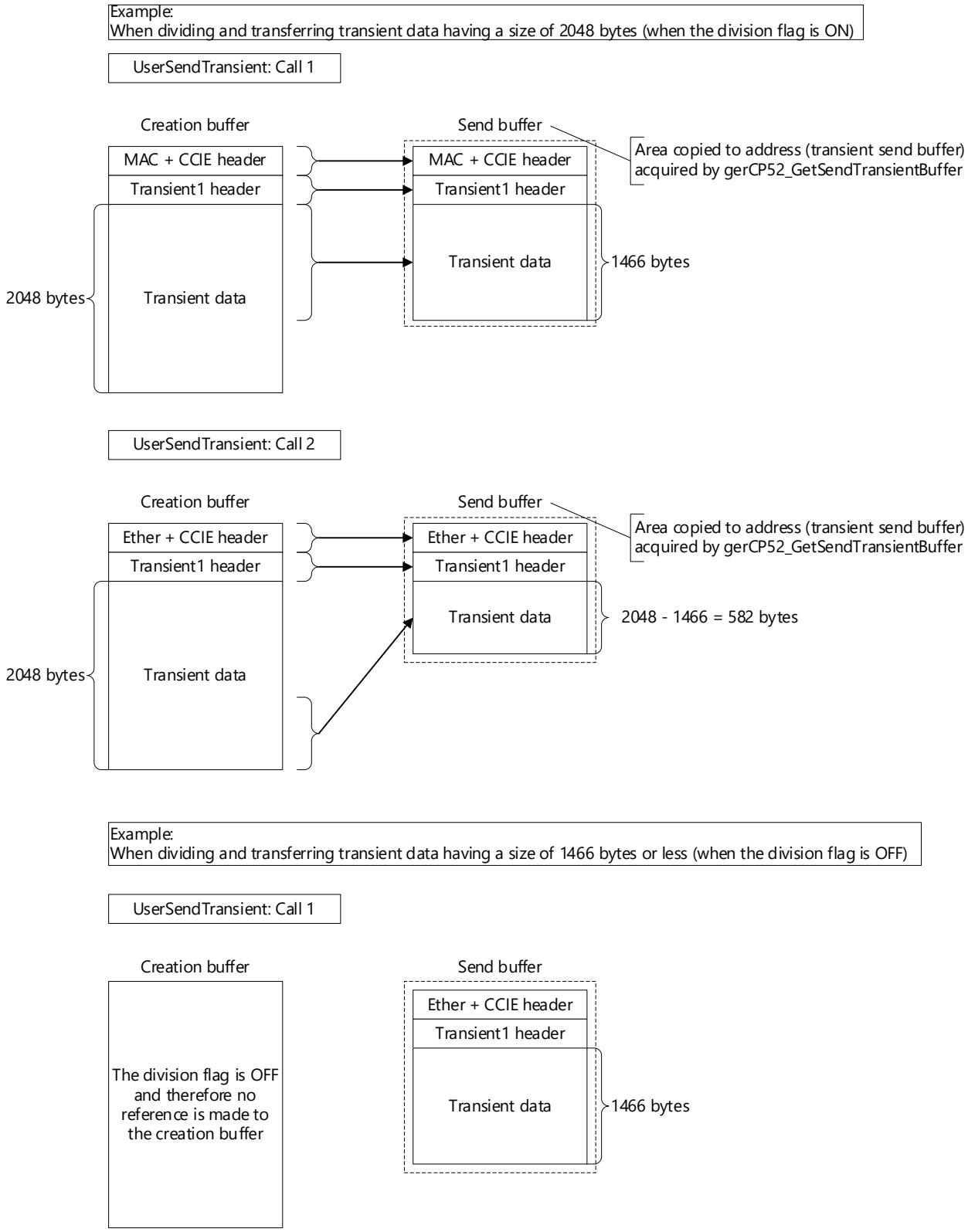


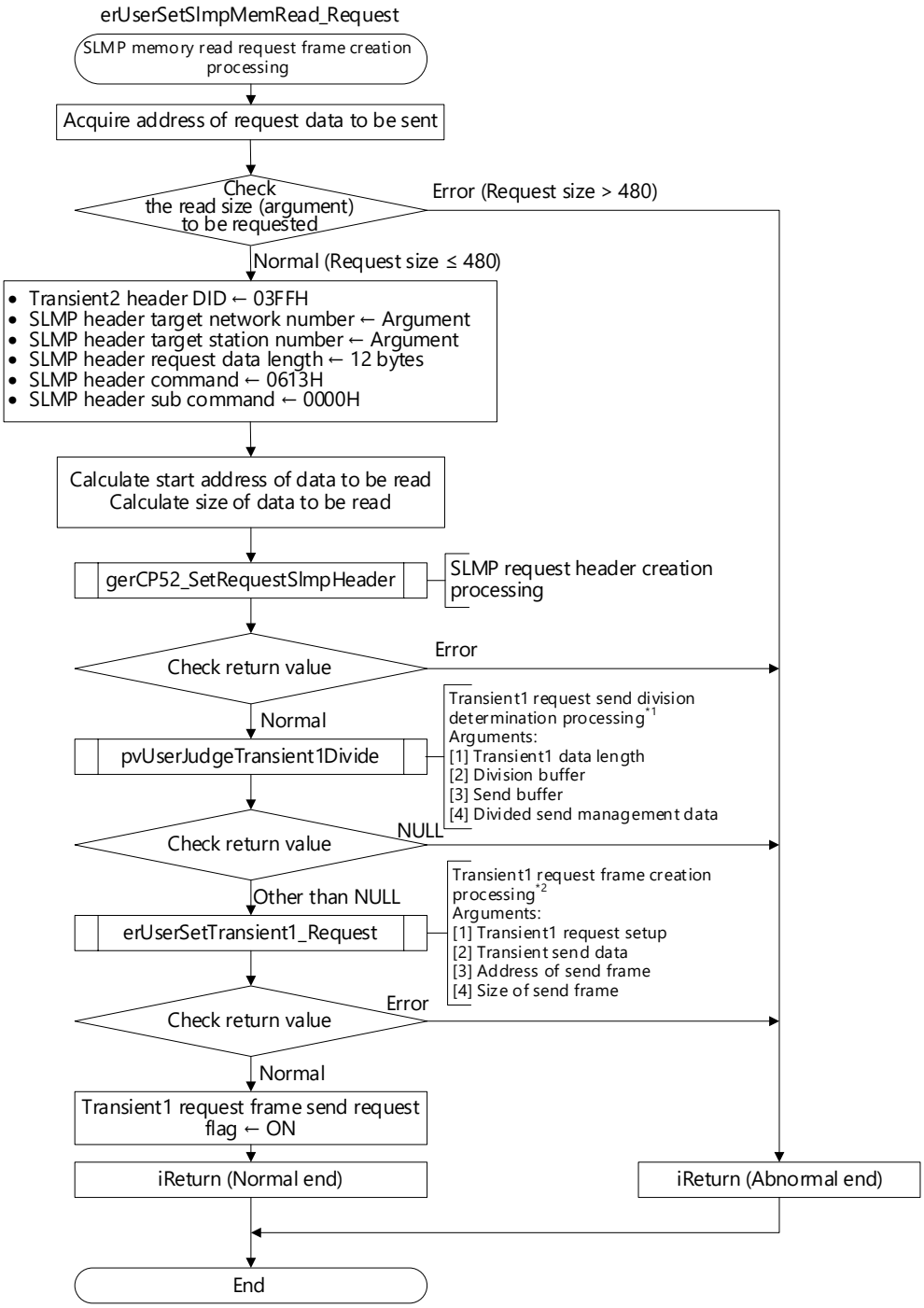
Figure 10.3.13-3 Flowchart for Transient1, Transient2, and TransientAck Send Processing (3/3)

[Sending data by dividing data into blocks]
When the transient data requested to be sent is 1466 to 2048 bytes, the transient data can be divided and sent.
Implement this processing in accordance with specifications of the CP520 application product.
The following shows an image of the process for divided sending.
For details regarding the Transient1 frame, refer to Appendix 1.2 "Transient1 frame".



10.3.14 SLMP memory read request frame creation processing

This function creates SLMP memory read request frame to be sent to another station. This processing is an example of the processing for creating SLMP request frame.
For other commands, add processing as required.
Implement this processing only when its own station is an intelligent device station.



*1: For details, refer to Section 10.3.15 "Transient1 request send division determination processing".
*2: For details, refer to Section 10.3.16 "Transient1 request frame creation processing".

Figure 10.3.14-1 Flowchart for SLMP Memory Read Request Frame Creation Processing

10.3.15 Transient1 request send division determination processing

This function determines if a frame should be divided prior to sending when creating a Transient1 request frame.

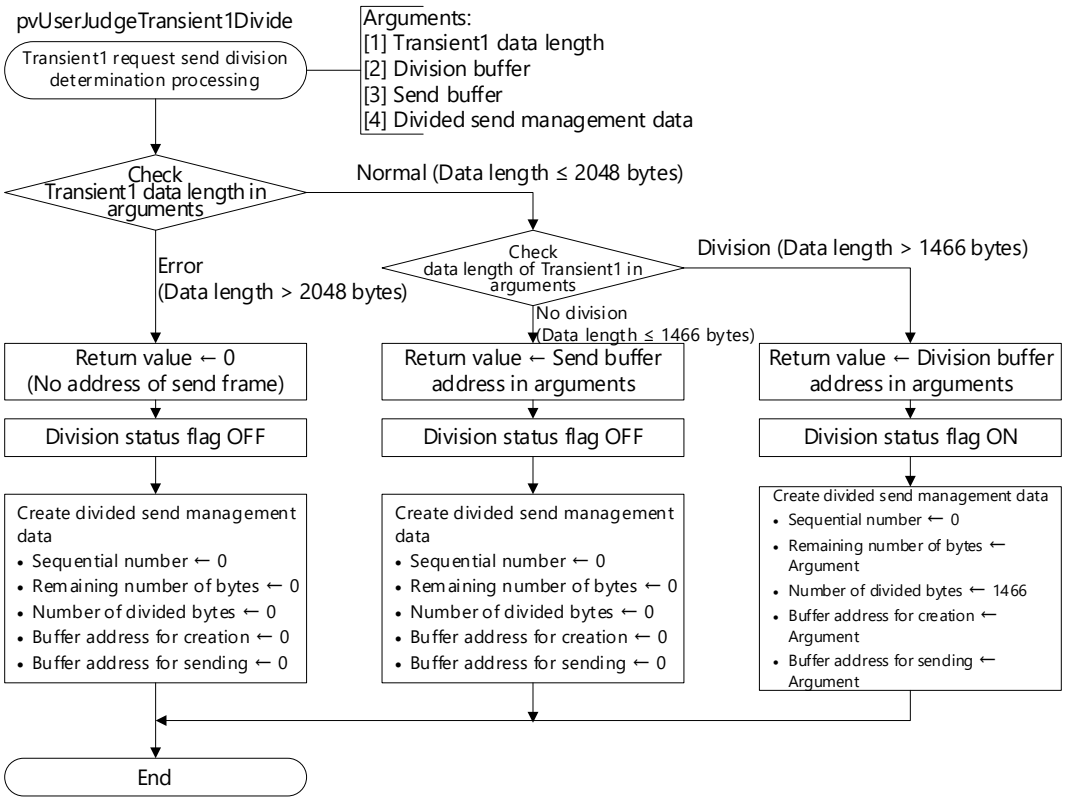


Figure 10.3.15-1 Flowchart for Transient1 Request Send Division Determination Processing

10.3.16 Transient1 request frame creation processing

This function creates a request frame (from the MAC header to the Transient1 header) when an SLMP memory read request is sent from its own station to another station.
Implement this processing only when its own station is an intelligent device station.

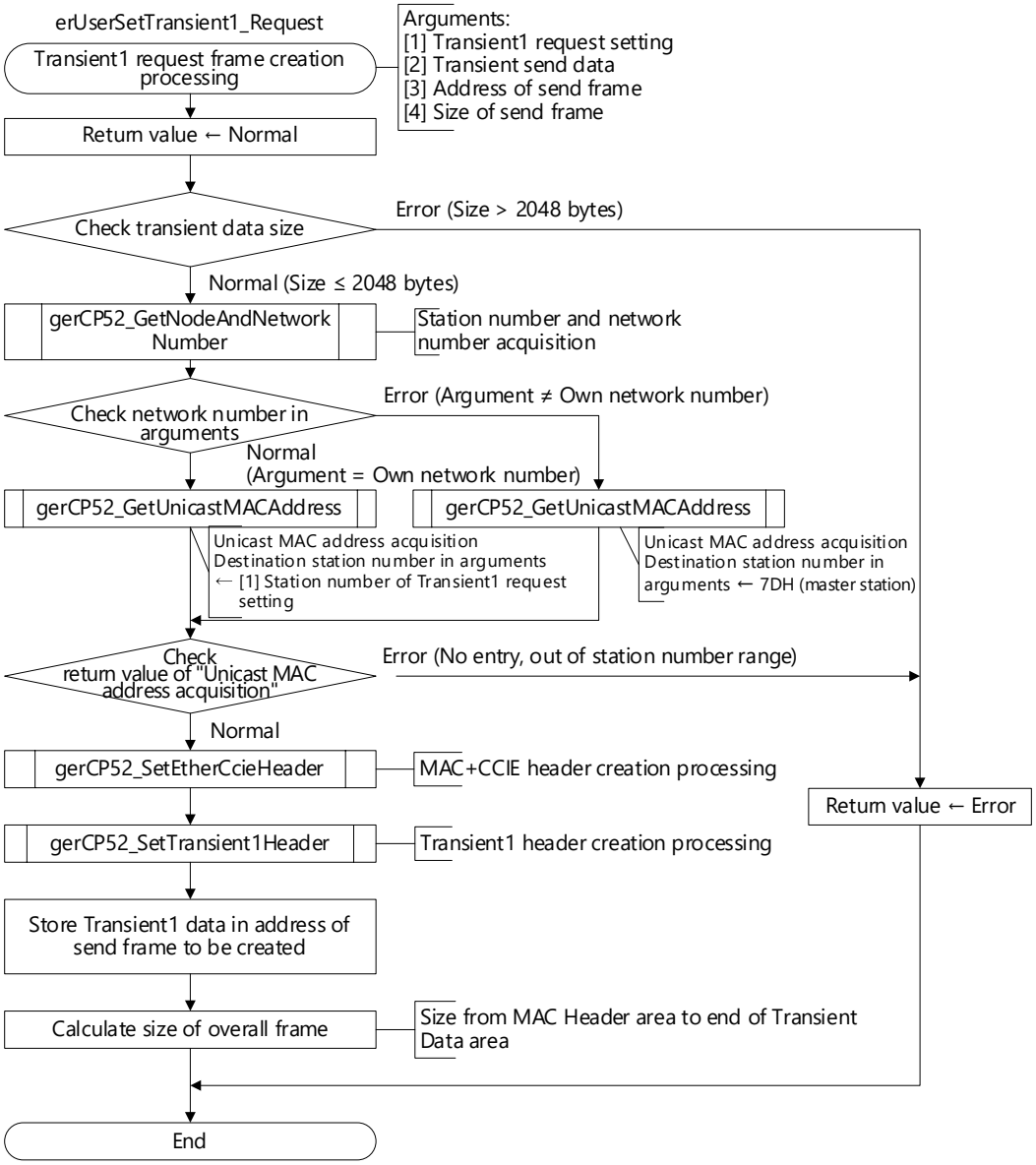


Figure 10.3.16-1 Flowchart for Transient1 Request Frame Creation Processing

10.3.17 SLMP memory read response receive processing

This function receives response frames for SLMP memory read requested by its own station to other stations.
Implement this processing only when its own station is an intelligent device station.

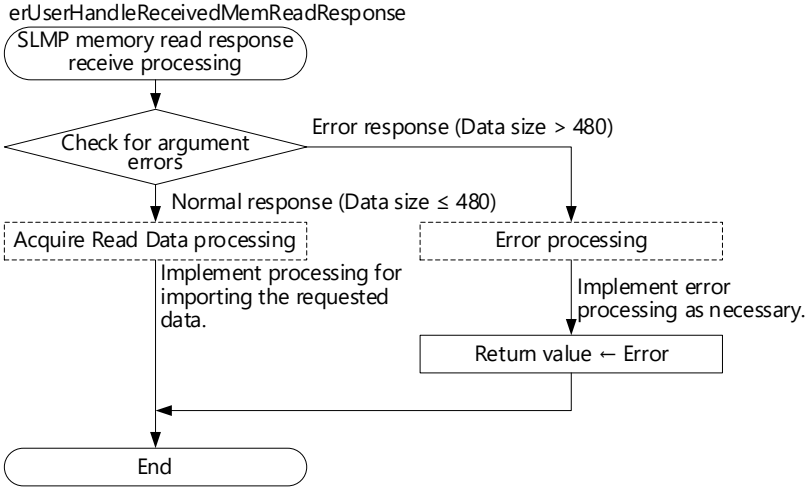


Figure 10.3.17-1 Flowchart for SLMP Memory Read Response Receive Processing

10.3.18 Transient2 request frame creation processing

This function creates Transient2 request frame to be sent to another station. This processing is an example of the processing for creating Transient2 request frame. For other commands, add processing as required.
Implement this processing only when its own station is an intelligent device station.

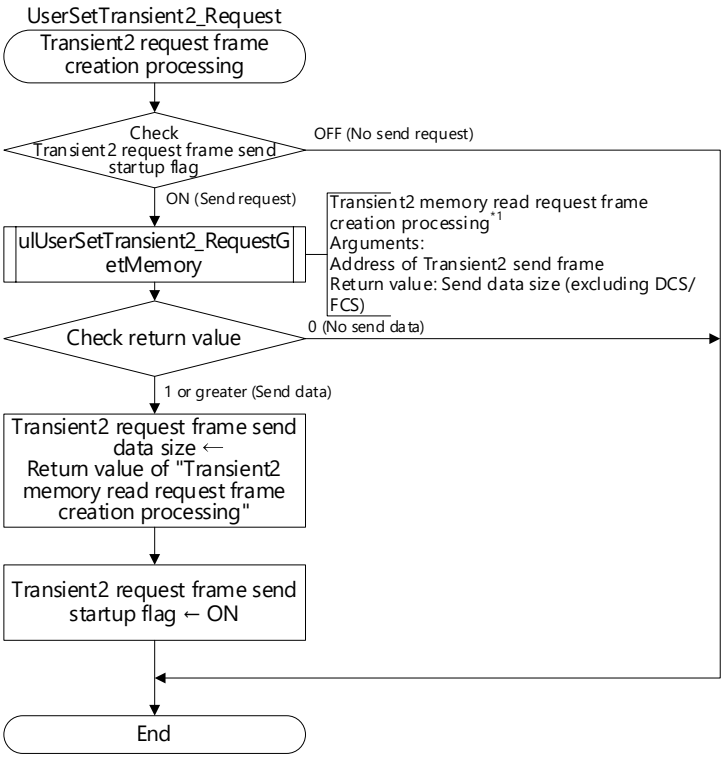


Figure 10.3.18-1 Flowchart for Transient2 Request Frame Creation Processing

*1: For details, refer to Section 10.3.19 "Transient2 memory read request frame creation processing".

10.3.19 Transient2 memory read request frame creation processing

This function creates a request frame when a Transient2 memory read request is to be sent from its own station to another station.

Implement this processing only when its own station is an intelligent device station.

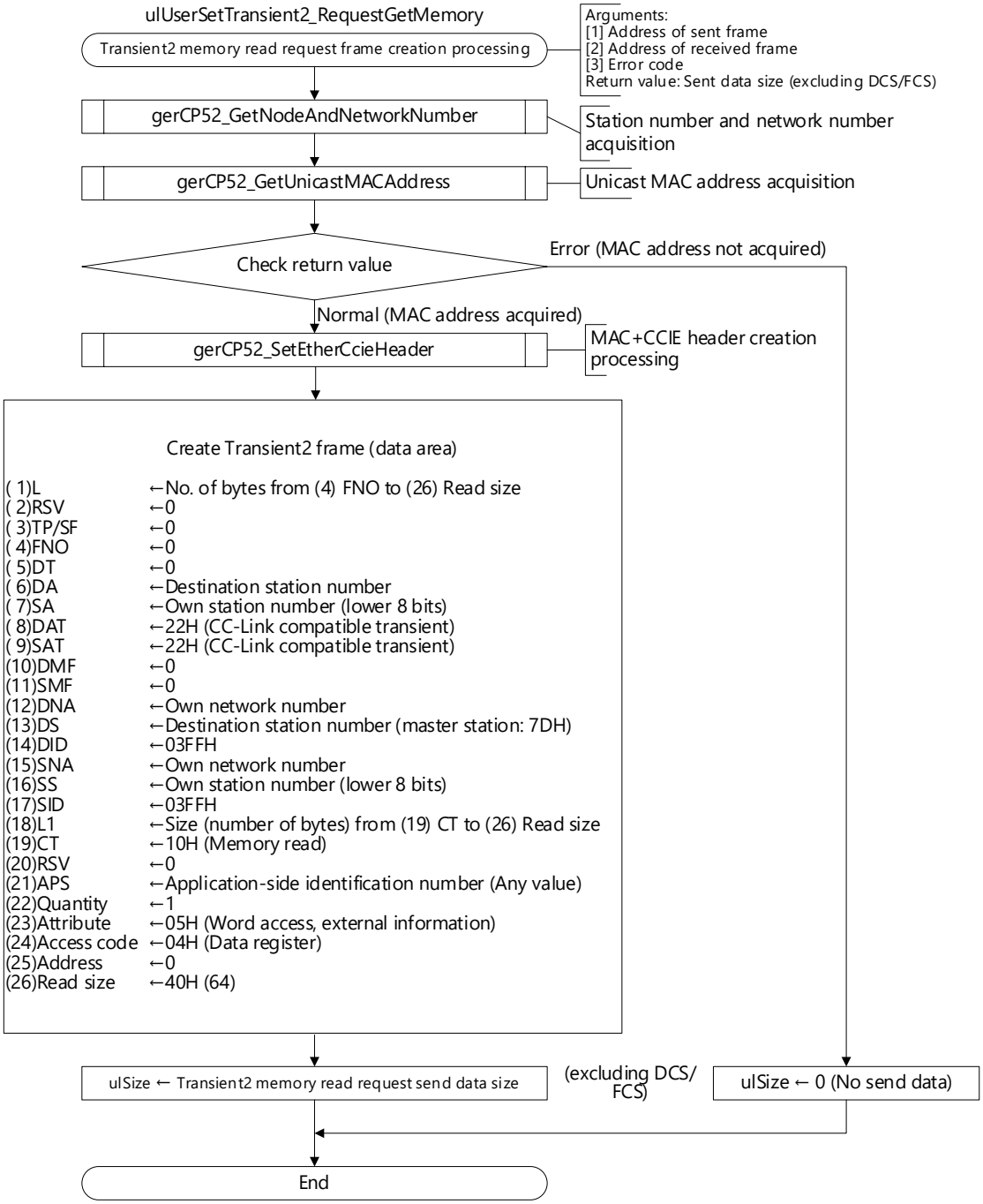


Figure 10.3.19-1 Flowchart for Transient2 Memory Read Request Frame Creation Processing

The flow above illustrates the command processing for the settings below. Any other setup results in error.

(1) Destination station number: 7DH (Master station)
(2) Access code: 04H (Data register)
(3) Attribute: 05H (Word access, external information)
(4) Address (start address of read destination): 0
(5) Read size: 40H (64)

10.3.20 Transient2 memory read response receive processing

This function receives response frames for Transient2 memory read requested by its own station to another station. Implement this processing only when its own station is an intelligent device station.

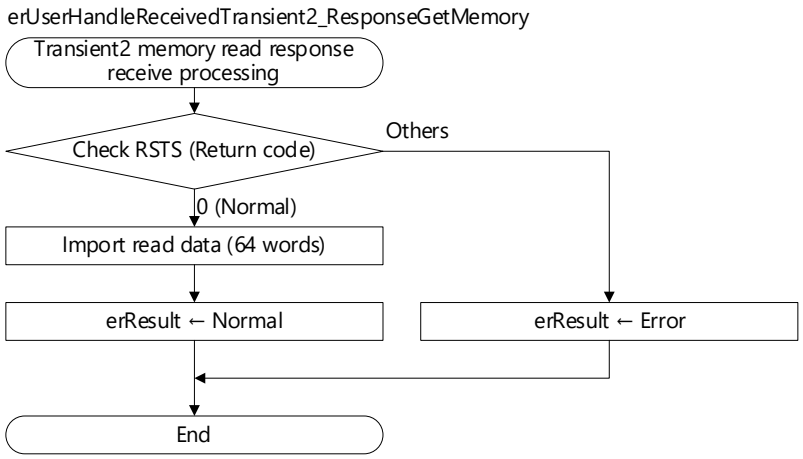


Figure 10.3.20-1 Flowchart for Transient2 Memory Read Response Receive Processing

The flow above illustrates the command processing for the settings below. Any other setup results in error.

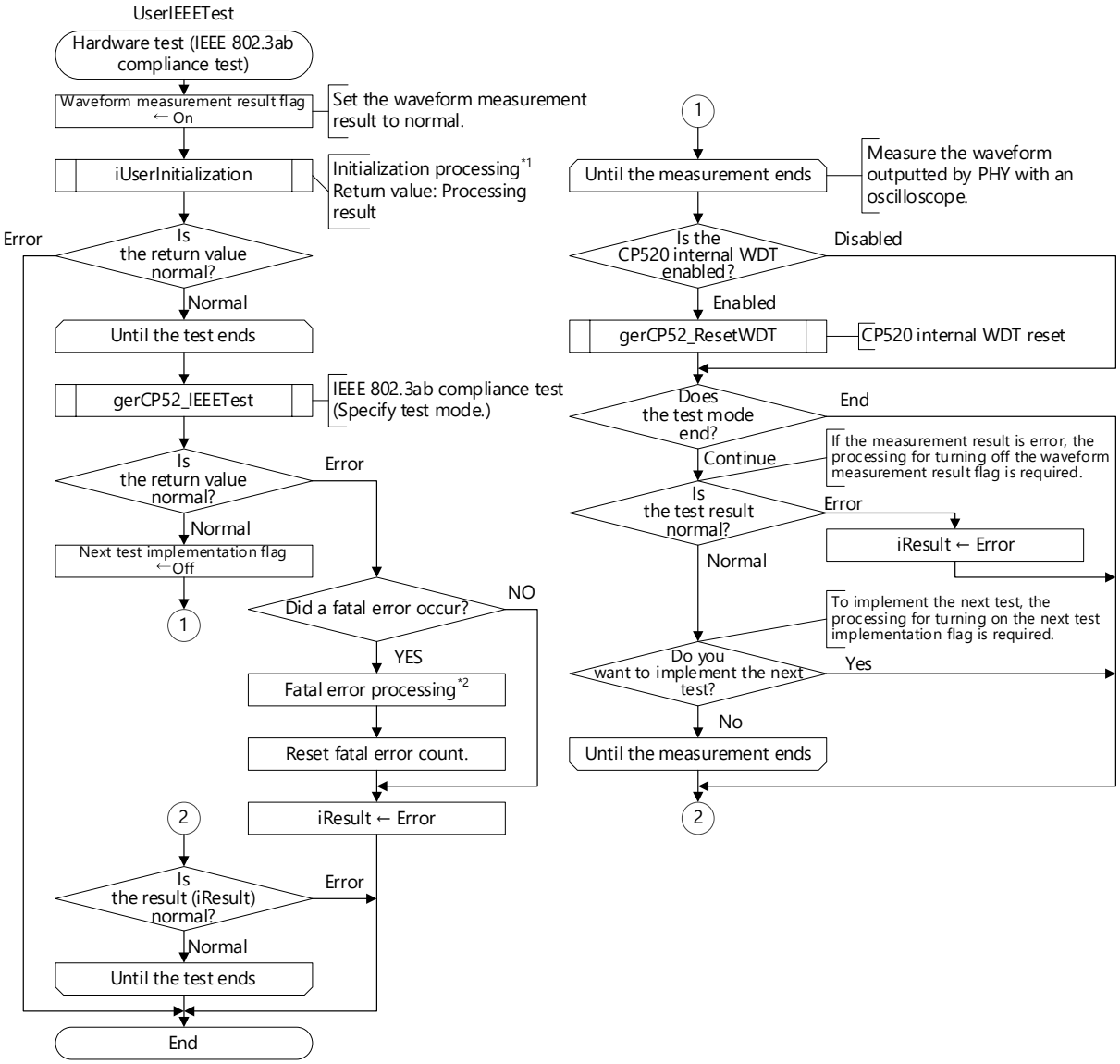
(1) Destination station number: 7DH (Master station)
(2) Access code: 04H (Data register)
(3) Attribute: 05H (Word access, external information)
(4) Address (start address of read destination): 0
(5) Read size: 40H (64)

10.4 User Program Details (Hardware Test Related)

Implement the hardware test as independent processing, not as main processing (iUserMainRoutine).
(Implementation examples: From outside (station number / network number switch or engineering tool), implement a function that switches to "Hardware Test Mode (Offline Mode)" other than the normal operation mode (online mode).)

10.4.1 Hardware test (IEEE 802.3ab compliance test)

The hardware test needs to be implemented to implement the "1000BASE-T compliance test" of the conformance test.



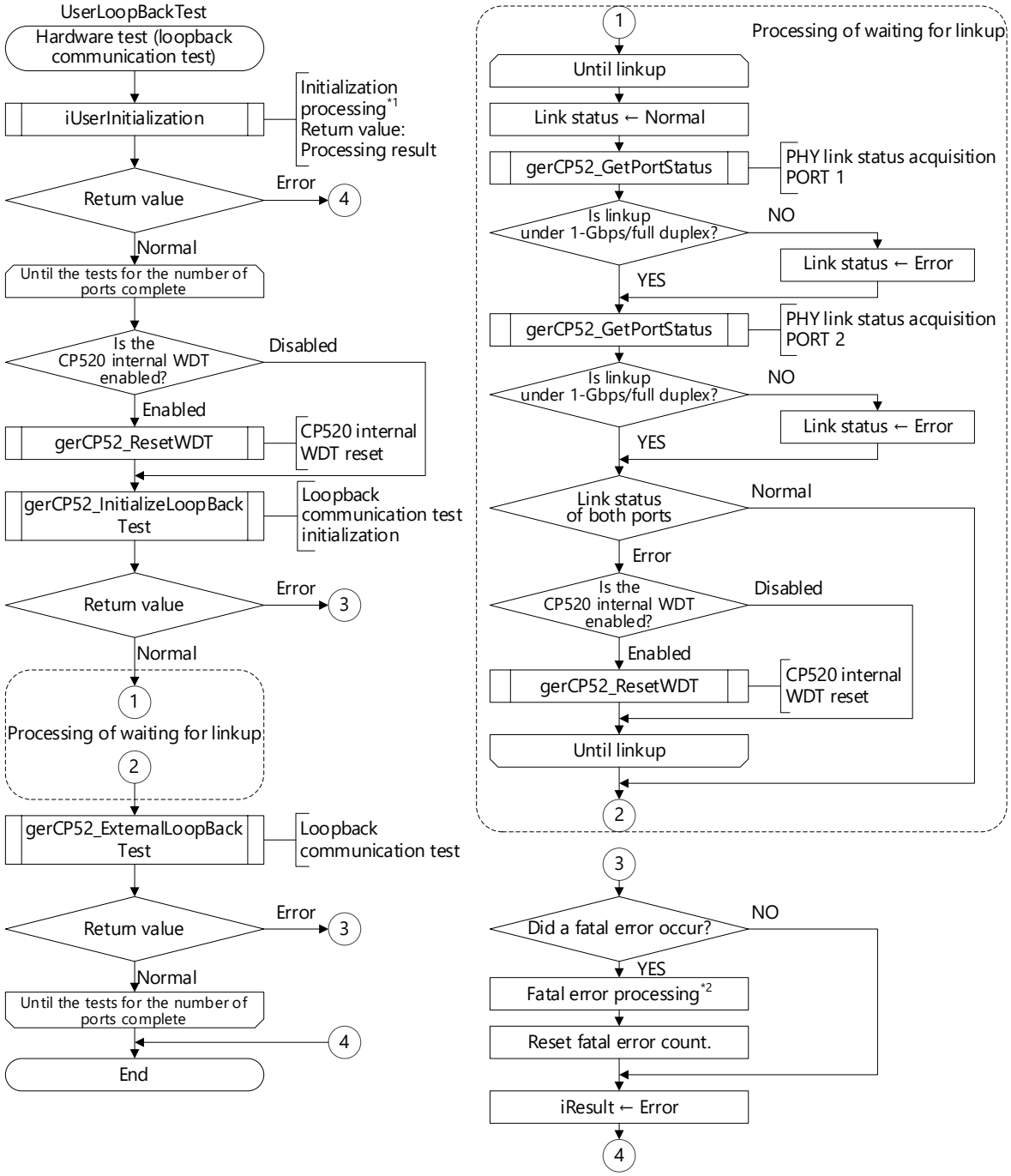
*1: For details, refer to Section 10.2.2 "Initialization processing".

*2: When a fatal error occurs in CP520, the gerCP52_IEEETest function calls the function below created by the user. Be sure to acquire the CP520 fatal error.

- gCP52_CallbackFatalError

Figure 10.4.1-1 Flowchart for Hardware Test (IEEE 802.3ab Compliance Test)

The Hardware test (loopback communication test) checks if there is a hardware error in CP520.
Implement this test with Ethernet ports 1 and 2 connected by an Ethernet cable.



*1: For details, refer to Section 10.2.2 "Initialization processing".
*2: When a fatal error occurs in CP520, the gerCP52_IEEETest function calls the function below created by the user. Be sure to acquire the CP520 fatal error.
• gCP52_CallbackFatalError

Figure 10.4.2-1 Flowchart for Hardware Test (Loopback Communication Test)

11 CP520 DRIVER RELATED SPECIFATIONS

This chapter describes the specifications of the CP520 driver interface functions and CP520 driver callback functions that make up the CP520 driver.

11.1 Overview of Each Function

(1) Overview

The following table provides an overview of each function and indicates whether or not function changes are required.

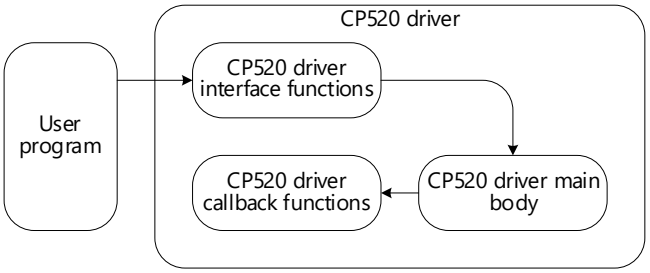


Figure 11.1-1 Relationship Between Functions

Table 11.1-1 Overview of Each Function

Program Part Name	Overview	Need for Change
CP520 driver interface function	A function called when a function of the CP520 driver is used from the user program (File: CP52_Interface.c)	×
CP520 driver callback function	A function used when the user program requests callback from the CP520 driver. This function describes the processing on the user program side for events that occur in the CP520 driver. (File: CP520_Callback.c)	○
CP520 driver main body	The main body of the driver area that is called by CP520 driver interface functions and controls CP520 (Files: Files below the driver folder excluding CP52_Interface.c.)	×

(2) Description specifications

The following table lists the description specifications of each function.

Table 11.1-2 Source Code Description Specifications

Item	Description	Remarks
C language standard	ANSI C compliant	Extended specifications of the compiler maker are partially used.
Tab length	4	-
Return code	CR+LF	-

(3) Type definition and error code

The following tables list the types and error codes defined in the CP520 driver.

Table 11.1-3 CP520 Driver Type List

No.	Defined Type	Implementation
1	VOID	void
2	CHAR	char
3	UCHAR	unsigned char
4	SHORT	short
5	USHORT	unsigned short
6	INT	int
7	UINT	unsigned int
8	LONG	long
9	ULONG	unsigned long
10	ERRCODE	int
11	BOOL	int

Table 11.1-4 CP520 Driver Error Code List

No.	Symbol	Value	Description
1	CP52_OK	0	Normal
2	CP52_ERR	-1	Abnormal end (status error / mismatch)
3	CP52_ERR_OTHER	-2	(Error occurred in driver inside library)
4	CP52_ERR_OUTOFRANGE	-3	Out of range
5	CP52_ERR_EMPTY	-4	Empty
6	CP52_ERR_OVERFLOW	-5	Overflow
7	CP52_ERR_NOENTRY	-6	No entry
8	CP52_ERR_NOPERMIT	-7	Not permitted
9	CP52_ERR_NODATA	-8	No data
10	CP52_ERR_NOMYSTATUS	-9	No valid MyStatus

11.2 CP520 Driver Interface Function List

The following lists the interface functions of the CP520 driver.

Table 11.2-1 CP520 Driver Interface Function List

Function Category (Reference Section)	Function Name	Function Type	Overview
Initial setup (Section 11.3.1 "Initial setup")	gulCP52_GetResetStatus	ULONG	Reset status acquisition
	gerCP52_Initialize	ERRCODE	CP520 initialization
	gerCP52_SetNodeAndNetworkNumber	ERRCODE	Station number and network number setting
	gerCP52_Start	ERRCODE	CP520 communication start
WDT (Section 11.3.2 "Watchdog timer")	gerCP52_ResetWDT	ERRCODE	CP520 internal WDT reset
	gerCP52_DisableWDT	ERRCODE	CP520 internal WDT disablement
	gerCP52_EnableWDT	ERRCODE	CP520 internal WDT enablement
	gerCP52_SetWDT	ERRCODE	CP520 internal WDT time limit setting
Event (Section 11.3.3 "Event")	gerCP52_GetEvent	ERRCODE	CP520 event detection
	gerCP52_Main	ERRCODE	CP520 event detection main processing
	gerCP52_RestartEvent	ERRCODE	CP520 event restart
	gerCP52_UpdateMIB	ERRCODE	MIB information update
	gerCP52_MyStaRcvTkn	ERRCODE	Receive processing of token frame addressed to the own station
Cyclic transmission (Section 11.3.4 "Cyclic transmission")	gerCP52_SetCyclicStop	ERRCODE	Cyclic transmission stop for user application-side reasons
	gerCP52_ClearCyclicStop	ERRCODE	Cyclic transmission stop clear for user application-side reasons
	gerCP52_GetReceivedCyclicData	ERRCODE	Cyclic receive data acquisition
	gerCP52_GetMasterNodeStatus	ERRCODE	Master station status acquisition
	gerCP52_SetMyStatus	ERRCODE	MyStatus send data setting
	gerCP52_SetSendCyclicData	ERRCODE	Cyclic send data setting
Own station status setup (Section 11.3.5 "Own station status setup")	gerCP52_SetNodeStatus	ERRCODE	Own station status setting
	gerCP52_ForceStop	ERRCODE	CP520 own station error setting
Own station status acquisition (Section 11.3.6 "Own station status acquisition")	gerCP52_GetNodeAndNetworkNumber	ERRCODE	Station number and network number acquisition
	gerCP52_GetCurrentCyclicSize	ERRCODE	Acquisition of cyclic transmission size specified from master station
	gerCP52_GetCommumicationStatus	ERRCODE	Data link status acquisition
	gerCP52_GetPortStatus	ERRCODE	PHY link status acquisition
	gerCP52_GetCyclicStatus	ERRCODE	Cyclic transmission status acquisition
	gerCP52_GetMIB	ERRCODE	MIB information acquisition
	gerCP52_ClearMIB	ERRCODE	MIB information clear
LED control (Section 11.3.7 "LED control")	gerCP52_SetERRLED	ERRCODE	LED control (ERR.)
	gerCP52_SetUSER1LED	ERRCODE	LED control (USER LED 1)
	gerCP52_SetUSER2LED	ERRCODE	LED control (USER LED 2)
	gerCP52_SetRUNLED	ERRCODE	LED control (RUN)
	gerCP52_DisableLED	ERRCODE	LED control function disablement
	gerCP52_EnableLED	ERRCODE	LED control function enablement
	gerCP52_UpdateLedStatus	ERRCODE	Communication status display LED update
Network time (Section 11.3.8 "Network time")	gerCP52_GetNetworkTime	ERRCODE	Network time (serial value) acquisition
	gerCP52_SetNetworkTime	ERRCODE	Network time (serial value) setting
	gerCP52_NetworkTimeToDate	ERRCODE	Network time (serial value) to clock information conversion
	gerCP52_DateToNetworkTime	ERRCODE	Clock information to network time (serial value) conversion
MDIO access (Section 11.3.9 "MDIO access")	gerCP52_EnableMACIPAccess	ERRCODE	MAC IP access enablement
	gerCP52_DisableMACIPAccess	ERRCODE	MAC IP access disablement
	gerCP52_WritePHY	ERRCODE	PHY internal register write
	gerCP52_ReadPHY	ERRCODE	PHY internal register read
	gerCP52_CheckPHY	ERRCODE	PHY check processing

Function Category (Reference Section)	Function Name	Function Type	Overview
Transient reception (Section 11.3.10 "Transient reception")	gerCP52_MainReceiveTransient1	ERRCODE	Transient reception main processing 1
	gerCP52_MainReceiveTransient2	ERRCODE	Transient reception main processing 2
	gerCP52_EnableReceiveTransient	ERRCODE	Transient reception enable/disable setting for user reasons
	gblCP52_GetReceiveTransientStatus	BOOL	Status acquisition of transient reception enable/disable setting for user reasons
	gerCP52_SetMACAddressTableData	ERRCODE	Node information distribution data (MAC address table) setting
Transient request reception (Section 11.3.11 "Transient request reception")	gerCP52_ReceivedMACAddressData	ERRCODE	Node information distribution frame receive processing
	gerCP52_ReceivedStatisticInfoRequest	ERRCODE	Statistical information acquisition request frame receive processing
	gerCP52_ReceivedUnitInfoRequest	ERRCODE	Detailed node information acquisition request frame receive processing
	gerCP52_ReceivedOptionInfoRequest	ERRCODE	Option information acquisition request frame receive processing
	gerCP52_ReceivedSelectInfoRequest	ERRCODE	Selected station information acquisition request frame receive processing
	gerCP52_ReceivedContactTestRequest	ERRCODE	Communication test request frame receive processing
	gerCP52_ReceivedCableTestRequest	ERRCODE	Cable test request frame receive processing
	gerCP52_ReceiveRemoteResetRequest	ERRCODE	SLMP remote reset request frame receive processing
	gCP52_SetSlmpError_Response	VOID	SLMP error response frame creation processing
	gerCP52_ErrCheckReqFieldNetworkReceived	ERRCODE	CC-Link IE Field specific request receive frame error check processing
	gusCP52_ErrCheckReqSlmpReceived	USHORT	SLMP request receive frame error check processing
Transient send frame header creation (Section 11.3.12 "Transient send frame header creation")	gerCP52_SetEtherCcieHeader	ERRCODE	MAC+CCIE header creation processing
	gerCP52_SetTransient1Header	ERRCODE	Transient1 header creation processing
	gerCP52_SetRequestSlmpHeader	ERRCODE	SLMP request header creation processing
	gerCP52_SetResponseSlmpHeader	ERRCODE	SLMP response header creation processing
Transient send (Section 11.3.13 "Transient send")	gerCP52_GetUnitInformation	ERRCODE	Unit information acquisition
	gusCP52_GetNodeID	USHORT	Node ID acquisition
	gerCP52_GetMulticastMACAddress	ERRCODE	Multicast MAC address acquisition
	gerCP52_GetUnicastMACAddress	ERRCODE	Unicast MAC address acquisition
	gerCP52_GetSendTransientBuffer	ERRCODE	Transient send buffer acquisition
	gerCP52_RequestSendingTransient	ERRCODE	Transient send request
	gerCP52_MainSendTransient	ERRCODE	Transient send main processing
Hardware test (Section 11.3.14 "Hardware test")	gerCP52_IEEETest	ERRCODE	IEEE 802.3ab compliance test
	gerCP52_InitializeLoopBackTest	ERRCODE	Loopback communication test initialization
	gerCP52_ExternalLoopBackTest	ERRCODE	Loopback communication test

11.3 CP520 Driver Interface Function Details

This section describes how to use the CP520 driver interface functions and the details of related functions.

11.3.1 Initial setup

(1) gulCP52_GetResetStatus

Function	Reset status acquisition			
Call format	ULONG gulCP52_GetResetStatus (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_RESET_PWRON(1): Power-on reset CP52_RESET_SYSTEM(2): System reset			
Description	This function acquires the reset status. Call this function before gerCP52_Initialize (Section 11.3.1 (2)).			

(2) gerCP52_Initialize

Function	CP520 initialization			
Call format	ERRCODE gerCP52_Initialize (const UCHAR* puchMACAddr, const CP52_UNITINFO_T *pstUnitInfo, const CP52_UNITINIT_T *pstUnitInit)			
Argument	Name	Variable name	Description	I/O
	const UCHAR	*puchMACAddr	Own station MAC address Set as follows for 12-34-56-78-90-AB: puchMACAddr[0]: 12H puchMACAddr[1]: 34H puchMACAddr[2]: 56H puchMACAddr[3]: 78H puchMACAddr[4]: 90H puchMACAddr[5]: ABH	Input
	const CP52_UNITINFO_T	*pstUnitInfo	CP520 unit information For details, refer to "Table 11.3.1-1 CP52_UNITINFO_T List".	Input
	const CP52_UNITINIT_T	*pstUnitInit	CP520 initial setup For details, refer to "Table 11.3.1-2 CP52_UNITINIT_T List".	Input
Return value	CP52_OK: Normal end			
Description	This function performs CP520 initialization and PHY reset. Calling this function disables the CP520 internal WDT. When you want to use the CP520 internal WDT, call gerCP52_EnableWDT (Section 11.3.2(3)gerCP52_EnableWDT). *: When a fatal error occurs in CP520, this function calls gCP52_CallbackFatalError (Section 11.5(1) gCP52_CallbackFatalError) created by the user. Be sure to execute error processing in accordance with the error code.			

The following describes the configuration of the argument CP52_UNITINFO_T of gerCP52_Initialize.

Table 11.3.1-1 CP52_UNITINFO_T List

No.	Member		Overview	Setting Description
1	ULONG	ulMaxRySize	RY size (bytes)*1	Specifies the RY size (bytes) communicable by the own station in increments of 1 byte. The maximum value for an intelligent device station is 256 bytes. The maximum value for a remote device station is 16 bytes.
2	ULONG	ulMaxRWwSize	RWw size (words)*1	Specifies the RWw size (words) communicable by the own station in increments of 2 words. The maximum value for an intelligent device station is 1024 words. The maximum value for a remote device station is 64 words.
3	ULONG	ulMaxRxSize	RX size (bytes)*1	Specifies the RX size (bytes) communicable by the own station in increments of 1 byte. The maximum value for an intelligent device station is 256 bytes. The maximum value for a remote device station is 16 bytes.
4	ULONG	ulMaxRWrSize	RWr size (words)*1	Specifies the RWr size (words) communicable by the own station in increments of 2 words. The maximum value for an intelligent device station is 1024 words. The maximum value for a remote device station is 64 words.
5	ULONG	ulMyStationPortTotal Number	No. of own station ports	Specifies the number of physical CC-Link IE Field Network ports of its own station. Set "2" or "1".
6	ULONG	ulTokenHoldTime;	Token hold time	Specifies the maximum time its own station holds a token after token passing begins, in µs. Set 23 µs.
7	ULONG	ulIOType	Node information (I/O type)	Specifies the I/O type. 00b indicates mixed, 01b indicates input, 10b indicates output, and 11b indicates composite. Mixed is used in a case when the input and output are mixed and the input and output use the same address. Composite is used in a case where the input and output are mixed and the input and output do not use the same address.
8	ULONG	ulNetVersion	Network firmware version	Specifies the firmware version of the network. The firmware version is any version defined by the user.
9	ULONG	ulNetModelType	Network model type	Specifies the model type (deviceType) specified by the CC-Link Partner Association.*2
10	ULONG	ulNetUnitModelCode	Network model code	Specifies the model code of the network. The model code is any code defined by the user. Manage the code so that it is unique within the same vendor code.
11	ULONG	ulNetVendorCode	Network vendor code	Specifies the vendor code (vendorCode) acquired when the vendor became a member of the CC-Link Partner Association, in BCD. (When the vendor code is 5678, 5678H is specified.)*2
12	UCHAR	auchNetUnitModel Name[20]	Network model name	Specifies the model name of the network (in 20-byte character string (ASCII code)). The model name is any name defined by the user. Manage the name so that it is unique within the same vendor code.
13	UCHAR	auchNetVendor Name[32]	Network vendor name	Specifies the vendor name of the network (in 32-byte character string (ASCII code)). The vendor name is any name (company name, brand name, etc.) defined by the user.
14	USHORT	usHwVersion	Network hardware version	Specifies the network hardware version. The hardware version is any version defined by the user.
15	USHORT	usDeviceVersion	Device version	Specifies the device version (Version). The device version (Version) indicates the version of the functions of the developed device. This information is used for associating the developed device with CSP+ files.

No.	Member		Overview	Setting Description
16	BOOL	blInformationFlag;	Controller information status flag	Enables/Disables Nos. 14-21 in this table. CP52_FALSE indicates disable, and CP52_TRUE indicates enable. Disabled when there is only a communication function (example: QJ71GF11-T2).
17	ULONG	ulCtrlVersion	Controller firmware version	Specifies the firmware version of the controller. The firmware version is any version defined by the user.
18	ULONG	ulCtrlModelType	Controller model type	Specifies the model type (deviceType) specified by the CC-Link Partner Association.*2
19	ULONG	ulCtrlUnitModelCode	Controller model code	Specifies the model name of the controller. The model code is any code defined by the user. Manage the code so that it is unique within the same vendor code.
20	ULONG	ulCtrlVendorCode	Controller vendor code	Specifies the vendor code (vendorCode) acquired when the vendor became a member of the CC-Link Partner Association, in BCD. (When the vendor code is 5678, 5678H is specified.)*2
21	UCHAR	auchCtrlUnitModel Name[20]	Controller model name	Specifies the model name of the controller (in 20-byte character string (ASCII code)). The model name is any name defined by the user. Manage the name so that it is unique within the same vendor code.
22	UCHAR	auchCtrlVendorName [32]	Controller vendor name	Specifies the vendor name of the controller (in 32-byte character string (ASCII code)). The vendor name is any name defined by the user.
23	ULONG	ulVendorInformation	Controller vendor device specific information	Specifies the vendor device specific information of the controller. The vendor device specific information is any information defined by the user.

*1: If the set size is different from the one specified by the master station (the one set in GX Works2/GX Works3), the size specified by the master station is used.

*2: Refer to Section 2.2 "Acquiring a Vendor Code and Selecting a Device Type".

Device Version: Supplemental Information

[Background]
When the software version of a CP520 application product is upgraded, specification changes sometimes occur, such as the addition of slave station parameter processing or command execution.
When the specifications of a CP520 application product change, the CSP+ file also needs to be updated in accordance with the specification change.

[Purpose of device version]
The information that identifies the specifications before and after a change is the device version. The device version is used to indicate the specifications of the CP520 application product that correspond to each CSP+ file.

(a) Purpose of use by engineering tool
The engineering tool manages all CSP+ files having different device versions, making it possible to provide optimum functions and UI in accordance with the used version of the CP520 application product.

(b) Purpose of use by end user
The end user can select the CSP+ file for the device actually used upon comparing the device versions described in the CSP+ file and the version of the CP520 application product used.
For details, refer to "DEVICE_INFO Part" in the "Control & Communication System Profile Specification".

Network and Controller: Supplemental Information

1) Definition of network and controller
Network: A communication section comprising CP520 and the peripheral circuit in the own station
Controller: A functional section which is unique to the user (such as I/O section, temperature adjustment section and robot section) in the own station

2) Setting of network
Network setting is required. The following items are checked in the conformance test.

No.8 Network firmware version	No.10 Network model code
No.9 Network model type	No.11 Network vendor code

3) Setting of controller
Controller setting is optional.
Set the controller in the following cases. (In other cases, controller setting is not required.)
- When performing the parameter processing/command execution of slave station after verifying the vendor code/model code described in the CSP+ file against the controller information of the connected slave stations.
- When the CP520 application product (network) is a communication optional item for a product (controller) such as series products.
- When the manufacturer of controller and network is different.

The following shows the configuration of the argument "CP52_UNITINIT_T" of gerCP52_Initialize.

Table 11.3.1-2 CP52_UNITINIT_T List

No.	Member		Overview	Setting Description
1	BOOL	blNMIUse	NMI interrupt use	Specify "CP52_TRUE" when you want to use the CP520 internal WDT function, and "CP52_FALSE" when you do not. Specifying "CP52_TRUE" changes the NMIL pin to "Low" when the CP520 internal WDT overflows.
2	BOOL	blInterruptUse	CPU interrupt function use	Specify "CP52_TRUE" when you want to use the CP520 CPU interrupt function, and "CP52_FALSE" when you do not. Specifying "CP52_TRUE" changes the INTL pin to "Low" when a CP520 interrupt occurs.
3	BOOL	blFailedProcess1	Failed process setting 1	Specify "CP52_TRUE". When any of the signals below are true, CP520 changes to bypass mode. (Communication frames are neither sent nor received. A received frame is forwarded as is to another port.) [1] When the WDTIL signal is True (Low) [2] When the CP520 internal WDT times out To clear bypass mode, power-on reset or system reset is required.
4	BOOL	blFailedProcess2	Failed process setting 2	Specify "CP52_TRUE". When an own station error is set (gerCP52_ForceStop), CP520 changes to bypass mode. (Communication frames are neither sent nor received. A received frame is forwarded as is to another port.) To clear the own station error, power-on reset or system reset is required. For details on gerCP52_ForceStop, refer to (2) in Section 11.3.5 "Own station status setup".
5	ULONG	ulNodeType	Node type	Specifies the node type of its own station. Specify (0033H) for an intelligent device station. Specify (0034H) for a remote device station.
6	BOOL	blTransientReceiveEnable	Transient reception function	Specify "CP52_TRUE". The transient reception function support status is specified. "CP52_TRUE": Supported "CP52_FALSE": Not supported
7	BOOL	blMACAddressTableRequest	Initial value of Node information distribution request	Specify "CP52_TRUE" when the transient transmission client function is implemented, and specify "CP52_FALSE" when it is not implemented. [Node information] Node information indicates the correspondence between the MAC addresses and station numbers of other stations. When "CP52_TRUE" is specified, node information is distributed from the master station by multicast. When "CP52_FALSE" is specified, discard the received Node information distribution frames using the user program. [When Transient frames are sent] When transient frames are actively sent (with client), node information is used. When a response is returned to the send source (with server), the response can be returned using the send source MAC address, and therefore node information is not used.
8	ULONG	ulRunStatus	Initial value of detailed application operation status	Specifies the initial value of the detailed application operation status within nodeStatus of the MyStatus frame. CP52_RUNSTS_UNSUPPORTED (0000H): Detailed application operation status notification not supported CP52_RUNSTS_STOP (0001H): Application stopped CP52_RUNSTS_RUN (0002H): Application running CP52_RUNSTS_NOTEXIST (0003H): Application substance does not exist

No.	Member		Overview	Setting Description
9	ULONG	ulErrorStatus	Initial value of detailed application error status	Sets the initial value of the detailed application error status of the nodeStatus field of the MyStatus frame. CP52_ERRSTS_NONE (0000H): No error CP52_ERRSTS_WARNING (0001H): Minor error CP52_ERRSTS_ERROR (0002H): Moderate error CP52_ERRSTS_FATALERROR (0003H): Major error
10	ULONG	ulUserInformation	Initial value of vendor specific node information	Specifies the initial value of vendorSpfNodeInfo of the MyStatus frame.
11	ULONG	ulOptionSupport	Initial value of option status	Set this to "CP52_TRUE" (recommended) when options are supported, and to "CP52_FALSE" when options are not supported. [Option] An option is an extended function of CC-Link IE Field Network, and includes the SLMP frame send/receive function and CC-Link IE Field Network diagnostic function.
12	ULONG	ulSlmpSupport	Initial value of SLMP support bit	Set this to "CP52_TRUE" (recommended) when SLMP frames are sent and received, and to "CP52_FALSE" when they are not. * To send and receive SLMP frames, set both this and the "Initial value of option status" to "CP52_TRUE".
13	ULONG	ulSlmpDiagnosisSupport	Initial value of diagnostic function support status	Set this to "CP52_TRUE" (recommended) when the CC-Link IE Field Network diagnostic function is supported, and to "CP52_FALSE" when it is not. * To support the CC-Link IE Field Network diagnostic function, set this as well as the "Initial value of option status" and the "Initial value of SLMP support bit" to "CP52_TRUE".
14	CP52_PHY_SETTING_T	stPHYSetting[2]	Initial value of PHY setting	Sets the MDI/MID-X and the Master/Slave setting for each port. Refer to "Table 11.3.1-3 CP52_PHY_SETTING_T List".

Table 11.3.1-3 CP52_PHY_SETTING_T List

No.	Member		Overview	Setting Description
1	ULONG	ulMDI	MDI setting	Specify MDI/MDI-X for each port. When you want to use the fast linkup function, set PORT1 to "CP52_MDI_FORCED_MDI" and PORT2 to "CP52_MDI_FORCED_MDIX". When you do not want to use the fast linkup function, set "CP52_MDI_AUTO". CP52_MDI_AUTO (0000H): Auto CP52_MDI_FORCED_MDI (0001H): Forced MDI CP52_MDI_FORCED_MDIX (0002H): Forced MDI-X
2	ULONG	ulClk	1000BASE-T clock setting	Specify Master/Slave for each port. When you want to use the fast linkup function, set PORT1 to "CP52_CLOCK_MASTER" and PORT2 to "CP52_CLOCK_SLAVE". When you do not want to use the fast linkup function, set "CP52_CLOCK_AUTO". CP52_CLOCK_AUTO (0000H): Auto CP52_CLOCK_MASTER (0001H): Forced master CP52_CLOCK_SLAVE (0002H): Forced slave

(3) gerCP52_SetNodeAndNetworkNumber

Function	Station number and network number setting			
Call format	ERRCODE gerCP52_SetNodeAndNetworkNumber (UCHAR uchNetworkNumber,USHORT usNodeNumber)			
Argument	Name	Variable name	Description	I/O
	UCHAR	uchNetworkNumber	Network number (value range: 1 to 239)	Input
	USHORT	usNodeNumber	Station number (value range: 1 to 120)	Input
Return value	CP52_OK: Normal end CP52_ERR: Abnormal end (status error in library) CP52_ERR_OUTOFRANGE: Station number out of range or network number out of range			
Description	This function sets the station number and network number in CP520. When the return value is CP52_ERR_OUTOFRANGE, the station number and network number are not set. Add error processing to the call source function. *: This function needs to be called after iUserInitialization (Section 10.2.2 "Initialization processing") before calling gerCP52_Start (Section 11.3.1 (4)) by iUserStart (Section 10.2.3 "Communication start processing"). Calling this function before executing the above processing results in a CP52_ERR (abnormal end; status error in library).			

(4) gerCP52_Start

Function	CP520 communication start			
Call format	ERRCODE gerCP52_Start(VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end CP52_ERR: Abnormal end			
Description	This function instructs to start communication to CP520. *: When a fatal error occurs in CP520, this function calls gCP52_CallbackFatalError (Section 11.5(1) gCP52_CallbackFatalError) created by the user. Be sure to execute error processing in accordance with the error code.			

11.3.2 Watchdog timer

(1) gerCP52_ResetWDT

Function	CP520 internal WDT reset			
Call format	ERRCODE gerCP52_ResetWDT (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end			
Description	This function resets the CP520 internal WDT. *: If you want to call a function within Section 9.3.2 "Watchdog timer" after this function is called, wait 1.032µs or longer.			

(2) gerCP52_DisableWDT

Function	CP520 internal WDT disablement			
Call format	ERRCODE gerCP52_DisableWDT (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end			
Description	This function disables the CP520 internal WDT. *: If you want to call a function within Section 9.3.2 "Watchdog timer" after this function is called, wait 1.032µs or longer. CP520 enables the CP520 internal WDT immediately after reset. (Initial value of CP520 internal WDT time limit setting: 3.2 s.) The CP520 internal WDT is disabled in gerCP52_Initialize (Section 11.3.1(2)gerCP52_Initialize). Implement one of the following when the period until startup of gerCP52_Initialize takes time ・ Call this function to disable the CP520 internal WDT. ・ Call gerCP52_ResetWDT (Section 11.3.2 (1) gerCP52_ResetWDT) to reset the CP520 internal WDT. (Make sure that the CP520 internal WDT does not time out.)			

(3) gerCP52_EnableWDT

Function	CP520 internal WDT enablement			
Call format	ERRCODE gerCP52_EnableWDT (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end			
Description	This function enables the CP520 internal WDT. *: If you want to call a function within Section 11.3.2 "Watchdog timer" after this function is called, wait 1.032µs or longer. CP520 disables the CP520 internal WDT when gerCP52_Initialize (Section 11.3.1(2)gerCP52_Initialize) is called. Be sure to implement this function when you want to use the CP520 internal WDT.			

(4) gerCP52_SetWDT

Function	CP520 internal WDT time limit setting			
Call format	ERRCODE gerCP52_SetWDT (USHORT usWDTCOUNT)			
Argument	Name	Variable name	Description	I/O
	USHORT	usWDTCOUNT	CP520 internal WDT time limit setting 0000H: 100ms 0001H: 200ms 0002H: 300ms … 001FH: 3.2 s	Input
Return value	CP52_OK: Normal end			
Description	This function sets the CP520 internal WDT time limit. *: If you want to call a function within Section 11.3.2 "Watchdog timer" after this function is called, wait 1.032μs or longer. If the CP520 internal WDT time limit setting is changed by this function while the CP520 internal WDT is running (after gerCP52_EnableWDT (Section 11.3.2 (3)gerCP52_EnableWDT) is called), the CP520 internal WDT runs using the new time limit setting when gerCP52_ResetWDT (Section 11.3.2 (1)gerCP52_ResetWDT) is called. (Until gerCP52_ResetWDT is called, the CP520 internal WDT runs using the CP520 internal WDT time limit setting prior to the change.)			

11.3.3 Event

(1) gerCP52_GetEvent

Function	CP520 event detection			
Call format	ERRCODE gerCP52_GetEvent (CP52_EVTPRM_INTERRUPT_T *pstEvent)			
Argument	Name	Variable name	Description	I/O
	CP52_EVTPRM_INTERRUPT_T	*pstEvent	Interrupt cause For details, refer to "Table 11.3.3-1 CP52_EVTPRM_INTERRUPT_T List".	Output
Return value	CP52_OK: Normal end			
Description	This function detects CP520 events.			

The following describes the configuration of CP52_EVTPRM_INTERRUPT_T.

Table 11.3.3-1 CP52_EVTPRM_INTERRUPT_T List

No.	Member		Overview
1	ULONG	b1ZCommConnect	Connect communication
2	ULONG	b1ZCommDisconnect	Disconnect communication
3	ULONG	b1ZCommConnectToDisconnect	Connect communication → Disconnect communication
4	ULONG	b1ZCommDisconnectToConnect	Disconnect communication → Connect communication
5	ULONG	b1ZChangeStNoNetNo	Change station number and network number
6	ULONG	b1ZChangeActCommand	Change run command
7	ULONG	b1ZPrmFrmRcv_OK	Parameter frame reception
8	ULONG	b1ZReserve1	Reserved
9	ULONG	b1ZPrmChkFrmRcv_OK	ParamCheck frame reception (when parameters match)
10	ULONG	b3ZReserve2	Reserved
11	ULONG	b1ZRecvNonCyclic	Transient reception
12	ULONG	b1ZSendFinNonCyclic	Transient send complete
13	ULONG	b7ZReserve3	Reserved
14	ULONG	b1ZMasterWatchTimeout	Master watch timer timeout occurred
15	ULONG	bAZReserve4	Reserved

(2) gerCP52_Main

Function	CP520 event detection main processing			
Call format	ERRCODE gerCP52_Main (const CP52_EVTPRM_INTERRUPT_T *pstEvent)			
Argument	Name	Variable name	Description	I/O
	const CP52_EVTPRM_INTERRUPT_T	*pstEvent	Interrupt cause	Input
Return value	CP52_OK: Normal end CP52_ERR: Abnormal end (status error in library)			
Description	This function performs processing in response to a CP520 event. *: This function needs to be called after IUserInitialization (Section 10.2.2 "Initialization processing") and iUserStart (Section 10.2.3 "Communication start processing"). Calling this function before executing the above processing results in a CP52_ERR (abnormal end; status error in library).			

(3) gerCP52_RestartEvent

Function	CP520 event restart			
Call format	ERRCODE gerCP52_RestartEvent (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end			
Description	This function restarts events stopped by gerCP52_GetEvent (Section 11.3.3 (1)gerCP52_GetEvent).			

(4) gerCP52_UpdateMIB

Function	MIB information update			
Call format	ERRCODE gerCP52_UpdateMIB (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end CP52_ERR: Abnormal end (MIB information collection error (status error in library / mismatch)) CP52_ERR_OTHER: Abnormal end (MIB information collection error (error occurred in driver inside library))			
Description	This function updates the MIB information. *: When the return value of this function is a value other than CP52_OK, the function calls gCP52_CallbackFatalError (Section 11.5(1) gCP52_CallbackFatalError) created by the user. Be sure to execute error processing in accordance with the error code.			

(5) gerCP52_MyStaRcvTkn

Function	Receive processing of token frame addressed to the own station			
Call format	ERRCODE gerCP52_MyStaRcvTkn (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end			
Description	This function receives the token frame which is addressed to the own station.			

11.3.4 Cyclic transmission

(1) gerCP52_SetCyclicStop

Function	Cyclic transmission stop for user application-side reasons			
Call format	ERRCODE gerCP52_SetCyclicStop (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end			
Description	This function stops cyclic transmission for device-side reasons. If you want to clear the stop status, call the function gerCP52_ClearCyclicStop (Section 11.3.4 (2)gerCP52_ClearCyclicStop).			

(2) gerCP52_ClearCyclicStop

Function	Cyclic transmission stop clear for user application-side reasons			
Call format	ERRCODE gerCP52_ClearCyclicStop (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end			
Description	This function clears cyclic transmission stop that was called by the function gerCP52_SetCyclicStop (Section 11.3.4 (1)gerCP52_SetCyclicStop).			

(3) gerCP52_GetReceivedCyclicData

Function	Cyclic receive data acquisition			
Call format	ERRCODE gerCP52_GetReceivedCyclicData (VOID *pRyDst, VOID *pRWwDst, BOOL blEnable)			
Argument	Name	Variable name	Description	I/O
	VOID	*pRyDst	RY area	Output
	VOID	*pRWwDst	RWw area*1	Output
	BOOL	blEnable	Enables/Disables copying. CP52_TRUE: Enable CP52_FALSE: Disable	Input
Return value	CP52_OK: Normal end (received data present) CP52_ERR: Abnormal end (no received data)			
Description	This function stores cyclic receive data from the master station in the addresses indicated by pRyDst and pRWwDst. Note, however, that when blEnable is set to CP52_FALSE, the cyclic receive data is discarded. The return value changes to CP52_ERR.*2 *1: Set the start address of the RWw area in increments of 4 bytes (0 or multiple of 4). *2: CP52_ERR: Abnormal end (no received data) While a CP52_ERR occurs when no cyclic communication is received from the previous call of gerCP52_GetReceivedCyclicData to the current call of gerCP52_GetReceivedCyclicData, this does not indicate an error.			

(4) gerCP52_GetMasterNodeStatus

Function	Master station status acquisition			
Call format	ERRCODE gerCP52_GetMasterNodeStatus (BOOL *pblRunSts, BOOL *pblErrSts, ULONG *pulErrCode)			
Argument	Name	Variable name	Description	I/O
	BOOL	*pblRunSts	Master station application operation status CP52_TRUE: Running CP52_FALSE: Stopped	Output
	BOOL	*pblErrSts	Master station application error status CP52_TRUE: Error CP52_FALSE: No error	Output
	ULONG	*pulErrCode	Master station error code	Output
Return value	CP52_OK: Normal end (MyStatus frame received from master station) CP52_ERR: Abnormal end (MyStatus frame not received from master station due to no data link (data link disconnected))			
Description	This function acquires the status of the master station from the MyStatus frame received from the master station. When the MyStatus frame is not received from the master station due to no data link (data link disconnected), the arguments are as follows: pblRunSts: CP52_FALSE pblErrSts: CP52_FALSE pulErrCode: 0			

(5) gerCP52_SetMyStatus

Function	MyStatus send data setting			
Call format	ERRCODE gerCP52_SetMyStatus (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end			
Description	This function sets its own station status specified by gerCP52_SetNodeStatus in CP520 (Section 11.3.5(1) gerCP52_SetNodeStatus).			

(6) gerCP52_SetSendCyclicData

Function	Cyclic send data setting			
Call format	ERRCODE gerCP52_SetSendCyclicData (const VOID *pRxSrc, const VOID *pRWrSrc, BOOL blEnable)			
Argument	Name	Variable name	Description	I/O
	const VOID	*pRxSrc	RX area	Input
	const VOID	*pRWrSrc	RWr area*1	Input
	BOOL	blEnable	Enables/Disables update. CP52_TRUE: Enable CP52_FALSE: Disable	Input
Return value	CP52_OK: Normal end			
Description	This function sets the cyclic send data stored in the addresses specified by pRxSrc and pRWrSrc to CP520. Note, however, that when blEnable is set to CP52_FALSE, cyclic send data is not set. (The return value changes to CP52_ERR.) *1: Set the start address of the RWr area in increments of 4 bytes (0 or multiple of 4).			

11.3.5 Own station status setup

(1) gerCP52_SetNodeStatus

Function	Own station status setting			
Call format	ERRCODE gerCP52_SetNodeStatus (ULONG ulRunSts, ULONG ulErrSts, ULONG ulErrCode,ULONG ulUserInformation)			
Argument	Name	Variable name	Description	I/O
	ULONG	ulRunSts	Detailed application operation status CP52_RUNSTS_UNSUPPORTED(0): Detailed application operation status notification not supported CP52_RUNSTS_STOP(1): Application stopped CP52_RUNSTS_RUN(2): Application running CP52_RUNSTS_NOTEXIST(3): Application substance does not exist	Input
	ULONG	ulErrSts	Detailed application error status CP52_ERRSTS_NONE(0): No error CP52_ERRSTS_WARNING(1): Minor error CP52_ERRSTS_ERROR(2): Moderate error CP52_ERRSTS_FATALERROR(3): Major error	Input
	ULONG	ulUserInformation	Vendor specific node information	Input
Return value	CP52_OK: Normal end			
Description	This function sets its own station status as information to be sent in a MyStatus frame.			

(2) gerCP52_ForceStop

Function	CP520 own station error setting			
Call format	ERRCODE gerCP52_ForceStop (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end			
Description	This function sets an own station error in CP520. To clear the own station error, power-on reset or system reset is required.			

11.3.6 Own station status acquisition

(1) gerCP52_GetNodeAndNetworkNumber

Function	Station number and network number acquisition			
Call format	ERRCODE gerCP52_GetNodeAndNetworkNumber (USHORT *pusNodeNumber,UCHAR *puchNetworkNumber)			
Argument	Name	Variable name	Description	I/O
	USHORT	*pusNodeNumber	Station number	Output
	UCHAR	*puchNetworkNumber	Network number	Output
Return value	CP52_OK: Normal end			
Description	This function acquires the station number and network number.			

(2) gerCP52_GetCurrentCyclicSize

Function	Acquisition of cyclic transmission size specified from master station			
Call format	ERRCODE gerCP52_GetCurrentCyclicSize (CP52_CYCLIC_SIZE_T *pstCyclicSize)			
Argument	Name	Variable name	Description	I/O
	CP52_CYCLIC_SIZE_T	*pstCyclicSize	Cyclic transmission size For details, refer to "Table 11.3.6-1 CP52_CYCLIC_SIZE_T List".	Output
Return value	CP52_OK: Normal end			
Description	This function acquires the cyclic transmission size specified from the master station in the parameter frame. The functions gerCP52_GetReceivedCyclicData (Section 11.3.4(3)gerCP52_GetReceivedCyclicData) and gerCP52_SetSendCyclicData (Section 11.3.4(6)gerCP52_SetSendCyclicData) input and output cyclic send and reception data in the size acquired by this function.			

Table 11.3.6-1 CP52_CYCLIC_SIZE_T List

No.	Member		Description
1	ULONG	ulRySize	RY size (byte)
2	ULONG	ulRWwSize	RWw size (byte)
3	ULONG	ulRxSize	RX size (byte)
4	ULONG	ulRWrSize	RWr size (byte)

(3) gerCP52_GetCommumicationStatus

Function	Data link status acquisition			
Call format	ERRCODE gerCP52_GetCommumicationStatus (ULONG *pulCommSts)			
Argument	Name	Variable name	Description	I/O
	ULONG	*pulCommSts	Data link status CP52_COMMSTS_CYC_DLINK(2): Data link in operation (cyclic transmission in progress) CP52_COMMSTS_TOKEN_PASS(1): Data link in operation (cyclic transmission stopped) CP52_COMMSTS_DISCONNECT(0): No data link (disconnected)	Output
Return value	CP52_OK: Normal end			
Description	This function acquires the data link status. Turn the D LINK LED on/off according to the data link status. CP52_COMMSTS_CYC_DLINK(2): LED on CP52_COMMSTS_TOKEN_PASS(1): LED blinking CP52_COMMSTS_DISCONNECT(0): LED off *: For D LINK LED on/off control, refer to UserUpdateLed (Section 10.2.11 "LED update processing").			

(4) gerCP52_GetPortStatus

Function	PHY link status acquisition				
Call format	ERRCODE gerCP52_GetPortStatus (ULONG ulPort, ULONG *pulLinkStatus, ULONG *pulSpeed, ULONG *pulDuplex)				
Argument	Name	Variable name	Description		I/O
	ULONG	ulPort	Port specification	CP52_PORT1(0): PORT1 CP52_PORT2(1): PORT2	Input
	ULONG	*pulLinkStatus	Link status	CP52_LINKUP(1): Link up CP52_LINKDOWN(0): Link down	Output
	ULONG	*pulSpeed	Speed*1	CP52_SPEED_1G(0): 1Gbps CP52_SPEED_100M(1): 100Mbps CP52_SPEED_10M(2): 10Mbps	Output
	ULONG	*pulDuplex	Full duplex / Half duplex *1	CP52_DUPLEX_FULL(0): Full duplex CP52_DUPLEX_HALF(1): Half duplex	Output
Return value	CP52_OK: Normal end				
Description	This function acquires the PHY link status. *1: Enabled when the second argument *pulLinkStatus is CP52_LINKUP (1). Do not use this when the second argument is CP52_LINKDOWN (0).				

(5) gerCP52_GetCyclicStatus

Function	Cyclic transmission status acquisition			
Call format	ERRCODE gerCP52_GetCyclicStatus (CP52_CYCLIC_STA_T *pstCyclicStatus)			
Argument	Name	Variable name	Description	I/O
	CP52_CYCLIC_STA_T	*pstCyclicStatus	Cyclic transmission status For details, refer to "Table 11.3.6-2 CP52_CYCLIC_STA_T List".	Output
Return value	CP52_OK: Normal end			
Description	This function acquires the cyclic transmission status.			

The following describes the configuration of CP52_CYCLIC_STA_T.

Table 11.3.6-2 CP52_CYCLIC_STA_T List

No.	Member		Bit	Overview	Description
1	USHORT	b3ZComonParamkeepCond	b2-0	Cyclic transmission parameter hold status	001b: Parameter normally received 010b: Not received or ID mismatch 011b: Checking 100b: Parameter abnormally received
2	USHORT	b1ZParamCheckCond	b3	Cyclic transmission parameter check status	0b: Checked 1b: Checking
3	USHORT	b1ZMyNodeNoRangeOut	b4	Station number invalid setting status	0b: In range 1b: Out of range
4	USHORT	b1ZMyNodeReserveSetup	b5	Reserved station setting status	0b: Non-reserved node 1b: Reserved node
5	USHORT	b1ZCyclicOpeInstructPackage	b6	Cyclic transmission implementation instruction (batch) setting status	0b: Run 1b: Stop
6	USHORT	b1ZCyclicOpeInstructVarious	b7	Cyclic transmission implementation instruction (individual) setting status	0b: Run 1b: Stop
7	USHORT	b1ZReserved1	b8	Reserved	-
8	USHORT	b1ZMyMpuAbnomal	b9	Cyclic transmission continuation not possible error status	0b: No error 1b: Cyclic transmission continuation not possible error
9	USHORT	b1ZMyNodeNumberDuplicate	b10	Station number duplication status	0b: No duplication 1b: Duplication
10	USHORT	b1ZReserved2	b11	Reserved	-
11	USHORT	b1ZNodeTypeWrong	b12	Station type invalid / Specified size invalid status	0b: Normal 1b: Invalid
12	USHORT	b1ZReserved3	b13	Reserved	-
13	USHORT	b1ZDLinkState	b14	Disconnection status	0b: Not disconnected (cyclic transmission in progress or token passing in progress) 1b: Disconnected
14	USHORT	b1ZCyclicState	b15	Stop status due to own reasons	0b: Not stopped 1b: Cyclic transmission stopped due to reason other than the above

(6) gerCP52_GetMIB

Function	MIB information acquisition			
Call format	ERRCODE gerCP52_GetMIB (CP52_MIB_T *pstMIB)			
Argument	Name	Variable name	Description	I/O
	CP52_MIB_T	*pstMIB	CP520 MIB information For details, refer to (1) to (3) in Section 10.2.13 "MIB information acquisition processing".	Output
Return value	CP52_OK: Normal end			
Description	This function acquires MIB information.			

(7) gerCP52_ClearMIB

Function	MIB information clear			
Call format	ERRCODE gerCP52_ClearMIB (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end			
Description	This function clears MIB information.			

Caution
MIB information is non-disclosed information. Do not disclose the information to the end user.

11.3.7 LED control

(1) gerCP52_SetERRLED

Function	LED control (ERR.)			
Call format	ERRCODE gerCP52_SetERRLED (ULONG ulCtrl)			
Argument	Name	Variable name	Description	I/O
	ULONG	ulCtrl	LED control CP52_LED_OFF: LED off CP52_LED_ON: LED on CP52_LED_BLINK: LED blinking	Input
Return value	CP52_OK: Normal end			
Description	This function turns on and off the ERR. LED. *: The LED cannot be turned off or set to blinking when a CP520 internal WDT, external WDT, or own station error occurs.			

(2) gerCP52_SetUSER1LED

Function	LED control (USER LED 1)			
Call format	ERRCODE gerCP52_SetUSER1LED (ULONG ulCtrl)			
Argument	Name	Variable name	Description	I/O
	ULONG	ulCtrl	LED control CP52_LED_OFF: LED off CP52_LED_ON: LED on CP52_LED_BLINK: LED blinking	Input
Return value	CP52_OK: Normal end			
Description	This function turns on and off USER LED 1. *: The LED cannot be turned on or set to blinking when a CP520 internal WDT, external WDT, or own station error occurs.			

(3) gerCP52_SetUSER2LED

Function	LED control (USER LED 2)			
Call format	ERRCODE gerCP52_SetUSER2LED (ULONG ulCtrl)			
Argument	Name	Variable name	Description	I/O
	ULONG	ulCtrl	LED control CP52_LED_OFF: LED off CP52_LED_ON: LED on CP52_LED_BLINK: LED blinking	Input
Return value	CP52_OK: Normal end			
Description	This function turns on and off USER LED 2. *: The LED cannot be turned on or set to blinking when a CP520 internal WDT, external WDT, or own station error occurs.			

(4) gerCP52_SetRUNLED

Function	LED control (RUN)			
Call format	ERRCODE gerCP52_SetRUNLED (ULONG ulCtrl)			
Argument	Name	Variable name	Description	I/O
	ULONG	ulCtrl	LED control CP52_LED_OFF: LED off CP52_LED_ON: LED on	Input
Return value	CP52_OK: Normal end			
Description	This function turns on and off the RUN LED. *: The LED cannot be turned on when a CP520 internal WDT, external WDT, or own station error occurs.			

(5) gerCP52_DisableLED

Function	LED control function disablement			
Call format	ERRCODE gerCP52_DisableLED (USHORT usBitPattern)			
Argument	Name	Variable name	Description	I/O
	USHORT	usBitPattern	LED control function disablement(ON: Disable, OFF: Hold previous value) Bit 0: Disable RUN LED Bit 2: Disable USER LED 2 Bit 4: Disable USER LED 1 Bit 6: Disable D LINK LED Bit 8: Disable ERR. LED Bit10: Disable port 1 L ER LED Bit11: Disable port 2 L ER LED (Bits 1, 3, 5, 7, 9, and 12-15: Not used)	Input
Return value	CP52_OK: Normal end			
Description	This function disables the LED function. *: The function cannot be disabled when a CP520 internal WDT, external WDT, or own station error occurs.			

(6) gerCP52_EnableLED

Function	LED control function enablement			
Call format	ERRCODE gerCP52_EnableLED (USHORT usBitPattern)			
Argument	Name	Variable name	Description	I/O
	USHORT	usBitPattern	LED control function enablement(ON: Enable, OFF: Hold previous value) Bit 0: Enable RUN LED Bit 2: Enable USER LED 2 Bit 4: Enable USER LED 1 Bit 6: Enable D LINK LED Bit 8: Enable ERR. LED Bit10: Enable port 1 L ER LED Bit11: Enable port 2 L ER LED (Bits 1, 3, 5, 7, 9, and 12-15: Not used)	Input
Return value	CP52_OK: Normal end			
Description	This function enables the LED function.			

(7) gerCP52_UpdateLedStatus

<table>
<tr><td>Function</td><td colspan="4">Communication status display LED update</td></tr>
<tr><td>Call format</td><td colspan="4">ERRCODE gerCP52UpdateLedStatus (VOID)</td></tr>
<tr><td rowspan="2">Argument</td><td>Name</td><td>Variable name</td><td>Description</td><td>I/O</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Return value</td><td colspan="4">CP52_OK: Normal end</td></tr>
<tr><td>Description</td><td colspan="4">This function controls the D LINK LED of its own station in accordance with the data link status of the argument acquired by the Data link status acquisition processing (Section 11.3.6(3) gerCP52_GetCommumicationStatus).
<table>
<tr><th>Data Link Status</th><th>D LINK LED</th></tr>
<tr><td>Data link in operation (cyclic transmission in progress)</td><td>On</td></tr>
<tr><td>Data link in operation (cyclic transmission stopped)</td><td>Blinking</td></tr>
<tr><td>No data link (disconnected)</td><td>Off</td></tr>
</table>
In addition, the function controls the L ER1 LED and L ER2 LED in accordance with the result of token passing during ring connection.
<table>
<tr><th>Token Passing</th><th>L ER1 LED</th><th>L ER2 LED</th></tr>
<tr><td>Token not passed (disconnected)</td><td>Off</td><td>Off</td></tr>
<tr><td>Token passing in progress and both ports enabled</td><td>Off</td><td>Off</td></tr>
<tr><td>Token passing in progress and only PORT1 enabled</td><td>Off</td><td>On</td></tr>
<tr><td>Token passing in progress and only PORT2 enabled</td><td>On</td><td>Off</td></tr>
</table></td></tr>
</table>

11.3.8 Network time

(1) gerCP52_GetNetworkTime

Function	Network time (serial value) acquisition			
Call format	ERRCODE gerCP52_GetNetworkTime (USHORT *pusSerial)			
Argument	Name	Variable name	Description	I/O
	USHORT	*pusSerial	Network time pusSerial[0]: Network time (bits 15-0) pusSerial[1]: Network time (bits 31-16) pusSerial[2]: Network time (bits 47-32)	Output
Return value	CP52_OK: Normal end			
Description	This function acquires the network time (serial value in increments of 15.2587890625 μs given a starting point of January 1, 2000, 00:00:00).			

(2) gerCP52_SetNetworkTime

Function	Network time (serial value) setting			
Call format	ERRCODE gerCP52_SetNetworkTime (const USHORT *pusSerial)			
Argument	Name	Variable name	Description	I/O
	const USHORT	*pusSerial	Network time pusSerial[0]: Network time (bits 15-0) pusSerial[1]: Network time (bits 31-16) pusSerial[2]: Network time (bits 47-32)	Input
Return value	CP52_OK: Normal end			
Description	This function sets the network time (serial value in increments of 15.2587890625 μs given a starting point of January 1, 2000, 00:00:00).			

(3) gerCP52_NetworkTimeToDate

Function	Network time (serial value) to clock information conversion			
Call format	ERRCODE gerCP52_NetworkTimeToDate (CP52_TIMEINFO_T *pstTimeInfo, const USHORT *pusSerial)			
Argument	Name	Variable name	Description	I/O
	CP52_TIMEINFO_T	*pstTimeInfo	Clock information For details, refer to "Table 11.3.8-1 CP52_TIMEINFO_T List".	Output
	const USHORT	*pusSerial	Network time pusSerial[0]: Network time (bits 31-16) pusSerial[1]: Network time (bits 47-32)	Input
Return value	CP52_OK: Normal end			
Description	This function converts the network time (serial value in increments of seconds given a starting point of January 1, 2000, 00:00:00) to clock information [year/month/day/hour/minute/second/millisecond (fixed to 0)/day of the week].			

The following describes the configuration of CP52_TIMEINFO_T.

Table 11.3.8-1 CP52_TIMEINFO_T List

No.	Member		Overview
1	USHORT	usYear	Year (2000-2136)
2	USHORT	usMonth	Month (1-12)
3	USHORT	usDay	Day (1-31)
4	USHORT	usHour	Hour (0-23)
5	USHORT	usMin	Minute (0-59)
6	USHORT	usSec	Second (0-59)
7	USHORT	usMsec	Millisecond (0-999)
8	USHORT	usWday	Day of week (0 (Sunday)-6 (Saturday))

(4) gerCP52_DateToNetworkTime

Function	Clock information to network time (serial value) conversion			
Call format	ERRCODE gerCP52_DateToNetworkTime (const CP52_TIMEINFO_T *pstTimeInfo, USHORT *pusSerial)			
Argument	Name	Variable name	Description	I/O
	const CP52_TIMEINFO_T	*pstTimeInfo	Clock information	Input
	USHORT	*pusSerial	Network time pusSerial[0]: Network time (bits 15-0) pusSerial[1]: Network time (bits 31-16) pusSerial[2]: Network time (bits 47-32)	Output
Return value	CP52_OK: Normal end CP52_ERR: Abnormal end			
Description	This function converts clock information (year/month/day/hour/minute/second) to network time (serial value in increments of seconds given a starting point of January 1, 2000, 00:00:00). (ausSerial[0]: Network time (bits 15-0) is fixed to 0.) *: A year other than 2000-2136 results in a CP52_ERR. The CP520 driver does not check for any errors other than the above. Implement error processing in the user program to ensure that there are no leap year or date errors.			

11.3.9 MDIO access

(1) gerCP52_EnableMACIPAccess

Function	MAC IP access enablement			
Call format	ERRCODE gerCP52_EnableMACIPAccess (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end CP52_ERR: Abnormal end (MDIO command end wait error)			
Description	This function enables MAC IP access. *: Shorten the period from MAC IP access enablement to MAC IP access disablement (gerCP52_DisableMACIPAccess (Section 11.3.9 (2)gerCP52_DisableMACIPAccess) to the extent possible. (If the user uses interrupts, use the function with the interrupts disabled from MAC IP access enablement to MAC IP access disablement.) When the return value of this function is a value other than CP52_OK, the function calls gCP52_CallbackFatalError (Section 11.5(1) gCP52_CallbackFatalError) created by the user. Be sure to execute error processing in accordance with the error code.			

(2) gerCP52_DisableMACIPAccess

Function	MAC IP access disablement			
Call format	ERRCODE gerCP52_DisableMACIPAccess (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end			
Description	This function disables the MAC IP access.			

(3) gerCP52_WritePHY

Function	PHY internal register write			
Call format	ERRCODE gerCP52_WritePHY (ULONG ulPort, ULONG ulAddr, ULONG ulData)			
Argument	Name	Variable name	Description	I/O
	ULONG	ulPort	Port subject to register writing CP52_PORT1(0): PORT1 CP52_PORT2(1): PORT2	Input
	ULONG	ulAddr	PHY register address	Input
	ULONG	ulData	Data to be written to PHY	Input
Return value	CP52_OK: Normal end CP52_ERR: Abnormal end (MDIO command end wait error)			
Description	This function writes data to the PHY internal register in MDIO. *: Use this function during the period from gerCP52_EnableMACIPAccess (Section 11.3.9 (1)gerCP52_EnableMACIPAccess) to gerCP52_DisableMACIPAccess (Section 11.3.9 (2)gerCP52_DisableMACIPAccess). When the return value of this function is a value other than CP52_OK, the function calls gCP52_CallbackFatalError (Section 11.5(1) gCP52_CallbackFatalError) created by the user. Be sure to execute error processing in accordance with the error code.			

(4) gerCP52_ReadPHY

Function	PHY internal register read			
Call format	ERRCODE gerCP52_ReadPHY (ULONG ulPort, ULONG ulAddr, ULONG *ulData)			
Argument	Name	Variable name	Description	I/O
	ULONG	ulPort	Port subject to register reading CP52_PORT1(0): PORT1 CP52_PORT2(1): PORT2	Input
	ULONG	ulAddr	PHY register address	Input
	ULONG	*ulData	Data read from PHY	Output
Return value	CP52_OK: Normal end CP52_ERR: Abnormal end (MDIO command end wait error)			
Description	This function reads the PHY internal register in MDIO. *: Use this function during the period from gerCP52_EnableMACIPAccess (Section 11.3.9 (1)gerCP52_EnableMACIPAccess) to gerCP52_DisableMACIPAccess (Section 11.3.9 (2)gerCP52_DisableMACIPAccess). When the return value of this function is a value other than CP52_OK, the function calls gCP52_CallbackFatalError (Section 11.5(1) gCP52_CallbackFatalError) created by the user. Be sure to execute error processing in accordance with the error code.			

(5) gerCP52_CheckPHY

Function	PHY check processing			
Call format	ERRCODE gerCP52_CheckPHY(VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end			
Description	This function acquires the PHY link status.			

11.3.10 Transient reception

(1) gerCP52_MainReceiveTransient1

Function	Transient reception main processing 1			
Call format	ERRCODE gerCP52_MainReceiveTransient1 (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end			
Description	This function acquires the transient frames received by CP520.			

(2) gerCP52_MainReceiveTransient2

Function	Transient reception main processing 2			
Call format	ERRCODE gerCP52_MainReceiveTransient2 (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end			
Description	This function delivers the received transient frames acquired by gerCP52_MainReceiveTransient1 (Section 11.3.10 (1)gerCP52_MainReceiveTransient1) to the user program using gerCP52_CallbackReceivedTransient (Section 11.5(3)gerCP52_CallbackReceivedTransient).			

(3) gerCP52_EnableReceiveTransient

Function	Transient reception enable/disable setting for user reasons			
Call format	ERRCODE gerCP52_EnableReceiveTransient (BOOL blEnable)			
Argument	Name	Variable name	Description	I/O
	BOOL	blEnable	Reception enable/disable setting CP52_TRUE: Enable reception CP52_FALSE: Disable reception	Input
Return value	CP52_OK: Normal end			
Description	This function enables or disables transient reception for user reasons. When the return value of gerCP52_CallbackReceivedTransient created by the user is CP52_ERR, "Transient reception enable/disable setting for user reasons" is set to "Disable reception". Be sure to set reception to "Enable reception" using this function once reception becomes possible.			

(4) gblCP52_GetReceiveTransientStatus

Function	Status acquisition of transient reception enable/disable setting for user reasons			
Call format	BOOL gblCP52_GetReceiveTransientStatus (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	Status of reception enable/disable setting CP52_TRUE: Reception enabled CP52_FALSE: Reception disabled			
Description	This function acquires the status of transient reception enable/disable setting for user reasons.			

(5) gerCP52_SetMACAddressTableData

Function	Node information distribution data (MAC address table) setting			
Call format	ERRCODE gerCP52_SetMACAddressTableData (UCHAR uchSeqNumber, CP52_MACADDRESSDATA_T *pstMacAddrDat)			
Argument	Name	Variable name	Description	I/O
	UCHAR	uchSeqNumber	Sequential distribution number (value range: 1-7)	Input
	CP52_MACADDRESSDATA_T	*pstMacAddrDat	Information such as MAC address (MAC address table)	Input
Return value	CP52_OK: Normal end CP52_ERR_OUTOFRANGE: Station number out of range or sequential distribution number out of range			
Description	This function sets the information (MAC address table), such as the MAC address, acquired by node information distribution from the master station, and the sequential distribution number. *: Register the station number of the master station as 7DH. If CP52_FALSE is set by the initial value of Node information distribution request (No. 7 of "Table 11.3.1-2 CP52_UNITINIT_T List"), this function does not need to be called.			

The following describes the configuration of CP52_MACADDRESSDATA_T.

Table 11.3.10-1 CP52_MACADDRESSDATA_T List

No.	Member		Overview	Remarks
1	USHORT	usNodeNumber	Station number (1-120, Master station: 7DH)	-
2	UCHAR	uchTransientReceiveEnable	Transient reception function (CP52_ENABLE/CP52_DISABLE)	-
3	UCHAR	auchMacAddress[6]	MAC address	-

11.3.11 Transient request reception

(1) gerCP52_ReceivedMACAddressData

Function	Node information distribution frame receive processing			
Call format	ERRCODE gerCP52_ReceivedMACAddressData (const VOID* pvReceivedData, ULONG ulDataSize)			
Argument	Name	Variable name	Description	I/O
	const VOID*	pvReceivedData	Received data storage area	Input
	ULONG	ulDataSize	Received data size	Input
Return value	CP52_OK: Normal end CP52_ERR: Destination station number error or destination network number error in received data			
Description	This function creates the MAC address data of the other station using gerCP52_SetMACAddressTableData (Section 11.3.10(5)gerCP52_SetMACAddressTableData).			

(2) gerCP52_ReceivedStatisticInfoRequest

Function	Statistical information acquisition request frame receive processing			
Call format	ERRCODE gerCP52_ReceivedStatisticInfoRequest (VOID* pvSendFrame, ULONG* pulDataSize, const VOID* pvReceivedData, const UCHAR* puchSA)			
Argument	Name	Variable name	Description	I/O
	VOID*	pvSendFrame	Send frame	Output
	ULONG*	pulDataSize	Send data size	Output
	const VOID*	pvReceivedData	Received data storage area	Input
	const UCHAR*	puchSA	Send source node MAC address	Input
Return value	CP52_OK: Normal end CP52_ERR: Destination station number error or destination network number error in received data			
Description	This function creates Statistical information acquisition response frame using the received data specified in the argument.			

(3) gerCP52_ReceivedUnitInfoRequest

Function	Detailed node information acquisition request frame receive processing			
Call format	ERRCODE gerCP52_ReceivedUnitInfoRequest (VOID* pvSendFrame, ULONG* pulDataSize, const VOID* pvReceivedData, const UCHAR* puchSA)			
Argument	Name	Variable name	Description	I/O
	VOID*	pvSendFrame	Send frame	Output
	ULONG*	pulDataSize	Send data size	Output
	const VOID*	pvReceivedData	Received data storage area	Input
	const UCHAR*	puchSA	Send source node MAC address	Input
Return value	CP52_OK: Normal end CP52_ERR: Destination station number error or destination network number error in received data			
Description	This function creates Detailed node information acquisition response frame using the received data specified in the argument.			

(4) gerCP52_ReceivedOptionInfoRequest

Function	Option information acquisition request frame receive processing			
Call format	ERRCODE gerCP52_ReceivedOptionInfoRequest (VOID* pvSendFrame,ULONG* pulDataSize,const VOID* pvReceivedData,const UCHAR* puchSA,const USHORT usSupportFunction)			
Argument	Name	Variable name	Description	I/O
	VOID*	pvSendFrame	Send frame	Output
	ULONG*	pulDataSize	Send data size	Output
	const VOID*	pvReceivedData	Received data storage area	Input
	const UCHAR*	puchSA	Send source node MAC address	Input
	const USHORT	usSupportFunction	Option function support	Input
Return value	CP52_OK: Normal end CP52_ERR: Destination station number error or destination network number error in received data			
Description	This function creates Option information acquisition response frame using the received data specified in the argument.			

(5) gerCP52_ReceivedSelectInfoRequest

Function	Selected station information acquisition request frame receive processing			
Call format	ERRCODE gerCP52_ReceivedSelectInfoRequest (VOID* pvSendFrame,ULONG* pulDataSize,const VOID* pvReceivedData,const UCHAR* puchSA,const VOID* pvCP52TLedInfo)			
Argument	Name	Variable name	Description	I/O
	VOID*	pvSendFrame	Address of send frame	Output
	ULONG*	pulDataSize	Send data size	Output
	const VOID*	pvReceivedData	Received data storage area	Input
	const UCHAR*	puchSA	Send source node MAC address	Input
	const VOID*	pvCP52TLedInfo	Own station LED information	Input
Return value	CP52_OK: Normal end CP52_ERR: Destination station number error or destination network number error in received data			
Description	This function creates Selected station information acquisition response frame using the received data specified in the argument.			

(6) gerCP52_ReceivedContactTestRequest

Function	Communication test request frame receive processing			
Call format	ERRCODE gerCP52_ReceivedContactTestRequest (VOID* pvSendFrame,ULONG* pulDataSize,const VOID* pvReceivedData,const UCHAR* puchSA)			
Argument	Name	Variable name	Description	I/O
	VOID*	pvSendFrame	Send frame	Output
	ULONG*	pulDataSize	Send data size	Output
	const VOID*	pvReceivedData	Received data storage area	Input
	const UCHAR*	puchSA	Send source node MAC address	Input
Return value	CP52_OK: Normal end CP52_ERR: Destination station number error or destination network number error in received data			
Description	This function creates Communication test response frame using the received data specified in the argument.			

(7) gerCP52_ReceivedCableTestRequest

Function	Cable test request frame receive processing			
Call format	ERRCODE gerCP52_ReceivedCableTestRequest (VOID* pvSendFrame,ULONG* pulDataSize,const VOID* pvReceivedData,const UCHAR* puchSA)			
Argument	Name	Variable name	Description	I/O
	VOID*	pvSendFrame	Send frame	Output
	ULONG*	pulDataSize	Send data size	Output
	const VOID*	pvReceivedData	Received data storage area	Input
	const UCHAR*	puchSA	Send source node MAC address	Input
Return value	CP52_OK: Normal end CP52_ERR: Destination station number error or destination network number error in received data			
Description	This function creates Cable test response frame using the received data specified in the argument.			

(8) gerCP52_ReceiveRemoteResetRequest

Function	SLMP remote reset request frame receive processing			
Call format	ERRCODE gerCP52_ReceiveRemoteResetRequest (VOID* pvSendFrame,ULONG* pulDataSize,const VOID* pvReceivedData,const UCHAR* puchSA)			
Argument	Name	Variable name	Description	I/O
	VOID*	pvSendFrame	Send frame	Output
	ULONG*	pulDataSize	Send data size	Output
	const VOID*	pvReceivedData	Received data storage area	Input
	const UCHAR*	puchSA	Send source node MAC address	Input
Return value	CP52_OK: Normal end CP52_ERR: Destination station number error or destination network number error in received data			
Description	This function checks if the station number and network number of the received SLMP remote reset response frame is within the set range. A response frame is not sent when the SLMP remote reset request is normally received.			

(9) gCP52_SetSlmpError_Response

Function	SLMP error response frame creation processing			
Call format	VOID gCP52_SetSlmpError_Response (VOID* pvSendFrame,ULONG* pulDataSize, const VOID* pvReceivedData,const UCHAR* puchSA,USHORT usFinCode)			
Argument	Name	Variable name	Description	I/O
	VOID*	pvSendFrame	Send frame	Output
	ULONG*	pulDataSize	Send data size	Output
	const VOID*	pvReceivedData	Received data storage area	Input
	const UCHAR*	puchSA	Send source node MAC address	Input
	USHORT	usFinCode	End code	
Return value	None			
Description	This function creates SLMP error response frame. The function stores the argument (usFinCode) in the end code of the created response frame.			

(10) gerCP52_ErrCheckReqFieldNetworkReceived

Function	CC-Link IE Field specific request receive frame error check processing			
Call format	ERRCODE gerCP52_ErrCheckReqFieldNetworkReceived (const VOID* pvReceivedData)			
Argument	Name	Variable name	Description	I/O
	const VOID*	pvReceivedData	Received data storage area	Input
Return value	CP52_OK: Normal end CP52_ERR: Destination station number error or destination network number error in received data			
Description	This function checks if the destination station number and network number of the received CC-Link IE Field specific request frame is within the set range.			

(11) gusCP52_ErrCheckReqSlmpReceived

Function	SLMP request receive frame error check processing			
Call format	USHORT gusCP52_ErrCheckReqSlmpReceived (const VOID* pvReceivedData)			
Argument	Name	Variable name	Description	I/O
	const VOID*	pvReceivedData	Received data storage area	Input
Return value	CP52_SLMP_FINCODE_OK: Normal (0000H) Other than above: Destination station number error or destination network number error in received data			
Description	This function checks if the destination station number and network number of the received SLMP request frame is within the set range.			

11.3.12 Transient send frame header creation

(1) gerCP52_SetEtherCcieHeader

Function	MAC+CCIE header creation processing			
Call format	ERRCODE gerCP52_SetEtherCcieHeader (const UCHAR* puchSndMac,const UCHAR* puchMyMac, UCHAR uchFrameClassification,UCHAR uchDataClassification,CP52_NONCICLIC_FRAME_T* pstCOMMON)			
Argument	Name	Variable name	Description	I/O
	const UCHAR*	puchSndMac	Destination MAC address	Input
	const UCHAR*	puchMyMac	Own MAC address	Input
	UCHAR	uchFrameClassification	Frame type	Input
	UCHAR	uchDataClassification	Data type	Input
	CP52_NONCICLIC_FRAME_T*	pstCOMMON	Address of created MAC + CCIE header For details, refer to Appendix 1.1 "Common format".	Output
Return value	Return value of erCP52T_TxFrame_CreateEtherCcieHeader (CP52_OK: Normal end only)			
Description	This function creates MAC header and CCIE header for pstCOMMON by calling erCP52T_TxFrame_CreateEtherCcieHeader.			

(2) gerCP52_SetTransient1Header

Function	Transient1 header creation processing			
Call format	ERRCODE gerCP52_SetTransient1Header (USHORT usDataSubClassification,USHORT usTransientDataSize, CP52_TRAN1_HEAD_T* pstHEAD)			
Argument	Name	Variable name	Description	I/O
	USHORT	usDataSubClassification	Data sub-type	Input
	USHORT	usTransientDataSize	Size of transient data	Input
	CP52_TRAN1_HEAD_T*	pstHEAD	Address of created Transient1 header For details, refer to Appendix 1.2 "Transient1 frame".	Output
Return value	Return value of erCP52T_TxFrame_CreateTransient1Header (CP52_OK: Normal end, CP52_Error: Error in argument)			
Description	This function creates Transient1 header for pstHEAD by calling erCP52T_TxFrame_CreateTransient1Header.			

(3) gerCP52_SetRequestSlmpHeader

Function	SLMP request header creation processing			
Call format	ERRCODE gerCP52_SetRequestSlmpHeader (CP52_SLMP_REQUSET_SETTING_T* pstSlmpReqSetting, CP52_SLMP_REQUEST_FRAME_T* pstSlmpExHead, ULONG* pulAllDataSize,USHORT* pusReqSerialNo)			
Argument	Name	Variable name	Description	I/O
	CP52_SLMP_REQUSET_SETTING_T*	pstSlmpReqSetting	Target station setting For details, refer to "Table 11.3.12-1 CP52_SLMP_REQUSET_SETTING_T List".	Input
	CP52_SLMP_REQUEST_FRAME_T *	pstSlmpExHead	Address of created Transient2 + SLMP header to be created For details, refer to "Table 11.3.12-2 CP52_SLMP_REQUEST_FRAME_T List".	Output
	ULONG*	pulAllDataSize	Entire SLMP data size	Output
	USHORT*	pusReqSerialNo	Serial number	Output
Return value	Return value of gerCP52T_TxFrame_CreateRequestSlmpHeader (CP52_OK: Normal end, CP52_Error: Error in argument)			
Description	This function creates Transient2 header + SLMP header (for request) for pstSlmpExHead by calling erCP52T_TxFrame_CreateRequestSlmpHeader.			

Table 11.3.12-1 CP52_SLMP_REQUSET_SETTING_T List

No.	Member		Description
1	USHORT	usConectInfo	Target station type number
2	USHORT	usNwNo	Target station network number
3	UCHAR	uchNode	Target station number
4	USHORT	usL	Data length
5	USHORT	usCommand	Command
6	USHORT	usSubCommand	Subcommand

Table 11.3.12-2 CP52_SLMP_REQUEST_FRAME_T List

No.	Member		Description
1	CP52_CCLINK_HEAD_T	stCCLinkHead	Transient2 header information*1
2	CP52_SLMP_HEAD_T	stSlmpHead	SLMP header information*2
3	USHORT	usTimer	Monitoring timer*2
4	USHORT	usCommand	Command*2
5	USHORT	usSubCommand	Subcommand*2

*1: For details, refer to Appendix 1.3 "CC-Link compatible transient frame".

*2: For details, refer to Appendix 1.4 "SLMP frame".

(4) gerCP52_SetResponseSlmpHeader

Function	SLMP response header creation processing			
Call format	ERRCODE gerCP52_SetResponseSlmpHeader (const CP52_SLMP_REQUEST_FRAME_T* pstReqSlmpExHead, USHORT usSlmpDataSize,CP52_SLMP_RESPONSE_FRAME_T* pstSlmpExHead)			
Argument	Name	Variable name	Description	I/O
	CP52_SLMP_REQUEST_FRAME_T *	pstReqSlmpExHead	Received SLMP request frame For details, refer to "Table 11.3.12-3 CP52_SLMP_RESPONSE_FRAME_T List".	Input
	ULONG	usSlmpDataSize	Size of SLMP data area	Input
	CP52_SLMP_RESPONSE_FRAME_T *	pstSlmpExHead	Created Transient2 + SLMP header For details, refer to "Table 11.3.12-3 CP52_SLMP_RESPONSE_FRAME_T List".	Output
Return value	Return value of erCP52T_TxFrame_CreateResponseSlmpHeader (CP52_OK: Normal end, CP52_Error: Error in argument)			
Description	This function creates Transient2 header + SLMP header (for response) for pstSlmpExHead by calling erCP52T_TxFrame_CreateResponseSlmpHeader.			

Table 11.3.12-3 CP52_SLMP_RESPONSE_FRAME_T List

No.	Member		Description
1	CP52_CCLINK_HEAD_T	stCCLinkHead	Transient2 header information*1
2	USHORT	usRSTS	Return status*1
3	CP52_SLMP_HEAD_T	stSlmpHead	SLMP header information*2
4	USHORT	usFinCode	End code*2

*1: For details, refer to Appendix 1.3 "CC-Link compatible transient frame".

*2: For details, refer to Appendix 1.4 "SLMP frame".

11.3.13 Transient send

(1) gerCP52_GetUnitInformation

Function	Unit information acquisition			
Call format	ERRCODE gerCP52_GetUnitInformation (CP52_UNITINFO_T *pstUnitInfo, CP52_UNITNETWORKSETTING_T *pstUnitNetworkSetting)			
Argument	Name	Variable name	Description	I/O
	CP52_UNITINFO_T	*pstUnitInfo	Unit information	Output
	CP52_UNITNETWORKSETTING_T	*pstUnitNetworkSetting	Network operation setting	Output
Return value	CP52_OK: Normal end			
Description	This function acquires the setting information of its own station. The acquired setting information is used when creating Detailed node information acquisition response frame.			

The following describes the configuration of CP52_UNITNETWORKSETTING_T.

Table 11.3.13-1 CP52_UNITNETWORKSETTING_T List

No.	Member		Overview
1	ULONG	ulFrameSendCount	No. of sends during token hold
2	ULONG	ulFrameSendInterval	Frame send interval
3	ULONG	ulTokenSendCount	No. of token sends

(2) gusCP52_GetNodeID

Function	Node ID acquisition			
Call format	USHORT gusCP52_GetNodeID (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	Node ID			
Description	This function acquires the node ID. The acquired node ID is used when performing transient send.			

(3) gerCP52_GetMulticastMACAddress

Function	Multicast MAC address acquisition			
Call format	ERRCODE gerCP52_GetMulticastMACAddress (UCHAR *puchMACAddr)			
Argument	Name	Variable name	Description	I/O
	UCHAR	*puchMACAddr	Multicast address When 13-34-56-78-90-AB is set, the following addresses are returned: puchMACAddr[0]: 13H puchMACAddr[1]: 34H puchMACAddr[2]: 56H puchMACAddr[3]: 78H puchMACAddr[4]: 90H puchMACAddr[5]: ABH	Output
Return value	CP52_OK: Normal end CP52_ERR: Abnormal end [The multicast MAC address cannot be acquired due to no data link (data link disconnected).]			
Description	This function acquires the multicast MAC address. The acquired multicast MAC address is used as the destination address when transient send is performed to all stations connected to the network.			

(4) gerCP52_GetUnicastMACAddress

Function	Unicast MAC address acquisition			
Call format	ERRCODE gerCP52_GetUnicastMACAddress (USHORT usNodeNumber,UCHAR *puchMACAddr)			
Argument	Name	Variable name	Description	I/O
	USHORT	usNodeNumber	Station number (value range: 1-120, master station: 7DH)	Input
	UCHAR	*puchMACAddr	Unicast address When 12-34-56-78-90-AB is set, the following addresses are returned: puchMACAddr[0]: 12H puchMACAddr[1]: 34H puchMACAddr[2]: 56H puchMACAddr[3]: 78H puchMACAddr[4]: 90H puchMACAddr[5]: ABH	Output
Return value	CP52_OK: Normal end CP52_ERR_NOENTRY: No entry CP52_ERR_OUTOFRANGE: Station number out of range			
Description	This function acquires the unicast MAC address corresponding to the station number from Node information distribution frame received from the master station. Set the master station number to 7DH. *: When there is no data link (data link disconnected), the unicast MAC address cannot be acquired (the return value becomes CP52_ERR_NOENTRY).			

(5) gerCP52_GetSendTransientBuffer

Function	Transient send buffer acquisition			
Call format	ERRCODE gerCP52_GetSendTransientBuffer (USHORT usSize, VOID** ppvSendBuffAddr, UCHAR *puchSendBuffNo, UCHAR *puchConnectionInfo)			
Argument	Name	Variable name	Description	I/O
	USHORT	usSize	Send data size excluding DCS/FCS	Input
	VOID	**ppvSendBuffAddr	Transient send buffer address	Output
	UCHAR	*puchSendBuffNo	Transient send buffer number	Output
	UCHAR	*puchConnectionInfo	Transient connection information	Output
Return value	CP52_OK: Normal end (transient send buffer acquired) CP52_ERR: Abnormal end (transient send buffer acquisition error)			
Description	This function inquires whether or not there is space in the transient send area for send of the "send data size", and returns the following information if there is space: ・ Transient send buffer address ・ Transient send buffer number ・ Transient connection information *: In the following case, transient send cannot be performed and the process ends in error (CP52_ERR: Abnormal end): ・ When there is no data link (data link disconnected) ・ When the send data size is greater than 1510 bytes When you want to perform transient send, execute the following: ・ Acquire the transient send buffer number using this function. ・ Store the send data in the acquired transient send buffer. ・ Request transient send using gerCP52_RequestSendingTransient (Section 11.3.13 (6)gerCP52_RequestSendingTransient).			

(6) gerCP52_RequestSendingTransient

Function	Transient send request			
Call format	ERRCODE gerCP52_RequestSendingTransient (UCHAR uchSendBuffNo, USHORT usSize)			
Argument	Name	Variable name	Description	I/O
	UCHAR	uchSendBuffNo	Transient send buffer number	Input
	USHORT	usSize	Send data size excluding DCS/FCS	Input
Return value	CP52_OK: Normal end CP52_ERR: Abnormal end (transient send request error)			
Description	This function specifies send to the transient send buffer number acquired by gerCP52_GetSendTransientBuffer (Section 11.3.13 gerCP52_GetSendTransientBuffer). Before executing this function, perform the following: ・ Acquire the transient send buffer using gerCP52_GetSendTransientBuffer. ・ Store the send data in the acquired transient send buffer. *: In the following case, transient send cannot be performed and the process ends in error (CP52_ERR: Abnormal end): ・ When there is no data link (data link disconnected) Any error that occurs after send is requested by this function is notified by the return value of gerCP52_MainSendTransient (Section 11.3.13 (7)gerCP52_MainSendTransient). Set the send data size to the same size as the value specified in gerCP52_GetSendTransientBuffer.			

(7) gerCP52_MainSendTransient

Function	Transient send main processing			
Call format	ERRCODE gerCP52_MainSendTransient (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end			
Description	This function acquires the transient send end result. This function calls gerCP52_CallbackTransientSendingComplete (Section 11.5(4)gerCP52_CallbackTransientSendingComplete) to issue a notification regarding the status (send result) of the target send descriptor.			

11.3.14 Hardware test

(1) gerCP52_IEEETest

Function	IEEE 802.3ab compliance test			
Call format	ERRCODE gerCP52_IEEETest (USHORT usMode)			
Argument	Name	Variable name	Description	I/O
	USHORT	usMode	IEEE 802.3ab compliance test mode CP52_IEEE_MODE1(1): MODE1 CP52_IEEE_MODE2(2): MODE2 CP52_IEEE_MODE3(3): MODE3 CP52_IEEE_MODE4(4): MODE4 CP52_IEEE_END(5): Test end	Input
Return value	CP52_OK: Normal end CP52_ERR: Abnormal end			
Description	This function sets the waveform output for test mode in PHY in accordance with the IEEE 802.3ab compliance test mode of the argument. *: When the return value of this function is a value other than CP52_OK, the function calls gCP52_CallbackFatalError (Section 11.5(1) gCP52_CallbackFatalError) created by the user. Be sure to execute error processing in accordance with the error code.			

(2) gerCP52_InitializeLoopBackTest

Function	Loopback communication test initialization			
Call format	ERRCODE gerCP52_InitializeLoopBackTest (VOID)			
Argument	Name	Variable name	Description	I/O
	-	-	-	-
Return value	CP52_OK: Normal end CP52_ERR: Abnormal end			
Description	This function performs initialization for executing the loopback communication test. *: When the return value of this function is a value other than CP52_OK, the function calls gCP52_CallbackFatalError (Section 11.5(1) gCP52_CallbackFatalError) created by the user. Be sure to execute error processing in accordance with the error code.			

(3) gerCP52_ExternalLoopBackTest

Function	Loopback communication test			
Call format	ERRCODE gerCP52_ExternalLoopBackTest (ULONG ulPort)			
Argument	Name	Variable name	Description	I/O
	ULONG	ulPort	Test target port CP52_PORT1(0): PORT1 CP52_PORT2(1): PORT2	Input
Return value	CP52_OK: Normal end CP52_ERR: Abnormal end			
Description	This function sends a frame from the test target port specified in the argument, and verifies the received result using the other port. When implementing this test, connect Ethernet PORT 1 and Ethernet PORT 2 using an Ethernet cable. *: When the return value of this function is a value other than CP52_OK, the function calls gCP52_CallbackFatalError (Section 11.5(1) gCP52_CallbackFatalError) created by the user. Be sure to execute error processing in accordance with the error code.			

11.4 CP520 Driver Callback Function List

The following describes the CP520 driver callback functions.

Table 11.4-1 CP520 Driver Callback Function List

No.	Function Classification	Function Name	Function Type	Overview
1	Error processing	gCP52_CallbackFatalError	VOID	CP520 fatal error acquisition
2	Own station status acquisition	gerCP52_CallbackCommandFromMaster	ERRCODE	Command acquisition from master station
3	Transient send/receive	gerCP52_CallbackReceivedTransient	ERRCODE	Received transient frame acquisition
4		gerCP52_CallbackTransientSendingComplete	ERRCODE	Transient send completion status acquisition

11.5 CP520 Driver Callback Function Details

The internal processing of CP520 driver callback functions needs to be customized by the user.
The following describes the details of the CP520 driver callback functions.

(1) gCP52_CallbackFatalError

Function	CP520 fatal error acquisition			
Call format	VOID gCP52_CallbackFatalError (ULONG ulErrorCode, ULONG ulErrorInfo)			
Argument	Name	Variable name	Description	I/O
	ULONG	ulErrorCode	Fatal error code	Input
	ULONG	ulErrorInfo	Fatal error information (Address of function when error occurred.)	Input
Return value	None			
Description	This function acquires CP520 fatal errors. The CP520 driver calls this function when a CP520 fatal error is detected. The error code detected by the CP520 driver is not notified to other stations. Function internal processing is freely implemented by the vendor.			

Table 11.5-1 List of Fatal Error Codes of gCP52_CallBackFatalError Function

Fatal Error Code (ulErrorCode)	Fatal Error Information (ulErrorInfo)	Fatal Error Description	Action
D52A	Driver internal call source function Address of erCP52D_MDIO_WaitCommandComplete	Communication LSI error	・ The error is most likely a malfunction caused by noise, etc. Check the distance between lines and cables as well as device grounding, and implement noise countermeasures accordingly. ・ Implement a hardware test. If the error occurs again, most likely the hardware is faulty.
D52B	Driver internal call source function Address of erCP52D_ResetMAC	Communication LSI error	
D52C	Driver internal call source function Address of gerCP52D_StartRing	Communication LSI error	

(2) gerCP52_CallbackCommandFromMaster

Function	Command acquisition from master station			
Call format	ERRCODE gerCP52_CallbackCommandFromMaster (ULONG pulCommand)			
Argument	Name	Variable name	Description	I/O
	ULONG	pulCommand	Command status from master station For details, refer to "Table 11.5-2 ulCommand List".	Input
Return value	CP52_OK: Normal end			
Description	This function acquires commands by Parameter frame reception from the master station. The CP520 driver calls this function when Parameter frame is received from the master station. Function internal processing is freely implemented by the user.			

The following describes the configuration of ulCommand.

Table 11.5-2 ulCommand List

No.	Bit	Overview	Description
1	b0	Cyclic transmission stop instruction (station number out of range)	1b: Stop instruction 0b: No stop instruction
2	b1	Cyclic transmission stop instruction (reserved station setting)	1b: Stop instruction 0b: No stop instruction
3	b2	Cyclic transmission stop instruction (master station instruction)	1b: Stop instruction 0b: No stop instruction
4	b3	Cyclic transmission stop instruction (station number duplication)	1b: Stop instruction 0b: No stop instruction
5	b15-4	Reserved	-
6	b16	Station type invalid (own station type does not match station type specified by master station)	1b: Station type invalid 0b: Station type valid
7	b17	Specified size invalid*1	1b: Specified size invalid 0b: Specified size valid
8	b31-18	Reserved	-

*1: The cyclic transmission size specified by the master station is greater than the allowable maximum size (size specified by gerCP52_Initialize (Section 11.3.1gerCP52_Initialize) for own station cyclic transmission.

(3) gerCP52_CallbackReceivedTransient

Function	Received transient frame acquisition			
Call format	ERRCODE gerCP52_CallbackReceivedTransient (VOID *pvRcv, USHORT usFrameSize)			
Argument	Name	Variable name	Description	I/O
	VOID	*pvRcv	Reception buffer	Input
	USHORT	usFrameSize	Frame size excluding FCS	Input
Return value	CP52_OK: Normal end CP52_ERR: Abnormal end			
Description	This function acquires received transient frames. The CP520 driver calls this function when a transient frame is received. Function internal processing is freely implemented by the user. *: Set the start address of the reception buffer in increments of 4 bytes (0 or multiple of 4). When the return value is a value other than CP52_OK, "Transient reception enable/disable setting for user reasons" is set to "Disable reception" Be sure to set transient reception for users reasons to "Enable reception" by calling gerCP52_EnableReceiveTransient (Section 11.3.10(3) gerCP52_EnableReceiveTransient) once reception becomes possible.			

(4) gerCP52_CallbackTransientSendingComplete

Function	Transient send completion status acquisition			
Call format	ERRCODE gerCP52_CallbackTransientSendingComplete (UCHAR uchSendBuffNo, ERRCODE erSendStatus)			
Argument	Name	Variable name	Description	I/O
	UCHAR	uchSendBuffNo	Transient send buffer number	Input
	ERRCODE	erSendStatus	Status of target transient send buffer(send result) CP52_OK: Transient send normal completion CP52_ERR: Transient send abnormal completion	Input
Return value	CP52_OK: Normal end			
Description	This function acquires the send status (send result) of the transient send buffer. The CP520 driver calls this function when send of a transient frame ends. Function internal processing is freely implemented by the user.			

12 LINK DEVICE SYSTEM AREA

A part of link devices in a slave station connected to CC-Link IE Field Network can be defined as a system area. A system area is used to notify other stations of the status of the own station and to instruct operation from the master station to the own station.

Defining a part of link devices as a system area is optional. To define a system area, assign the bits of link devices as indicated in "Table 12-1 System Area Bit Assignments (Example)".
The following table shows an example of defining a system area for the remote input (RX) and the remote output (RY). When defining a system area for the remote registers (RWr, RWw), replace RX with RWw and RY with RWw.

Table 12-1 System Area Bit Assignments (Example)

Bit	Name	Bit	Name
RX(S+0)	Reserved	RY(S+0)	Reserved
RX(S+1)		RY(S+1)	
RX(S+2)		RY(S+2)	
RX(S+3)		RY(S+3)	
RX(S+4)		RY(S+4)	
RX(S+5)		RY(S+5)	
RX(S+6)		RY(S+6)	
RX(S+7)	Warning status flag	RY(S+7)	
RX(S+8)	Initial data processing request flag	RY(S+8)	Initial data processing complete flag
RX(S+9)	Initial data setting complete flag	RY(S+9)	Initial data setting request flag
RX(S+A)	Error status flag	RY(S+A)	Error reset request flag
RX(S+B)	Remote ready	RY(S+B)	Reserved
RX(S+C)	Reserved	RY(S+C)	
RX(S+D)		RY(S+D)	
RX(S+E)		RY(S+E)	
RX(S+F)		RY(S+F)	

S: Start number of system area

This section describes the details of each bit in the system area, using the remote input (RX) and the remote output (RY) as an example.

(1) Remote ready: RX(S+B)

This bit indicates that data can be sent and received between the master station and the own station.

Turn on the bit after the CP520 application product is powered on or reset.

Turn off the bit when data cannot be sent or received between the master station and the own station due to Error status flag.

Note that leave the bit on when Warning status flag is on.

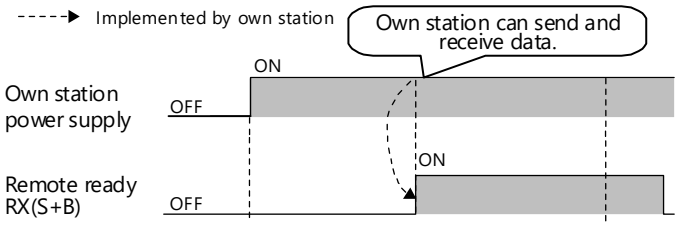


Figure 12.1-1 Timing Chart: Remote ready

(2) Initial data processing request flag: RX(S+8), Initial data processing complete flag: RY(S+8)

These bits are used to request initial data processing from the own station to the master station after the CP520 application product is powered on or reset.

After the initial data processing completes, turn on Remote ready.

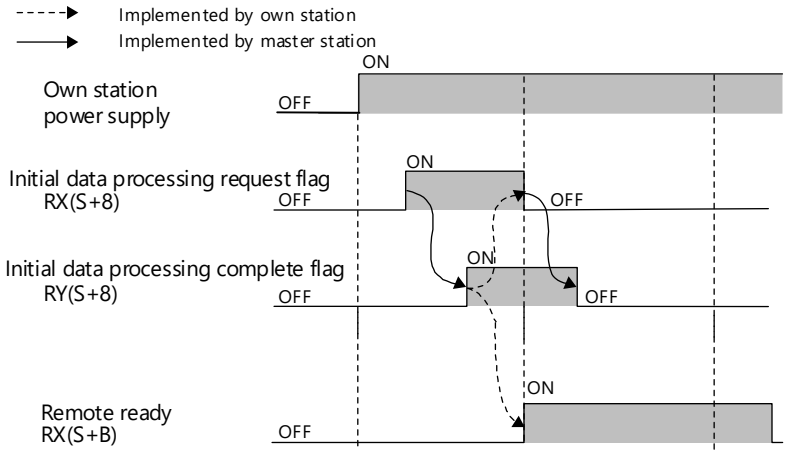


Figure 12.1-2 Timing Chart: Initial Data Processing Request/Complete Flag

(3) Initial data setting complete flag: RX(S+9), Initial data setting request flag: RY(S+9)
These bits are used to request initial data setting from the master station to the own station.
After the initial data are set, turn on Remote ready.

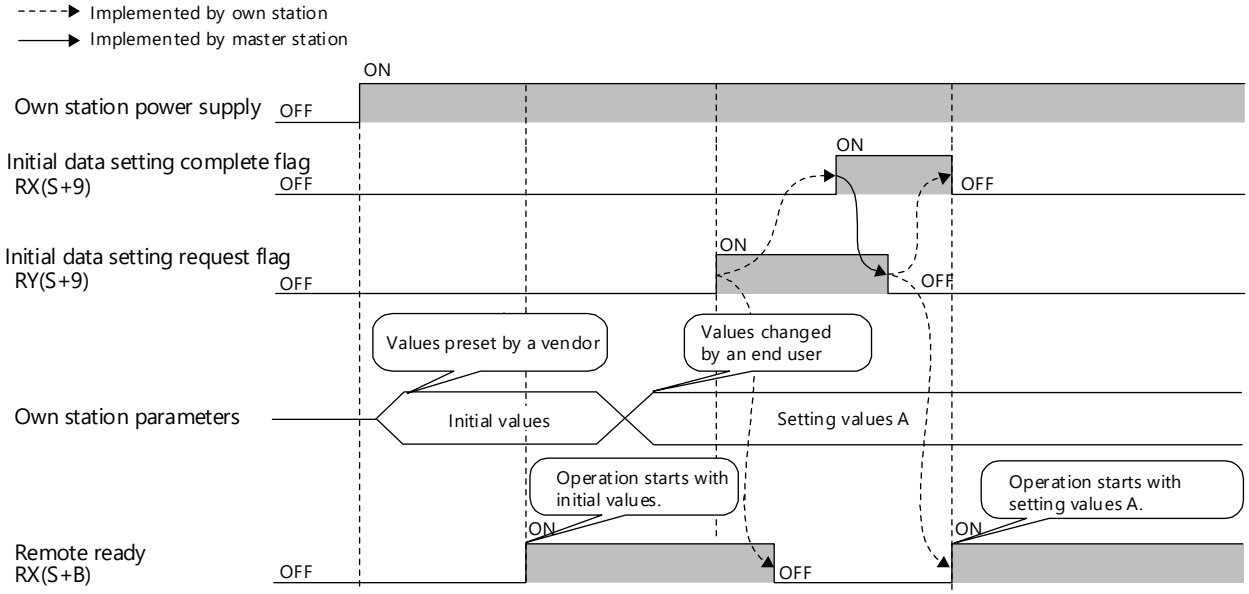


Figure 12.1-3 Timing Chart: Initial Data Setting Complete/Request Flag

(4) Implementation of Initial data processing request/complete flag and Initial data setting complete/request flag
When these flags are implemented, turn on Remote ready after both the initial data processing and the initial data setting processing complete.

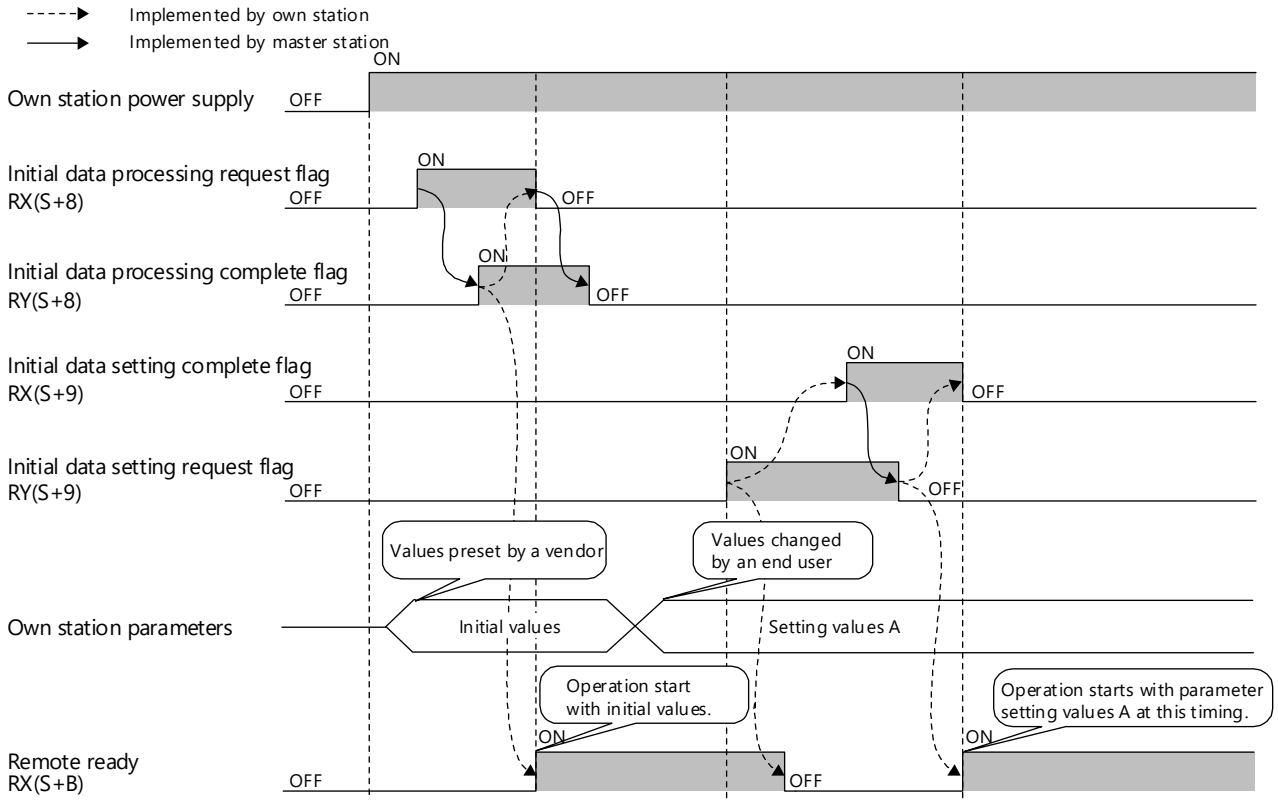


Figure 12.1-4 Timing Chart: Initial Data Processing and Setting

(5) Error status flag: RX(S+A), Error reset request flag: RY(S+A)

These bits are used to notify or clear a moderate/major error of the own station. (The station can no longer continue its operation.)

Turn on Error status flag when a moderator/major error occurs in the own station.

The master station clears the error and turns on Error reset request flag.

The own station turns off Error status flag and clears the error code storage area.

Turn off Remote ready from error occurrence to error clear.

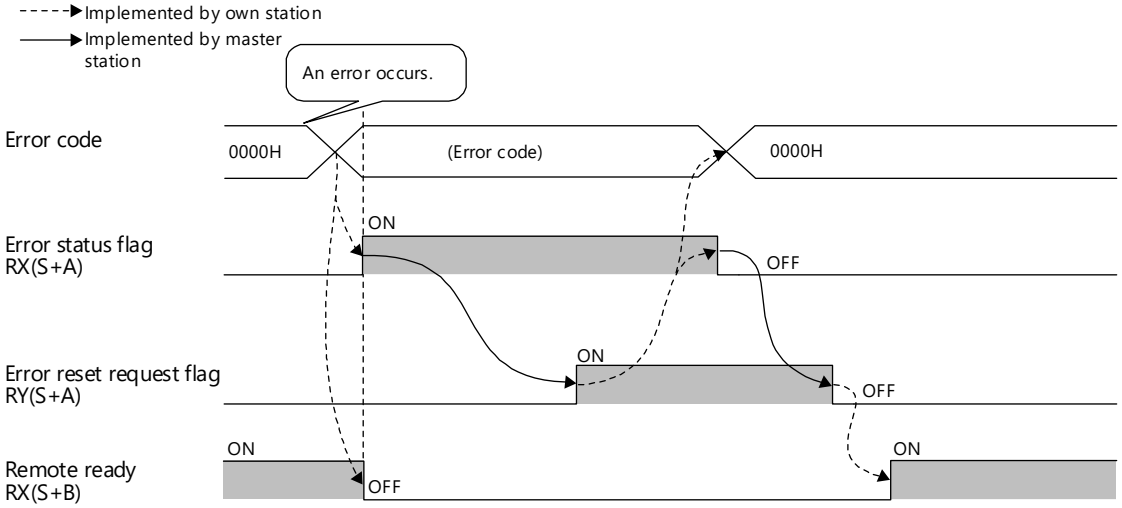


Figure 12.1-5 Timing Chart: Error Status Flag, Error Reset Request Flag

(6) Warning status flag: RX(S+7)

This bit is used to notify a minor error of the own station. (The station can continue its operation.)

Turn on this flag when a minor error occurs in the own station.

When the master station eliminates the error cause, the own station clears the warning code and turn off this flag.

Leave Remote ready on from warning occurrence to warning clear.

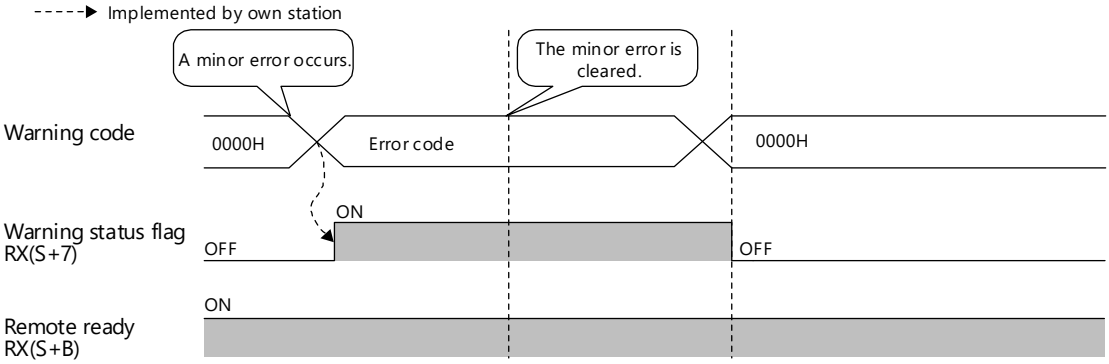


Figure 12.1-6 Timing Chart: Warning Status Flag

13 TROUBLESHOOTING

This chapter provides the questions asked from users[*1] to the Mitsubishi Electric Open System Center and the corresponding answers in the form of troubleshooting. The questions and answers are common to CP220 and CP520. Refer to this information during development.

*1: Users refer to manufacturers developing products using the following:

- CC-Link IE Field Network Intelligent Device Station Communication LSI CP220
- CC-Link IE Field Network Remote Device Station Communication LSI CP220

13.1 Hardware Design

(1) Parts

No.	Question	Answer
1	I have heard that production of components described in the "Component List" of this manual will be discontinued. What are the alternative components?	The components in the "Component List" are not specified components. Note, however, that the following components need to be selected carefully. Select them referring to Section 7.3.1 "Component selection precautions". • RJ-45 connector • Pulse transformer • 25 MHz crystal oscillator • 2.097152 MHz crystal oscillator
2	Is inclusion of a network number and station number hardware switch required by the conformance test?	The conformance test implemented by the CC-Link Partner Association does not include switch related test items, and therefore switch selection is optional.

(1) Initial processing

No.	Question	Answer
1	Does the written MAC address need to be different for each product? Is it OK to use the same MAC address for products with the same model name?	A different MAC address needs to be written for each product. Write a different MAC address even for products with the same model name.
2	What do the terms "network" and "controller" mean?	The meaning of each term is as follows. Network: A communication section comprising CP520 and the peripheral circuit in the own station Controller: A functional section which is unique to the vendor (I/O section, sensor section, temperature adjustment section, etc.) in the own station

(2) Version and model type

No.	Question	Answer
1	What should I set as the network model type and controller model type?	Set the model type specified by the CC-Link Partner Association.

(3) Others

No.	Question	Answer
1	An error occurred during the loopback test. What should I check?	Check the following three points: ・ The external WDT detection circuit is connected to WDTIL of CP520. (During normal periods: High) ・ When the external WDT detection circuit has not detected an error, WDTIL is not "Low". ・ When the CP520 internal WDT is used, the gerCP52_ResetWDT function is periodically called to reset the CP520 internal WDT.
2	Can a part of RX/RY be defined as system areas?	Yes, a part of RX/RY can be defined as system areas. For details, refer to Chapter 12 "LINK DEVICE SYSTEM AREA" and "CC-Link IE Field Network Specification (Device Profile)" (BAP-C2005ENG-007).

(1) Specifications

No.	Question	Answer
1	When the master station and slave stations send multiple frames to each other, Node information distribution frame is distributed twice during the same cycle from the master station. Is this correct according to the specifications?	Yes, that is correct. The master station sends Node information distribution frames twice during the refresh phase. Note that the frame is sent only once in high speed mode.
2	When a Transient1 frame is received from the master station, does the own station need to return a TransientAck frame at the timing of initial cyclic data?	Transient transmission is a communication method that does not guarantee punctuality. Therefore, the own station does not need to return a TransientAck frame during the initial cyclic transmission cycle after a Transient1 frame has been received. The transient transmission send/receive timing is not related with the cyclic transmission cycle.
3	Which should I define as an attribute in the Transient2 request frame, internal information or external information?	Define an attribute in the Transient2 request frame as desired. For example, for a Mitsubishi master/local module, the master/local module information is defined as internal information, and the controller (programmable controller CPU) information is defined as external information.
4	When accessing a word device in the memory area of a slave station from the master station using a Transient2 frame, what should I specify as the access code?	When accessing a word device of a slave station, for example, specify 04H as the access code to access any address of the slave station.
5	Is the method used to limit transient transmission (link scan unit limit method, node unit limit method) CP520 dependent? Does the CP520-side firmware need to be aware of the method?	The method is not CP520 dependent, but master station dependent. The CP520-side firmware does not need to be aware of the method.
6	How are SLMP frames configured?	A Transient2 header and an SLMP frame are stored in the data area of a Transient1 frame, and transmitted.
7	While 254 stations are connectable to a single network, the station numbers for Mitsubishi Electric products are set within the range of 1 to 120. Am I correct to interpret this as meaning 120 CC-Link IE Field Network compatible products are connectable to a single network, and the remaining station numbers are for Ethernet products connected via an Ethernet adapter module or the like?	No. According to the CC-Link IE Field Network specifications defined by the CC-Link Partner Association, 254 CC-Link IE Field Network compatible products are connectable. On the other hand, Mitsubishi Electric master station specifications allow connections of 120 CC-Link IE Field Network compatible products. Therefore, in the reference manual and sample codes, the number of connectable products is described as 120 maximum in accordance with the specifications of the Mitsubishi Electric master station.
8	I/O types include mixed (00H) and composite (11H). When using RX00 to RX3F for input and RY00 to RY1F for output, which I/O type should be set? When shall composite (11H) be set?	In this case, the I/O type is mixed (00H). Mixed: The input and output are mixed and the input and output use the same addresses (for example: RX00 to RX0F, RY00 to RY0F). Cases where the addresses partially overlap, such as in RX00 to RX3F, RY00 to RY1F are also included. Composite: The input and output are mixed and the input and output use the different addresses (for example: RX00 to RX07, RY08 to RY0F).
9	Under what conditions does the master station detect a slave station as a "cyclic transmission faulty station"?	The master station detects a slave station as a "cyclic transmission faulty station" under the following conditions: ・ The slave station does not send cyclic data. ・ The slave station sent a faulty MyStatus frame. At the same time, the master station turns on the bit, corresponding to the faulty station, of Data link status (each station) (SW00B0 to SW00B7).

(2) Others

No.	Question	Answer
1	How do I use transient transmission to access the memory area of a slave station from the master station?	Use a Transient2 memory read/write request frame, an SLMP memory read/write request frame, or the like.
2	Are there any commands that perform similar processing in Transient2 and SLMP frames? (For example, Transient2 memory read/write command and SLMP memory read/write command)	Yes, there are commands that perform similar processing. (For example, the Transient2 memory read/write command and the SLMP memory read/write command are similar.)
3	To set slave station parameters from GX Works2/GX Works3, is it necessary to implement SLMP frame send/receive processing?	Yes.
4	Is there a CC-Link IE Field dedicated protocol analyzer?	No, there is no CC-Link IE Field dedicated protocol analyzer. Use the general-purpose Ethernet protocol analyzer.
5	When I use the protocol analyzer to monitor line data, can I use a commercial hub?	Yes, a commercial hub can be used if the hub is equipped with a mirroring function. However, we recommend using the wiring components recommended by the CC-Link Partner Association for the actual use in a plant.

13.4 Performance and Functions

(1) Performance

No.	Question	Answer
1	I want to calculate the link scan time from the number of slaves connected. Is there a formula?	Refer to the "MELSEC-Q CC-Link IE Field Network Master/Local Module User's Manual" (SH-080917ENG).
2	How do I shorten the link scan time?	The link scan time can be shortened by reducing the following based on the link scan time calculation formula. ・ Number of link device points ・ Number of connected slave stations
3	What factors cause link scan time delays?	The link scan time is delayed by the following factors: ・ Number of RX/RY and RWw/RWr points set to each station ・ Number of connected slave stations ・ Clear/Hold setting of input data in network operation settings (in high speed mode only) ・ Transient transmission status ・ Disconnected/returned station status ・ Number of interrupt settings (condition check processing of interrupt request to programmable controller CPU) ・ Processing time between master station and submaster station when the submaster function is used
4	What is the extent of the link scan time difference between the cyclic transmission modes ("High Speed Mode" and "Normal Mode")?	Refer to the "MELSEC-Q CC-Link IE Field Network Master/Local Module User's Manual" (SH-080917ENG).
5	Is the best effort method "High Speed Mode"?	No. The best effort method is a control method applied when "Asynchronous" is set to the link scan mode setting under the network configuration settings with the "Constant link Scan" checkbox deselected using GX Works2/GX Works3. For link scan mode settings, refer to the "MELSEC-Q CC-Link IE Field Network Master/Local Module User's Manual" (SH-080917ENG).

(2) Function

No.	Question	Answer
1	When developing an intelligent device station, is it mandatory to implement the transient transmission client function in terms of product specifications?	No, it is not necessary to implement the client function.

13.5 Conformance Test

(1) IEEE 1000BASE-T compliance test

No.	Question	Answer
1	The compliance test includes test modes 1 to 4. To output the required waveforms, is it OK to execute the UserIEEETest function once? Or, do I need to create a loop?	The method of execution, such as executing the UserIEEETest function once or creating a loop, is not particularly specified. The gerCP52_IEEETest function called by the UserIEEETest function instructs PHY to output the waveforms 1 to 4 for the test mode specified in the argument. To output the test mode waveforms 1 to 4 based on desired timing, the gerCP52IEEETest function needs to be executed four times using different argument. The following two patterns are suggested to get the waveforms. ・ When the UserIEEETest function is executed once, call the function gerCP52_IEEETest four times. ・ When the UserIEEETest function is executed once, call the function gerCP52_IEEETest once. Repeat this processing four times. Note that the above patterns are only examples. Customize the UserIEEETest function in accordance with the specifications of your company.
2	What are the specifications of the gerCP52_IEEETest function?	The gerCP52_IEEETest function outputs waveforms in four modes on the basis of IEEE Std. 802.3 specifications.

(2) CSP+

No.	Question	Answer
1	Does REQUEST_TYPE in the CSP+ file define SLMPPDU only? Can the user newly define and register REQUEST_TYPE?	Yes, SLMPPDU only. The user cannot newly define the term.

13.6 Others

No.	Question	Answer
1	The module name appears as "Unknown" under "Network Status" on the CC-IE Field Diagnostics window of the engineering tool. How do I correctly display the name?	Upgrade the engineering tool to the latest version. For the version upgrade, please consult your local Mitsubishi representative. When a Mitsubishi Electric programmable controller is used as the master station, the following version is required. QJ71GF11-T2/LJ71GF11-T2: Serial number 17042 or later RJ71GF11-T2/RJ71EN71: Firmware version 06 or later

Appendix 1 Frame Format

The following table lists frames that are created during sending or analyzed during receiving by the user program. This section describes the formats of frames in the following table for your reference to create and analyze frames.

Table Appendix 1-1 List of Frames Created/Analyzed by User Program

No.	Frame Name	Frame Type (FType)		Data Type (DataType)		Data Sub-Type	
1	SLMP	22H	Transient1	05H	Network common	0002H	SLMP
2	CC-Link compatible transient	25H	Transient2	04H	CC-Link compatible	-	-
3	TransientAck	23H	TransientAck	*1	*1	*1	*1

*1: TransientAck sends an acknowledgement response using the data type and data sub-type of the received frame.

Appendix 1.1 Common format

The frames of the CC-Link IE Field Network are IEEE 802.3 Ethernet frame compatible. The following shows the format common to the frames of the CC-Link IE Field Network.

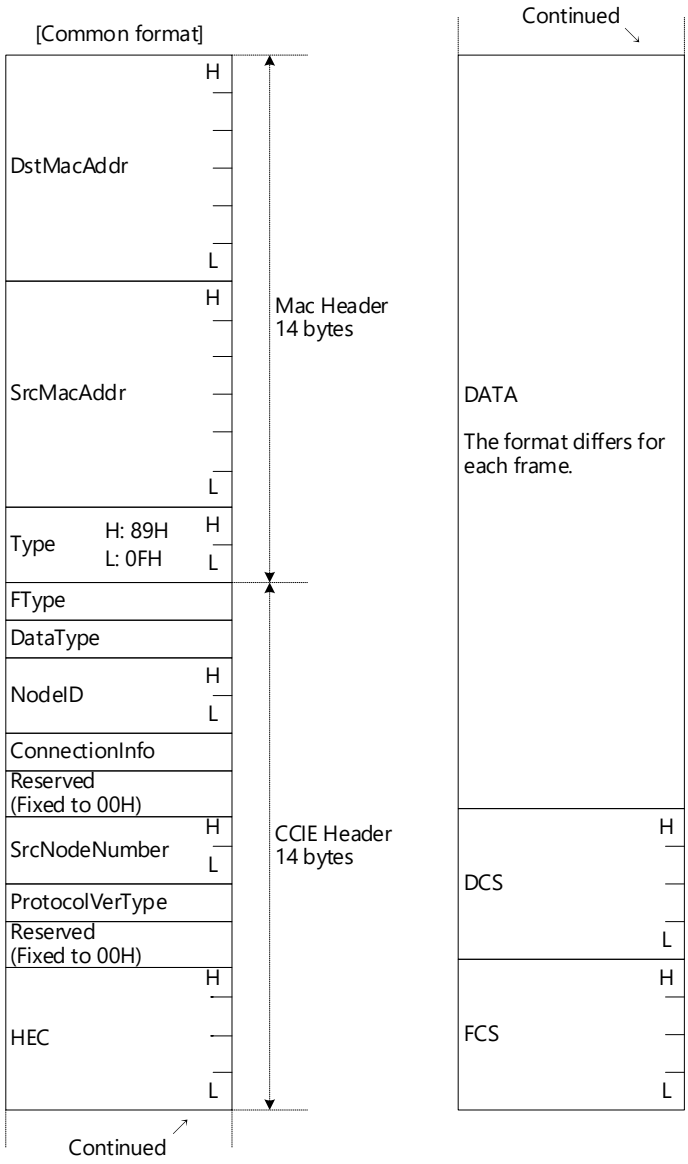


Figure Appendix 1.1-1 Overview of Frame Common Format

The following table describes the details of items defined in the frame common format. All items are set when a frame is sent by the CP520 driver.

Table Appendix 1.1-1 Details of Frame Common Format

Item	Description	Value	Remarks
Dst/SrcMacAddr (first octet)	MAC address of send destination/source	Value managed by IEEE*1	01H when the MAC address is 01-23-45-67-89-AB
Dst/SrcMacAddr (second octet)	MAC address of send destination/source		23H when the MAC address is 01-23-45-67-89-AB
Dst/SrcMacAddr (third octet)	MAC address of send destination/source		45H when the MAC address is 01-23-45-67-89-AB
Dst/SrcMacAddr (fourth octet)	MAC address of send destination/source	Value managed by user*1	67H when the MAC address is 01-23-45-67-89-AB
Dst/SrcMacAddr (fifth octet)	MAC address of send destination/source		89H when the MAC address is 01-23-45-67-89-AB
Dst/SrcMacAddr (sixth octet)	MAC address of send destination/source		ABH when the MAC address is 01-23-45-67-89-AB
Type	Type	Fixed to 890FH*1	Indicates that the frame is a CC-Link IE Field Network frame.
FType	Frame type	*2	-
DataType	Data type		-
NodeID	Node identifier	00H to F0H (0 to 240)*1	Management information of each slave station connected to the master station (The number differs from a station number.)
ConnectionInfo	Transient identification information	01H to FFH (1 to 255)	Information for identifying the transient frame sent during one token hold
SrcNodeNumber	Own station number	0001H to 0078H (1 to 120)*1	-
ProtocolVerType	Bits 7-4 Protocol version	Fixed to 0H	-
	Bits 3-0 Protocol type	Fixed to 1H	-
HEC	Header Error Control	-	-
DCS	Data Check Sequence	-	-
FCS	Frame Check Sequence	-	-

*1: Set using big endian.

*2: Refer to "Table Appendix 1-1 List of Frames Created/Analyzed by User Program".

Appendix 1.2 Transient1 frame

The following shows the basic format of a Transient1 frame.

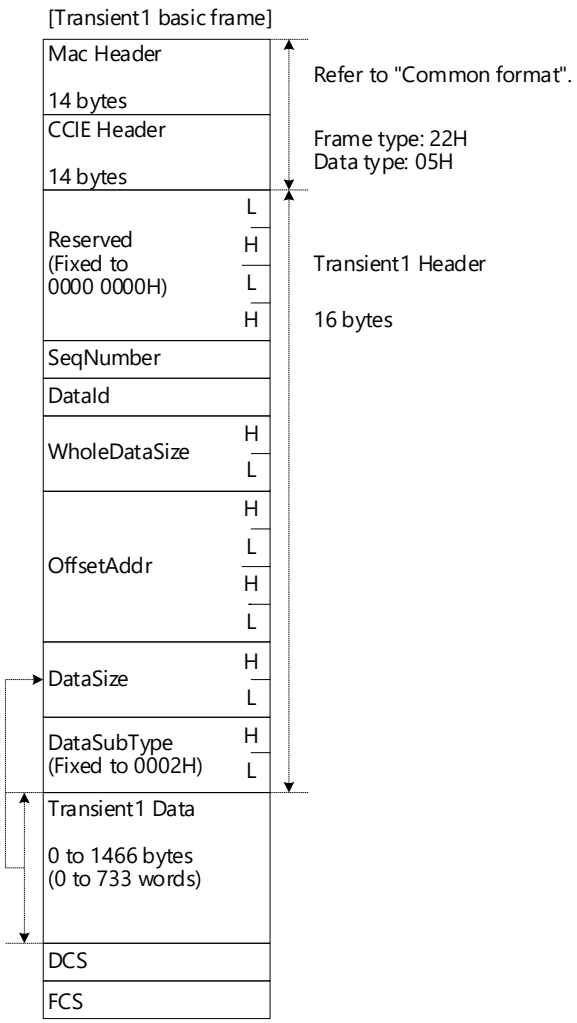


Figure Appendix 1.2-1 Overview of Transient1 Frame Basic Format

The following table describes the details of items defined in the Transient1 frame basic format.

Table Appendix 1.2-1 Details of Transient1 Frame Basic Format

Item	Description		Value	Remarks
SeqNumber	Bit 7	Final frame identification	0b: Divided frame 1b: Final divided frame	A number assigned when transient data is divided
	Bits 6-0	Transient1 frame sequential number	00H to 7FH (0 to 127)	
DataId	Transient data identification number		00H to FFH (0 to 255)	Set the same identification number for the frames after divided.
WholeDataSize	Entire transient data size	Intelligent device station	0000H to 0800H (0 to 2048)*1	Entire transient data size (in bytes) before divided
		Remote device station	0000H to 0400H (0 to 1024)*1	
OffsetAddr	Offset address from the start of entire transient data		0000 0000H to 7FFF FFFFH*1	When not divided: Fixed to 0 Start frame when divided: Fixed to 0 For the second frame and later, the storage location within the entire transient data is indicated using an offset address from the start of the data.
DataSize	Size of transient data in the frame		0000H to 05BAH (0 to 1466)*1	Transient data size (in bytes) after divided
DataSubType	Data sub-type		0002H: SLMP*1	SLMP only in this manual.

*1: Set using big endian.

The following shows the format when a Transient1 frame is divided.
In the following example, the transient data is SLMP[*1] and the transient data area addresses are set to 1000H to 1800H.
*1: For the details of SLMP, refer to Appendix 1.4 "SLMP frame".

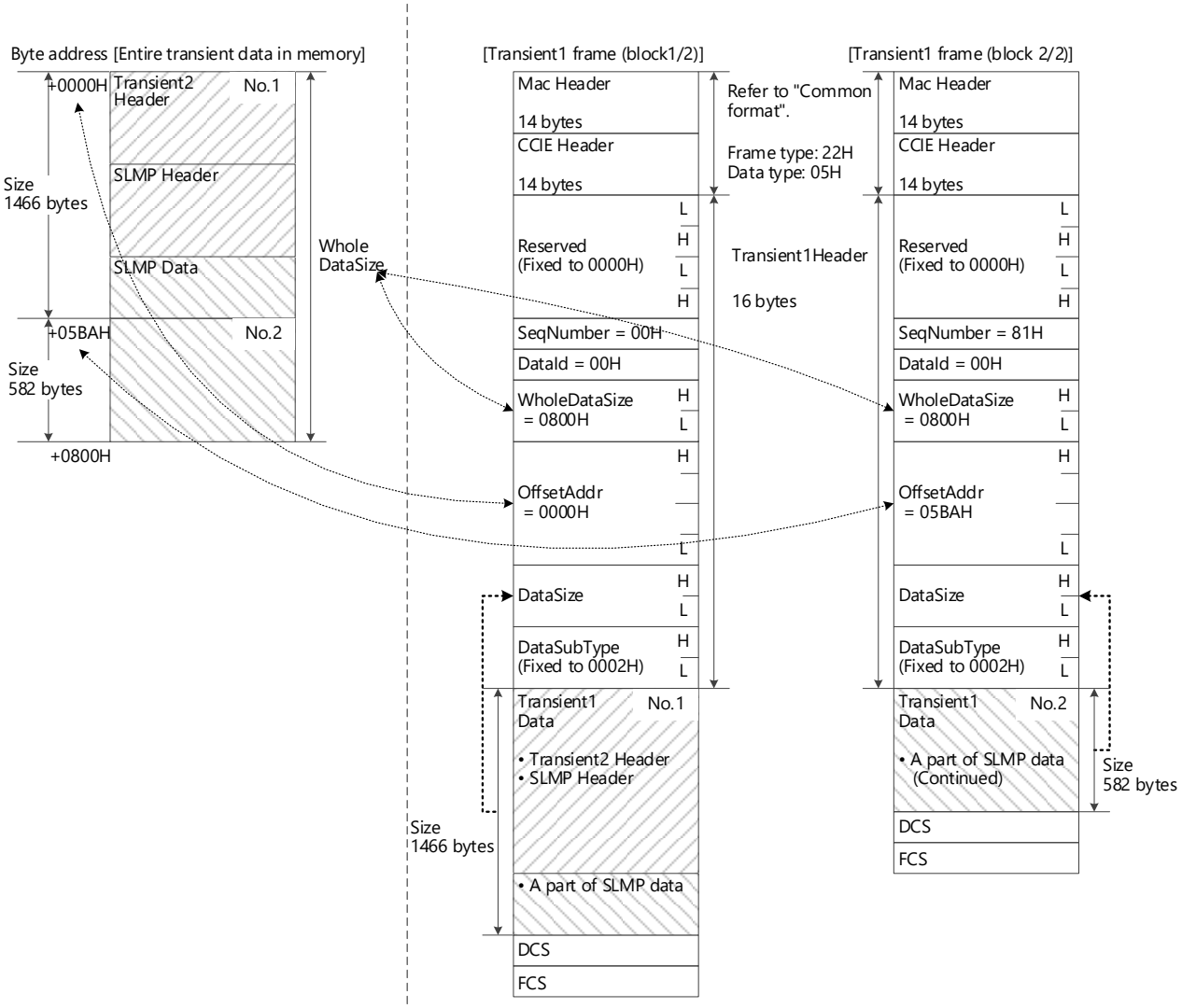


Figure Appendix 1.2-2 Example of Transient1 Frame Division

The following shows the basic format of a CC-Link compatible transient frame.

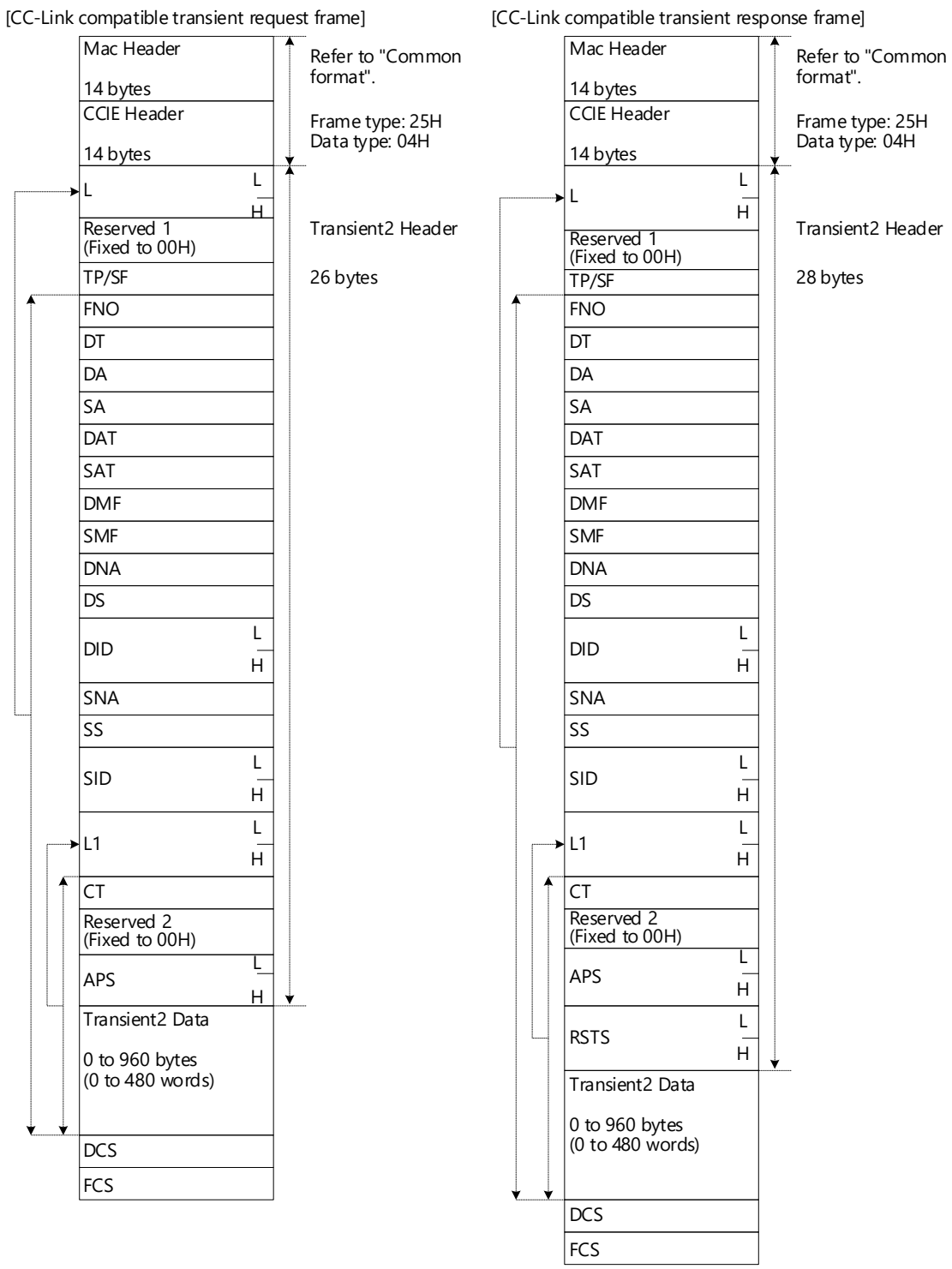


Figure Appendix 1.3-1 Overview of CC-Link Compatible Transient Frame Basic Format

(1) Details of CC-Link compatible transient frame basic format
The following table describes the details of items defined in the CC-Link transient frame basic format.

Table Appendix 1.3-1 Details of CC-Link Compatible Transient Frame Basic Format

Item	Description	Value	Remarks
L	Frame length	22 to 982: CC-Link compatible transient 41 to 1440: SLMP	Set the data length in bytes. CC-Link compatible transient: FNO to Transient2 Data SLMP: RSV to SLMP Data
TP/SF	Type/Sequence number	Fixed to 00H	-
FNO	Start frame identification number/Divided frame number	Fixed to 00H	-
DT	Priority/Response frame necessity	Fixed to 00H	-
DA	Destination station number	01H to 78H (1 to 120): Station number 7DH: Specified control station/master station 7EH: Current control station/master station FFH: Global request	Set the station number of the destination station. (Same value as DS.)
SA	Source station number	01H to 78H (1 to 120): Station number	Set the station number of the execution station. (Same value as SS.)
DAT	Destination application type	Fixed to 22H	-
SAT	Source application type	Fixed to 22H	-
DMF	Execution module destination flag	00H: CC-Link compatible transient 03H: SLMP	-
SMF	Execution module source flag	00H: CC-Link compatible transient 03H: SLMP	-
DNA	Destination network number	01H to EFH (1 to 239)	Set the network number of the destination station.
DS	Destination station number 02	01H to 78H (1 to 120): Station number 7DH: Specified control station/master station 7EH: Current control station/master station FFH: Global request	Set the station number of the destination station. (Same value as DA.)
DID	Destination identification number	Fixed to 03FFH	-
SNA	Source network number	01H to EFH (1 to 239)	Set the network number of the execution station.
SS	Source station number 02	01H to 78H (1 to 120): Station number	Set the station number of the execution station. (Same value as SA.)
SID	Source identification number	Fixed to 03FFH	-
L1	Data length	-	Set the data length after CT in bytes.
CT	Command type	04H to 1FH: CC-Link compatible transient 30H: SLMP request B0H: SLMP response	For details of CC-Link compatible transient command type, refer to "(2)Details of command type (CT)" in this section.
APS	Application number (Bits 15-8)	Fixed to 00H	Set a number to identify the frame when the source station sends a request.
	Application number (Bits 7-0)	00H to FFH	
RSTS	Return code	0000H: Normal Other than 0000H: Error code	During response only. For details of return code (RSTS), refer to "(3)Details of return code (RSTS)" in this section.

(2) Details of command type (CT)

The following shows the data structure of the command type (CT).

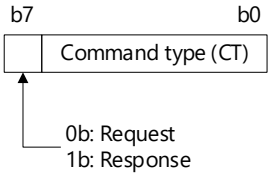


Figure Appendix 1.3-2 Data Structure of CC-Link Compatible Transient Command Type

The following table lists the CC-Link compatible transient commands described in this manual.
For the frame format of each command, refer to Appendix 1.3.1 and subsequent sections.

Table Appendix 1.3-2 CC-Link Compatible Transient Command List

Command Type	Description
04H	Memory access information acquisition request
84H	Memory access information acquisition response
08H	Remote RUN request
88H	Remote RUN response
09H	Remote STOP request
89H	Remote STOP response
10H	Memory read request
90H	Memory read request
12H	Memory write request
92H	Memory write response

(3) Details of return code (RSTS)

The return code (RSTS) is an area where the server stores the error code in the response frame when an error exists in the client request frame.

[When the own station is a client]
During the response frame receive processing, the error code of an error detected in the request frame sent by the own station is stored.
Refer to the user's manual of the request destination device (Mitsubishi Electric product or partner manufacturer product) and correct the request frame creation processing or the request send processing.

[When the own station is a server]
During the response frame send processing, store the error code of an error detected in the request frame sent by the client.
The error code can be defined by a user. The following table lists error code examples.
(Error codes of Nos. 2 to 7 in the table are described in the sample code.)

Table Appendix 1.3-3 Examples of Error Codes Stored in Return Code

No.	Error Code	Description (Definition in the CP520_Transient.h file)	Action
1	0000H	Normal	-
2	D203H	Transient data read/write address specification error (USER_ERR_WRREQ_ADDRESS_OUTOFRANGE)	Correct the read/write addresses in the transient request source, and perform the processing again.
3	D213H	Transient data command error (USER_ERR_WRREQ_COMMAND_OUTOFRANGE)	Correct the request command in the transient request source, and perform the processing again.
4	D218H	Transient data read/write data size error (USER_ERR_WRREQ_SIZE_OUTOFRANGE)	Correct the read/write data size in the transient request source, and perform the processing again.
5	D219H	Transient data attribute code error (USER_ERR_WRREQ_ATTRIBUTE_OUTOFRANGE)	Correct the attribute code in the transient request source, and perform the processing again.
6	D21AH	Transient data access code error (USER_ERR_WRREQ_ACCESSCODE_OUTOFRANGE)	Correct the access code in the transient request source, and perform the processing again.
7	D2AEH	Transient data destination station number error (USER_ERR_NOTTOONESELF)	Transient data addressed to a different network/station number has been received. Check the network number and the destination station number, and perform the processing again.
8	D2A0H	Receive buffer full error	・ Check the network status by executing the CC-Link IE Field Network diagnostics. ・ When transient data reception of the destination station is overloaded, have the send source send the data after a desired period of time has elapsed.
9	D2A1H	Send buffer full error	・ Decrease the transient transmission frequency, and perform the processing again. ・ Check that there is no error in the cable and switching hub connections in the request source.
10	D2A3H	Transient data frame length (L) error	Correct the corresponding error in the Transient2 header, and perform the processing again.
11	D2A4H	Transient data reserved (RSV) error	
12	D2A5H	Transient data destination station number (DA) error	
13	D2A6H	Transient data source station number (SA) error	
14	D2A7H	Transient data destination application type (DAT) error	
15	D2A8H	Transient data source application type (SAT) error	
16	D2A9H	Transient data destination network number (DNA) error	
17	D2AAH	Transient data destination station number (DS) error	
18	D2ABH	Transient data source network number (SNA) error	
19	D2ACH	Transient data source number (SS) error	
20	D2ADH	Transient data length (L1) error	

Appendix 1.3.1 Memory read

Executing the memory read command (CT=10H) allows you to retrieve data from devices of another station controller.
The following shows the format of a memory read frame.
Note that this frame is sent when the dedicated instruction RIRD is executed in a Mitsubishi Electric programmable controller.

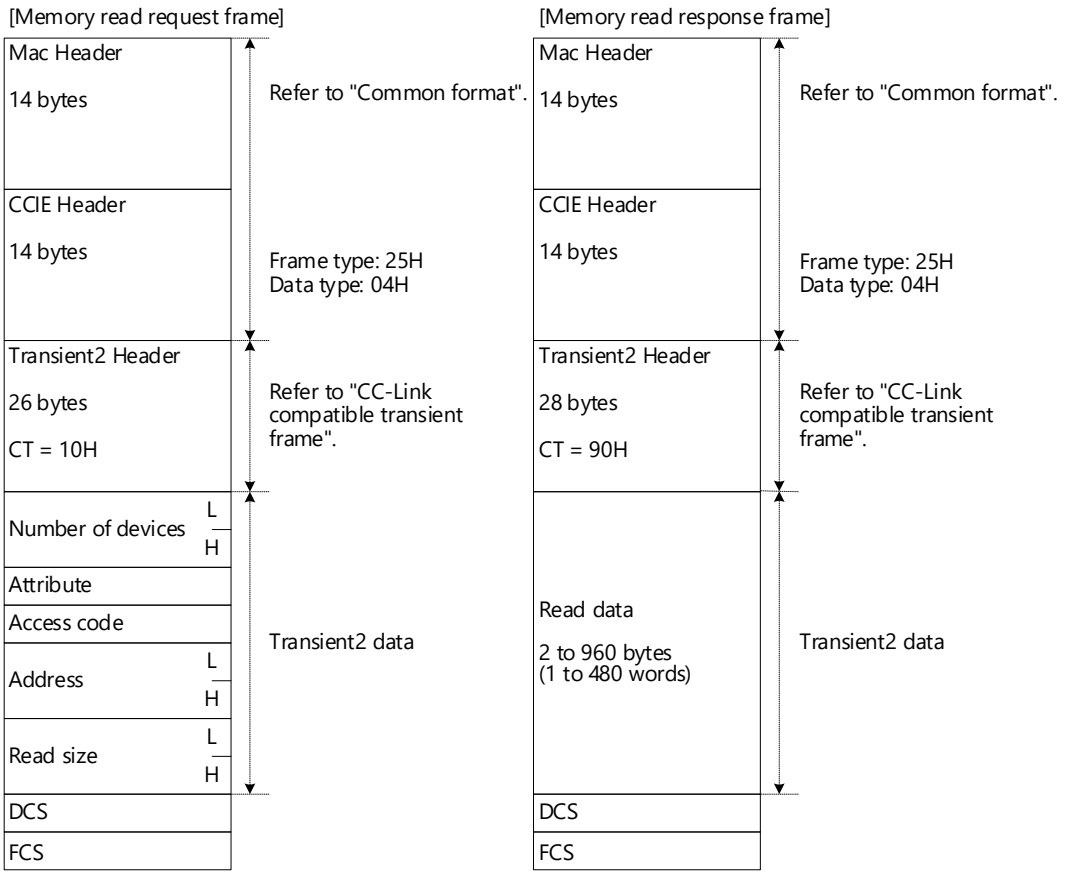


Figure Appendix 1.3.1-1 Overview of Memory Read Frame Format

The following table describes the details of items defined in the memory read frame format.

Table Appendix 1.3.1-1 Details of Memory Read Frame Format

Item	Description	Value	Remarks
Number of devices	Set the number of devices to be read.	Fixed to 0001H	-
Attribute	Set the attribute of the target device of the request destination.	-	For details, refer to Appendix 1.3.3 "Access codes and attributes".
Access code	Set the access code of the target device of the request destination.	-	For details, refer to Appendix 1.3.3 "Access codes and attributes".
Address	Set the start address of the device to be read. (Set a value within the access range.)	Any offset value	Specify 0 or a multiple of 16 when the device type is bit, and 0 or a multiple of 2 when the device type is byte.
Read size	Set the size of the data to be read (in words).	1 to 480 words	-

Appendix 1.3.2 Memory write

Executing the memory write command (CT=12H) allows you to write data to devices of another station controller. The following shows the format of a memory write frame.
Note that this frame is sent when the dedicated instruction RIWT is executed in a Mitsubishi Electric programmable controller.

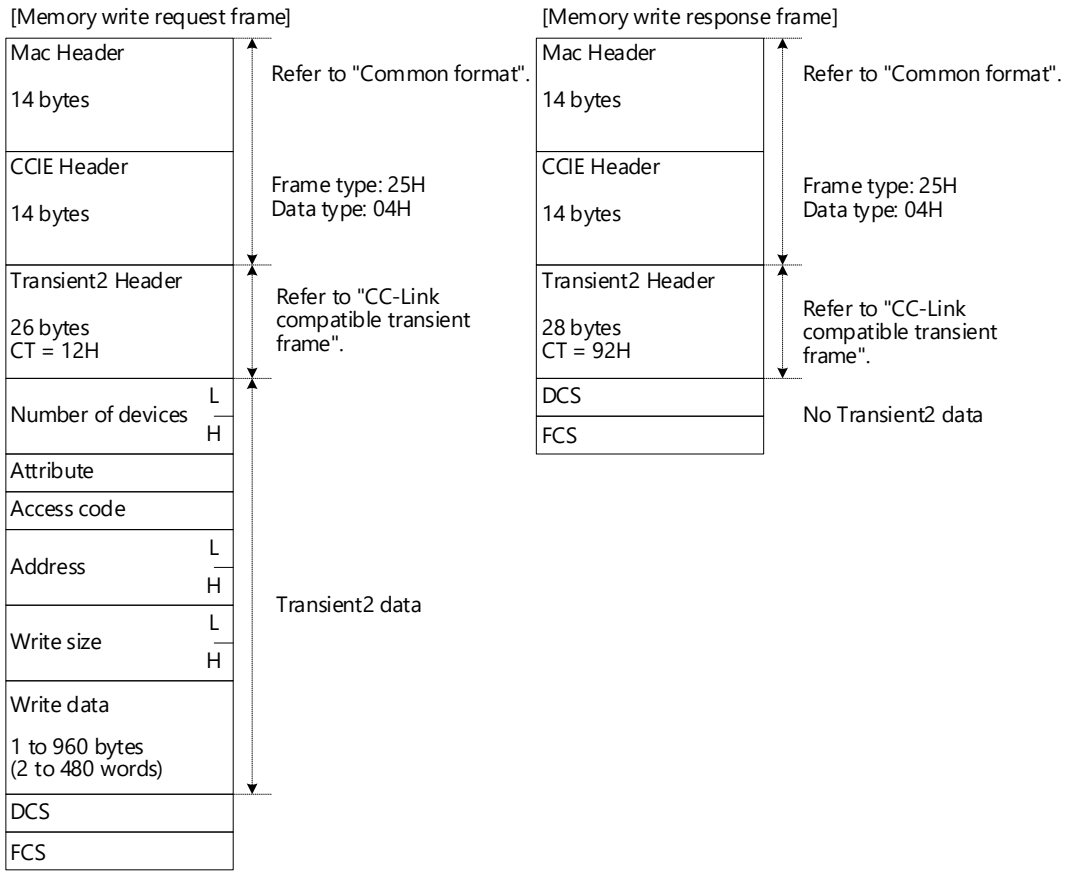


Figure Appendix 1.3.2-1 Overview of Memory Write Frame Format

The following table describes the details of items defined in the memory write frame format.

Table Appendix 1.3.2-1 Details of Memory Write Frame Format

Item	Description	Value	Remarks
Number of devices	Set the number of devices to be written.	Fixed to 0001H	-
Attribute	Set the attribute of the target device of the request destination.	-	For details, refer to Appendix 1.3.3 "Access codes and attributes".
Access code	Set the access code of the target device of the request destination.	-	For details, refer to Appendix 1.3.3 "Access codes and attributes".
Address	Set the start address of the device to be written. (Set a value within the access range.)	Any offset value	Specify 0 or a multiple of 16 when the device type is bit, and 0 or a multiple of 2 when the device type is byte.
Write size	Set the size of the data to be written (in words).	1 to 480 words	-
Write data	Set the data to be written.	Any value to be written	-

Appendix 1.3.3 Access codes and attributes

The following are the definitions of an access code and an attribute.

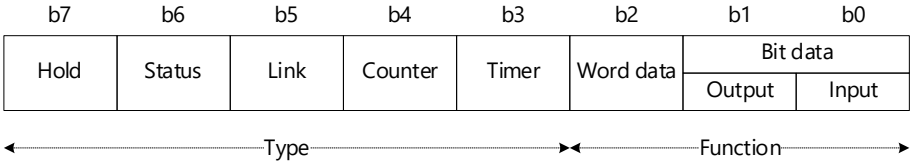


Figure Appendix 1.3.3-1 Access Code Definition

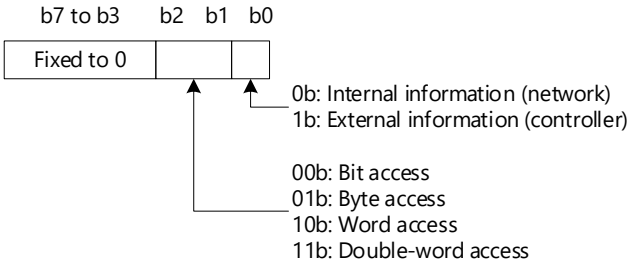


Figure Appendix 1.3.3-2 Attribute Definition

[When the own station is a server]
Set the access codes and attribute of the own station so that another station can access the own station by using the memory read/write commands.

[When the own station is a client]
Refer to the following table when accessing another station (Mitsubishi Electric product) from the own station by using the memory read/write commands.
The number of device points (size) differs depending on the programmable controller. For the accessible range, refer to the user's manual of the programmable controller used.
When accessing to a station other than Mitsubishi Electric products, refer to the user's manual of the station.

Table Appendix 1.3.3-1 Mitsubishi Electric Product Access Code List

Device	Symbol	Device Type		Unit	Access Code[*1]	Attribute Code[*1]
		Bit	Word			
Input relay	X	○	-	Hexadecimal	01H	05H
Output relay	Y	○	-	Hexadecimal	02H	
Special relay	SM	○	-	Decimal	43H	
Special register	SD	-	○	Decimal	44H	
Internal relay	M	○	-	Decimal	03H	
Latch relay	L	○	-	Decimal	83H	
Timer (contact)	T	○	-	Decimal	09H	
Timer (coil)	T	○	-	Decimal	0AH	
Timer (current value)	T	-	○	Decimal	0CH	
Retentive timer (contact)	ST	○	-	Decimal	89H	
Retentive timer (coil)	ST	○	-	Decimal	8AH	
Retentive timer (current value)	ST	-	○	Decimal	8CH	
Counter (contact)	C	○	-	Decimal	11H	
Counter (coil)	C	○	-	Decimal	12H	
Counter (current value)	C	-	○	Decimal	14H	
Data register	D[*2]	-	○	Decimal	04H	
File register	R	-	○	Decimal	84H	
Link relay	B	○	-	Hexadecimal	23H	
Link register	W[*2]	-	○	Hexadecimal	24H	
Link special relay	SB	○	-	Hexadecimal	63H	
Link special register	SW	-	○	Hexadecimal	64H	

*1: If the target station is a station other than the master/local module, refer to the user's manual of the target station for the access codes and attribute codes.

*2: The extended data register (D65536 and later) and the extended link register (W10000 and later) cannot be specified.

The following figure shows the basic format of an SLMP frame.

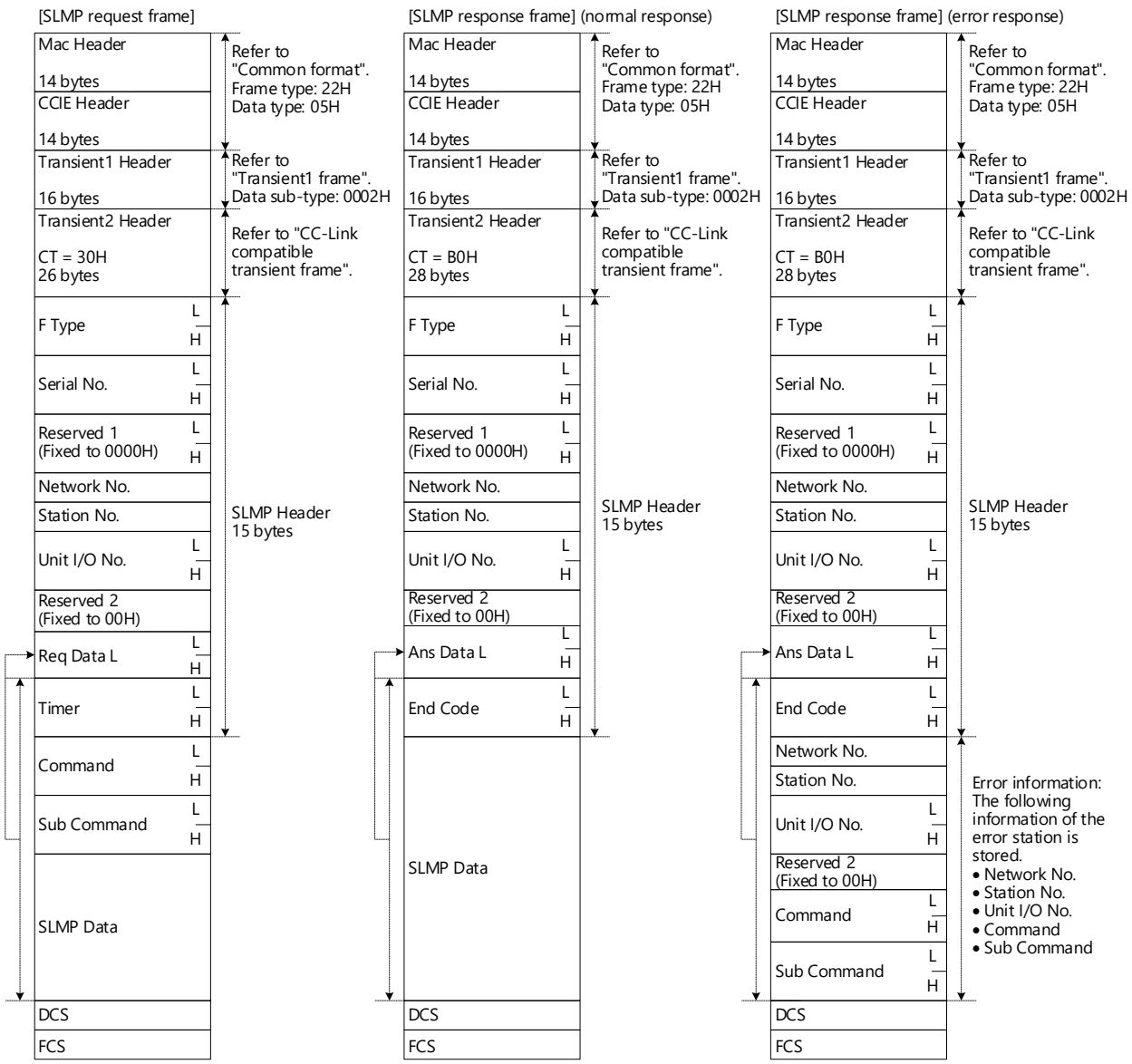


Figure Appendix 1.4-1 Overview of SLMP Frame Basic Format

(1) Details of SLMP frame basic format

The following table describes the details of items defined in the SLMP frame basic format.

Table Appendix 1.4-1 Details of SLMP Frame Basic Format

Item	Description	Value	Remarks
F Type	Frame type	0054H: Request 00D4H: Response	-
Serial No.	Serial number	0000H to FFFFH	Set a number to identify the frame. Set the same value for a request frame and the corresponding response frame.
Network No.	Destination station network number	00H: Own station 01H to EFH (1 to 239): Other stations	Set the network number of the destination station.
Station No.	Destination station number	01H to 78H (1 to 120): Station number 7DH: Specified control station/master station 7EH: Current control station/master station FFH: Own station*1	Set the destination station number. *1: Effective only when the Network No. is set to 00H.
Unit I/O No.	Destination module I/O number	03FFH: Fixed	Set the access destination CPU module.
Req Data L	Request data length	-	Set the request data size, from Timer to the end of the data area, in bytes.
Ans Data L	Response data length	-	Set the response data size, from End Code to the end of the data area, in bytes.
Timer	Monitoring timer	0001H to FFFFH 0000H: Unlimited	Request frame only. Set the wait time (in increments of 250ms) for the client to receive a response from the server. Recommended values: Own station: 0001H to 0028H (0.25 to 10s) Other stations: 0002H to 00F0H (0.5 to 60s)
End Code	End code	0000H: Normal end Other than 0000H: Error code	Response frame only. For details of end codes, refer to Details of end code (End Code) in this section.

(2) Details of end code (End Code)

The end code (End Code) is an area where the server stores the error code in the response frame when an error exists in the client request frame.

[When the own station is a client]

During the response frame receive processing, the error code of an error detected in the request frame sent by the own station is stored.

Refer to the user's manual of the request destination device (Mitsubishi Electric product or partner manufacturer product) and correct the request frame creation processing or the request send processing.

[When the own station is a server]

During the response frame send processing, store the error code of an error detected in the request frame sent by the client.

The error code can be defined by a user. The following table lists error code examples.

Table Appendix 1.4-2 Examples of Error Codes Stored in End Code

No.	Category	Error Code	Description	Action
1	Successful completion	0000H	The request was processed normally.	-
2	General error	C059H	・ There is an error in the command/subcommand specification. ・ A command other than that in the specified sequence was received.	Correct the command/subcommand, and send the request again.
3		C05CH	There is an error in the request message.	Correct the request message, and send the request again.
4		C061H	The request data length and data size do not match.	Correct the request data or the request data length, and send the request again.
5		CEE0H	Another request is being executed. The request cannot be processed.	Wait for a while, and send the request again.
6		CEE1H	The request message size exceeds the range that can be processed.	Correct the request message, and send the request again.
7		CEE2H	The response message size exceeds the range that can be processed.	Correct the request message, and send the request again.
8	Server information	CF10H	The specified server information number does not exist.	Correct the server information number, and send the request again.
9	Communication settings	CF20H	An item that cannot be set is included in the request message.	Correct the setting item (CSP+), and send the request again.
10	Parameter settings	CF30H	The specified parameter ID does not exist.	Correct the parameter and the parameter ID (CSP+), and send the request again.
11		CF31H	The write exclusive start processing has not been performed. The request cannot be processed.	Execute the write exclusive start processing, and send the request again.
12	Communication status	CF70H	An error occurred in the communication path of the relay destination. The request cannot be processed.	Check the communication path, and send the request again.
13		CF71H	A timeout occurred. The processing was interrupted.	Check the status of the destination device, and send the request again.

Appendix 1.4.1 SLMP memory read frame

Executing the SLMP memory read command (Command=0613H, Sub Command=0000H) allows you to retrieve data from the buffer memory of another station (SLMP-compatible device).
The following shows the format of SLMP memory read frame.

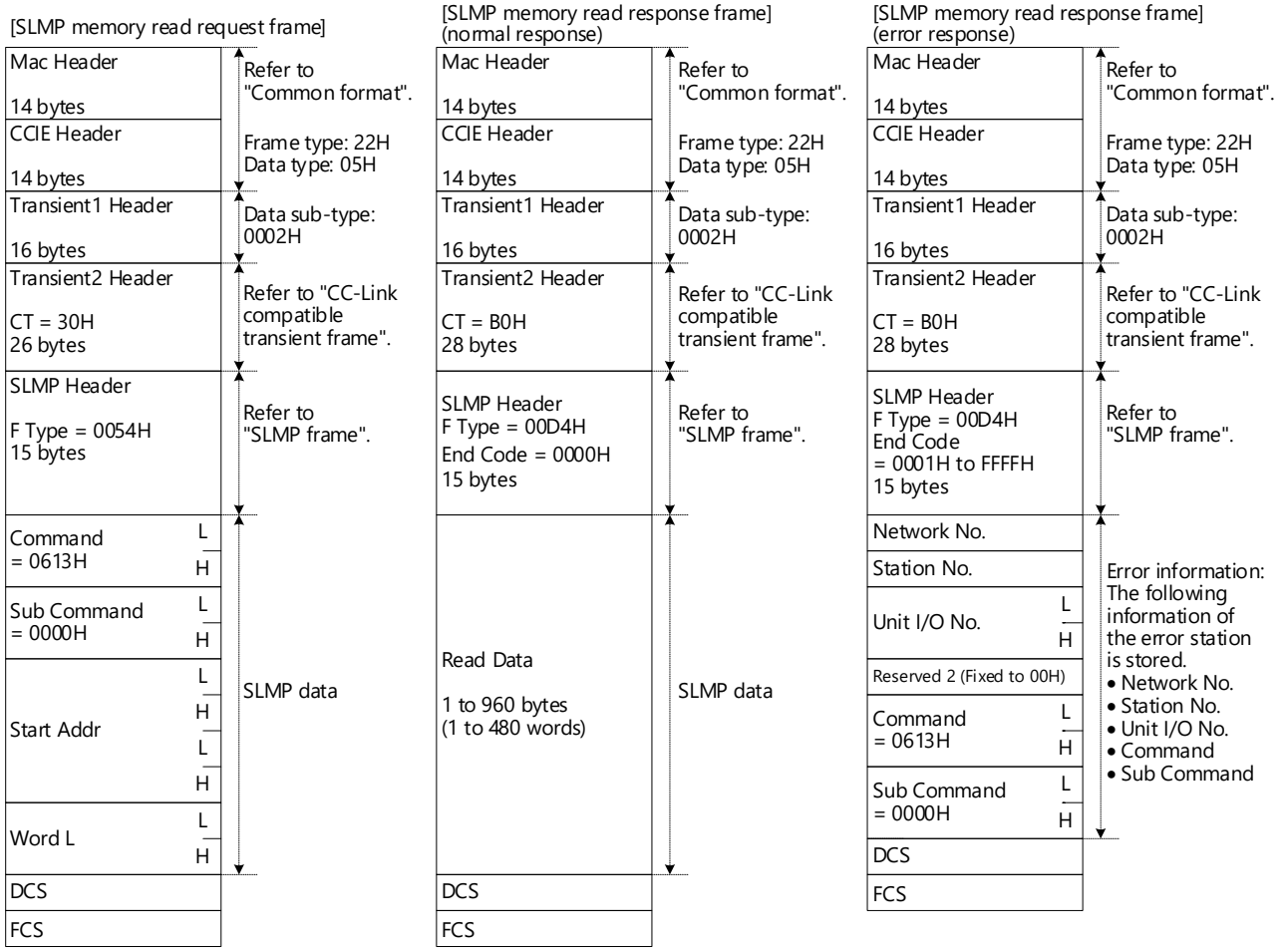


Figure Appendix 1.4.1-1 Overview of SLMP Memory Read Frame Format

The following table describes the details of items defined in the SLMP memory read frame format.

Table Appendix 1.4.1-1 Details of SLMP Memory Read Frame Format

Item	Description	Value	Remarks
Command	Command	Fixed to 0613H	-
Sub Command	Subcommand	Fixed to 0000H	-
Start Addr	Start address	-	Specify the start address of the buffer memory to be read.
Word L	Word length	1H to 1E0H (1 to 480)	Specify the word length of the buffer memory to be read.

Appendix 1.4.2 SLMP memory write frame

Executing the SLMP memory write command (Command=1613H, Sub Command=0000H) allows you to write data to the buffer memory of another station (SLMP-compatible device).
The following shows the format of an SLMP memory write frame.

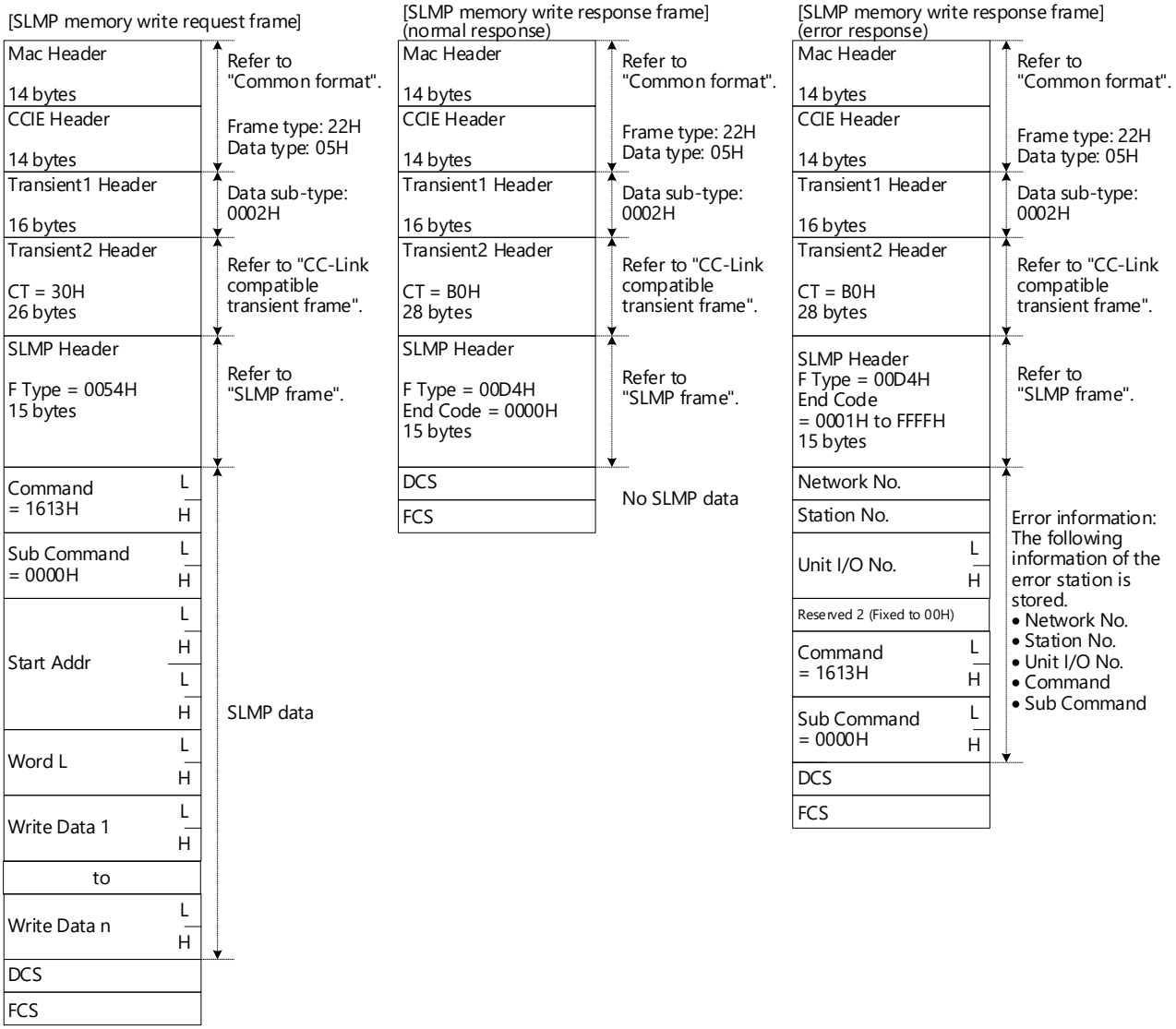


Figure Appendix 1.4.2-1 Overview of SLMP Memory Write Frame Format

The following table describes the details of items defined in the SLMP memory write frame format.

Table Appendix 1.4.2-1 Details of SLMP Memory Write Frame Format

Item	Description	Value	Remarks
Command	Command	Fixed to 1613H	-
Sub Command	Subcommand	Fixed to 0000H	-
Start Addr	Start address	-	Specify the start address of the buffer memory to be written.
Word L	Word length	1H to 1E0H (1 to 480)	Specify the word length of the buffer memory to be written.

Appendix 1.5 TransientAck frame

The following shows the format of a TransientAck frame.

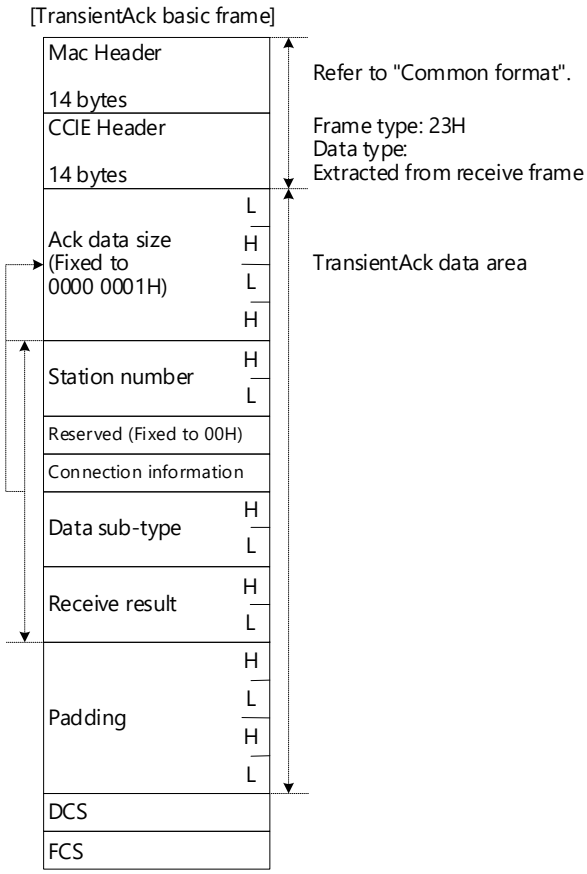


Figure Appendix 1.5-1 Overview of TransientAck Frame Format

The following table describes the details of items defined in the TransientAck frame format.

Table Appendix 1.5-1 Details of TransientAck Frame Format

Item	Description	Value	Remarks
Ack data size	Data size from station number to receive result	Fixed value: 0000 0001H	-
Station number	TransientAck frame destination station number	Station number of received transient frame send source	When a transient frame is received from the master station (send source station number: 0000H), set the destination station number after converting the value to "007DH".
Connection information	Connection information loopback value of Ack send target frame (ConnectionInformation)	Connection information of received transient frame	-
Data sub-type	Data sub-type of received transient frame	Transient1: 0002H Transient2: 0000H	There is no data sub-type for Transient2 frames. Set "0000H" for an acknowledgement response to a Transient2 frame.
Receive result	Receive result (RET) of transient frame	Normal: 0000H Error: Other than 0000H	-
Padding	Padding (16 bytes)	-	To satisfy the minimum Ethernet frame size of 64 bytes, padding is automatically performed by CP520.

Appendix 2 Port Functions

Appendix 2.1 Features

The CP520 port functions offer the following features:

- I/O port pins: 106
- Multiplexed with I/O pin functions of peripheral modules
- Input or output can be specified in bit units.

Note

1) Switching from a signal for a peripheral module that is multiplexed with a port pin to port mode by changing the multiplexed function might lead to a spike, depending on the state of the pin at the time.
   The following general countermeasure for spikes should therefore be implemented in software.
   - Switch the pin function while the peripheral module is stopped.
   - If the multiplexed pin in use is an interrupt signal, clear the interrupt request flag and then remove masking of the interrupt.
   - Only switch the mode after the output value is fixed.
2) Do not externally apply an intermediate potential to input buffers because these buffers do not implement through-current countermeasures.

Appendix 2.2 Port configuration

CP520 incorporates twelve 8-bit ports and one 10-bit port (EXTP).

Nine are 3-state I/O ports (including EXTP) and four are for real-time control.
Input or output can be specified for ports in 1-bit units. The basic structure of ports is the 8-bit unit, but ports P0x to P3x, P4x to P7x, RP0x to RP3x (x = 0 to 7), and EXTP0 to EXTP9 can also be grouped to enable reading and writing in 32-bit units.
The real-time port pins (RP00 to RP37) can be used for input and output in synchronization with interrupt signals.

Each port can be accessed in 8/16/32-bit units by register settings.

Each port has the registers listed below, which are used to make the I/O settings and to select and specify the multiplexed functions of the port pins.

Table Appendix 2.2-1 Multiplexed Function Selection Registers

(n = 0 to 7, m = 0 to 3, p = 0, 1)

<table>
<tr><th rowspan="2">Register Name</th><th colspan="2">Application and Operation</th></tr>
<tr><th>Read</th><th>Write</th></tr>
<tr><td>Port registers
(Pn, RPm, EXTPp)</td><td>Used to read the value of the output latch.</td><td>Used to set a value to the output latch.</td></tr>
<tr><td>Port mode registers
(PMn, RPMm, EXTPMp)</td><td>Used to read whether the port is in input or output mode.</td><td>Used to set the port to input or output mode.</td></tr>
<tr><td>Port mode control registers
(PMCn, RPMCm, EXTPMCp)</td><td>Used to read whether the port pins are selected as port pins or as multiplexed function pins.</td><td>Used to select whether the port pins are used as port pins or as multiplexed function pins.</td></tr>
<tr><td>Port function control registers
(PFCn, RPFCm, EXTPFCp)</td><td rowspan="2">Used to read the selection status of multiplexed functions.</td><td rowspan="2">Used to select multiplexed functions.</td></tr>
<tr><td>Port function control expansion registers
(PFCEn, RPFCEm, EXTPFCEp)</td></tr>
<tr><td>Port pin input registers
(PINn, RPINm, EXTPINp)</td><td>Used to read the input level of the port pin.</td><td>Cannot be written.</td></tr>
</table>

Remarks

If a port pin having multiple multiplexed functions which include an external interrupt input is set to control mode by using the PMCn or RPMCm register, and the multiplexed function is an input, the external interrupt input is also multiplexed.

Operation is not guaranteed if the setting has been made not to allocate a multiplexed pin. For example, if multiplexed functions 2 and 4 are not allocated in the same way as the P14 pin, operation does not proceed correctly even if the bits of the PFC and PFCE registers for the given function are set to High.
For the allocation of multiplexed pins, refer to Appendix 2.5 "List of selectable multiplexed functions".

The basic circuit configuration of the port registers and port pin is shown below.

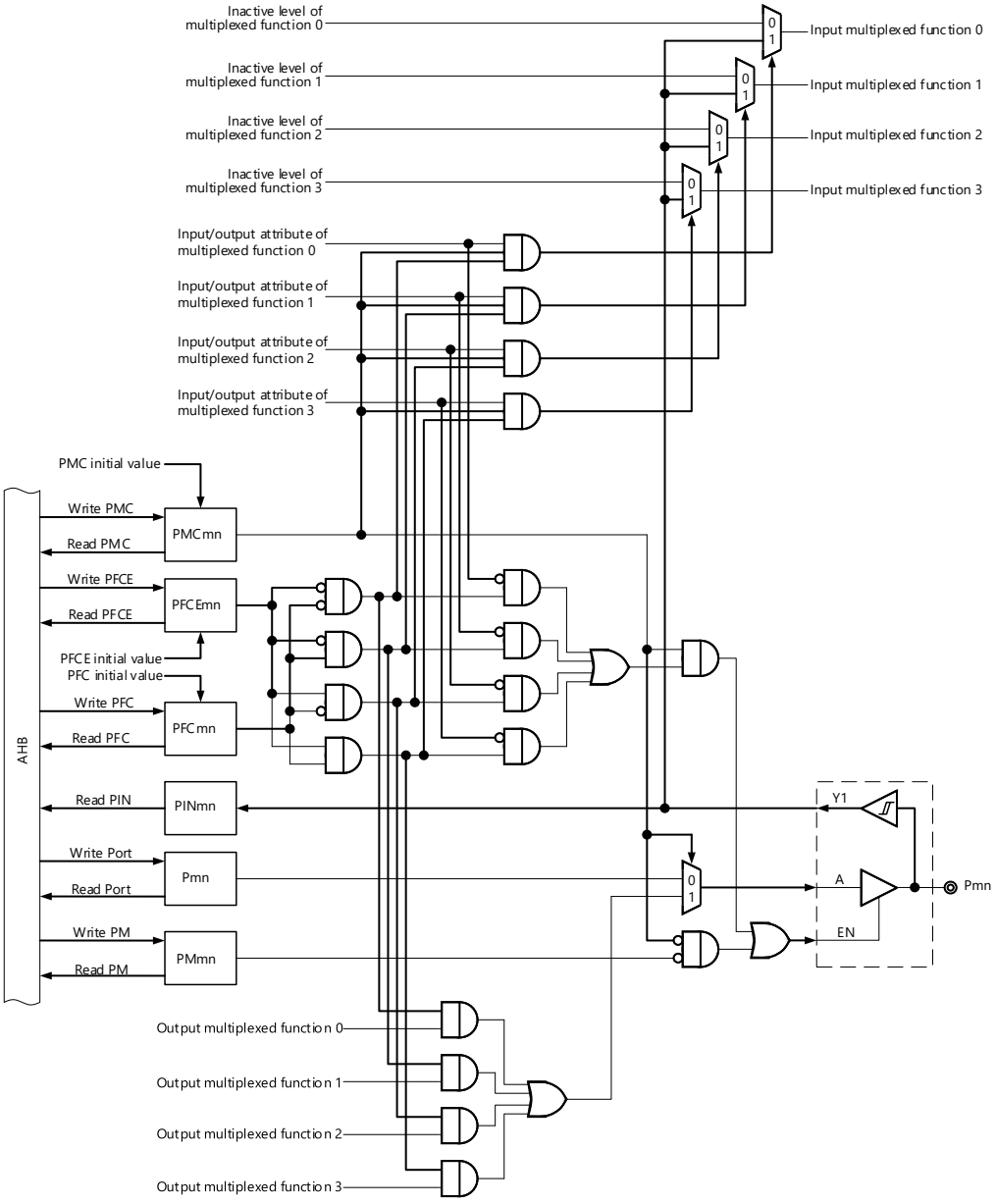


Figure Appendix 2.2-1 Basic Circuit Configuration of Ports

Table Appendix 2.3-1 List of Port Registers

Register Name	Symbol	Address
Port register 0 (8 bits)	P0B	400A 3000H
Port register 1 (8 bits)	P1B	400A 3001H
Port register 2 (8 bits)	P2B	400A 3002H
Port register 3 (8 bits)	P3B	400A 3003H
Port register 4 (8 bits)	P4B	400A 3004H
Port register 5 (8 bits)	P5B	400A 3005H
Port register 6 (8 bits)	P6B	400A 3006H
Port register 7 (8 bits)	P7B	400A 3007H
Port register 0 (16 bits)	P0H	400A 3000H
Port register 2 (16 bits)	P2H	400A 3002H
Port register 4 (16 bits)	P4H	400A 3004H
Port register 6 (16 bits)	P6H	400A 3006H
Port register 0 (32 bits)	P0W	400A 3000H
Port register 4 (32 bits)	P4W	400A 3004H
Port mode register 0 (8 bits)	PM0B	400A 3010H
Port mode register 1 (8 bits)	PM1B	400A 3011H
Port mode register 2 (8 bits)	PM2B	400A 3012H
Port mode register 3 (8 bits)	PM3B	400A 3013H
Port mode register 4 (8 bits)	PM4B	400A 3014H
Port mode register 5 (8 bits)	PM5B	400A 3015H
Port mode register 6 (8 bits)	PM6B	400A 3016H
Port mode register 7 (8 bits)	PM7B	400A 3017H
Port mode register 0 (16 bits)	PM0H	400A 3010H
Port mode register 2 (16 bits)	PM2H	400A 3012H
Port mode register 4 (16 bits)	PM4H	400A 3014H
Port mode register 6 (16 bits)	PM6H	400A 3016H
Port mode register 0 (32 bits)	PM0W	400A 3010H
Port mode register 4 (32 bits)	PM4W	400A 3014H
Port mode control register 0 (8 bits)	PMC0B	400A 3020H
Port mode control register 1 (8 bits)	PMC1B	400A 3021H
Port mode control register 2 (8 bits)	PMC2B	400A 3022H
Port mode control register 3 (8 bits)	PMC3B	400A 3023H
Port mode control register 4 (8 bits)	PMC4B	400A 3024H
Port mode control register 5 (8 bits)	PMC5B	400A 3025H
Port mode control register 6 (8 bits)	PMC6B	400A 3026H
Port mode control register 7 (8 bits)	PMC7B	400A 3027H
Port mode control register 0 (16 bits)	PMC0H	400A 3020H
Port mode control register 2 (16 bits)	PMC2H	400A 3022H
Port mode control register 4 (16 bits)	PMC4H	400A 3024H
Port mode control register 6 (16 bits)	PMC6H	400A 3026H
Port mode control register 0 (32 bits)	PMC0W	400A 3020H
Port mode control register 4 (32 bits)	PMC4W	400A 3024H
Port function control register 0 (8 bits)	PFC0B	400A 3030H
Port function control register 1 (8 bits)	PFC1B	400A 3031H
Port function control register 2 (8 bits)	PFC2B	400A 3032H
Port function control register 3 (8 bits)	PFC3B	400A 3033H
Port function control register 4 (8 bits)	PFC4B	400A 3034H
Port function control register 5 (8 bits)	PFC5B	400A 3035H
Port function control register 6 (8 bits)	PFC6B	400A 3036H
Port function control register 7 (8 bits)	PFC7B	400A 3037H
Port function control register 0 (16 bits)	PFC0H	400A 3030H
Port function control register 2 (16 bits)	PFC2H	400A 3032H
Port function control register 4 (16 bits)	PFC4H	400A 3034H
Port function control register 6 (16 bits)	PFC6H	400A 3036H
Port function control register 0 (32 bits)	PFC0W	400A 3030H
Port function control register 4 (32 bits)	PFC4W	400A 3034H
Port function control expansion register 0 (8 bits)	PFCE0B	400A 3040H

Register Name	Symbol	Address
Port function control expansion register 1 (8 bits)	PFCE1B	400A 3041H
Port function control expansion register 2 (8 bits)	PFCE2B	400A 3042H
Port function control expansion register 3 (8 bits)	PFCE3B	400A 3043H
Port function control expansion register 4 (8 bits)	PFCE4B	400A 3044H
Port function control expansion register 5 (8 bits)	PFCE5B	400A 3045H
Port function control expansion register 6 (8 bits)	PFCE6B	400A 3046H
Port function control expansion register 7 (8 bits)	PFCE7B	400A 3047H
Port function control expansion register 0 (16 bits)	PFCE0H	400A 3040H
Port function control expansion register 2 (16 bits)	PFCE2H	400A 3042H
Port function control expansion register 4 (16 bits)	PFCE4H	400A 3044H
Port function control expansion register 6 (16 bits)	PFCE6H	400A 3046H
Port function control expansion register 0 (32 bits)	PFCE0W	400A 3040H
Port function control expansion register 4 (32 bits)	PFCE4W	400A 3044H
Port pin input register 0 (8 bits)	PIN0B	400A 3050H
Port pin input register 1 (8 bits)	PIN1B	400A 3051H
Port pin input register 2 (8 bits)	PIN2B	400A 3052H
Port pin input register 3 (8 bits)	PIN3B	400A 3053H
Port pin input register 4 (8 bits)	PIN4B	400A 3054H
Port pin input register 5 (8 bits)	PIN5B	400A 3055H
Port pin input register 6 (8 bits)	PIN6B	400A 3056H
Port pin input register 7 (8 bits)	PIN7B	400A 3057H
Port pin input register 0 (16 bits)	PIN0H	400A 3050H
Port pin input register 2 (16 bits)	PIN2H	400A 3052H
Port pin input register 4 (16 bits)	PIN4H	400A 3054H
Port pin input register 6 (16 bits)	PIN6H	400A 3056H
Port pin input register 0 (32 bits)	PIN0W	400A 3050H
Port pin input register 4 (32 bits)	PIN4W	400A 3054H
RT port register 0 (8 bits)	RP0B	400A 3400H
RT port register 1 (8 bits)	RP1B	400A 3401H
RT port register 2 (8 bits)	RP2B	400A 3402H
RT port register 3 (8 bits)	RP3B	400A 3403H
RT port register 0 (16 bits)	RP0H	400A 3400H
RT port register 2 (16 bits)	RP2H	400A 3402H
RT port register 0 (32 bits)	RP0W	400A 3400H
RT port mode register 0 (8 bits)	RPM0B	400A 3410H
RT port mode register 1 (8 bits)	RPM1B	400A 3411H
RT port mode register 2 (8 bits)	RPM2B	400A 3412H
RT port mode register 3 (8 bits)	RPM3B	400A 3413H
RT port mode register 0 (16 bits)	RPM0H	400A 3410H
RT port mode register 2 (16 bits)	RPM2H	400A 3412H
RT port mode register 0 (32 bits)	RPM0W	400A 3410H
RT port mode control register 0 (8 bits)	RPMC0B	400A 3420H
RT port mode control register 1 (8 bits)	RPMC1B	400A 3421H
RT port mode control register 2 (8 bits)	RPMC2B	400A 3422H
RT port mode control register 3 (8 bits)	RPMC3B	400A 3423H
RT port mode control register 0 (16 bits)	RPMC0H	400A 3420H
RT port mode control register 2 (16 bits)	RPMC2H	400A 3422H
RT port mode control register 0 (32 bits)	RPMC0W	400A 3420H
RT port function control register 0 (8 bits)	RPFC0B	400A 3430H
RT port function control register 1 (8 bits)	RPFC1B	400A 3431H
RT port function control register 2 (8 bits)	RPFC2B	400A 3432H
RT port function control register 3 (8 bits)	RPFC3B	400A 3433H
RT port function control register 0 (16 bits)	RPFC0H	400A 3430H
RT port function control register 2 (16 bits)	RPFC2H	400A 3432H
RT port function control register 0 (32 bits)	RPFC0W	400A 3430H
RT port function control expansion register 0 (8 bits)	RPFCE0B	400A 3440H
RT port function control expansion register 1 (8 bits)	RPFCE1B	400A 3441H
RT port function control expansion register 2 (8 bits)	RPFCE2B	400A 3442H
RT port function control expansion register 3 (8 bits)	RPFCE3B	400A 3443H
RT port function control expansion register 0 (16 bits)	RPFCE0H	400A 3440H

Register Name	Symbol	Address
RT port function control expansion register 2 (16 bits)	RPFCE2H	400A 3442H
RT port function control expansion register 0 (32 bits)	RPFCE0W	400A 3440H
RT port pin input register 0 (8 bits)	RPIN0B	400A 3450H
RT port pin input register 1 (8 bits)	RPIN1B	400A 3451H
RT port pin input register 2 (8 bits)	RPIN2B	400A 3452H
RT port pin input register 3 (8 bits)	RPIN3B	400A 3453H
RT port pin input register 0 (16 bits)	RPIN0H	400A 3450H
RT port pin input register 2 (16 bits)	RPIN2H	400A 3452H
RT port pin input register 0 (32 bits)	RPIN0W	400A 3450H
EXT port register 0 (8 bits)	EXTP0B	400A 3800H
EXT port register 1 (8 bits)	EXTP1B	400A 3801H
EXT port register 0 (16 bits)	EXTP0H	400A 3800H
EXT port register 0 (32 bits)	EXTP0W	400A 3800H
EXT port mode register 0 (8 bits)	EXTPM0B	400A 3810H
EXT port mode register 1 (8 bits)	EXTPM1B	400A 3811H
EXT port mode register 0 (16 bits)	EXTPM0H	400A 3810H
EXT port mode register 0 (32 bits)	EXTPM0W	400A 3810H
EXT port mode control register 0 (8 bits)	EXTPMC0B	400A 3820H
EXT port mode control register 1 (8 bits)	EXTPMC1B	400A 3821H
EXT port mode control register 0 (16 bits)	EXTPMC0H	400A 3820H
EXT port mode control register 0 (32 bits)	EXTPMC0W	400A 3820H
EXT port function control register 0 (8 bits)	EXTPFC0B	400A 3830H
EXT port function control register 1 (8 bits)	EXTPFC1B	400A 3831H
EXT port function control register 0 (16 bits)	EXTPFC0H	400A 3830H
EXT port function control register 0 (32 bits)	EXTPFC0W	400A 3830H
EXT port function control expansion register 0 (8 bits)	EXTPFCE0B	400A 3840H
EXT port function control expansion register 1 (8 bits)	EXTPFCE1B	400A 3841H
EXT port function control expansion register 0 (16 bits)	EXTPFCE0H	400A 3840H
EXT port function control expansion register 0 (32 bits)	EXTPFCE0W	400A 3840H
EXT port pin input register 0 (8 bits)	EXTPIN0B	400A 3850H
EXT port pin input register 1 (8 bits)	EXTPIN1B	400A 3851H
EXT port pin input register 0 (16 bits)	EXTPIN0H	400A 3850H
EXT port pin input register 0 (32 bits)	EXTPIN0W	400A 3850H
Buffer switching register P0L	DRCTLP0L	4001 0220H
Buffer switching register P0H	DRCTLP0H	4001 0224H
Buffer switching register P1L	DRCTLP1L	4001 0228H
Buffer switching register P1H	DRCTLP1H	4001 022CH
Buffer switching register P2L	DRCTLP2L	4001 0230H
Buffer switching register P2H	DRCTLP2H	4001 0234H
Buffer switching register P3L	DRCTLP3L	4001 0238H
Buffer switching register P3H	DRCTLP3H	4001 023CH
Buffer switching register P4L	DRCTLP4L	4001 0240H
Buffer switching register P4H	DRCTLP4H	4001 0244H
Buffer switching register P5L	DRCTLP5L	4001 0248H
Buffer switching register P5H	DRCTLP5H	4001 024CH
Buffer switching register P6L	DRCTLP6L	4001 0250H
Buffer switching register P6H	DRCTLP6H	4001 0254H
Buffer switching register P7L	DRCTLP7L	4001 0258H
Buffer switching register P7H	DRCTLP7H	4001 025CH
Buffer switching register RP0L	DRCTLRP0L	4001 0260H
Buffer switching register RP0H	DRCTLRP0H	4001 0264H
Buffer switching register RP1L	DRCTLRP1L	4001 0268H
Buffer switching register RP1H	DRCTLRP1H	4001 026CH
Buffer switching register RP2L	DRCTLRP2L	4001 0270H
Buffer switching register RP2H	DRCTLRP2H	4001 0274H
Buffer switching register RP3L	DRCTLRP3L	4001 0278H
Buffer switching register RP3H	DRCTLRP3H	4001 027CH
Buffer switching register EXTP0L	DRCTLEXTP0L	4001 0280H
Buffer switching register EXTP0H	DRCTLEXTP0H	4001 0284H
Buffer switching register EXTP1L	DRCTLEXTP1L	4001 0288H

Appendix 2.4.1 Port registers (P, RP, EXTP)

CP520 incorporates twelve 8-bit ports and one 10-bit port (EXTP).
Nine are 3-state I/O ports (including EXTP) and four are for real-time control. Input or output can be specified for ports in 1-bit units. The port registers are used for writing the output levels for output port pins. When read, the value of the given port register is read. The PIN, RPIN, and EXTPIN registers are used to read the levels on input pins.
Register details are described in 32-bit notation.

・ P0W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3000H	31 - 24	P37 - P30	R/W	These bits set the value of the output latch when the port is used in output mode. If read, the value of the output latch is read.	0000 0000H
	23 - 16	P27 - P20			
	15 - 8	P17 - P10			
	7 - 0	P07 - P00			

・ P4W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3004H	31 - 24	P77 - P70	R/W	These bits set the value of the output latch when the port is used in output mode. If read, the value of the output latch is read.	0000 0000H
	23 - 16	P67 - P60			
	15 - 8	P57 - P50			
	7 - 0	P47 - P40			

・ EXTP0W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3800H	31 - 10	-	R/W	Reserved (Write: 0 / Read: 0)	0000 0000H
	9 - 0	EXTP9 - EXTP0		These bits set the value of the output latch when the port is used in output mode. If read, the value of the output latch is read.	

・ RP0W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3400H	31 - 24	RP37 - RP30	R/W	These bits set the value of the output latch when the port is used in output mode. If read, the value of the output latch is read.	0000 0000H
	23 - 16	RP27 - RP20			
	15 - 8	RP17 - RP10			
	7 - 0	RP07 - RP00			

Appendix 2.4.2 Port mode registers (PM, RPM, EXTPM)

These registers are used to set a port to input or output mode. Register details are described in 32-bit notation.

・ PM0W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3010H	31 - 24	PM37 - PM30	R/W	These bits set the port to input or output mode. 0b: Output mode (output buffer is on) 1b: Input mode (output buffer is off) (initial value)	FFFF FFFFH
	23 - 16	PM27 - PM20			
	15 - 8	PM17 - PM10			
	7 - 0	PM07 - PM00			

・ PM4W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3014H	31 - 24	PM77 - PM70	R/W	These bits set the port to input or output mode. 0b: Output mode (output buffer is on) 1b: Input mode (output buffer is off) (initial value)	FFFF FFFFH
	23 - 16	PM67 - PM60			
	15 - 8	PM57 - PM50			
	7 - 0	PM47 - PM40			

・ EXTPM0W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3810H	31 - 10	-	R/W	Reserved (Write: 0 / Read: 0)	0000 03FFH
	9 - 0	EXTPM9 - EXTPM0		These bits set the port to input or output mode. 0b: Output mode (output buffer is on) 1b: Input mode (output buffer is off) (initial value)	

・ RPM0W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3410H	31 - 24	RPM37 - RPM30	R/W	These bits set the port to input or output mode. 0b: Output mode (output buffer is on) 1b: Input mode (output buffer is off) (initial value)	FFFF FFFFH
	23 - 16	RPM27 - RPM20			
	15 - 8	RPM17 - RPM10			
	7 - 0	RPM07 - RPM00			

Appendix 2.4.3 Port mode control registers (PMC, RPMC, EXTPMC)

These registers are for selecting whether the port pins are used as port pins or as multiplexed function pins. Register details are described in 32-bit notation.

The multiplexed functions are selected using the following registers:

- Port mode control registers
- Port function control registers
- Port function control expansion registers

For details, refer to Appendix 2.5 "List of selectable multiplexed functions".

- PMC0W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3020H	31 - 24	PMC37 - PMC30	R/W	These bits select whether the port pins are used as port pins or as multiplexed function pins. 0b: Port mode (the inactive level is input for multiplexed input pin functions.) 1b: Multiplexed function (control mode)	0000 0000H*1
	23 - 16	PMC27 - PMC20			
	15 - 8	PMC17 - PMC10			
	7 - 0	PMC07 - PMC00			

*1: The initial value depends on the state of the pins. For details, refer to Section 5.3 "Pin States".

- PMC4W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3024H	31 - 24	PMC77 - PMC70	R/W	These bits select whether the port pins are used as port pins or as multiplexed function pins. 0b: Port mode (the inactive level is input for multiplexed input pin functions.) 1b: Multiplexed function (control mode)	0000 0000H*1
	23 - 16	PMC67 - PMC60			
	15 - 8	PMC57 - PMC50			
	7 - 0	PMC47 - PMC40			

*1: The initial value depends on the state of the pins. For details, refer to Section 5.3 "Pin States".

- EXTPMC0W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3820H	31 - 10	-	R/W	Reserved (Write: 0 / Read: 0)	0000 0000H*1
	9 - 0	EXTPMC9 - EXTPMC0		These bits select whether the port pins are used as port pins or as multiplexed function pins. 0b: Port mode (the inactive level is input for multiplexed input pin functions.) 1b: Multiplexed function (control mode)	

*1: The initial value depends on the state of the pins. For details, refer to Section 5.3 "Pin States".

- RPMC0W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3420H	31 - 24	RPMC37 - RPMC30	R/W	These bits select whether the port pins are used as port pins or as multiplexed function pins. 0b: Port mode (the inactive level is input for multiplexed input pin functions.) 1b: Multiplexed function (control mode)	0000 0000H*1
	23 - 16	RPMC27 - RPMC20			
	15 - 8	RPMC17 - RPMC10			
	7 - 0	RPMC07 - RPMC00			

*1: The initial value depends on the state of the pins. For details, refer to Section 5.3 "Pin States".

Appendix 2.4.4 Port function control registers (PFC, RPFC, EXTPFC)

These registers are used to specify which multiplexed function is to be used. These registers can be set in 1-bit units.
Register details are described in 32-bit notation.
The multiplexed functions are selected using the following registers:

- Port mode control registers
- Port function control registers
- Port function control expansion registers

For details, refer to Appendix 2.5 "List of selectable multiplexed functions".

Remarks
・ To use multiplexed function 1 or 2, the corresponding bit in the PFCE, RPFCE, or EXTPFCE register must be set to 0. ・ To use multiplexed function 3 or 4, the corresponding bit in the PFCE, RPFCE, or EXTPFCE register must be set to 1.

・ PFC0W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3030H	31 - 24	PFC37 - PFC30	R/W	These bits specify whether to use multiplexed function 1 or multiplexed function 2. 0b: Multiplexed function 1, multiplexed function 3 1b: Multiplexed function 2, multiplexed function 4	0000 0000H*1
	23 - 16	PFC27 - PFC20			
	15 - 8	PFC17 - PFC10			
	7 - 0	PFC07 - PFC00			

*1: The initial value depends on the state of the pins. For details, refer to Section 5.3 "Pin States".

・ PFC4W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3034H	31 - 24	PFC77 - PFC70	R/W	These bits specify whether to use multiplexed function 1 or multiplexed function 2. 0b: Multiplexed function 1, multiplexed function 3 1b: Multiplexed function 2, multiplexed function 4	0000 0000H*1
	23 - 16	PFC67 - PFC60			
	15 - 8	PFC57 - PFC50			
	7 - 0	PFC47 - PFC40			

*1: The initial value depends on the state of the pins. For details, refer to Section 5.3 "Pin States".

・ EXTPFC0W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3830H	31 - 10	-	R/W	Reserved (Write: 0 / Read: 0)	0000 0000H
	9 - 0	EXTPFC9 - EXTPFC0		These bits specify whether to use multiplexed function 1 or multiplexed function 2. 0b: Multiplexed function 1, multiplexed function 3 1b: Multiplexed function 2, multiplexed function 4	

・ RPFC0W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3430H	31 - 24	RPFC37 - RPFC30	R/W	These bits specify whether to use multiplexed function 1 or multiplexed function 2. 0b: Multiplexed function 1, multiplexed function 3 1b: Multiplexed function 2, multiplexed function 4	0000 0000H*1
	23 - 16	RPFC27 - RPFC20			
	15 - 8	RPFC17 - RPFC10			
	7 - 0	RPFC07 - RPFC00			

*1: The initial value depends on the state of the pins. For details, refer to Section 5.3 "Pin States".

Appendix 2.4.5 Port function control expansion registers (PFCE, RPFCE, EXTPFCE)

These registers are used to specify which multiplexed extended function is to be used. These registers can be set in 1-bit units. Register details are described in 32-bit notation.

The multiplexed functions are selected using the following registers:

- Port mode control registers
- Port function control registers
- Port function control expansion registers

For details, refer to Appendix 2.5 "List of selectable multiplexed functions".

- PFCE0W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3040H	31 - 24	PFCE37 - PFCE30	R/W	These bits specify whether to use multiplexed function 1 and 2 or multiplexed function 3 and 4. 0b: Multiplexed function 1, multiplexed function 2 1b: Multiplexed function 3, multiplexed function 4	0000 00C0H
	23 - 16	PFCE27 - PFCE20			
	15 - 8	PFCE17 - PFCE10			
	7 - 0	PFCE07 - PFCE00			

- PFCE4W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3044H	31 - 24	PFCE77 - PFCE70	R/W	These bits specify whether to use multiplexed function 1 and 2 or multiplexed function 3 and 4. 0b: Multiplexed function 1, multiplexed function 2 1b: Multiplexed function 3, multiplexed function 4	0000 0000H
	23 - 16	PFCE67 - PFCE60			
	15 - 8	PFCE57 - PFCE50			
	7 - 0	PFCE47 - PFCE40			

- EXTPFCE0W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3840H	31 - 10	-	R/W	Reserved (Write: 0 / Read: 0)	0000 0000H
	9 - 0	EXTPFCE9 - EXTPFCE0		These bits specify whether to use multiplexed function 1 and 2 or multiplexed function 3 and 4. 0b: Multiplexed function 1, multiplexed function 2 1b: Multiplexed function 3, multiplexed function 4	

- RPFCE0W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3440H	31 - 24	RPFCE37 - RPFCE30	R/W	These bits specify whether to use multiplexed function 1 and 2 or multiplexed function 3 and 4. 0b: Multiplexed function 1, multiplexed function 2 1b: Multiplexed function 3, multiplexed function 4	0000 0000H*1
	23 - 16	RPFCE27 - RPFCE20			
	15 - 8	RPFCE17 - RPFCE07			
	7 - 0	RPFCE07 - RPFCE00			

*1: The initial value depends on the state of the pins. For details, refer to Section 5.3 "Pin States".

Appendix 2.4.6 Port pin input registers (PIN, RPIN, EXTPIN)

These are read-only registers for reading the input level of port pins. Register details are described in 32-bit notation.

・ PIN0W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3050H	31 - 24	PIN37 - PIN30	R	These bits are for reading the input level of the port pins.	Pin level
	23 - 16	PIN27 - PIN20			
	15 - 8	PIN17 - PIN10			
	7 - 0	PIN07 - PIN00			

・ PIN4W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3054H	31 - 24	PIN77 - PIN70	R	These bits are for reading the input level of the port pins.	Pin level
	23 - 16	PIN67 - PIN60			
	15 - 8	PIN57 - PIN50			
	7 - 0	PIN47 - PIN40			

・ EXTPIN0W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3850H	31 - 10	-	R	Reserved (Read: 0)	Pin level
	9 - 0	EXTPIN9 - EXTPIN0		These bits are for reading the input level of the port pins.	

・ RPIN0W

Byte Address	Bit	Bit Name	R/W	Description	Initial Value
400A 3450H	31 - 24	RPIN37 - RPIN30	R	These bits are for reading the input level of the port pins.	Pin level
	23 - 16	RPIN27 - RPIN20			
	15 - 8	RPIN17 - RPIN10			
	7 - 0	RPIN07 - RPIN00			

Appendix 2.5 List of selectable multiplexed functions

The table below lists the combinations of multiplexed functions that can be specified by using the port-related registers. (m = 0 to 7, n = 0 to 7)

(1) Ports (P00-P77)

Table Appendix 2.5-1 List of Selectable Multiplexed Functions for Ports (P00-P77)

Pin ID	Pin Name	PMCmn = 0 (Port Mode)		PMCmn = 1 (Control Mode)			
				PFCEmn = 0		PFCEmn = 1	
		PMmn = 0 (Output Port)	PMmn = 1 (Input Port)	PFCmn = 0 (Multiplexed Function 1)	PFCmn = 1 (Multiplexed Function 2)	PFCmn = 0 (Multiplexed Function 3)	PFCmn = 1 (Multiplexed Function 4)
AB10	P00	P00 (output mode)	P00 (input mode)	INTPZ0	-	CCI_RUNLEDZ	P00_RESERVED4
AA10	P01	P01 (output mode)	P01 (input mode)	INTPZ1	-	CCI_USER1LEDZ	P01_RESERVED4
AB9	P02	P02 (output mode)	P02 (input mode)	INTPZ2	-	CCI_DLINKLEDZ	P02_RESERVED4
AA9	P03	P03 (output mode)	P03 (input mode)	INTPZ3	-	CCI_ERRLEDZ	P03_RESERVED4
AB8	P04	P04 (output mode)	P04 (input mode)	INTPZ4	-	CCI_LERR1LEDZ	P04_RESERVED4
AA8	P05	P05 (output mode)	P05 (input mode)	INTPZ5	-	CCI_LERR2LEDZ	P05_RESERVED4
AB7	P06	P06 (output mode)	P06 (input mode)	-	-	CCI_SDLEDZ	P06_RESERVED4
AA7	P07	P07 (output mode)	P07 (input mode)	-	-	CCI_RDLEDZ	P07_RESERVED4
A12	P10	P10 (output mode)	P10 (input mode)	SMIO2	-	-	P10_RESERVED4
A11	P11	P11 (output mode)	P11 (input mode)	SMIO3	-	-	P11_RESERVED4
B12	P12	P12 (output mode)	P12 (input mode)	CSZ3	-	CCI_WDTIZ	P12_RESERVED4
B11	P13	P13 (output mode)	P13 (input mode)	CSZ2	-	P13_RESERVED3	P13_RESERVED4
A10	P14	P14 (output mode)	P14 (input mode)	SMSCK	-	-	P14_RESERVED4
B10	P15	P15 (output mode)	P15 (input mode)	SMIO0	-	-	P15_RESERVED4
A9	P16	P16 (output mode)	P16 (input mode)	SMIO1	-	-	P16_RESERVED4
B9	P17	P17 (output mode)	P17 (input mode)	SMCSZ	-	-	P17_RESERVED4
M22	P20	P20 (output mode)	P20 (input mode)	RXD0	-	P20_RESERVED3	P20_RESERVED4
M21	P21	P21 (output mode)	P21 (input mode)	TXD0	-	P21_RESERVED3	P21_RESERVED4
N22	P22	P22 (output mode)	P22 (input mode)	INTPZ8	-	P22_RESERVED3	P22_RESERVED4
N21	P23	P23 (output mode)	P23 (input mode)	INTPZ9	-	P23_RESERVED3	P23_RESERVED4
N20	P24	P24 (output mode)	P24 (input mode)	INTPZ10	P24_RESERVED2	P24_RESERVED3	P24_RESERVED4
P22	P25	P25 (output mode)	P25 (input mode)	WDTOUTZ	-	P25_RESERVED3	P25_RESERVED4
P21	P26	P26 (output mode)	P26 (input mode)	TINJ1 / TIND5	TOUTJ1 / TOUTD5	P26_RESERVED3	P26_RESERVED4
R21	P27	P27 (output mode)	P27 (input mode)	TINJ0 / TIND4	TOUTJ0 / TOUTD4	-	P27_RESERVED4
Y22	P30	P30 (output mode)	P30 (input mode)	RXD1	-	-	P30_RESERVED4
Y21	P31	P31 (output mode)	P31 (input mode)	TXD1	-	-	P31_RESERVED4
AA21	P32	P32 (output mode)	P32 (input mode)	DMAREQZ1	P32_RESERVED2	P32_RESERVED3	P32_RESERVED4
AA20	P33	P33 (output mode)	P33 (input mode)	DMAACKZ1	-	P33_RESERVED3	P33_RESERVED4
AB19	P34	P34 (output mode)	P34 (input mode)	DMATCZ1	-	-	P34_RESERVED4
AA19	P35	P35 (output mode)	P35 (input mode)	CSISCK1	INTPZ22	-	P35_RESERVED4
AA17	P36	P36 (output mode)	P36 (input mode)	CSISI1	INTPZ23	-	P36_RESERVED4
AA16	P37	P37 (output mode)	P37 (input mode)	CSISO1	INTPZ24	-	P37_RESERVED4
A4	P40	P40 (output mode)	P40 (input mode)	A1	HA1	-	-
B6	P41	P41 (output mode)	P41 (input mode)	WAITZ	HWAITZ	-	-
A5	P42	P42 (output mode)	P42 (input mode)	CSICS00	HERROUTZ	P42_RESERVED3	-
A6	P43	P43 (output mode)	P43 (input mode)	CSICS01	HBUSCLK	P43_RESERVED3	-
B8	P44	P44 (output mode)	P44 (input mode)	CSZ1	HPGCSZ	-	P44_RESERVED4
A7	P45	P45 (output mode)	P45 (input mode)	CSISCK0	WAITZ1	-	-
B7	P46	P46 (output mode)	P46 (input mode)	CSISI0	WAITZ2	-	-
A8	P47	P47 (output mode)	P47 (input mode)	CSISO0	WAITZ3	-	-
AB6	P50	P50 (output mode)	P50 (input mode)	INTPZ6	-	CCI_USER2LEDZ	P50_RESERVED4
AA6	P51	P51 (output mode)	P51 (input mode)	INTPZ7	-	P51_RESERVED3	P51_RESERVED4
AB5	P52	P52 (output mode)	P52 (input mode)	TINJ3 / TIND7	TOUTJ3/ TOUTD7	CCI_NMIZ	P52_RESERVED4
AA5	P53	P53 (output mode)	P53 (input mode)	P53_RESERVED1	CCI_INTZ	-	-
AB4	P54	P54 (output mode)	P54 (input mode)	P54_RESERVED2	P54_RESERVED2	P54_RESERVED3	P54_RESERVED4
AA4	P55	P55 (output mode)	P55 (input mode)	P55_RESERVED2	P55_RESERVED2	P55_RESERVED3	P55_RESERVED4
AB3	P56	P56 (output mode)	P56 (input mode)	P56_RESERVED2	P56_RESERVED2	P56_RESERVED3	-
AA3	P57	P57 (output mode)	P57 (input mode)	TINJ2 / TIND6	TOUTJ2/ TOUTD6	P57_RESERVED3	P57_RESERVED4
W22	P60	P60 (output mode)	P60 (input mode)	SCL0	-	-	P60_RESERVED4
W21	P61	P61 (output mode)	P61 (input mode)	SDA0	-	-	P61_RESERVED4
V21	P62	P62 (output mode)	P62 (input mode)	RTDMAREQZ	ETH_MDC	P62_RESERVED3	P62_RESERVED4
V22	P63	P63 (output mode)	P63 (input mode)	RTDMAACKZ	ETH_MDIO	P63_RESERVED3	P63_RESERVED4
U21	P64	P64 (output mode)	P64 (input mode)	RTDMATCZ	NRESET_OUT	P64_RESERVED3	P64_RESERVED4
U22	P65	P65 (output mode)	P65 (input mode)	DMAREQZ0	FASTLINK_FAIL	P65_RESERVED3	P65_RESERVED4
T21	P66	P66 (output mode)	P66 (input mode)	DMAACKZ0	-	P66_RESERVED3	P66_RESERVED4
T22	P67	P67 (output mode)	P67 (input mode)	DMATCZ0	-	P67_RESERVED3	P67_RESERVED4

Pin ID	Pin Name	PMCmn = 0 (Port Mode)		PMCmn = 1 (Control Mode)			
				PFCEmn = 0		PFCEmn = 1	
		PMmn = 0 (Output Port)	PMmn = 1 (Input Port)	PFCmn = 0 (Multiplexed Function 1)	PFCmn = 1 (Multiplexed Function 2)	PFCmn = 0 (Multiplexed Function 3)	PFCmn = 1 (Multiplexed Function 4)
AA15	P70	P70 (output mode)	P70 (input mode)	CSICS10	P70_RESERVED2	P70_RESERVED3	P70_RESERVED4
AA14	P71	P71 (output mode)	P71 (input mode)	CSICS11	P71_RESERVED2	P71_RESERVED3	P71_RESERVED4
AB13	P72	P72 (output mode)	P72 (input mode)	SLEEPING	P72_RESERVED2	P72_RESERVED3	P72_RESERVED4
AA13	P73	P73 (output mode)	P73 (input mode)	INTPZ11	P73_RESERVED2	P73_RESERVED3	P73_RESERVED4
AB12	P74	P74 (output mode)	P74 (input mode)	INTPZ12	P74_RESERVED2	P74_RESERVED3	P74_RESERVED4
AA12	P75	P75 (output mode)	P75 (input mode)	INTPZ13	XCLK1	P75_RESERVED3	P75_RESERVED4
AB11	P76	P76 (output mode)	P76 (input mode)	INTPZ14	-	P76_RESERVED3	P76_RESERVED4
AA11	P77	P77 (output mode)	P77 (input mode)	INTPZ15	-	P77_RESERVED3	P77_RESERVED4

(2) Real-time ports (RP00-RP37)

Table Appendix 2.5-2 List of Selectable Multiplexed Functions for Real-Time Ports (RP00-RP37)

Pin ID	Pin Name	RPMCmn = 0 (Port Mode)		RPMCmn = 1 (Control Mode)			
				RPFCEmn = 0		RPFCEmn = 1	
		RPMmn = 0 (Output Port)	RPMmn = 1 (Input Port)	RPFCmn = 0 (Multiplexed Function 1)	RPFCmn = 1 (Multiplexed Function 2)	RPFCmn = 0 (Multiplexed Function 3)	RPFCmn = 1 (Multiplexed Function 4)
H22	RP00	RP00 (output mode)	RP00 (input mode)	INTPZ16	SCL1	RP00_RESERVED3	RP00_RESERVED4
H21	RP01	RP01 (output mode)	RP01 (input mode)	INTPZ17	SDA1	RP01_RESERVED3	RP01_RESERVED4
G22	RP02	RP02 (output mode)	RP02 (input mode)	INTPZ18	-	RP02_RESERVED3	RP02_RESERVED4
G21	RP03	RP03 (output mode)	RP03 (input mode)	INTPZ19	-	RP03_RESERVED3	RP03_RESERVED4
F21	RP04	RP04 (output mode)	RP04 (input mode)	INTPZ20	-	RP04_RESERVED3	RP04_RESERVED4
H20	RP05	RP05 (output mode)	RP05 (input mode)	INTPZ21	-	RP05_RESERVED3	RP05_RESERVED4
H19	RP06	RP06 (output mode)	RP06 (input mode)	WRZ2 / BENZ2	HWRZ2 / HBENZ2	-	-
G20	RP07	RP07 (output mode)	RP07 (input mode)	WRZ3 / BENZ3	HWRZ3 / HBENZ3	RP07_RESERVED3	-
C20	RP10	RP10 (output mode)	RP10 (input mode)	D24/HD24	LED0_PHY0	RP10_RESERVED3	-
D20	RP11	RP11 (output mode)	RP11 (input mode)	D25/HD25	LED1_PHY0	RP11_RESERVED3	-
E20	RP12	RP12 (output mode)	RP12 (input mode)	D26/HD26	LED2_PHY0	RP12_RESERVED3	-
F20	RP13	RP13 (output mode)	RP13 (input mode)	D27/HD27	LED3_PHY0	RP13_RESERVED3	-
D19	RP14	RP14 (output mode)	RP14 (input mode)	D28/HD28	LED0_PHY1	RP14_RESERVED3	-
E19	RP15	RP15 (output mode)	RP15 (input mode)	D29/HD29	LED1_PHY1	RP15_RESERVED3	-
F19	RP16	RP16 (output mode)	RP16 (input mode)	D30/HD30	LED2_PHY1	RP16_RESERVED3	-
G19	RP17	RP17 (output mode)	RP17 (input mode)	D31/HD31	LED3_PHY1	RP17_RESERVED3	RP17_RESERVED4
B21	RP20	RP20 (output mode)	RP20 (input mode)	BCYSTZ / ADVZ	HBCYSTZ	RP20_RESERVED3	RP20_RESERVED4
C22	RP21	RP21 (output mode)	RP21 (input mode)	A21	-	RP21_RESERVED3	RP21_RESERVED4
C21	RP22	RP22 (output mode)	RP22 (input mode)	A22	-	RP22_RESERVED3	RP22_RESERVED4
D22	RP23	RP23 (output mode)	RP23 (input mode)	A23	-	RP23_RESERVED3	RP23_RESERVED4
D21	RP24	RP24 (output mode)	RP24 (input mode)	A24	INTPZ25	RP24_RESERVED3	RP24_RESERVED4
E22	RP25	RP25 (output mode)	RP25 (input mode)	A25	INTPZ26	RP25_RESERVED3	RP25_RESERVED4
E21	RP26	RP26 (output mode)	RP26 (input mode)	A26	INTPZ27	RP26_RESERVED3	RP26_RESERVED4
F22	RP27	RP27 (output mode)	RP27 (input mode)	A27	INTPZ28	-	RP27_RESERVED4
A20	RP30	RP30 (output mode)	RP30 (input mode)	D16/HD16	TOUTD8	TIND8	RP30_RESERVED4
A19	RP31	RP31 (output mode)	RP31 (input mode)	D17/HD17	TOUTD9	TIND9	RP31_RESERVED4
B20	RP32	RP32 (output mode)	RP32 (input mode)	D18/HD18	TOUTD10	TIND10	RP32_RESERVED4
B19	RP33	RP33 (output mode)	RP33 (input mode)	D19/HD19	TOUTD11	TIND11	RP33_RESERVED4
B18	RP34	RP34 (output mode)	RP34 (input mode)	D20/HD20	TOUTD12	TIND12	RP34_RESERVED4
B17	RP35	RP35 (output mode)	RP35 (input mode)	D21/HD21	TOUTD13	TIND13	RP35_RESERVED4
C18	RP36	RP36 (output mode)	RP36 (input mode)	D22/HD22	TOUTD14	TIND14	RP36_RESERVED4
C19	RP37	RP37 (output mode)	RP37 (input mode)	D23/HD23	TOUTD15	TIND15	RP37_RESERVED4

(3) EXTP ports (EXTP0-EXTP9)

Table Appendix 2.5-3 List of Selectable Multiplexed Functions for EXTP Ports (EXTP0-EXTP9)

Pin ID	Pin Name	EXTPMCp = 0 (Port Mode)		EXTPMCp = 1 (Control Mode)			
				EXTPFCEp = 0		EXTPFCEp = 1	
		EXTPMp = 0 (Output Port)	EXTPMp = 1 (Input Port)	EXTPFCp = 0 (Multiplexed Function 1)	EXTPFCp = 1 (Multiplexed Function 2)	EXTPFCp = 0 (Multiplexed Function 3)	EXTPFCp = 1 (Multiplexed Function 4)
P20	EXTP0	EXTP0 (output mode)	EXTP0 (input mode)	EXTP0_RESERVED1	TOUTD0	EXTP0_RESERVED3	TIND0
R20	EXTP1	EXTP1 (output mode)	EXTP1 (input mode)	EXTP1_RESERVED1	TOUTD1	EXTP1_RESERVED3	TIND1
T20	EXTP2	EXTP2 (output mode)	EXTP2 (input mode)	EXTP2_RESERVED1	TOUTD2	EXTP2_RESERVED3	TIND2
U20	EXTP3	EXTP3 (output mode)	EXTP3 (input mode)	WDTOUTZ	TOUTD3	EXTP3_RESERVED3	TIND3
Y14	EXTP4	EXTP4 (output mode)	EXTP4 (input mode)	EXTP4_RESERVED1	EXTP4_RESERVED2	EXTP4_RESERVED3	EXTP4_RESERVED4
W14	EXTP5	EXTP5 (output mode)	EXTP5 (input mode)	EXTP5_RESERVED1	EXTP5_RESERVED2	EXTP5_RESERVED3	EXTP5_RESERVED4
Y15	EXTP6	EXTP6 (output mode)	EXTP6 (input mode)	EXTP6_RESERVED1	EXTP6_RESERVED2	EXTP6_RESERVED3	EXTP6_RESERVED4
W15	EXTP7	EXTP7 (output mode)	EXTP7 (input mode)	EXTP7_RESERVED1	EXTP7_RESERVED2	EXTP7_RESERVED3	EXTP7_RESERVED4
Y16	EXTP8	EXTP8 (output mode)	EXTP8 (input mode)	EXTP8_RESERVED1	EXTP8_RESERVED2	EXTP8_RESERVED3	EXTP8_RESERVED4
W16	EXTP9	EXTP9 (output mode)	EXTP9 (input mode)	EXTP9_RESERVED1	EXTP9_RESERVED2	EXTP9_RESERVED3	EXTP9_RESERVED4

Appendix 2.6 Buffer switching registers (DRCTL)

For some port pins, the driving ability and the connection or disconnection of a pull-up or pull-down resistor is programmable.

Set up the DRCTL registers during initialization by a program after release from the reset state. After that, change the setting of a given DRCTL register only while the corresponding pins are not in use. For example, change the setting while only internal access is proceeding.

This register can be read and write in 32- or 16-bit units.

The settings of the DRCTL registers are effective for output pins regardless of their operating mode (port mode, or control mode, in which a multiplexed function is used).

Note

1) These registers are only writable after protection has been released by a special sequence of writing to the system protection command register (SYSPCMD).
   For how to release protection, refer to the description of the system protection command register (SYSPCMD).
   No special sequence is required for reading the register.
2) Take special care with pins in the high-impedance state, since changing the settings for the pull-up and pull-down resistors will place levels on the pins.

Appendix 2.6.1 Port 0 buffer switching register (DRCTLP0L, DRCTLP0H)

• DRCTLP0L

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0220H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	P03 pin	15	PUIOP03	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P03 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIOP03	R/W		
		13	IOLP031	R/W	These bits specify the driving ability of the P03 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		12	IOLP030	R/W		
	P02 pin	11	PUIOP02	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P02 pin. (Same as the P03 pin)	
		10	PDIOP02	R/W		
		9	IOLP021	R/W	These bits specify the driving ability of the P02 pin. (Same as the P03 pin)	
		8	IOLP020	R/W		
	P01 pin	7	PUIOP01	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P01 pin. (Same as the P03 pin)	
		6	PDIOP01	R/W		
		5	IOLP011	R/W	These bits specify the driving ability of the P01 pin. (Same as the P03 pin)	
		4	IOLP010	R/W		
	P00 pin	3	PUIOP00	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P00 pin. (Same as the P03 pin)	
		2	PDIOP00	R/W		
		1	IOLP001	R/W	These bits specify the driving ability of the P00 pin. (Same as the P03 pin)	
		0	IOLP000	R/W		

• DRCTLP0H

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0224H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	P07 pin	15	PUIOP07	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P07 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIOP07	R/W		
		13	IOLP071	R/W	These bits specify the driving ability of the P07 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		12	IOLP070	R/W		
	P06 pin	11	PUIOP06	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P06 pin. (Same as the P07 pin)	
		10	PDIOP06	R/W		
		9	IOLP061	R/W	These bits specify the driving ability of the P06 pin. (Same as the P07 pin)	
		8	IOLP060	R/W		
	P05 pin	7	PUIOP05	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P05 pin. (Same as the P07 pin)	
		6	PDIOP05	R/W		
		5	IOLP051	R/W	These bits specify the driving ability of the P05 pin. (Same as the P07 pin)	
		4	IOLP050	R/W		
	P04 pin	3	PUIOP04	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P04 pin. (Same as the P07 pin)	
		2	PDIOP04	R/W		
		1	IOLP041	R/W	These bits specify the driving ability of the P04 pin. (Same as the P07 pin)	
		0	IOLP040	R/W		

• DRCTLP1L

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0228H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	P13 pin	15	PUIOP13	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P13 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIOP13	R/W		
		13, 12	-	R/W	Reserved (Write: 01b / Read: 01b)	
	P12 pin	11	PUIOP12	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P12 pin. (Same as the P13 pin)	
		10	PDIOP12	R/W		
		9, 8	-	R/W	Reserved (Write: 01b / Read: 01b)	
	P11 pin	7	PUIOP11	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P11 pin. (Same as the P13 pin)	
		6	PDIOP11	R/W		
		5, 4	-	R/W	Reserved (Write: 01b / Read: 01b)	
	P10 pin	3	PUIOP10	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P10 pin. (Same as the P13 pin)	
		2	PDIOP10	R/W		
		1-0	-	R/W	Reserved (Write: 01b / Read: 01b)	

• DRCTLP1H

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 022CH	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	P17 pin	15	PUIOP17	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P17 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIOP17	R/W		
		13, 12	-	R/W	Reserved (Write: 01b / Read: 01b)	
	P16 pin	11	PUIOP16	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P16 pin. (Same as the P17 pin)	
		10	PDIOP16	R/W		
		9, 8	-	R/W	Reserved (Write: 01b / Read: 01b)	
	P15 pin	7	PUIOP15	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P15 pin. (Same as the P17 pin)	
		6	PDIOP15	R/W		
		5, 4	-	R/W	Reserved (Write: 01b / Read: 01b)	
	P14 pin	3	PUIOP14	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P14 pin. (Same as the P17 pin)	
		2	PDIOP14	R/W		
		1-0	-	R/W	Reserved (Write: 01b / Read: 01b)	

• DRCTLP2L

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0230H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	P23 pin	15	PUIOP23	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P23 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIOP23	R/W		
		13	IOLP231	R/W	These bits specify the driving ability of the P23 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		12	IOLP230	R/W		
	P22 pin	11	PUIOP22	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P22 pin. (Same as the P23 pin)	
		10	PDIOP22	R/W		
		9	IOLP221	R/W	These bits specify the driving ability of the P22 pin. (Same as the P23 pin)	
		8	IOLP220	R/W		
	P21 pin	7	PUIOP21	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P21 pin. (Same as the P23 pin)	
		6	PDIOP21	R/W		
		5	IOLP211	R/W	These bits specify the driving ability of the P21 pin. (Same as the P23 pin)	
		4	IOLP210	R/W		
	P20 pin	3	PUIOP20	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P20 pin. (Same as the P23 pin)	
		2	PDIOP20	R/W		
		1	IOLP201	R/W	These bits specify the driving ability of the P20 pin. (Same as the P23 pin)	
		0	IOLP200	R/W		

• DRCTLP2H

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0234H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	P27 pin	15	PUIOP27	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P27 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIOP27	R/W		
		13	IOLP271	R/W	These bits specify the driving ability of the P27 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		12	IOLP270	R/W		
	P26 pin	11	PUIOP26	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P26 pin. (Same as the P27 pin)	
		10	PDIOP26	R/W		
		9	IOLP261	R/W	These bits specify the driving ability of the P26 pin. (Same as the P27 pin)	
		8	IOLP260	R/W		
	P25 pin	7	PUIOP25	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P25 pin. (Same as the P27 pin)	
		6	PDIOP25	R/W		
		5	IOLP251	R/W	These bits specify the driving ability of the P25 pin. (Same as the P27 pin)	
		4	IOLP250	R/W		
	P24 pin	3	PUIOP24	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P24 pin. (Same as the P27 pin)	
		2	PDIOP24	R/W		
		1, 0	-	R/W	Reserved (Write: 01b / Read: 01b)	

• DRCTLP3L

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0238H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	P33 pin	15	PUIOP33	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P33 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIOP33	R/W		
		13	IOLP331	R/W	These bits specify the driving ability of the P33 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		12	IOLP330	R/W		
	P32 pin	11	PUIOP32	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P32 pin. (Same as the P33 pin)	
		10	PDIOP32	R/W		
		9	IOLP321	R/W	These bits specify the driving ability of the P32 pin. (Same as the P33 pin)	
		8	IOLP320	R/W		
	P31 pin	7	PUIOP31	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P31 pin. (Same as the P33 pin)	
		6	PDIOP31	R/W		
		5	IOLP311	R/W	These bits specify the driving ability of the P31 pin. (Same as the P33 pin)	
		4	IOLP310	R/W		
	P30 pin	3	PUIOP30	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P30 pin. (Same as the P33 pin)	
		2	PDIOP30	R/W		
		1	IOLP301	R/W	These bits specify the driving ability of the P30 pin. (Same as the P33 pin)	
		0	IOLP300	R/W		

• DRCTLP3H

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 023CH	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 5959H
	P37 pin	15	PUIOP37	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P37 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIOP37	R/W		
		13	IOLP371	R/W	These bits specify the driving ability of the P37 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		12	IOLP370	R/W		
	P36 pin	11	PUIOP36	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P36 pin. (Same as the P37 pin)	
		10	PDIOP36	R/W		
		9, 8	-	R/W	Reserved (Write: 01b / Read: 01b)	
	P35 pin	7	PUIOP35	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P35 pin. (Same as the P37 pin)	
		6	PDIOP35	R/W		
		5	IOLP351	R/W	These bits specify the driving ability of the P35 pin. (Same as the P37 pin)	
		4	IOLP350	R/W		
	P34 pin	3	PUIOP34	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P34 pin. (Same as the P37 pin)	
		2	PDIOP34	R/W		
		1	IOLP341	R/W	These bits specify the driving ability of the P34 pin. (Same as the P37 pin)	
		0	IOLP340	R/W		

• DRCTLP4L

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0240H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	P43 pin	15	PUIOP43	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P43 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIOP43	R/W		
		13, 12	-	R/W	Reserved (Write: 01b / Read: 01b)	
	P42 pin	11	PUIOP42	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P42 pin. (Same as the P43 pin)	
		10	PDIOP42	R/W		
		9, 8	-	R/W	Reserved (Write: 01b / Read: 01b)	
	P41 pin	7	PUIOP41	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P41 pin. (Same as the P43 pin)	
		6	PDIOP41	R/W		
		5, 4	-	R/W	Reserved (Write: 01b / Read: 01b)	
	P40 pin	3	PUIOP40	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P40 pin. (Same as the P43 pin)	
		2	PDIOP40	R/W		
		1-0	-	R/W	Reserved (Write: 01b / Read: 01b)	

• DRCTLP4H

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0244H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	P47 pin	15	PUIOP47	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P47 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIOP47	R/W		
		13, 12	-	R/W	Reserved (Write: 01b / Read: 01b)	
	P46 pin	11	PUIOP46	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P46 pin. (Same as the P47 pin)	
		10	PDIOP46	R/W		
		9, 8	-	R/W	Reserved (Write: 01b / Read: 01b)	
	P45 pin	7	PUIOP45	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P45 pin. (Same as the P47 pin)	
		6	PDIOP45	R/W		
		5, 4	-	R/W	Reserved (Write: 01b / Read: 01b)	
	P44 pin	3	PUIOP44	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P44 pin. (Same as the P47 pin)	
		2	PDIOP44	R/W		
		1	IOLP441	R/W	These bits specify the driving ability of the P44 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		0	IOLP440	R/W		

• DRCTLP5L

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0248H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 0999H
	-	15-12	-	R/W	Reserved (Write: 0 / Read: 0)	
	P52 pin	11	PUIOP52	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P52 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		10	PDIOP52	R/W		
		9, 8	-	R/W	Reserved (Write: 01b / Read: 01b)	
	P51 pin	7	PUIOP51	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P51 pin. (Same as the P52 pin)	
		6	PDIOP51	R/W		
		5, 4	-	R/W	Reserved (Write: 01b / Read: 01b)	
	P50 pin	3	PUIOP50	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P50 pin. (Same as the P52 pin)	
		2	PDIOP50	R/W		
		1	IOLP501	R/W	These bits specify the driving ability of the P50 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		0	IOLP500			

• DRCTLP5H

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 024CH	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9000H
	P57 pin	15	PUIOP57	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P57 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIOP57	R/W		
		13, 12	-	R/W	Reserved (Write: 01b / Read: 01b)	
	-	11-0	-	R/W	Reserved (Write: 0 / Read: 0)	

• DRCTLP6L

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0250H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	P63 pin	15	PUIOP63	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P63 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIOP63	R/W		
		13	IOLP631	R/W	These bits specify the driving ability of the P63 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		12	IOLP630	R/W		
	P62 pin	11	PUIOP62	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P62 pin. (Same as the P63 pin)	
		10	PDIOP62	R/W		
		9	IOLP621	R/W	These bits specify the driving ability of the P62 pin. (Same as the P63 pin)	
		8	IOLP620	R/W		
	P61 pin	7	PUIOP61	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P61 pin. (Same as the P63 pin)	
		6	PDIOP61	R/W		
		5	IOLP611	R/W	These bits specify the driving ability of the P61 pin. (Same as the P63 pin)	
		4	IOLP610	R/W		
	P60 pin	3	PUIOP60	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P60 pin. (Same as the P63 pin)	
		2	PDIOP60	R/W		
		1	IOLP601	R/W	These bits specify the driving ability of the P60 pin. (Same as the P63 pin)	
		0	IOLP600	R/W		

• DRCTLP6H

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0254H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	P67 pin	15	PUIOP67	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P67 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIOP67	R/W		
		13	IOLP671	R/W	These bits specify the driving ability of the P67 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		12	IOLP670	R/W		
	P66 pin	11	PUIOP66	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P66 pin. (Same as the P67 pin)	
		10	PDIOP66	R/W		
		9	IOLP661	R/W	These bits specify the driving ability of the P66 pin. (Same as the P67 pin)	
		8	IOLP660	R/W		
	P65 pin	7	PUIOP65	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P65 pin. (Same as the P67 pin)	
		6	PDIOP65	R/W		
		5	IOLP651	R/W	These bits specify the driving ability of the P65 pin. (Same as the P67 pin)	
		4	IOLP650	R/W		
	P64 pin	3	PUIOP64	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P64 pin. (Same as the P67 pin)	
		2	PDIOP64	R/W		
		1	IOLP641	R/W	These bits specify the driving ability of the P64 pin. (Same as the P67 pin)	
		0	IOLP640	R/W		

• DRCTLP7L

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0258H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	P73 pin	15	PUIOP73	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P73 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIOP73	R/W		
		13	IOLP731	R/W	These bits specify the driving ability of the P73 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		12	IOLP730	R/W		
	P72 pin	11	PUIOP72	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P72 pin. (Same as the P73 pin)	
		10	PDIOP72	R/W		
		9	IOLP721	R/W	These bits specify the driving ability of the P72 pin. (Same as the P73 pin)	
		8	IOLP720	R/W		
	P71 pin	7	PUIOP71	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P71 pin. (Same as the P73 pin)	
		6	PDIOP71	R/W		
		5	IOLP711	R/W	These bits specify the driving ability of the P71 pin. (Same as the P73 pin)	
		4	IOLP710	R/W		
	P70 pin	3	PUIOP70	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P70 pin. (Same as the P73 pin)	
		2	PDIOP70	R/W		
		1	IOLP701	R/W	These bits specify the driving ability of the P70 pin. (Same as the P73 pin)	
		0	IOLP700	R/W		

• DRCTLP7H

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 025CH	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	P77 pin	15	PUIOP77	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P77 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIOP77	R/W		
		13	IOLP771	R/W	These bits specify the driving ability of the P77 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		12	IOLP770	R/W		
	P76 pin	11	PUIOP76	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P76 pin. (Same as the P77 pin)	
		10	PDIOP76	R/W		
		9	IOLP761	R/W	These bits specify the driving ability of the P76 pin. (Same as the P77 pin)	
		8	IOLP760	R/W		
	P75 pin	7	PUIOP75	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P75 pin. (Same as the P77 pin)	
		6	PDIOP75	R/W		
		5	IOLP751	R/W	These bits specify the driving ability of the P75 pin. (Same as the P77 pin)	
		4	IOLP750	R/W		
	P74 pin	3	PUIOP74	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the P74 pin. (Same as the P77 pin)	
		2	PDIOP74	R/W		
		1	IOLP741	R/W	These bits specify the driving ability of the P74 pin. (Same as the P77 pin)	
		0	IOLP740	R/W		

Appendix 2.6.9 EXT port 0 buffer switching registers (DRCTLEXTP0L, DRCTLEXTP0H)

• DRCTLEXTP0L

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0280H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	EXTP3 pin	15	PUIOE03	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the EXTP3 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIOE03	R/W		
		13, 12	-	R/W	Reserved (Write: 01b / Read: 01b)	
	EXTP2 pin	11	PUIOE02	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the EXTP2 pin. (Same as the EXTP3 pin)	
		10	PDIOE02	R/W		
		9, 8	-	R/W	Reserved (Write: 01b / Read: 01b)	
	EXTP1 pin	7	PUIOE01	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the EXTP1 pin. (Same as the EXTP3 pin)	
		6	PDIOE01	R/W		
		5, 4	-	R/W	Reserved (Write: 01b / Read: 01b)	
	EXTP0 pin	3	PUIOE00	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the EXTP0 pin. (Same as the EXTP3 pin)	
		2	PDIOE00	R/W		
		1	IOLE001	R/W	These bits specify the driving ability of the EXTP0 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		0	IOLE000	R/W		

• DRCTLEXTP0H

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0284H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9599H
	EXTP7 pin	15	PUIOE07	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the EXTP7 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIOE07	R/W		
		13	IOLE071	R/W	These bits specify the driving ability of the EXTP7 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		12	IOLE070	R/W		
	EXTP6 pin	11	PUIOE06	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the EXTP6 pin. (Same as the EXTP7 pin)	
		10	PDIOE06	R/W		
		9	IOLE061	R/W	These bits specify the driving ability of the EXTP6 pin. (Same as the EXTP7 pin)	
		8	IOLE061	R/W		
	EXTP5 pin	7	PUIOE05	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the EXTP5 pin. (Same as the EXTP7 pin)	
		6	PDIOE05	R/W		
		5, 4	-	R/W	Reserved (Write: 01b / Read: 01b)	
	EXTP4 pin	3	PUIOE04	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the EXTP4 pin. (Same as the EXTP7 pin)	
		2	PDIOE04	R/W		
		1, 0	-	R/W	Reserved (Write: 01b / Read: 01b)	

Appendix 2.6.10 EXT port 1 buffer switching register (DRCTLEXTP1L)

• DRCTLEXTP1L

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0288H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 0099H
	-	15-8	-	R/W	Reserved (Write: 0 / Read: 0)	
	EXTP9 pin	7	PUIOE09	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the EXTP9 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		6	PDIOE09	R/W		
		5, 4	-	R/W	Reserved (Write: 01b / Read: 01b)	
	EXTP8 pin	3	PUIOE08	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the EXTP8 pin. (Same as the EXTP9 pin)	
		2	PDIOE08	R/W		
		1, 0	-	R/W	Reserved (Write: 01b / Read: 01b)	

Appendix 2.6.11 Real-time port 0 buffer switching register (DRCTLRP0L, DRCTLRP0H)

• DRCTLRP0L

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0260H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	RP03 pin	15	PUIORP03	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP03 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIORP03	R/W		
		13	IOLRP031	R/W	These bits specify the driving ability of the RP03 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		12	IOLRP030	R/W		
	RP02 pin	11	PUIORP02	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP02 pin. (Same as the RP03 pin)	
		10	PDIORP02	R/W		
		9	IOLRP021	R/W	These bits specify the driving ability of the RP02 pin. (Same as the RP03 pin)	
		8	IOLRP020	R/W		
	RP01 pin	7	PUIORP01	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP01 pin. (Same as the RP03 pin)	
		6	PDIORP01	R/W		
		5	IOLRP011	R/W	These bits specify the driving ability of the RP01 pin. (Same as the RP03 pin)	
		4	IOLRP010	R/W		
	RP00 pin	3	PUIORP00	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP00 pin. (Same as the RP03 pin)	
		2	PDIORP00	R/W		
		1	IOLRP001	R/W	These bits specify the driving ability of the RP00 pin. (Same as the RP03 pin)	
		0	IOLRP000	R/W		

• DRCTLRP0H

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0264H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	RP07 pin	15	PUIORP07	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP07 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIORP07	R/W		
		13, 12	-	R/W	Reserved (Write: 01b / Read: 01b)	
	RP06 pin	11	PUIORP06	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP06 pin. (Same as the RP07 pin)	
		10	PDIORP06	R/W		
		9, 8	-	R/W	Reserved (Write: 01b / Read: 01b)	
	RP05 pin	7	PUIORP05	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP05 pin. (Same as the RP07 pin)	
		6	PDIORP05	R/W		
		5, 4	-	R/W	Reserved (Write: 01b / Read: 01b)	
	RP04 pin	3	PUIORP04	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP04 pin. (Same as the RP07 pin)	
		2	PDIORP04	R/W		
		1	IOLRP041	R/W	These bits specify the driving ability of the RP04 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		0	IOLRP040	R/W		

• DRCTLRP1L

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0268H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	RP13 pin	15	PUIORP13	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP13 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIORP13	R/W		
		13	IOLRP131	R/W	These bits specify the driving ability of the RP13 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		12	IOLRP130	R/W		
	RP12 pin	11	PUIORP12	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP12 pin. (Same as the RP13 pin)	
		10	PDIORP12	R/W		
		9	IOLRP121	R/W	These bits specify the driving ability of the RP12 pin. (Same as the RP13 pin)	
		8	IOLRP120	R/W		
	RP11 pin	7	PUIORP11	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP11 pin. (Same as the RP13 pin)	
		6	PDIORP11	R/W		
		5	IOLRP111	R/W	These bits specify the driving ability of the RP11 pin. (Same as the RP13 pin)	
		4	IOLRP110	R/W		
	RP10 pin	3	PUIORP10	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP10 pin. (Same as the RP13 pin)	
		2	PDIORP10	R/W		
		1	IOLRP101	R/W	These bits specify the driving ability of the RP10 pin. (Same as the RP13 pin)	
		0	IOLRP100	R/W		

• DRCTLRP1H

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 026CH	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	RP17 pin	15	PUIORP17	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP17 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIORP17	R/W		
		13	IOLRP171	R/W	These bits specify the driving ability of the RP17 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		12	IOLRP170	R/W		
	RP16 pin	11	PUIORP16	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP16 pin. (Same as the RP17 pin)	
		10	PDIORP16	R/W		
		9	IOLRP161	R/W	These bits specify the driving ability of the RP16 pin. (Same as the RP17 pin)	
		8	IOLRP160	R/W		
	RP15 pin	7	PUIORP15	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP15 pin. (Same as the RP17 pin)	
		6	PDIORP15	R/W		
		5	IOLRP151	R/W	These bits specify the driving ability of the RP15 pin. (Same as the RP17 pin)	
		4	IOLRP150	R/W		
	RP14 pin	3	PUIORP14	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP14 pin. (Same as the RP17 pin)	
		2	PDIORP14	R/W		
		1	IOLRP141	R/W	These bits specify the driving ability of the RP14 pin. (Same as the RP17 pin)	
		0	IOLRP140	R/W		

• DRCTLRP2L

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0270H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	RP23 pin	15	PUIORP23	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP23 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIORP23	R/W		
		13	IOLRP231	R/W	These bits specify the driving ability of the RP23 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		12	IOLRP230	R/W		
	RP22 pin	11	PUIORP22	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP22 pin. (Same as the RP23 pin)	
		10	PDIORP22	R/W		
		9	IOLRP221	R/W	These bits specify the driving ability of the RP22 pin. (Same as the RP23 pin)	
		8	IOLRP220	R/W		
	RP21 pin	7	PUIORP21	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP21 pin. (Same as the RP23 pin)	
		6	PDIORP21	R/W		
		5	IOLRP211	R/W	These bits specify the driving ability of the RP21 pin. (Same as the RP23 pin)	
		4	IOLRP210	R/W		
	RP20 pin	3	PUIORP20	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP20 pin. (Same as the RP23 pin)	
		2	PDIORP20	R/W		
		1	IOLRP201	R/W	These bits specify the driving ability of the RP20 pin. (Same as the RP23 pin)	
		0	IOLRP200	R/W		

• DRCTLRP2H

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0274H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	RP27 pin	15	PUIORP27	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP27 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIORP27	R/W		
		13	IOLRP271	R/W	These bits specify the driving ability of the RP27 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		12	IOLRP270	R/W		
	RP26 pin	11	PUIORP26	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP26 pin. (Same as the RP27 pin)	
		10	PDIORP26	R/W		
		9	IOLRP261	R/W	These bits specify the driving ability of the RP26 pin. (Same as the RP27 pin)	
		8	IOLRP260	R/W		
	RP25 pin	7	PUIORP25	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP25 pin. (Same as the RP27 pin)	
		6	PDIORP25	R/W		
		5	IOLRP251	R/W	These bits specify the driving ability of the RP25 pin. (Same as the RP27 pin)	
		4	IOLRP250	R/W		
	RP24 pin	3	PUIORP24	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP24 pin. (Same as the RP27 pin)	
		2	PDIORP24	R/W		
		1	IOLRP241	R/W	These bits specify the driving ability of the RP24 pin. (Same as the RP27 pin)	
		0	IOLRP240	R/W		

• DRCTLRP3L

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 0278H	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	RP33 pin	15	PUIORP33	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP33 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIORP33	R/W		
		13	IOLRP331	R/W	These bits specify the driving ability of the RP33 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		12	IOLRP330	R/W		
	RP32 pin	11	PUIORP32	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP32 pin. (Same as the RP33 pin)	
		10	PDIORP32	R/W		
		9, 8	-	R/W	Reserved (Write: 01b / Read: 01b)	
	RP31 pin	7	PUIORP31	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP31 pin. (Same as the RP33 pin)	
		6	PDIORP31	R/W		
		5, 4	-	R/W	Reserved (Write: 01b / Read: 01b)	
	RP30 pin	3	PUIORP30	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP30 pin. (Same as the RP33 pin)	
		2	PDIORP30	R/W		
		1, 0	-	R/W	Reserved (Write: 01b / Read: 01b)	

• DRCTLRP3H

Byte Address	Item	Bit	Bit Name	R/W	Description	Initial Value
BASE + 027CH	-	31-16	-	R/W	Reserved (Write: 0 / Read: 0)	0000 9999H
	RP37 pin	15	PUIORP37	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP37 pin. 00b: Do not connect a pull-up or pull-down resistor. 01b: Connect a pull-down resistor. 10b: Connect a pull-up resistor. 11b: Setting prohibited	
		14	PDIORP37	R/W		
		13, 12	-	R/W	Reserved (Write: 01b / Read: 01b)	
	RP36 pin	11	PUIORP36	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP36 pin. (Same as the RP37 pin)	
		10	PDIORP36	R/W		
		9, 8	-	R/W	Reserved (Write: 01b / Read: 01b)	
	RP35 pin	7	PUIORP35	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP35 pin. (Same as the RP37 pin)	
		6	PDIORP35	R/W		
		5, 4	-	R/W	Reserved (Write: 01b / Read: 01b)	
	RP34 pin	3	PUIORP34	R/W	These bits specify whether to connect a pull-up or pull-down resistor to the RP34 pin. (Same as the RP37 pin)	
		2	PDIORP34	R/W		
		1	IOLRP341	R/W	These bits specify the driving ability of the RP34 pin. 01b: 6mA (recommended) 11b: 12mA Other than the above: Setting prohibited	
		0	IOLRP340	R/W		

Appendix 2.7 Operation of port functions

Operation of the ports differs depending on the I/O mode setting as described below.

Appendix 2.7.1 Reading and writing via I/O ports

(1) In output mode

If a value is written to a port register (Pn, RPm, or EXTPp), the value is written to that port's output latch (Pn, RPm, or EXTPp). The value of the output latch is output from the pin. The value written to the output latch is held until another value is written.

The value of the output latch (Pn, RPm, or EXTPp) can be read by reading the port register (Pn, RPm, or EXTPp).

To directly read the pin level, read a port pin input register (PINn, RPINm, or EXTPINp).
(n = 0 to 7, m = 0 to 3, p = 0, 1)

(2) In input mode

If a value is written to a port register (Pn, RPm, or EXTPp), the value is written to that port's output latch (Pn, RPm, or EXTPp). However, the pin state does not change because the output buffer is off.
The value written to the output latch is held until another value is written.

To read the input level, read a port pin input register (PINn, RPINm, or EXTPINp).
(n = 0 to 7, m = 0 to 3, p = 0, 1)

Appendix 2.7.2 Multiplexed function pin output state in control mode

The port pin level can be read directly by reading port pin input register n, m, or p (PINn, RPINm, or EXTPINp), regardless of the settings of the PMCn, RPMCm, and EXTPMCp registers, PMn, RPMm, and EXTPMp registers, PFCn, RPFCm, and EXTPFCp registers, and PFCEn, RPCEm, and EXTPEp registers.
(n = 0 to 7, m = 0 to 3, p = 0, 1)

Appendix 2.7.3 Trigger-synchronous ports (RP00-RP37)

The state of the 32-bit port pins RP00-RP37 can be updated in synchronization with an interrupt from an on-chip peripheral module.

Use the RPTRGMD register to set trigger-synchronous port control mode in 1-bit units. To select the target trigger, use the RPTFR0-RPTFR3 registers.

For details, refer to Section 9.7 "Trigger-Synchronous Port Source Registers (RP0TFR-RP3TFR)".

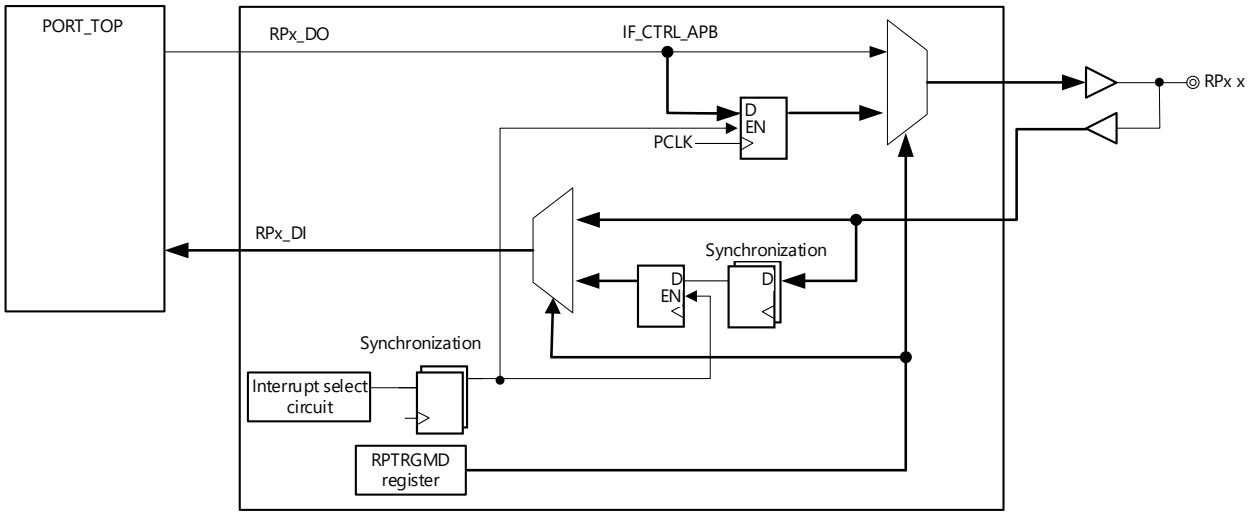


Figure Appendix 2.7.3-1 Configuration of Trigger-Synchronous Ports

Revisions

* The manual number is given on the bottom left of the back cover.

Print Date	*Manual Number	Revision
June 2016	SH(NA)-081570ENG-A	First Edition
March 2017	SH(NA)-081570ENG-B	Added Section 2.14.1 Modified CC-Link Partner Association (CLPA), Related Manuals, Section 2.12, Section 2.14, Section 3.8, Section 3.13, Section 3.13.2, Section 3.13.3, Section 3.14.2, Section 3.15, Section 4.1, Section 4.3.1, Section 4.3.2, Section 4.4, Section 4.5.2, Section 4.6.6, Section 4.6.8, Section 4.8.1, Section 4.8.2, Section 5.2, Section 5.3.3, Section 5.4, Section 6.3, Sections 6.7.6 to 6.7.9, Section 7.1, Section 7.2, Section 7.4, Sections 7.7 to 7.9, Section 8.1, Section 8.2.1, Section 8.2.7, Section 8.2.10, Section 8.2.11, Section 8.2.12, Section 8.2.14, Section 8.3.2, Section 8.3.5, Section 8.3.6, Section 8.3.13, Section 8.3.14, Sections 8.3.16 to 8.3.18, Section 8.4.1, Section 8.4.2, Section 9.2, Section 9.3.1, Sections 9.3.3 to 9.3.5, Section 9.3.7, Section 9.3.8, Section 9.3.13, Section 9.3.14, Section 9.5, Section 10.1, Sections 11.1 to 11.3, Section 11.5, Appendix 1.2, Appendix 1.3, Appendix 1.3.6, Appendix 1.4, Appendix 1.4.1, Appendix 1.4.2, Appendix 2.1, Appendix 2.2, Appendix 2.7.1 Deleted Section 7.5 Sections 7.6 to 7.12 are changed to Sections 7.5 to 7.11.
June 2017	SH(NA)-081570ENG-C	Modified Section 2.12, Section 3.14.2, Section 8.2.7, Section 8.2.10
July 2017	SH(NA)-081570ENG-D	Added Section 5.2.1, Section 5.2.2 Modified Section 1.3, Section 5.1, Section 5.2
June 2019	SH(NA)-081570ENG-E	Entire modification
March 2021	SH(NA)-081570ENG-F	Modified Notes Regarding This Manual, Relevant Manuals, Usage Precautions, CC-Link Partner Association (CLPA), Section 1.4, Section 1.7, Section 2.1, Section 2.3, Section 2.5, Section 2.6, Section 2.10, Section 3.2.3, Section 3.6, Section 4.6, Section 4.7.1, Section 5.2.1, Section 5.2.3, Section 5.2.4, Section 5.2.8, Section 5.2.16, Section 6.7.3, Section 6.7.5, Section 7.1, Section 7.2.1, Chapter 8, Chapter 9, Section 9.7, Section 9.8, Section 10.2.1, Section 10.3.2, Section 11.3.1, Section 11.3.6, Section 11.5, Trademarks Deleted Appendix 1.3.1 to Appendix 1.3.3 Appendix 1.3.4 to Appendix 1.3.6 are changed to Appendix 1.3.1 to Appendix 1.3.3.
March 2022	SH(NA)-081570ENG-G	Added/Modified Usage Precautions, Section 1.4, Section 2.11.1, Section 7.2.2, Section 10.2.1, Section 10.3.2, Section 10.3.4, Section 10.3.7, Section 10.3.13, Appendix 1.1

Warranty

Please confirm the following product warranty details before using the dedicated LSI.

1. Gratis Warranty Term and Gratis Warranty Range

If any faults or defects (hereinafter "Failure") found to be the responsibility of Mitsubishi occurs during use of the product within the gratis warranty term, the product shall be replaced at no cost via the sales representative or Mitsubishi Service Company.

[Gratis Warranty Term]

The gratis warranty term of the product shall be for one year after the date of purchase or delivery to a designated place. Note that after manufacture and shipment from Mitsubishi, the maximum distribution period shall be six (6) months, and the longest gratis warranty term after manufacturing shall be eighteen (18) months.

[Gratis Warranty Range]

(1) The range shall be limited to normal use within the usage state, usage methods and usage environment, etc., which follow the conditions and precautions, etc., given in the instruction manual, user's manual and caution labels on the product.

(2) Even within the gratis warranty term, a replacement fee shall be applied in the following cases.
   [1] Failure occurring from inappropriate storage or handling, carelessness or negligence by the user. Failure caused by the user's hardware or software design.
   [2] Failure caused by unapproved modifications, etc., to the product by the user.
   [3] When the Mitsubishi product is assembled into a user's device, failure that could have been avoided if functions or structures, judged as necessary in the legal safety measures the user's device is subject to or as necessary by industry standards, had been provided.
   [4] Failure caused by external irresistible forces such as fires or abnormal voltages, and failure caused by force majeure such as earthquakes, lightning, wind and water damage.
   [5] Failure caused by reasons unpredictable by scientific technology standards at time of shipment from Mitsubishi.
   [6] Any other failure found not to be the responsibility of Mitsubishi or that admitted not to be so by the user.

2. Handling after discontinuation of production

(1) Discontinuation of production shall be notified with Mitsubishi Technical Bulletins, etc.

(2) Product supply (including repair parts) is not available after production is discontinued.

3. Customer service

(1) When the cause of failure requires an investigation, Mitsubishi shall conduct the investigation using the dedicated LSI unit only. Please bring the dedicated LSI removed from the product to which it was incorporated to Mitsubishi. Mitsubishi will not conduct business travel in connection with the investigation.

(2) Overseas, replacements shall be provided by Mitsubishi's local FA Centers. Note that the conditions under which replacements are provided by each FA Center differ.

4. Exclusion of loss in opportunity and secondary loss from warranty liability

Regardless of the gratis warranty term, Mitsubishi shall not be liable for compensation to:

(1) Damages caused by any cause found not to be the responsibility of Mitsubishi.

(2) Loss in opportunity, lost profits incurred to the user by Failures of Mitsubishi products.

(3) Special damages and secondary damages whether foreseeable or not, compensation for accidents, and compensation for damages to products other than Mitsubishi products.

(4) Replacement by the user, maintenance of on-site equipment, start-up test run and other tasks.

5. Changes in product specifications

The specifications given in the catalogs, manuals, and technical documents are subject to change without prior notice.

Trademarks

Ethernet Based Open Network
CC-Link IE Compatible Product Reference Manual

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