

1200V LARGE DIIPM Ver.4 Series APPLICATION NOTE

PS22A7x

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1200V LARGE DIIPM Ver.4 Series APPLICATION NOTE

CHAPTER 1 INTRODUCTION

This application note describes the main features of 1200V Large DIIPM Ver.4 Series.

For the successor product, 1200V Large DIIPM Ver.6 series (PSSxxSA2FT) are available with same package and pin layout. When designing new products, Ver.6 series is recommended instead of Ver.4 series. For details about the Ver.6 series and differences from the Ver.4 series, refer to the Ver.6 series datasheets and application note.

1.1 Target Applications

Motor drives for industrial use, such as packaged air conditioners, general-purpose inverter, servo, except for automotive applications.

1.2 Product Line-up

Table 1-1 Line-up

Type Name	IGBT Rating	Motor Rating (Note 1)	Isolation Voltage
PS22A72	5A/1200V	0.75kW/440V AC	$V_{iso} = 2500V_{rms}$ (Sine 60Hz, 1min All shorted pins-heat sink)
PS22A73	10A/1200V	1.5kW/440V AC	
PS22A74	15A/1200V	2.2kW/440V AC	
PS22A76	25A/1200V	3.7kW/440V AC	
PS22A78-E	35A/1200V	5.5kW/440V AC	
PS22A79	50A/1200V	7.5kW/440V AC	

Note 1: These motor ratings are general ratings, so those may be changed by conditions.

1.3 Functions and Features

1200V Large DIIPM Ver.4 is a compact intelligent power module with transfer molding package favorable for larger mass production. And it includes power chips, drive and protection circuits.

1200V Large DIIPM Ver.4 realized higher thermal radiation performance by the insulated structure with high thermal conducting insulated sheet, so that it has higher current rating line-up up to 50A despite its mounting area decreases to 75% compared with previous 1200V Large DIIPM (Line-up is up to 25A).

In addition, since 600V rating series up to 75A are available with same package and pin layout, it is able to use the same designed PCB.

Outline photograph and internal cross-section structure are described in Fig.1-1 and Fig.1-2.

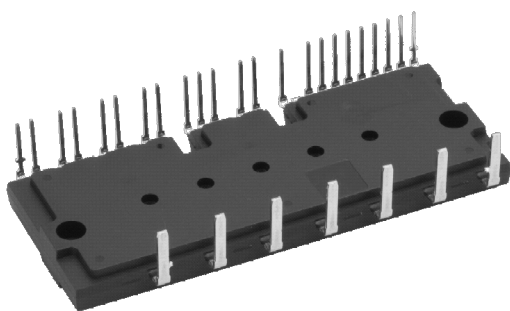


Fig.1-1 Package outline

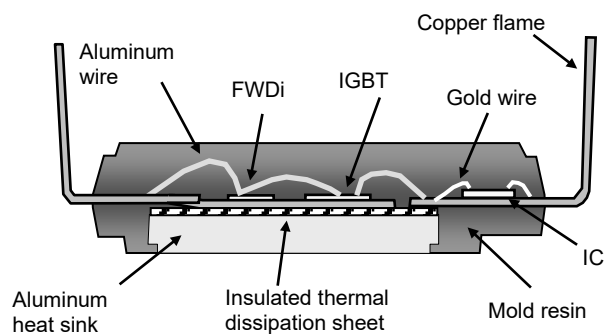


Fig.1-2 Internal cross-section structure

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Features:

- For P-side IGBTs
 - Drive circuit
 - High voltage level shift circuit
 - Control supply under voltage (UV) protection circuit (without fault signal output)
- For N-side IGBTs
 - Drive circuit
 - Short circuit (SC) protection circuit (by detecting sense current divided at N-side IGBT with external sense resistor)
 - Control supply under voltage (UV) protection circuit (with fault signal output)
 - Analog output of LVIC temperature
- Fault Signal Output
 - Corresponding to SC protection and N-side UV protection
- IGBT Drive Supply
 - Single DC15V power supply
- Control Input Interface
 - High active logic
- UL recognized
 - UL1557 File E80276

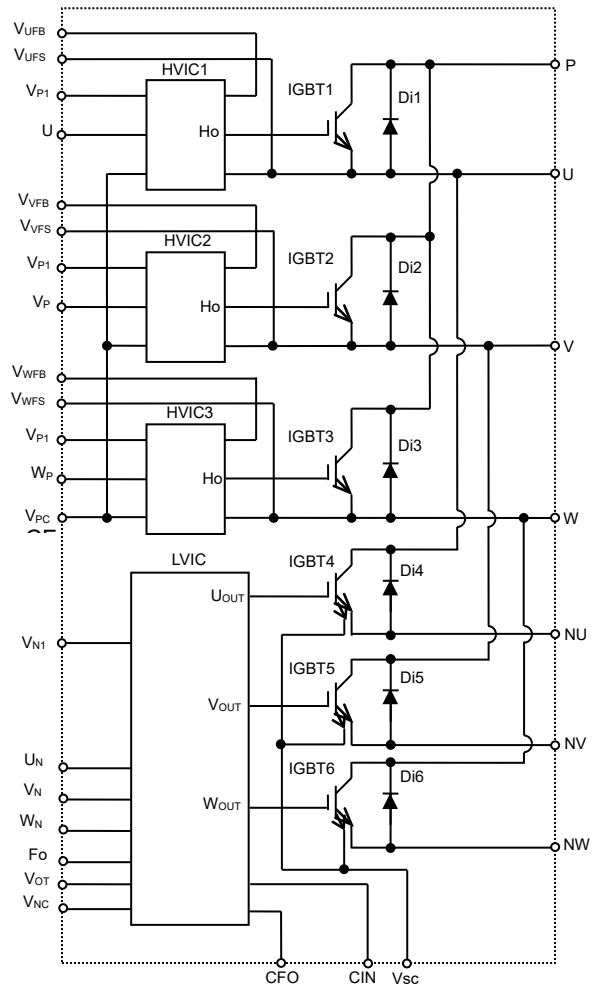


Fig.1-3 Internal circuit schematic

1.4 The Differences of Previous Series (1200V Large DIIPM PS2205*) and This Series

(1) Enlargement of maximum current rating to 50A

Due to change its insulation structure from mold resin insulation to insulated thermal dissipation sheet, it became possible to decrease the thermal resistance between junction and case $R_{th(j-c)}$ substantially. And also it incorporates Mitsubishi's latest power chips CSTBT. So that despite its mounting area decreases to 75%, it realized higher current rating up to 50A.

(2) Changing the method of short circuit protection (SC)

In the previous series the shunt resistor was inserted between N terminal and power GND line for detecting short circuit current. But the loss at the resistor escalates with increasing current rating, so high wattage type resistor is needed. In this series, the current detection method was changed to the one of detecting slight sense current divided from main current by using on-chip current sense IGBTs. So that the shunt resistor inserted to main flow path for SC protection becomes unnecessary and it can decrease loss. For more detail, refer [Section 2.2.1](#).

(3) Analog output function of LVIC temperature

This function measures temperature of the control LVIC by built in temperature detecting circuit on LVIC and output it by analog signal. But the heat generated at IGBT and FWDi transfers to LVIC through the mold package and the inner and outer heat sink. So that LVIC temperature cannot respond to rapid temperature change of those power chips effectively. (e.g. motor lock, short current)

It is able to replace the thermistor which was set on outer heat sink with this function. For more detail, refer [Section 2.2.3](#).

(4) Terminal layout

Because of additional functions above (2), (3) and divided N-side IGBT emitter, the terminal layout was changed from previous 1200V Large DIIPM series. For more detail, refer [Section 2.3](#).

1200V LARGE DIIPM Ver.4 Series APPLICATION NOTE**1.5 The Differences between 50A Rating PS22A79 and Others (PS22A72~PS22A78-E)**

In these products there are some differences between 50A rating PS22A79 and others (5A~35A rating) as below.

Table1-2 Differences of parts and functions

Item	PS22A79	PS22A72~PS22A78-E	Ref.
	50A	5A~35A	
Built-in IGBT	Sixth generation CSTBT	Fifth generation CSTBT	-
Temperature output function (V_{OT} Output)	Built-in But output characteristic and recommended outer circuit with V_{OT} terminal are different with 5A ~ 35A rating products.	Built-in	Section 2.2.3

Table1-3 Differences of characteristic and recommended condition

Item	Symbol	PS22A79	PS22A72~PS22A78-E
		50A	5A~35A
Temperature output	V_{OT}	2.26V~2.51V (LVIC temperature=75°C with pull down resistor 5kΩ)	3.57V~3.69V (LVIC temperature=85°C)
Arm-shoot-through blocking time	t_{dead}	Minimum 3.3μs	Minimum 3.0μs

There are other differences due to current rating. Please refer each datasheet for more detail.

CHAPTER2 SPECIFICATIONS AND CHARACTERISTICS

2.1 Specifications

The specifications are described below by using PS21A7A (75A/600V) as an example. Please refer to respective datasheet for the detailed description of other types.

2.1.1 Maximum Ratings

The maximum ratings of PS22A78-E are shown in Table 2-1.

Table 2-1 Maximum Ratings of PS22A78-E

MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)
INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage	Applied between P-NU,NV,NW	900	V
$V_{CC(\text{surge})}$	Supply voltage (surge)	Applied between P-NU,NV,NW	1000	V
V_{CES}	Collector-emitter voltage		1200	V
$\pm I_C$	Each IGBT collector current	$T_C = 25^\circ\text{C}$	35	A
$\pm I_{CP}$	Each IGBT collector current (peak)	$T_C = 25^\circ\text{C}$, up to 1ms	70	A
P_C	Collector dissipation	$T_C = 25^\circ\text{C}$, per 1 chip	129.9	W
T_j	Junction temperature		-20~+150	$^\circ\text{C}$

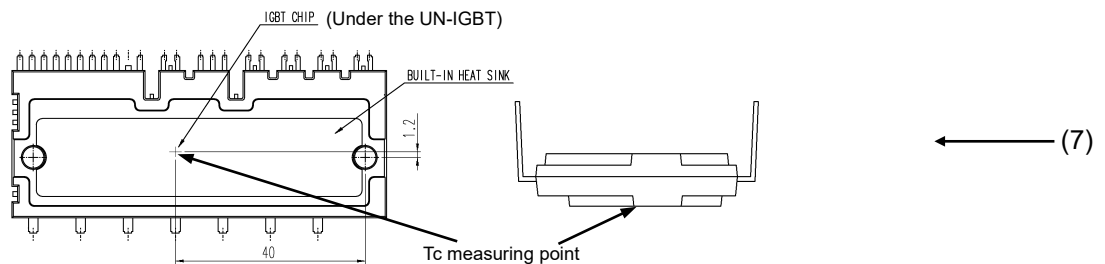
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between $V_{P1}-V_{PC}$, $V_{N1}-V_{NC}$	20	V
V_{DB}	Control supply voltage	Applied between $V_{UFB}-V_{UFS}$, $V_{VFB}-V_{VFS}$, $V_{WFB}-V_{WFS}$	20	V
V_{IN}	Input voltage	Applied between U_P , V_P , W_P-V_{PC} , U_N , V_N , W_N-V_{NC}	-0.5~ $V_D+0.5$	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	-0.5~ $V_D+0.5$	V
I_{FO}	Fault output current	Sink current at F_O terminal	1	mA
V_{SC}	Current sensing input voltage	Applied between $CIN-V_{NC}$	-0.5~ $V_D+0.5$	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(\text{PROT})}$	Self protection supply voltage limit (Short circuit protection capability)	$V_D = 13.5\sim 16.5\text{V}$, Inverter Part $T_j = 125^\circ\text{C}$, non-repetitive, up to 2 μs	800	V
T_C	Module case operation temperature	(Note 1)	-20~+100	$^\circ\text{C}$
T_{stg}	Storage temperature		-40~+125	$^\circ\text{C}$
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	2500	V_{rms}

Note 1: T_c measurement point



[Item explanation]

- (1) V_{CC} The maximum P-N voltage in no switching state. Voltage suppressing circuit such as a brake circuit is necessary if the voltage exceeds this value.
- (2) $V_{CC(\text{surge})}$ The maximum P-N surge voltage in switching state. snubber circuit is necessary if the voltage exceeds $V_{CC(\text{surge})}$.
- (3) V_{CES} The maximum sustained collector-emitter voltage of built-in IGBT.
- (4) $\pm I_C$ The allowable DC current continuously flowing at collect electrode (@ $T_C=25^\circ\text{C}$)
- (5) T_j The maximum junction temperature rating is 150°C . But for safe operation, it is recommended to limit the average junction temperature up to 125°C . Repetive temperature variation ΔT_j affects the life time of power cycle, so refer life time curves (Section 3.1.10) for safety design.
- (6) $V_{CC(\text{prot})}$ The maximum supply voltage for IGBT turning off safely in case of an SC fault. The power chip might be damaged if supply voltage exceeds this rating.
- (7) T_c position T_c (case temperature) is defined to be the temperature just underneath the specified power chip. Please mount a thermocouple on the heat sink surface at the defined position to get accurate temperature information. Due to the control schemes (e.g. Control scheme is different between P and N-side), there is the possibility that highest T_c point is different from above point. In such cases, it is necessary to change the measuring point to that under the highest power chip. (Refer Section 2.3.2)

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2.1.2 Thermal Resistance

Table 2-2 shows the thermal resistance of PS22A78-E.

Table 2-2 Thermal resistance of PS22A78-E

THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 2)	Inverter IGBT part (per 1/6 module)	-	-	0.77	K/W
$R_{th(j-c)F}$		Inverter FWDi part (per 1/6 module)	-	-	1.25	K/W

Note 2: Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100μm~+200μm on the contacting surface of DIIPM and heat sink. The contacting thermal resistance between DIIPM case and heat sink $R_{th(c-f)}$ is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ is about 0.2K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m·k).

The above data shows the thermal resistance between chip junction and case at steady state. The thermal resistance goes into saturation in about 10 seconds. The thermal resistance under 10sec is called as transient thermal impedance which is shown in Fig.2-1. $Z_{th(j-c)}^*$ is the normalized value of the transient thermal impedance. ($Z_{th(j-c)}^* = Z_{th(j-c)} / R_{th(j-c)max}$) For example, the IGBT transient thermal impedance of PS22A78-E in 0.1s is $0.77 \times 0.5 = 0.39K/W$.

The transient thermal impedance isn't used for constantly current, but for short period current (ms order). (E.g. In the cases at motor starting, at motor lock...)

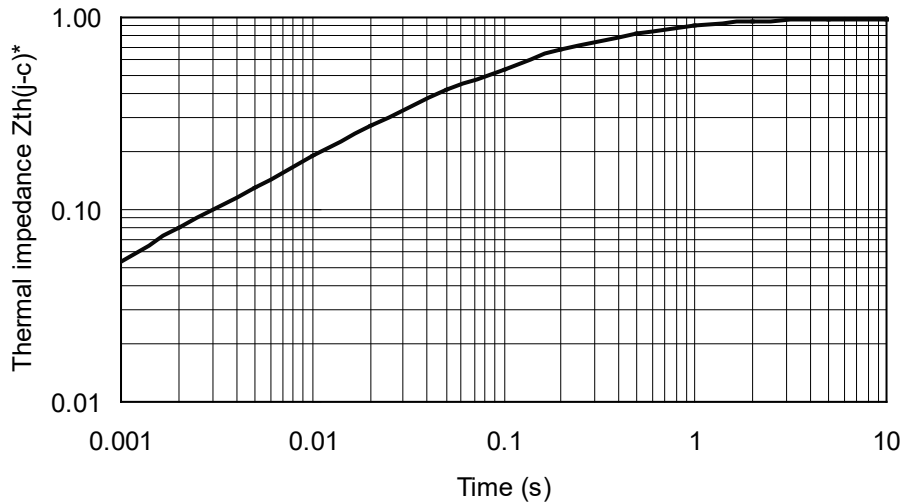


Fig.2-1 Typical transient thermal impedance

2.1.3 Electric Characteristics (Power Part)

Table 2-3 shows the typical static characteristics and switching characteristics of PS22A78-E.

Table 2-3 Static characteristics and switching characteristics of PS22A78-E

Inverter Part

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D = V_{DB} = 15V, V_{IN} = 5V, I_C = 35A$				V
		$T_J = 25^\circ C$	-	1.90	2.60	
		$T_J = 125^\circ C$	-	2.00	2.70	
V_{EC}	FWDi forward voltage	$V_{IN} = 0V, -I_C = 35A$	-	2.20	2.80	V
t_{on}	Switching times	$V_{CC} = 600V, V_D = V_{DB} = 15V$ $I_C = 35A, T_J = 125^\circ C, V_{IN} = 0 \leftrightarrow 5V$ Inductive Load (upper-lower arm)	0.50	1.20	1.90	μs
$t_{C(on)}$			-	0.60	0.90	μs
t_{off}			-	2.40	3.50	μs
$t_{C(off)}$			-	0.60	0.90	μs
t_r			-	0.50	-	μs
I_{CES}	Collector-emitter cut-off current	$V_{CE} = V_{CES}$				mA
		$T_J = 25^\circ C$	-	-	1	
		$T_J = 125^\circ C$	-	-	10	

Switching time definition and performance test method are shown in Fig.2-2 and 2-3.

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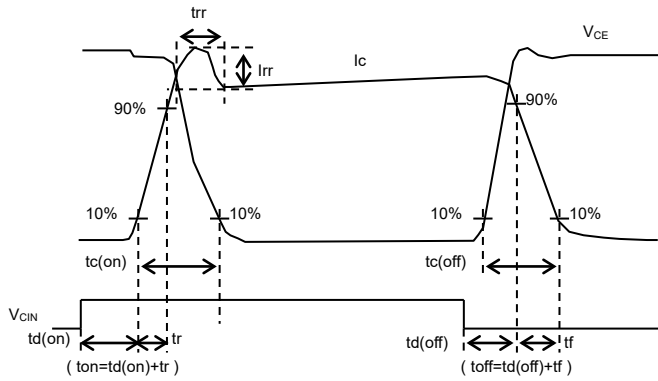


Fig.2-2 Switching time definition

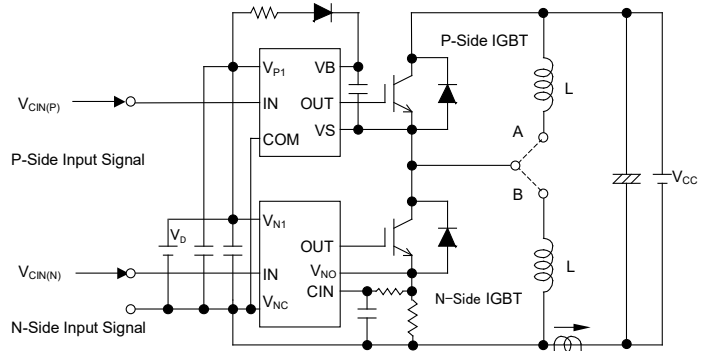
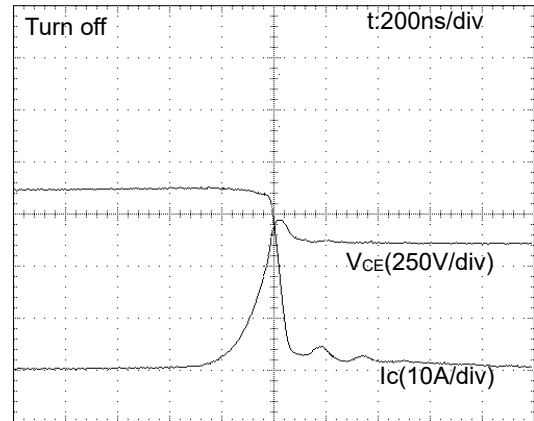
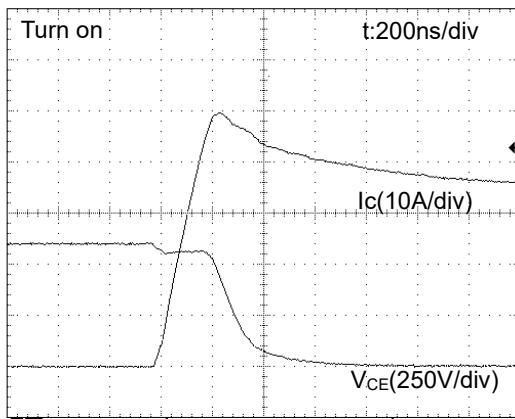


Fig.2-3 Evaluation circuit (inductive load)
Short A for N-side IGBT, and short B for P-side IGBT evaluation



Conditions: $V_{CC}=600V$, $V_D=V_{DB}=15V$, $T_j=125^\circ C$, $I_C=35A$, Inductive load half-bridge circuit

Fig.2-4 Typical switching waveform (PS22A78-E)

2.1.4 Electric Characteristics (Control Part)

Table 2-4 Control (Protection) characteristics of PS22A78-E

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
I_D	Circuit current	Total of $V_{P1}-V_{PC}$, $V_{N1}-V_{NC}$	$V_D=15V$, $V_{IN}=0V$	-	-	5.60	mA
I_{DB}			$V_D=15V$, $V_{IN}=5V$	-	-	5.60	
		Each part of $V_{UFB}-V_{UFS}$, $V_{VFB}-V_{VFS}$, $V_{WFB}-V_{WFS}$	$V_D=V_{DB}=15V$, $V_{IN}=0V$	-	-	1.10	
			$V_D=V_{DB}=15V$, $V_{IN}=5V$	-	-	1.10	
I_{SC}	Short circuit trip level	$-20^\circ C \leq T_j \leq 125^\circ C$, $R_s = 48.7\Omega (\pm 1\%)$, Not connecting outer shunt resistors to NU, NV, NW terminals (Note 3)	59.5	-	-	A	
UV_{DBt}	P-side Control supply under-voltage protection(UV)	$T_j \leq 125^\circ C$	Trip level	10.0	-	12.0	V
UV_{DBr}			Reset level	10.5	-	12.5	V
UV_{Dt}	N-side Control supply under-voltage protection(UV)	$T_j \leq 125^\circ C$	Trip level	10.3	-	12.5	V
UV_{Dr}			Reset level	10.8	-	13.0	V
V_{FOH}	Fault output voltage	$V_{SC} = 0V$, F_O terminal pulled up to 5V by 10k Ω	4.9	-	-	V	
V_{FOL}		$V_{SC} = 1V$, $I_{FO} = 1mA$	-	-	0.95	V	
t_{FO}	Fault output pulse width	$C_{FO}=22nF$ (Note 4)	1.6	2.4	-	ms	
I_{IN}	Input current	$V_{IN} = 5V$	0.70	1.00	1.50	mA	
$V_{th(on)}$	ON threshold voltage	Applied between U_P , V_P , W_P , U_N , V_N , W_N-V_{NC}	-	-	3.5	V	
$V_{th(off)}$	OFF threshold voltage		0.8	-	-		
V_{OT}	Temperature output	LVIC temperature = 85 $^\circ C$ (Note 5)	3.57	3.63	3.69	V	

Note 3: Short circuit protection detects sense current divided from main current at N-side IGBT and works for N-side IGBT only. In the case that outer shunt resistor is inserted into main current path, protection current level I_{SC} changes. For details, please refer the section about SC protection in this document.

4: Fault signal is output when short circuit or N-side control supply under-voltage protection works. The fault output pulse-width t_{FO} depends on the capacitance of C_{FO} . ($C_{FO} (typ.) = t_{FO} \times (9.1 \times 10^{-6}) [F]$)

5: DIIPIM doesn't shut down IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIIPIM immediately. This output might exceed 5V when temperature rises excessively, so it is recommended to insert a clamp Di between controller supply (e.g. 5V) and V_{OT} output for overvoltage protection.

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2.1.5 Recommended Operating Conditions

The recommended operating conditions of PS22A78-E are given in Table 2-5. Although these conditions are the recommended but not the necessary ones, it is highly recommended to operate the modules within these conditions so as to ensure DIIPM safe operation.

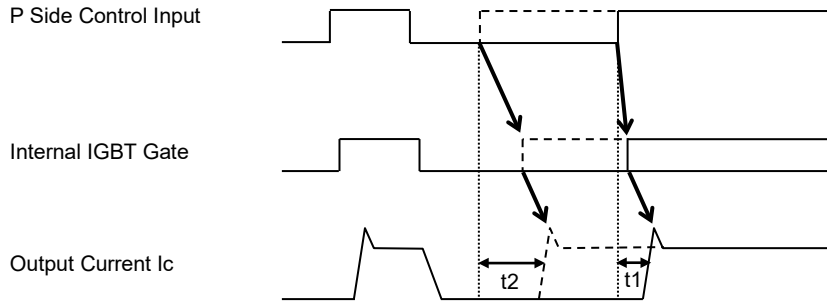
Table 2-5 Recommended operating conditions of PS22A78-E

RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
V_{CC}	Supply voltage	Applied between P-NU, NV, NW	350	600	800	V	
V_D	Control supply voltage	Applied between V_{P1} - V_{PC} , V_{N1} - V_{NC}	13.5	15.0	16.5	V	
V_{DB}	Control supply voltage	Applied between V_{UFB} - V_{UFS} , V_{VFB} - V_{VFS} , V_{WFB} - V_{WFS}	13.0	15.0	18.5	V	
$\Delta V_D, \Delta V_{DB}$	Control supply variation		-1	-	+1	V/ μ s	
t_{dead}	Arm shoot-through blocking time	For each input signal	3.0	-	-	μ s	
f_{PWM}	PWM input frequency	$T_C \leq 100^\circ\text{C}$, $T_J \leq 125^\circ\text{C}$	-	-	20	kHz	
I_O	Allowable r.m.s. current	$V_{CC} = 600\text{V}$, $V_D = 15\text{V}$, P.F = 0.8, Sinusoidal PWM $T_C \leq 100^\circ\text{C}$, $T_J \leq 125^\circ\text{C}$ (Note 7)	$f_{PWM} = 5\text{kHz}$	-	-	19.1	Arms
			$f_{PWM} = 15\text{kHz}$	-	-	12.8	
PWIN(on)	Minimum input pulse width	$350 \leq V_{CC} \leq 800\text{V}$, $13.5 \leq V_D \leq 16.5\text{V}$, $13.0 \leq V_{DB} \leq 18.5\text{V}$, $-20^\circ\text{C} \leq T_C \leq 100^\circ\text{C}$, N line wiring inductance less than 10nH (Note 9)	(Note 8)	1.5	-	-	μ s
PWIN(off)			$I_C \leq 35\text{A}$	2.3	-	-	
			$35\text{A} < I_C \leq 59.5\text{A}$	2.9	-	-	
V_{NC}	V_{NC} variation	Between V_{NC} -NU, NV, NW (including surge)	-5.0	-	+5.0	V	
T_J	Junction temperature		-20	-	+125	$^\circ\text{C}$	

- Note 7: The allowable r.m.s. current value depends on the actual application conditions.
- Note 8: DIIPM might not make response to the input on signal with pulse width less than PWIN (on).
- Note 9: DIIPM might make no response or delayed response (P-side IGBT only) for the input signal with off pulse width less than PWIN(off). Refer below about delayed response.

Delayed Response Against Shorter Input Off Signal Than PWIN(off) (P-side only)



Real line: off pulse width > PWIN(off); turn on time t_1
 Broken line: off pulse width < PWIN(off); turn on time t_2
 (t_1 : Normal switching time)

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2.1.6 Mechanical Characteristics and Ratings

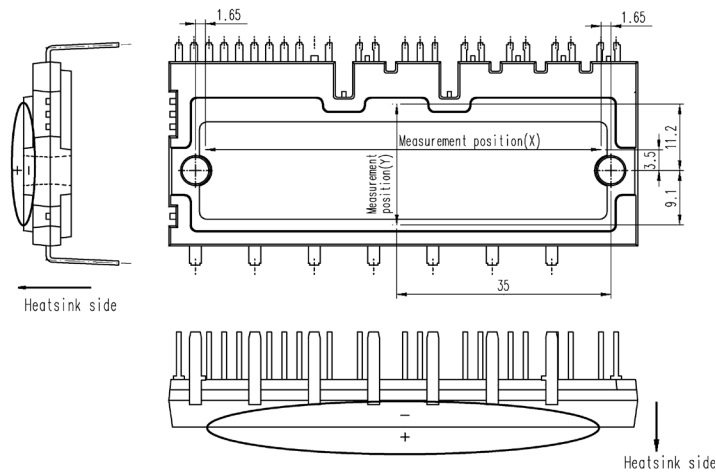
The mechanical characteristics and ratings are shown in Table 2-6
Please refer to Section 2.4 for the detailed mounting instruction.

Table 2-6 Mechanical characteristics and ratings of PS22A78-E

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M4	Recommended 1.18N·m	0.98	1.18	1.47	N·m
Terminal pulling strength	Load 19.6N	EIAJ-ED-4701	10	-	-	s
Terminal bending strength	Load 9.8N, 90deg. bend	EIAJ-ED-4701	2	-	-	times
Weight			-	46	-	g
Heat-sink flatness			-50	-	100	μm

Measurement point of heat-sink flatness



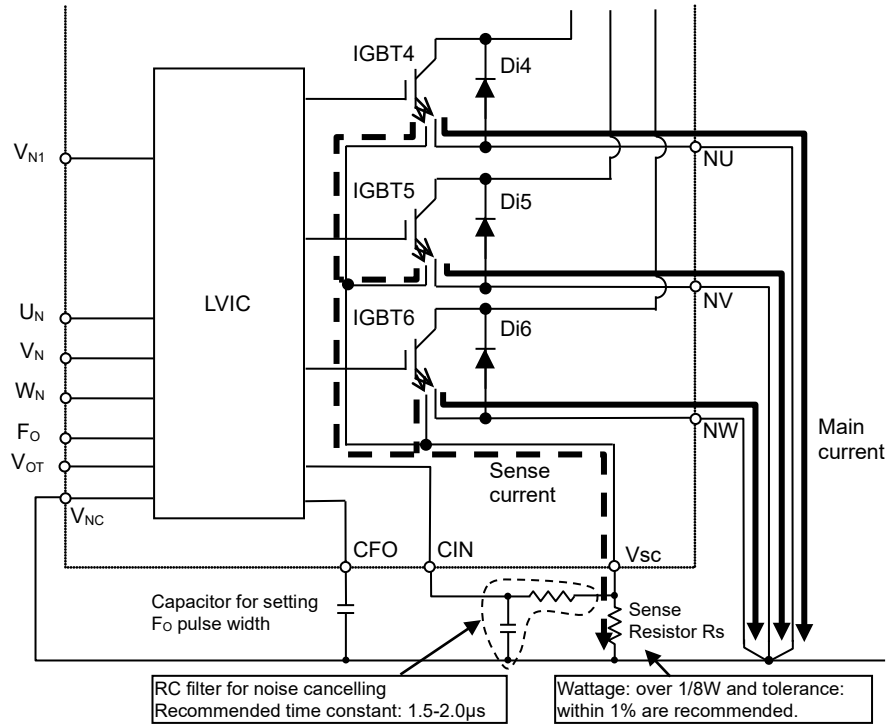
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2.2 Protective Functions and Operating Sequence

There are SC protection, UV protection and outputting LVIC temperature function in the large DIIPM Ver.4. The detailed information is described below.

2.2.1 Short Circuit Protection

In large DIIPM Ver.4 series, the method of SC protection is different from DIIPM Ver.3 series, which detects main current by shunt resistor inserted into main current path. It detects much smaller sense current, which is split at N-side IGBT, by measuring the potential of sense resistor connected to Vsc terminal. So high wattage type shunt resistor isn't necessary for SC protection, and the loss at shunt resistor can be reduced. (Fig.2-5)



*) This wattage of sense resistor is described as a guide, so it is recommended to evaluate on your real system well.

Fig.2-5 SC protection circuit

SC protection works by inputting the potential, which is generated by sense current flowing into the sense resistor, to the CIN terminal. When SC protection works, DIIPM shuts down all N-side IGBTs hardly and outputs F_o signal. (Its pulse width is set by C_{Fo} capacitor. $C_{FO} = t_{FO} \times 9.1 \times 10^{-6} [F]$) Tabel 2-7 describes specified sense resistance and minimum SC protection current in that case for each products.

To prevent malfunction, it is recommended to insert RC filter before inputting to CIN terminal and set the time constant to shut down within 2µs when short circuit occurs. (Time constant 1.5µ-2.0µs is recommended.) Also it is necessary to set the resistance of RC filter to ten or more times of the sense resistor R_s.(Hundred times is recommended.)

Table 2-7 SC protection trip level (Condition: T_j=-20°C~125°C, Not connecting outer shunt resistors to NU,NV,NW terminals.)

	R _s	Min.
PS22A79	34Ω	85.0A
PS22A78-E	48.7Ω	59.5A
PS22A76	82.5Ω	42.5A
PS22A74	82Ω	25.5A
PS22A73	107Ω	17.0A
PS22A72	261Ω	8.5A

For sense resistor, its large fluctuation leads to large fluctuation of SC trip level. So it is necessary to select small variation and good temperature characteristic type (within +/-1% is recommended).

Wattage of the sense resistor can be estimated in view of the fact that the maximum split ratio between the main and sense currents is about 4000:1. (In this case maximum sense current flows.)

The estimation example for PS22A78-E is described as below.

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[Estimation example]

(1) Normal operation state

It is assumed that the maximum main current for normal operation is 70A (rated current x 2, for keeping a margin) and the sense resistance is 48.7Ω.

In this case, The maximum sense current flows through the sense resistor is calculated as below.

$$70A / 4000 = 17.5mA$$

And the loss at the sense resistor is

$$P=I^2 \cdot R \cdot t=(17.5mA)^2 \times 48.7\Omega = \underline{15mW}$$

(2) Short circuit state

When short circuit occurs, its current depends on the condition, but up to IGBT saturation current (about 10 times of the rated current =350A) flows. So the sense current is

$$350A / 4000 = 87.5mA$$

But this current shut down within 2μs by SC protection. And the average loss at the sense resistor is

$$P=I^2 \cdot R \cdot t= (87.5mA)^2 \times 48.7\Omega \times 2\mu s / 1s =\underline{0.0007mW}$$

As explained above, over 1/8W wattage resistor will be suitable, but it is necessary to confirm on your real system finally.

[Remarks]

It takes more time (Table 2-8) from inputting over threshold voltage to CIN terminal to shutting down IGBTs. (Because of IC's transfer delay)

Table 2-8 Internal time delay of IC

Item	min	typ	max	Unit
IC transfer delay time	0.3	0.5	1.0	μs

Therefore, the total delay time from short circuit occurring to shutting down IGBTs is the sum of the delay by the outer RC filter and this IC delay.

[SC protection (N-side only)]

- a1. Normal operation: IGBT ON and outputs current.
- a2. Short circuit current detection (SC trigger) (It is recommended to set RC time constant 1.5~2.0μs so that IGBT shut down within 2.0μs when SC.)
- a3. All N-side IGBTs' gates are hard interrupted.
- a4. All N-side IGBTs turn OFF.
- a5. Fo outputs with a fixed pulse width determined by the external capacitance C_{F0}.
- a6. Input "L": IGBT off.
- a7. Fo finishes output, but IGBTs don't turn on until inputting next ON signal (L→H).
- (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- a8. Normal operation: IGBT ON and outputs current.

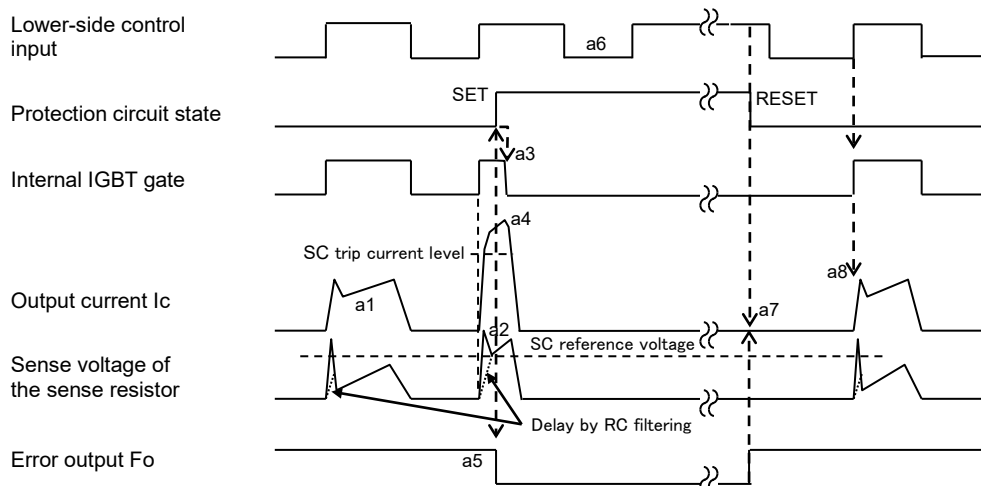


Fig.2-6 SC protection timing chart

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[About Short Circuit Protection by Sense IGBT]

This function aims to protect from Short Circuit like arm short or load short. If high accuracy of protection current level (e.g. protection for demagnetizing motor) is necessary, it is recommended to adopt the method by detecting the voltage at outer shunt resistors into main current path. In that case, the current split ratio between main and sense currents varies, thus minimum SC protection trip level changes from the value in Table 2-7. Therefore, adjustment of the sense resistance will be needed. The example of minimum SC trip level with outer shunt resistor is described in Table 2-9. (PS22A72, at sense resistance 261Ω) Please contact us about selecting sense resistance in the case of inserting outer shunt resistors.

Table 2-9 SC protection trip level (PS22A72, sense resistance 261Ω)

Outer shunt resistance	Minimum SC trip level
Nothing	8.5A
22mΩ	5.6A
68mΩ	4.3A

It is recommended to set outer shunt resistance to the value as shown in Table 2-10 or less because too large shunt resistance causes decrease of IGBT saturation current by decreasing gate voltage at large current. (Large current makes large voltage drop at shunt resistor.) For shunt resistor, select low parasitic inductance resistor like surface mounted device type and pattern the wiring from the N-side emitter (NU, NV, NW) terminals as short as possible because of reducing surge by shutdown at large short circuit current.

Table 2-10 Recommended maximum outer shunt resistance

	Rs
PS22A79	7mΩ
PS22A78-E	10mΩ
PS22A76	14mΩ
PS22A74	23mΩ
PS22A73	34mΩ
PS22A72	67mΩ

As a method that combines short circuit and over current protection function, there is a method which doesn't use sense resistor too. It is the same method as former DIIPM Ver.3 and the example of protection circuit is described in Fig.2-7.

The SC protection trip level is needed to set to double the rated current or less. And it is recommended to set the reference voltage of comparators to about 0.5V and select the shunt resistance in order that the SC trip level becomes double the rated current or less. (e.g. In the case that the protection level is set to rated current for PS22A78-E (rated current 35A), $R=0.5V/70A=7.2m\Omega$ or more)

When this protection method is applied, the rated sense resistor Rs should be connected between Vsc terminal and GND for protecting from surge too. (Don't leave it open.)

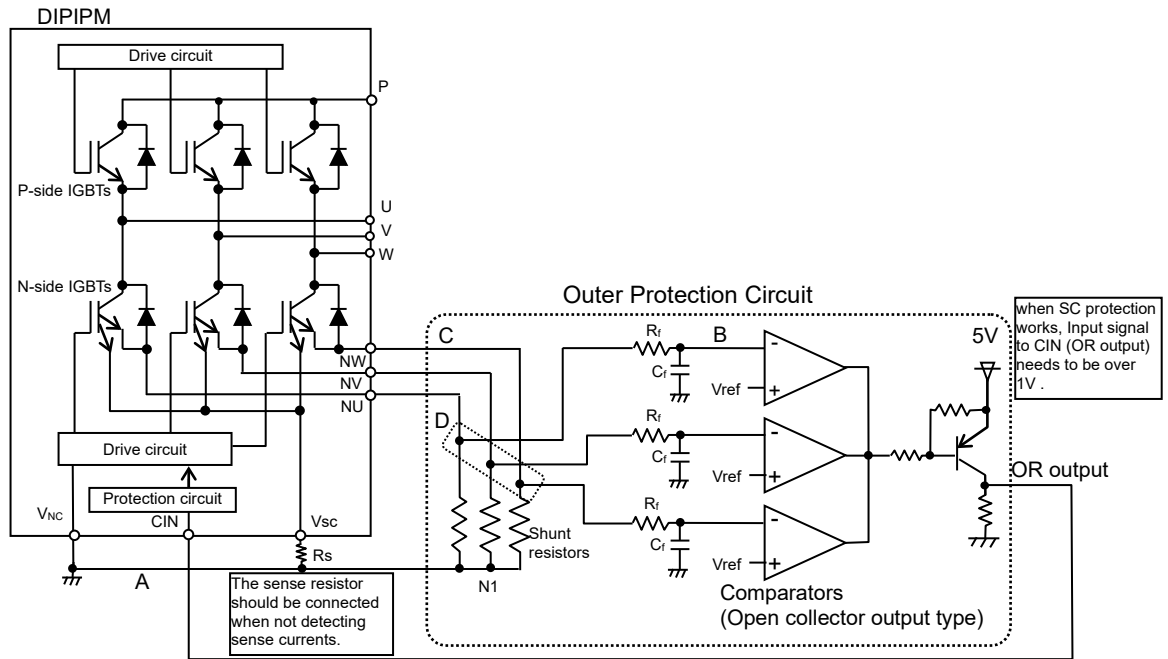


Fig.2-7 Example of SC protection circuit without detecting sense current.

Note:

- It is necessary to set the time constant $R_f C_f$ of external comparator input so that IGBT can stop within $2\mu s$ when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on. If additional RC filter is inserted into OR output, it is necessary to consider its delay too.
- The threshold voltage V_{ref} is recommended to set about 0.5V.
- Select the shunt resistance so that SC trip-level is less than double the rated current.
- To avoid malfunction, the wiring A, B, C should be as short as possible.
- The point D at which the wiring to comparator is divided should be near the terminal of shunt resistor.
- OR output high level should be over 1V at all temperature range.

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2.2.2 Control Supply UV Protection

The UV protection is designed for preventing unexpected operating behavior as described in Table 2-11.

Both P-side and N-side have UV protecting function. However, fault signal (Fo) output only corresponds to N-side UV protection. Fo output continuously during UV state.

In addition, there is a noise filter (typ. 10µs) integrated in the UV protection circuit to prevent instantaneous UV erroneous trip. Therefore, the control signals are still transferred in the initial 10µs after UV happened.

Table 2-11 DIIPM operating behavior versus control supply voltage

Control supply voltage	Operating behavior
0-4.0V (P, N)	Equivalent to zero power supply. UV function is inactive, no Fo output. Normally IGBT does not work. But, external noise may cause DIIPM malfunction (turns ON), so DC-link voltage need to turn on after control supply turning on. (Avoid inputting ON-signals to DIIPM before the control supply coming up to 13.5V)
4.0-UV trip level (P, N)	UV function becomes active and output Fo (N-side only). Even if control signals are applied, IGBT does not work
UV trip level-13.5V(N),13.0V(P)	IGBT can work. However, conducting loss and switching loss will increase, and result extra temperature rise at this state,.
13.5-16.5V (N), 13.0-18.5V (P)	Recommended conditions. (Normal operation)
16.5-20.0V (N),18.5-20.0V (P)	IGBT works. However, switching speed becomes fast and saturation current becomes large at this state, increasing SC broken risk.
20.0V- (P, N)	Over maximum voltage rating. The control circuit will be destroyed.

Ripple Voltage Limitation of Control Supply

If high frequency precipitous noise is superimposed to the control supply line, IC malfunction might happen and cause DIIPM erroneous operation. To avoid such problem happens, line ripple voltage should meet the following specifications:

$$dV/dt \leq \pm 1V/\mu s, \quad V_{ripple} \leq 2V_{p-p}$$

N-side UV Protection Sequence

- a1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but IGBT turns ON when inputting next ON signal (L→H).(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- a2. Normal operation: IGBT turn on and carry current.
- a3. V_D level drops to under voltage trip level. (UV_{Dt}).
- a4. All N-side IGBTs turn OFF in spite of control input condition.
- a5. Fo outputs for the period determined by the capacitance C_{FO} , but output is extended during V_D keeps below UV_{Dr} .
- a6. V_D level reaches UV_{Dr} .
- a7. Normal operation: IGBT ON and carry current.

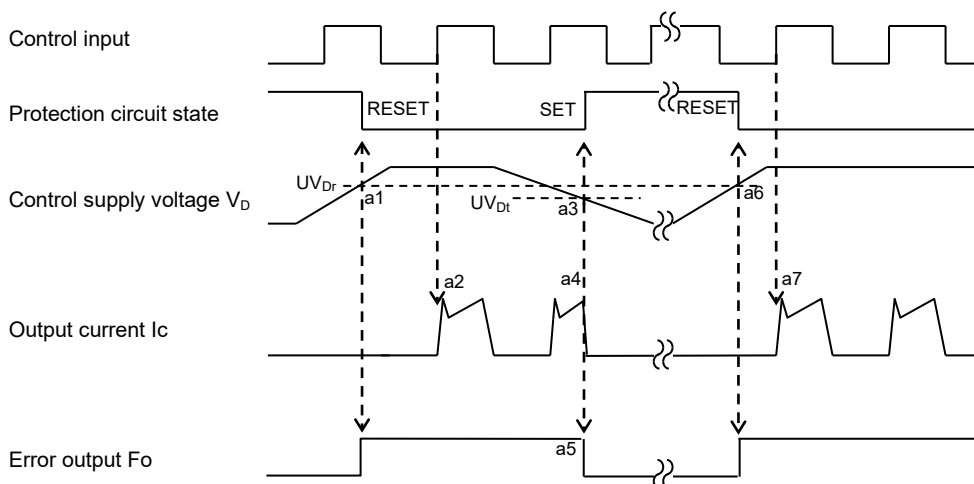


Fig.2-8 Timing chart of N-side UV protection

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P-side UV Protection Sequence

- b1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr} , IGBT can turn on when inputting next ON signal (L→H).
- b2. Normal operation: IGBT ON and outputs current.
- b3. V_{DB} level drops to under voltage trip level (UV_{DBt}).
- b4. IGBT of corresponding phase only turns OFF in spite of control input signal level, but there is no F_o signal output.
- b5. V_{DB} level reaches UV_{DBr} .
- b6. Normal operation: IGBT ON and carry current.

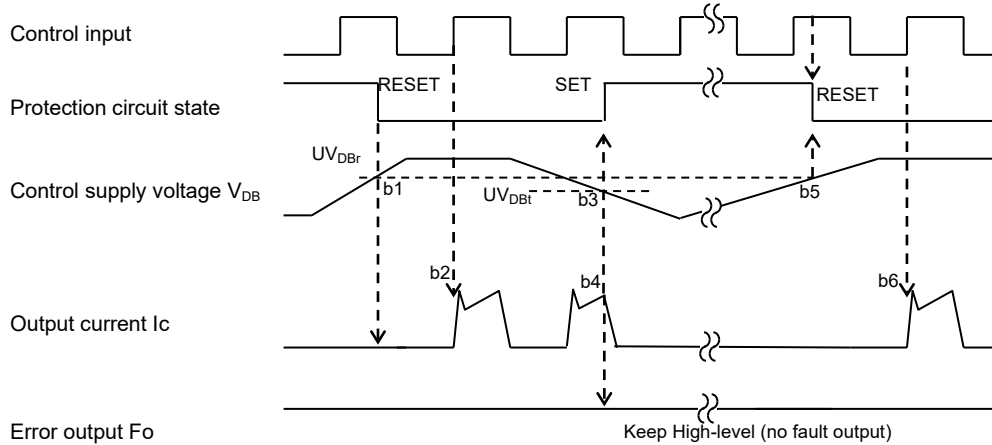


Fig.2-9 Timing Chart of P-side UV protection

2.2.3 Temperature Output Function

This function measures the temperature of control LVIC by built in temperature detecting circuit on LVIC. The heat generated at IGBT and FWDi transfers to LVIC through mold package and inner and outer heat sink. So that LVIC temperature cannot respond to rapid temperature change of power chips effectively. (e.g. motor lock, short current) It is recommended to use this function for protecting from excessive temperature rise by such cooling system down and continuance of overload operation. (Replacement from the thermistor which has been set on outer heat sink currently)

Also DIIPM cannot shutdown IGBT and output fault signal automatically when temperature rises excessively. When temperature exceeds the defined protect level, controller (MCU) should stop the DIIPM.

There are some differences about output characteristic and recommended outer circuit with V_{OT} terminal between 5A~35 A rating products and 50A PS22A79.

[A] Temperature output function for 5~35A rating products PS22A72, PS22A73, PS22A74, PS22A76 and PS22A78-E

(1) V_{OT} terminal circuit and outer additional circuit

Inner circuit of V_{OT} terminal is the output of OP amplifier circuit and is described as Fig.2-10
 If the resistor is inserted between V_{OT} and V_{NC} (control supply GND) terminals, then the current (calculated by V_{OT} output ÷ resistance of inserted resistor) always flows as additional circuit current of LVIC.
 The current capability of V_{OT} output is described as Table 2-12.

Table 2-12 Output capability
($T_c = -20^\circ\text{C} \sim 100^\circ\text{C}$)

	min.
Source	1.7mA
Sink	0.1mA

Source : Current flow from V_{OT} to outside.
 Sink : Current flow from outside to V_{OT} .

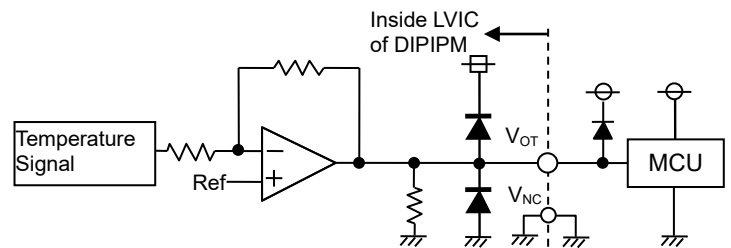


Fig.2-10 Inner circuit of V_{OT} terminal

This output might exceed 5V when temperature rises excessively, so it is recommended for protection of control part like MCU to insert a clamp Di between supply (e.g. 5V) of control part and this output.

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(2) V_{OT} output characteristics

The characteristics of V_{OT} output vs. LVIC temperature is described as Fig.2-11. Please handle the following characteristics as reference data to set over temperature protection. These curves are based on theoretical designed value excluding specified value in the target specification.

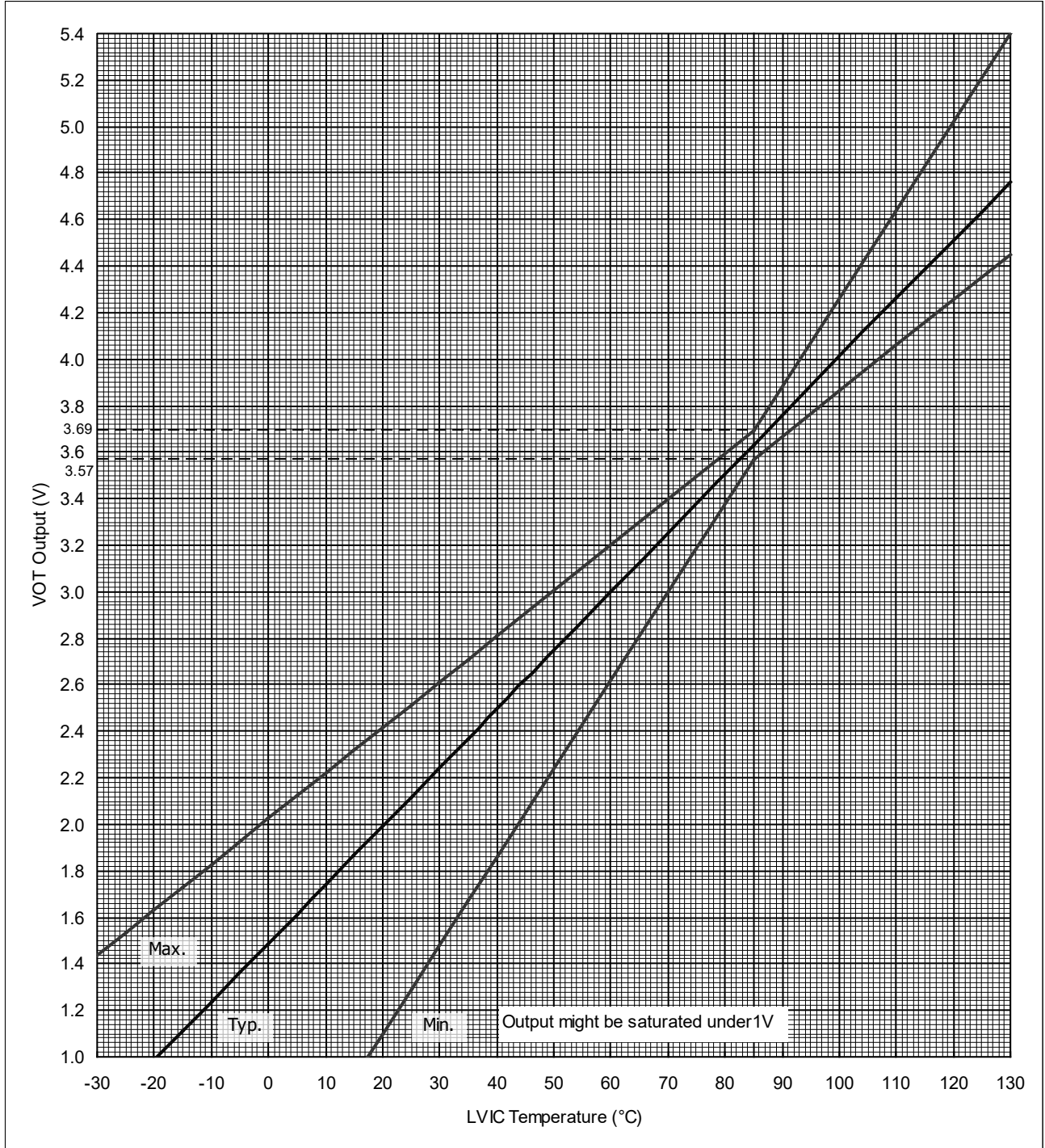


Fig.2-11 V_{OT} output vs. LVIC temperature

As mentioned above, the heat of power chips transfers to LVIC through the package and heat sink, and the relationship between LVIC temperature: $T_{ic}(=V_{OT}$ output), case temperature: T_c (measuring point is defined on the datasheet), and junction temperature: T_j depend on the system cooling condition, heat sink, control strategy, etc.

For example, the evaluation results in the case of using different size heat sink (Table 2-13) are described as Fig.2-12. As the result of evaluations, it is clear that two cases have different relationships between LVIC temperature T_{ic} and case temperature T_c .

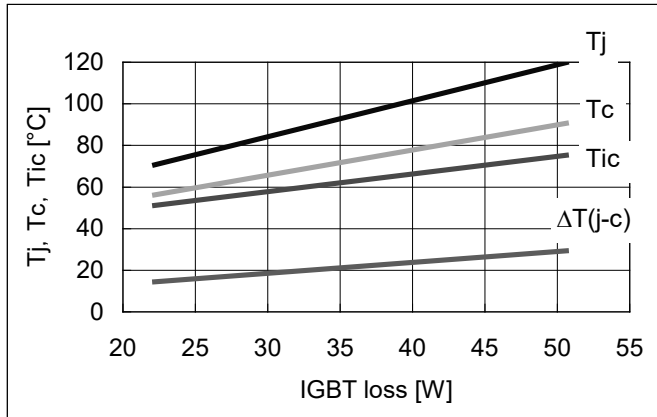
1200V LARGE DIIPM Ver.4 Series APPLICATION NOTE

So when setting the threshold temperature for protection, it is necessary to measure the relationship between them on your real system. And when setting threshold temperature T_{ic} , it is important to consider the protection temperature is at $T_c \leq 100^\circ\text{C}$ and $T_j \leq 150^\circ\text{C}$.

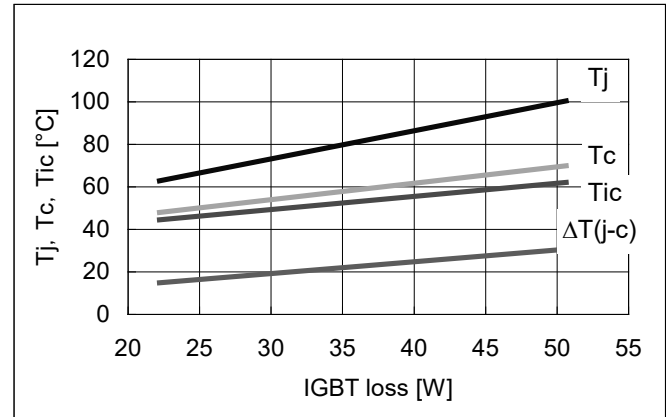
Measuring each temperatures @ only 1 IGBT chip turns on (DC current, $T_a=25^\circ\text{C}$)

Table 2-13 Outer heat sink

	Thermal resistance $R_{th}(f-a)$	Heat sink size (L x D x H)
A	2.20K/W	100 x 88 x 40 mm
B	1.35K/W	200 x 88 x 40 mm



(a) Heat sink A



(b) Heat sink B

Fig.2-12 IGBT loss vs. T_j , T_c , T_{ic} ($T_a=25^\circ\text{C}$, Typical)

A procedure example of setting protection temperature is described below.

Fig.2-13 indicates an example of the relationship between LVIC temperature T_{ic} , case temperature T_c and junction temperature T_j , and Fig.2-14 is the relationship between V_{OT} and T_c , which is obtained by combining Fig.2-11 and Fig.2-13.

If the protection level is set to $T_j=125^\circ\text{C}$ ($T_c=100^\circ\text{C}$), then V_{OT} threshold level should be set 3.75V which is the maximum value @ $T_c=100^\circ\text{C}$ in Fig.2-14.

In this case the variation of real T_c may become from 100°C to 115°C . But even if the real T_c will be maximum variation value 115°C , T_j becomes under 150°C ($125^\circ\text{C}+15^\circ\text{C}=140^\circ\text{C}<150^\circ\text{C}$).

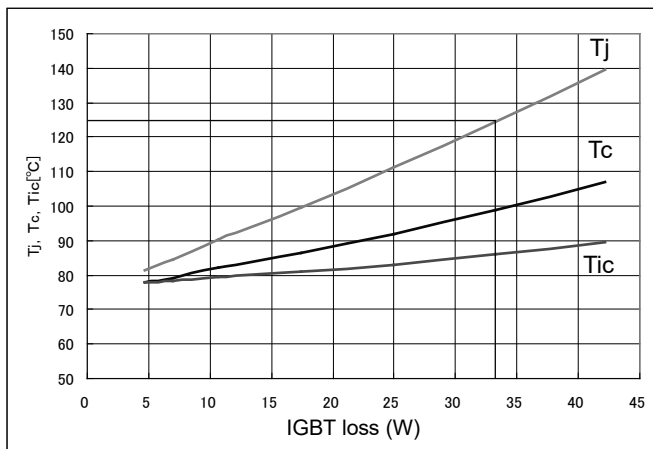


Fig.2-13 IGBT loss vs. T_j , T_c , T_{ic} (Typical) ($T_a=80^\circ\text{C}$)

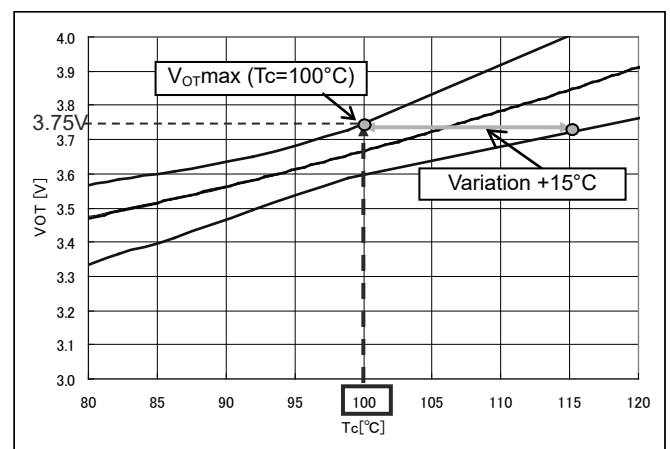


Fig.2-14 V_{OT} vs. T_c (Typical)

As mentioned above, the relationship between T_{ic} , T_c and T_j depends on the system cooling condition and control strategy, and so on. So please evaluate about these temperature relationship on your real system when considering the protection level.

If necessary, it is possible to ship the sample with the individual data of V_{OT} vs. LVIC temperature.

[B] Temperature output function for 50A rating product PS22A79

(1) V_{OT} terminal circuit and outer additional circuit

V_{OT} output circuit, which is described in Fig.2-15, is the output of OP amplifier circuit. The current capability of V_{OT} output is described as Table 2-14. Refer Fig.2-19 about output characteristics.

Table 2-14 Output capability
($T_c = -20^\circ\text{C} \sim 100^\circ\text{C}$)

	min.
Source	1.7mA
Sink	0.1mA

Source : Current flow from V_{OT} to outside.

Sink : Current flow from outside to V_{OT} .

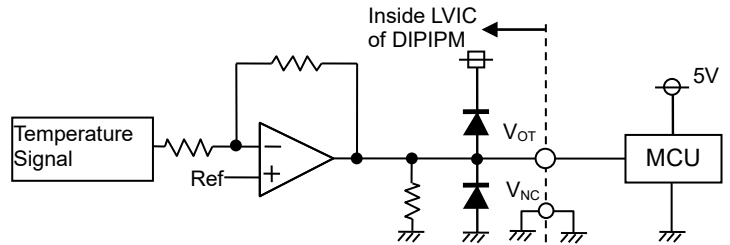


Fig.2-15 Inner circuit of V_{OT} terminal

- In the case of detecting lower temperature than room temperature

It is recommended to insert $5\text{k}\Omega$ or more ($5.1\text{k}\Omega$ is recommended.) pull down resistor for getting linear output characteristics at lower temperature than room temperature. When the pull down resistor is inserted between V_{OT} and V_{NC} (control GND), the extra current calculated by V_{OT} output voltage / pull down resistance flows as LVIC circuit current continuously. In the case of only using V_{OT} for detecting higher temperature than room temperature, it isn't necessary to insert the pull down resistor.

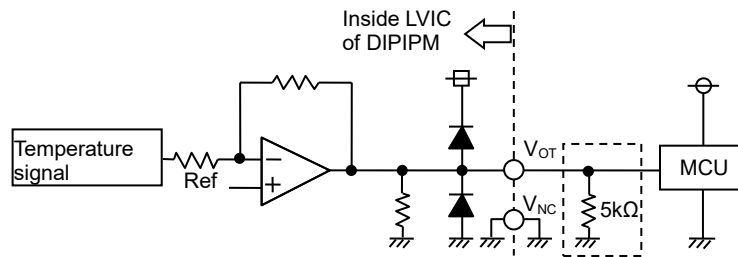


Fig.2-16 V_{OT} output circuit in the case of detecting low temperature

- In the case of using with low voltage controller(MCU)

In the case of using V_{OT} with low voltage controller (e.g. 3.3V MCU), V_{OT} output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and this output for preventing over voltage.

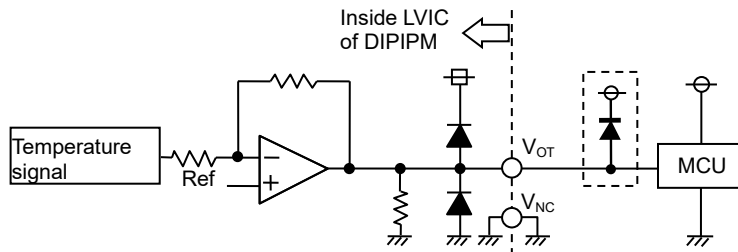


Fig.2-17 V_{OT} output circuit in the case of using with low voltage controller

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- In the case that the protection level exceeds control supply of the controller

In the case of using low voltage controller like 3.3V MCU, if it is necessary to set the trip V_{OT} level to control supply voltage (e.g. 3.3V) or more, there is the method of dividing the V_{OT} output by resistance voltage divider circuit and then inputting to A/D converter on MCU (Fig.2-18). In that case, sum of the resistances of divider circuit should be $5k\Omega$ or more. About the necessity of clamp diode, we consider that the divided output will not exceed the supply voltage of controller generally, so it will be unnecessary to insert the clamp diode. But it should be judged by the divided output level finally.

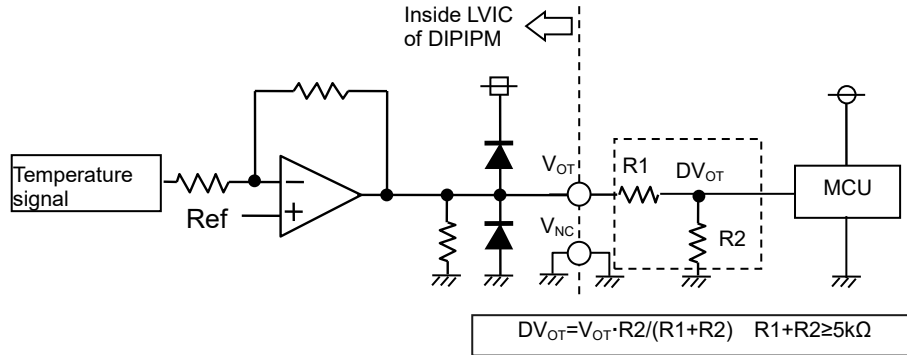


Fig.2-18 V_{OT} output circuit in the case with high protection level

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(2) V_{OT} output characteristics

The characteristics of V_{OT} output vs. LVIC temperature is described as Fig.2-19. Please handle the following characteristics as reference data to set over temperature protection. These curves are based on theoretical designed value excluding specified value in the target specification.

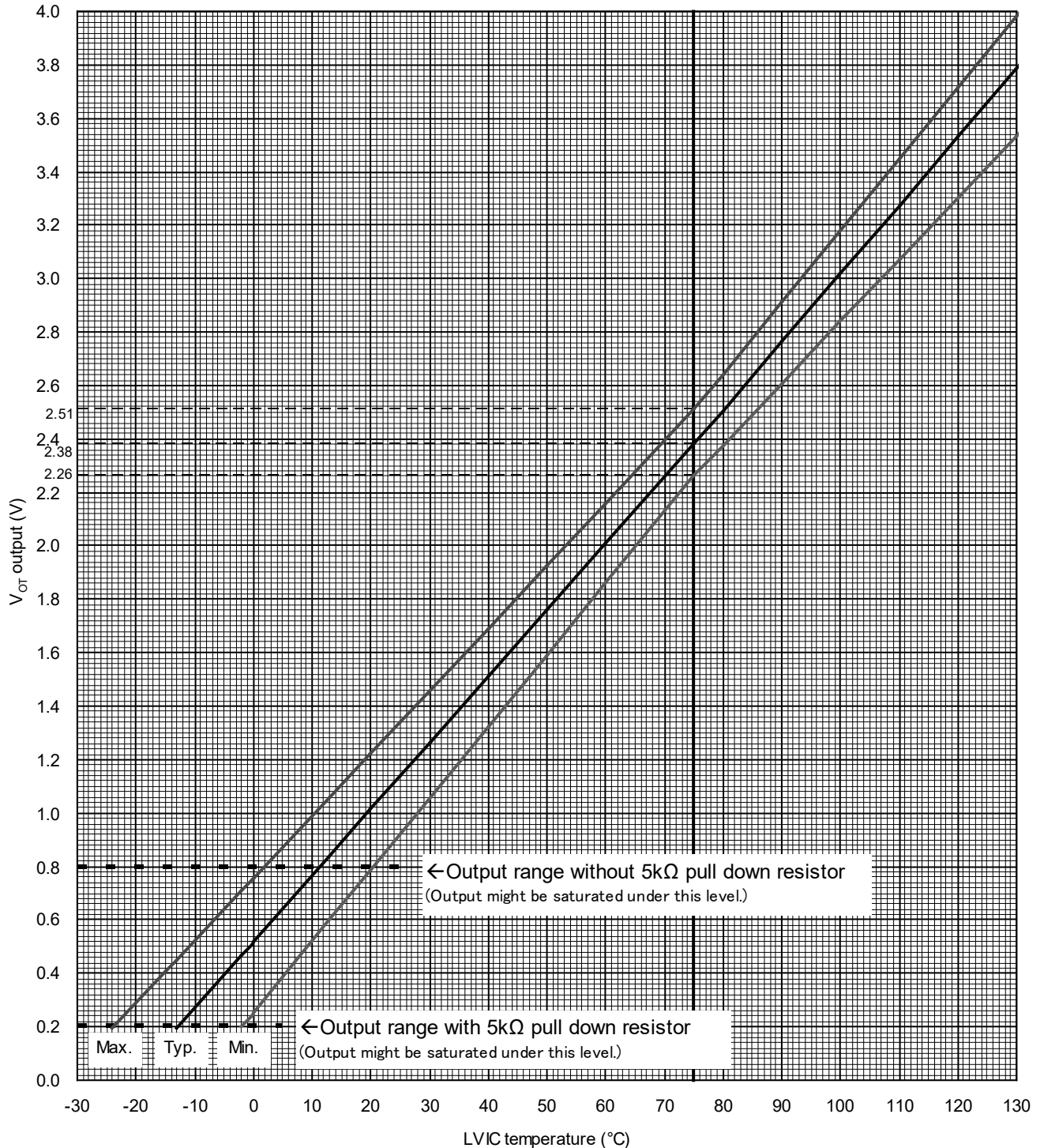


Fig.2-19 V_{OT} output vs. LVIC temperature

About setting method of protection temperature level, it is necessary to get the relationship between LVIC temperature, case temperature and junction temperature on your real system as with 5A~35A rating products mentioned above.

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2.3 Package Outlines

2.3.1 Outline Drawing

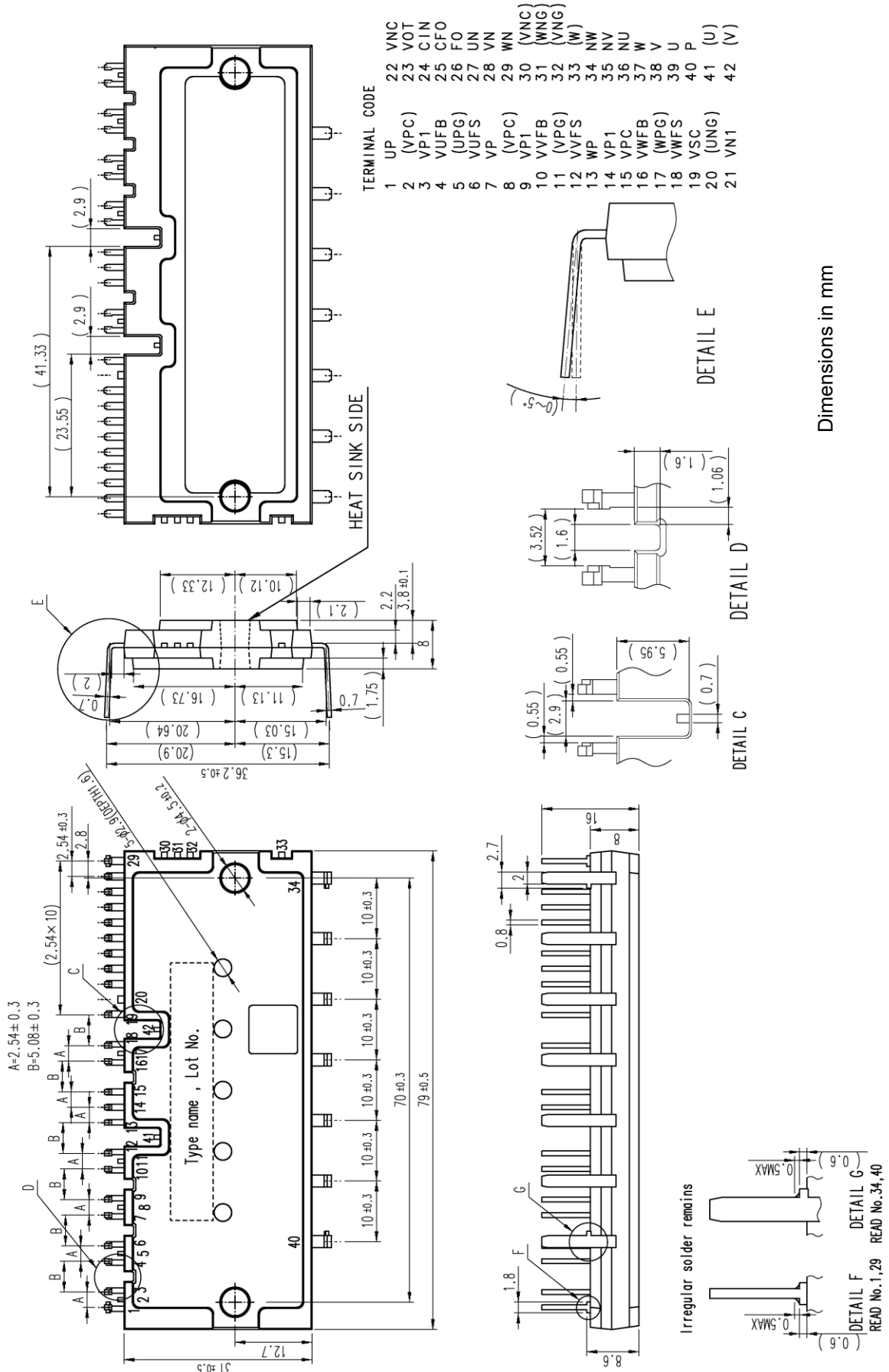


Fig.2-20 Outline drawing

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2.3.2 Power Chip Position

Fig.2-21 indicates the center position of the each power chips.
 (This figure is the view from laser marked side.)

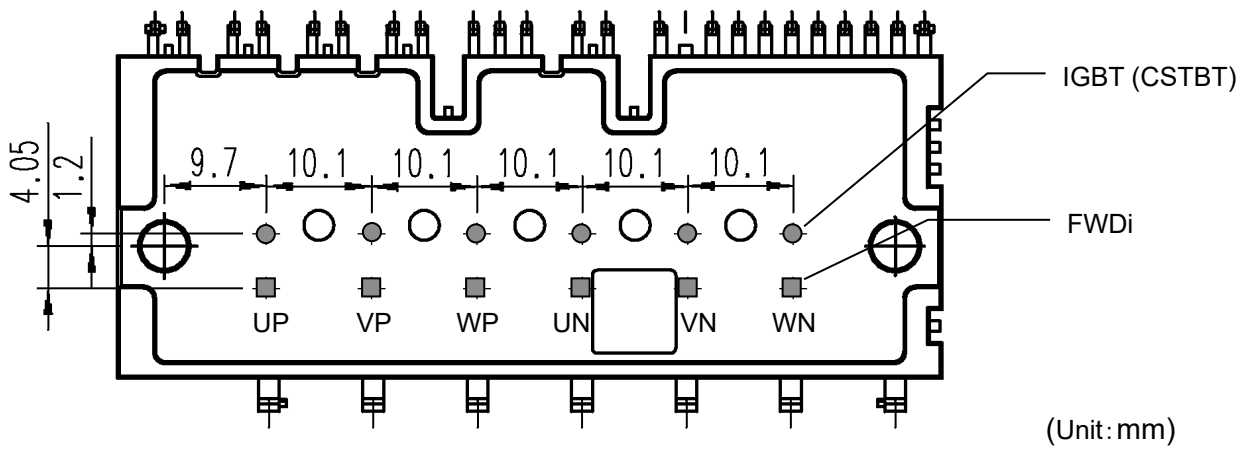


Fig.2-21 Power chip position

2.3.3 Marking Position

The laser marking specification is described in Fig.2-22.
 Company name, Country of origin, Type name, Lot number, and 2D code are marked in the upper side of module.

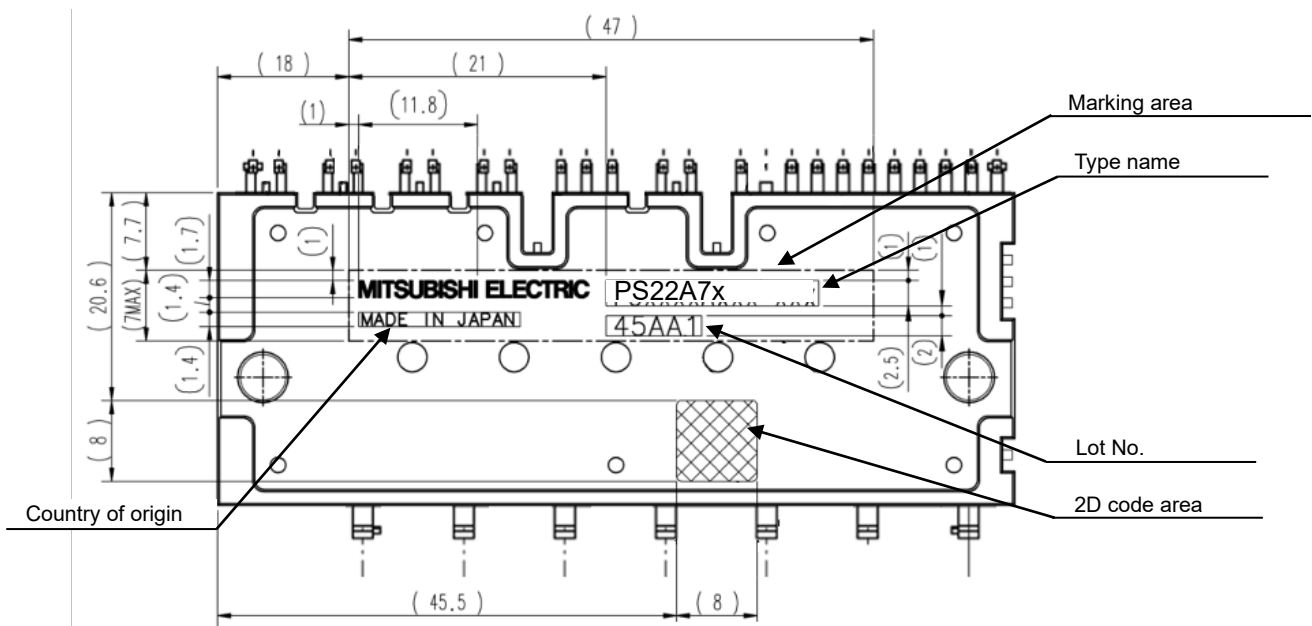
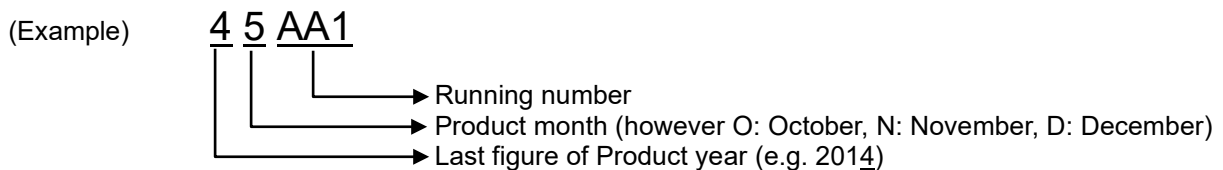


Fig.2-22 Laser marking view

The Lot number indicates production year, month, running number and country of origin.
 The detailed is described as below.



2.3.4 Terminal Description

Table 2-15 Terminal description

No.	Name	Description
1	U _P	U-phase P-side control input terminal
3	V _{P1}	U-phase P-side control supply positive terminal
4	V _{UFB}	U-phase P-side drive supply positive terminal
6	V _{UFS}	U-phase P-side drive supply GND terminal
7	V _P	V-phase P-side control input terminal
9	V _{P1}	V-phase P-side control supply positive terminal
10	V _{VFB}	V-phase P-side drive supply positive terminal
12	V _{VFS}	V-phase P-side drive supply GND terminal
13	W _P	W-phase P-side control input terminal
14	V _{P1}	W-phase P-side control supply positive terminal
15	V _{PC}	P-side control supply GND terminal
16	V _{WFB}	W-phase P-side drive supply positive terminal
18	V _{WFS}	W-phase P-side drive supply GND terminal
19	V _{SC}	Sense current detecting terminal
21	V _{N1}	N-side control supply positive terminal
22	V _{NC}	N-side control supply GND terminal
23	V _{OT}	LVIC temperature output terminal
24	CIN	SC trip voltage detect terminal
25	CFO	Fault pulse output width set terminal
26	F _O	Fault signal output terminal
27	U _N	U-phase N-side control input terminal
28	V _N	V-phase N-side control input terminal
29	W _N	W-phase N-side control input terminal
34	NW	W-phase N-side IGBT emitter terminal
35	NV	V-phase N-side IGBT emitter terminal
36	NU	U-phase N-side IGBT emitter terminal
37	W	W-phase output terminal
38	V	V-phase output terminal
39	U	U-phase output terminal
40	P	Inverter DC-link positive terminal

No.	Name	Description
2	V _{PC}	Internal use (Dummy pin) Don't connect all dummy pins to any other terminals or PCB pattern. (Leave no connect)
5	U _{PG}	
8	V _{PC}	
11	V _{PG}	
17	W _{PG}	
20	U _{NG}	
30	V _{NC}	
31	W _{NG}	
32	V _{NG}	
33	W	
41	U	
42	V	

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Table 2-16 Detailed description of input and output terminals

Item	Symbol	Description
P-side drive supply positive terminal	V_{UFB} - V_{UFS} V_{VFB} - V_{VFS} V_{WFB} - V_{WFS}	<ul style="list-style-type: none"> • Drive supply terminals for P-side IGBTs. • By virtue of applying the bootstrap circuit scheme, individual isolated power supplies are not needed for the DIIPM P-side IGBT drive. Each bootstrap capacitor is charged by the N-side V_D supply during ON-state of the corresponding N-side IGBT in the loop. • Abnormal operation might happen if the V_D supply is not aptly stabilized or has insufficient current capability. In order to prevent malfunction caused by such unstability as well as noise and ripple in supply voltage, a bypass capacitor with favorable frequency and temperature characteristics should be mounted very closely to each pair of these terminals. • Inserting a Zener diode (24V/1W) between each pair of control supply terminals is helpful to prevent control IC from surge destruction.
P-side drive supply GND terminal		
P-side control supply terminal	V_{P1} V_{N1}	<ul style="list-style-type: none"> • Control supply terminals for the built-in HVIC and LVIC. • In order to prevent malfunction caused by noise and ripple in the supply voltage, a bypass capacitor with favorable frequency characteristics should be mounted very closely to these terminals. • Carefully design the supply so that the voltage ripple caused by noise or by system operation is within the specified minimum limitation. • It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
N-side control supply terminal		
N-side control GND terminal	V_{PC} V_{NC}	<ul style="list-style-type: none"> • Control ground terminal for the built-in HVIC and LVIC. • Ensure that line current of the power circuit does not flow through this terminal in order to avoid noise influences.
Control input terminal	U_P, V_P, W_P U_N, V_N, W_N	<ul style="list-style-type: none"> • Control signal input terminals. • Voltage input type. These are internally connected to Schmitt trigger circuit. • The wiring of each input should be as short as possible to protect the DIIPM from noise interference. • Use RC coupling in case of signal oscillation.(Pay attention to threshold voltage of input terminal, because input circuit has pull down resistor (min 3.3kΩ))
Sense current detect terminal	V_{SC}	<ul style="list-style-type: none"> • The sense current split at N-side IGBT flows out from this terminal. For SC protection, connect predefined resistor here.
Short-circuit trip voltage detecting terminal	CIN	<ul style="list-style-type: none"> • Input the potential of V_{SC} terminal (with sense resistor) to CIN terminal for SC protection through RC filter (for the noise immunity). • The time constant of RC filter is recommended to be up to 2μs.
Fault signal output terminal	F_O	<ul style="list-style-type: none"> • Fault signal output terminal for N-side abnormal state(SC or UV). • This output is open drain type. F_O signal line should be pulled up to a 5V logic supply with over 5kΩ resistor (for limiting the F_O sink current I_{F_o} up to 1mA.) Normally 10kΩ is recommended.
Fault pulse output width setting terminal	CFO	<ul style="list-style-type: none"> • The terminal is for setting the fault pulse output width. • An external capacitor should be connected between this terminal and V_{NC}. • When 22nF capacitor is connected, then the F_O pulse width becomes 2.4ms. $t_{FO} = C_{FO} / (9.1 \times 10^{-6})$ (s)
Temperature output terminal	V_{OT}	<ul style="list-style-type: none"> • LVIC temperature is output by analog signal. It is output of OP amplifier internally. • It is recommended to connect 5.1kΩ pulldown resistor if output linearity is necessary under room temperature. (PS22A79 only)
Inverter DC-link positive terminal	P	<ul style="list-style-type: none"> • DC-link positive power supply terminal. • Internally connected to the collectors of all P-side IGBTs. • To suppress surge voltage caused by DC-link wiring or PCB pattern inductance, smoothing capacitor should be inserted very closely to the P and N terminal. It is also effective to add small film capacitor with good frequency characteristics.
Inverter DC-link negative terminal	NU, NV, NW	<ul style="list-style-type: none"> • Open emitter terminal of each N-side IGBT • If usage of common emitter is needed, connect these terminals together at the point as close from the package as possible.
Inverter power output terminal	U, V, W	<ul style="list-style-type: none"> • Inverter output terminals for connection to inverter load (e.g. AC motor). • Each terminal is internally connected to the intermediate point of the corresponding IGBT half bridge arm.

Note: Use oscilloscope to check voltage waveform of each power supply terminals and P&N terminals, the time division of OSC should be set to about 1 μ s/div. Please ensure the voltage (including surge) not exceed the specified limitation.

1200V LARGE DIIPM Ver.4 Series APPLICATION NOTE

2.4 Mounting Method

This section shows the electric spacing and mounting precautions.

2.4.1 Electric Spacing

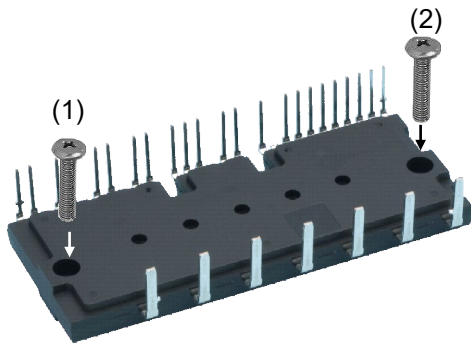
The electric spacing specification of Large DIIPM Ver.4 is shown in Table 2-17

Table 2-17 Minimum insulation distance

	Clearance (mm)	Creepage (mm)
Between live power terminals with high potential	7.1	7.8
Between live control terminals with high potential	3.1	5.6
Between terminals and heat sink	3.7	5.6

2.4.2 Mounting Method and Precautions

When installing the module to the heat sink, excessive or uneven fastening force might apply stress to inside chips. Then it will lead to a broken or degradation of the device. The recommended fastening procedure is shown in Fig.2-23. When fastening, it is necessary to use the torque wrench and fasten up to the specified torque. Also, pay attention not to have any desert remaining on the contact surface between the module and the heat sink.



Temporary fastening
(1)→(2)
Permanent fastening
(1)→(2)

Note: Generally, the temporary fastening torque is set to 20-30% of the maximum torque rating.
Not care the order of fastening (1) or (2), but need to fasten alternately.

Fig.2-23 Recommended screw fastening order

Table 2-18 Mounting torque and heat sink flatness specifications

Item	Condition	Min.	Typ.	Max.	Unit
Mounting torque	Recommended 1.18N·m, Screw : M4	0.98	-	1.47	N·m
Flatness of outer heat sink	Refer Fig.2-24	-50	-	+100	μm

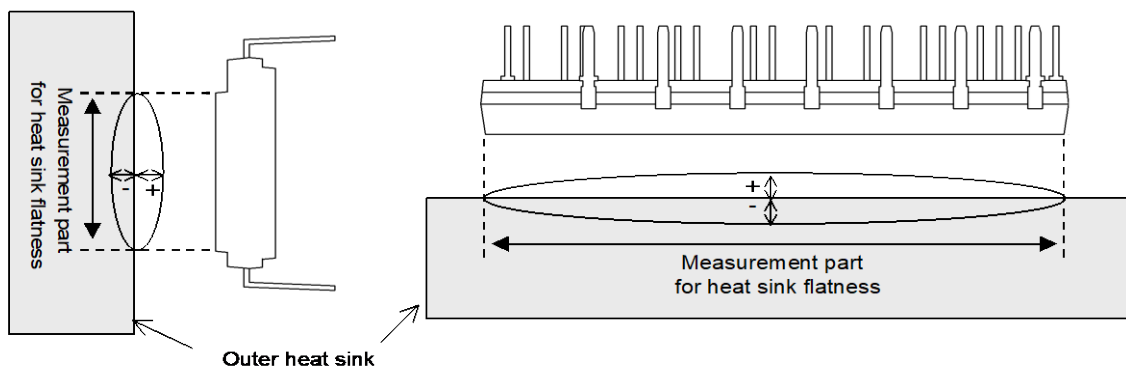


Fig.2-24 Measurement point of heat sink flatness

In order to get effective heat dissipation, it is necessary to keep the contact area as large as possible to minimize the contact thermal resistance. Regarding the heat sink flatness (warp, concavity and convexity) on the module installation surface, the surface finishing-treatment should be within Rz12.

Evenly apply thermally conductive grease with 100μ-200μm thickness over the contact surface between the module and the heat sink, which is also useful for preventing corrosion. The contacting thermal resistance between DIIPM case and heat sink $R_{th(c-f)}$ is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ is about 0.2K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m·k).

2.4.3 Soldering Conditions

The recommended soldering condition is mentioned as below.
(Note: The reflow soldering cannot be recommended for DIIPM.)

(1) Flow (wave) Soldering

DIIPM is tested on the condition described in Table 2-19 about the soldering thermostability, so the recommended conditions for flow (wave) soldering are soldering temperature is up to 265°C and the immersion time is within 11s.

However, the condition might need some adjustment based on flow condition of solder, the speed of the conveyer, and the land pattern and the through hole shape on the PCB, etc.

It is necessary to confirm whether it is appropriate or not for your real PCB finally.

Table 2-19 Reliability test specification

Item	Condition
Soldering Thermostability	260±5°C, 10±1s

(2) Hand soldering

Since the temperature impressed upon the DIIPM may changes based on the soldering iron types (wattages, shape of soldering tip, etc.) and the land pattern on PCB, we cannot suggest the recommended temperature condition for hand soldering.

As a general requirement of the temperature profile for hand soldering, the temperature of the root of the DIIPM terminal should be kept lower than 150°C for considering glass transition temperature (Tg) of the package molding resin and the thermal withstand capability of internal chips. Therefore, it is necessary to check the DIIPM terminal root temperature, solderability and so on in your real PCB, when configure the soldering temperature profile. (It is recommended to set the soldering time as short as possible.)

For reference, the evaluation example of hand soldering with 50W soldering iron is described as below.

[Evaluation method]

- a. Sample: Large DIIPM Ver.4
- b. Evaluation procedure
 - Put the soldering tip of 50W iron (temperature set to 400°C) on the terminal within 1mm from the toe.
 - (The lowest heat capacity terminal (=control terminal) is selected.)
 - Measure the temperature rise of the terminal root part by the thermocouple installed on the terminal root.

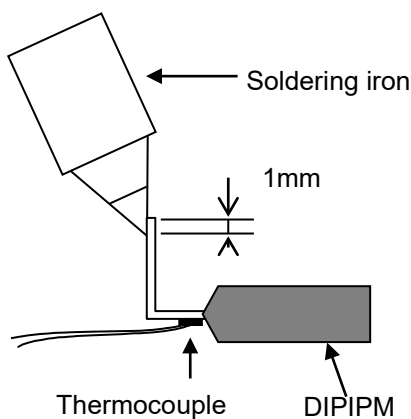


Fig.2-25 Heating and measuring point

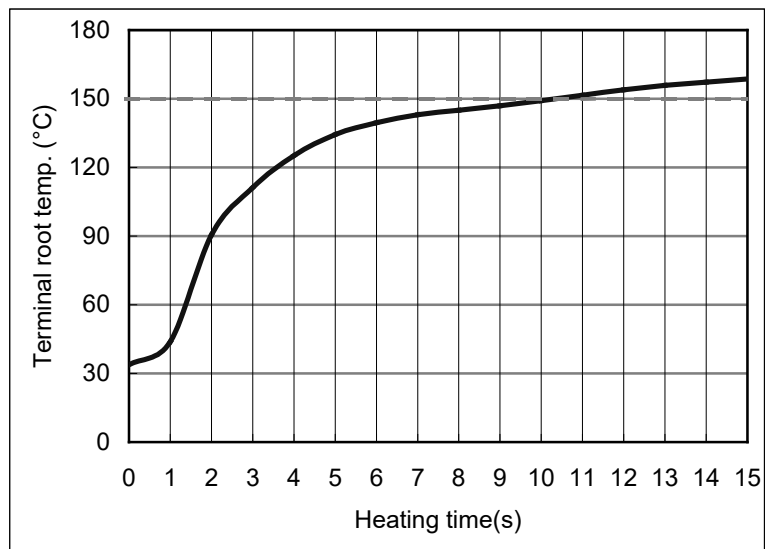


Fig.2-26 Temperature alteration of the terminal root (Example)

[Note]

For soldering iron, it is recommended to select one for semiconductor soldering (12~24V low voltage type, and the earthed iron tip) and with temperature adjustment function.

CHAPTER3 SYSTEM APPLICATION HIGHLIGHT

3.1 Application Guidance

This chapter states usage and interface circuit design hints.

3.1.1 System Connection

C1: Electrolytic type with good temperature and frequency characteristics

Note: the capacitance also depends on the PWM control strategy of the application system

C2: 0.22 μ -2 μ F ceramic capacitor with good temperature, frequency and DC bias characteristics

C3: 0.1 μ -0.22 μ F Film capacitor (for snubber)

D1: Bootstrap diode. High speed type with V_{RRM} : over $V_{ces}(=1200V)$, trr: up to 100ns

D2: Zener diode 24V/1W for surge absorber

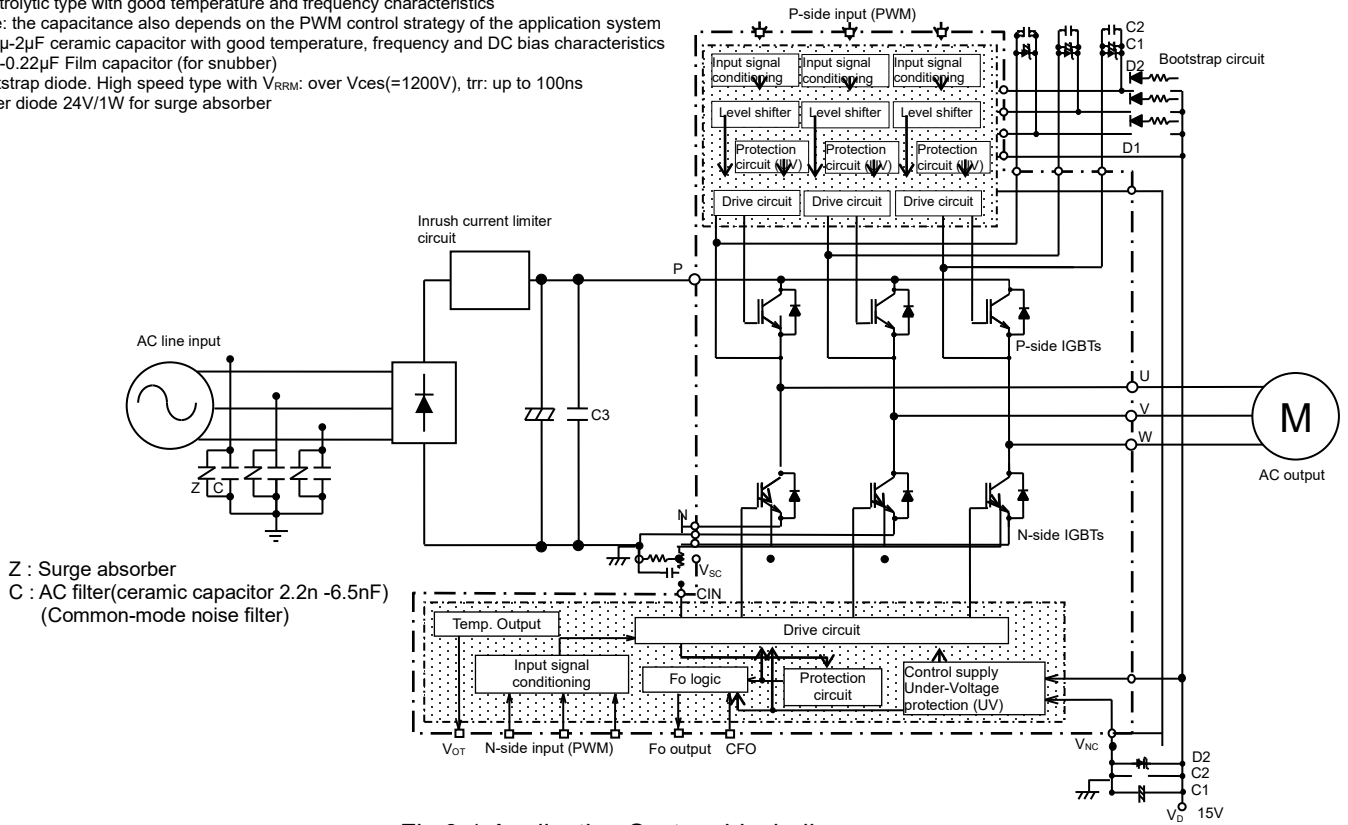


Fig.3-1 Application System block diagram

1200V LARGE DIIPM Ver.4 Series APPLICATION NOTE

3.1.2 Interface Circuit (Direct Coupling Interface example)

Fig.3-2 shows a typical application circuit of connecting with MCU or DSP directly.

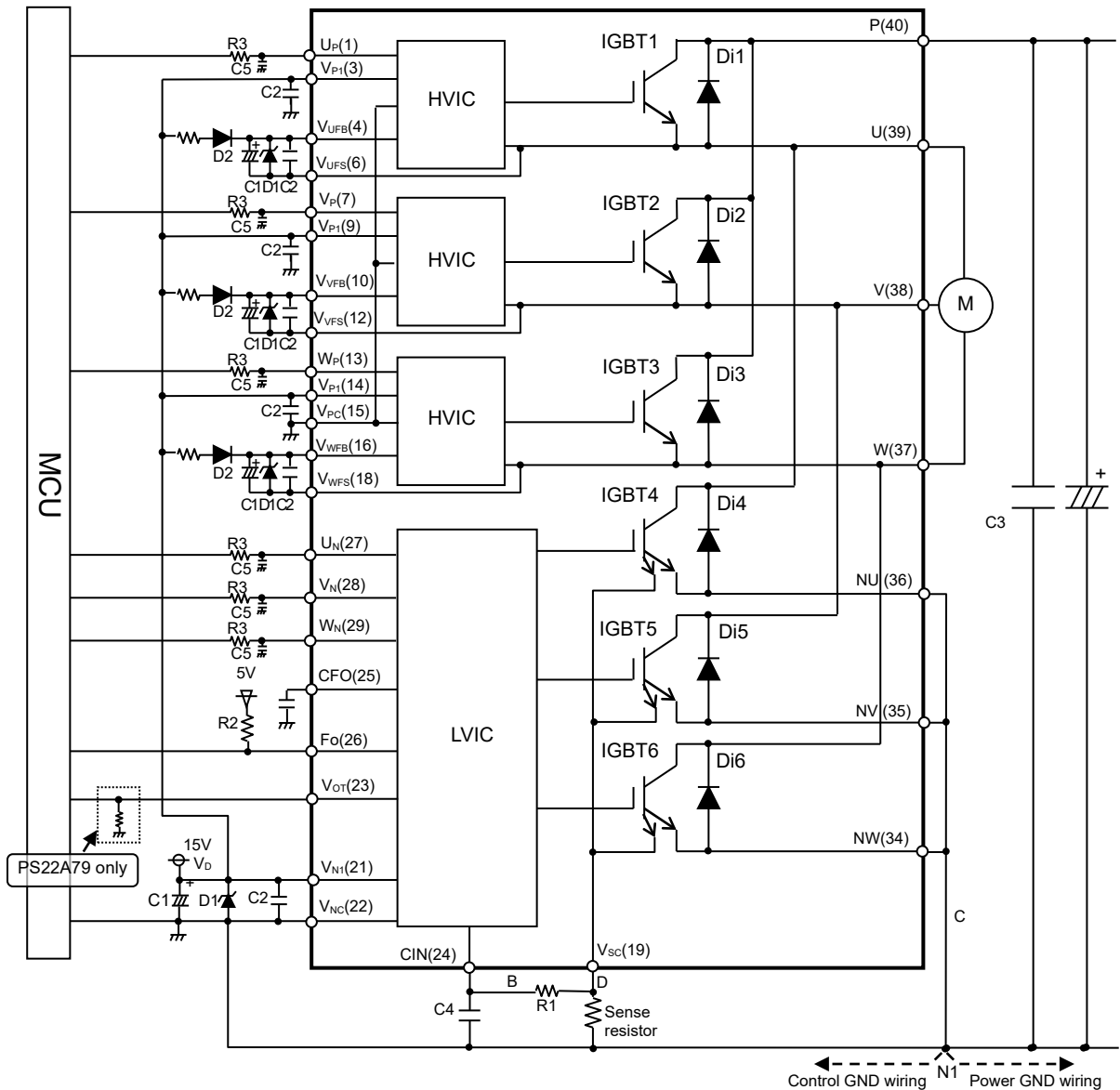


Fig.3-2 Interface circuit example (Direct coupling)

- Note
- 1 :If control GND and power GND are patterned by common wiring, it may cause malfunction by fluctuation of power GND level. It is recommended to connect control GND and power GND at only a N1 point at which NU, NV, NW are connected to power GND line.
 - 2 :It is recommended to insert a Zener diode D1 (24V/1W) between each pair of control supply terminals to prevent surge destruction.
 - 3 :To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally inserting a 0.1μ~0.22μF snubber capacitor C3 between the P-N1 terminals is recommended.
 - 4 :For RC filter for preventing protection circuit malfunction it is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2μs. (1.5μs~2μs is general value.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is recommended. If R1 is too small, it may leads to delay of protection. So R1 should be min. 10 times larger resistance than Rs. (100 times is recommended.)
 - 5 :To prevent erroneous operation, the wiring of A, B, C should be as short as possible.
 - 6 :For sense resistor, the variation within 1%(including temperature characteristics), low inductance type is recommended. And the over 1/8W is recommended, but it is necessary to evaluate in your real system finally.
 - 7 :To prevent erroneous SC protection, the wiring from Vsc terminal to CIN filter should be divided at the point D that is close to the terminal of sense resistor. And the wiring should be patterned as short as possible.
 - 8 :All capacitors should be mounted as close to the terminals of the DIIPM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2: 0.22μ~2.0μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.)
 - 9 :Input drive is High-active type. There is a min. 3.3kΩ pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. And it is strongly recommended to insert RC filter (e.g. R3=100Ω and C5=1000pF) and confirm the input signal level to meet the turn-on and turn-off threshold voltage. Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.
 - 10 :Fo output is open drain type. It should be pulled up to MCU or control power supply (e.g. 5V,15V) by a resistor that makes IFO up to 1mA. (IFO is estimated roughly by the formula of control power supply voltage divided by pull-up resistance. In the case of pulled up to 5V, 10kΩ (5kΩ or more) is recommended.)
 - 11 :Error signal output width (tr_o) can be set by the capacitor connected to C_{Fo} terminal. C_{Fo}(typ.) = tr_o × (9.1 × 10⁻⁶) (F)
 - 12 :High voltage (V_{RRM} =1200V or more) and fast recovery diode (trr=less than 100ns or less) should be used for D2 in the bootstrap circuit.
 - 13 :If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause erroneous operation. To avoid such problem, voltage ripple of control supply line should meet dV/dt ≤±1V/μs, Vripples≤2Vp-p.
 - 14 :For DIIPM, it isn't recommended to drive same load by parallel connection with other phase IGBT or other DIIPM.

1200V LARGE DIIPM Ver.4 Series APPLICATION NOTE

3.1.3 Interface Circuit (Opto-coupler Isolated Interface)

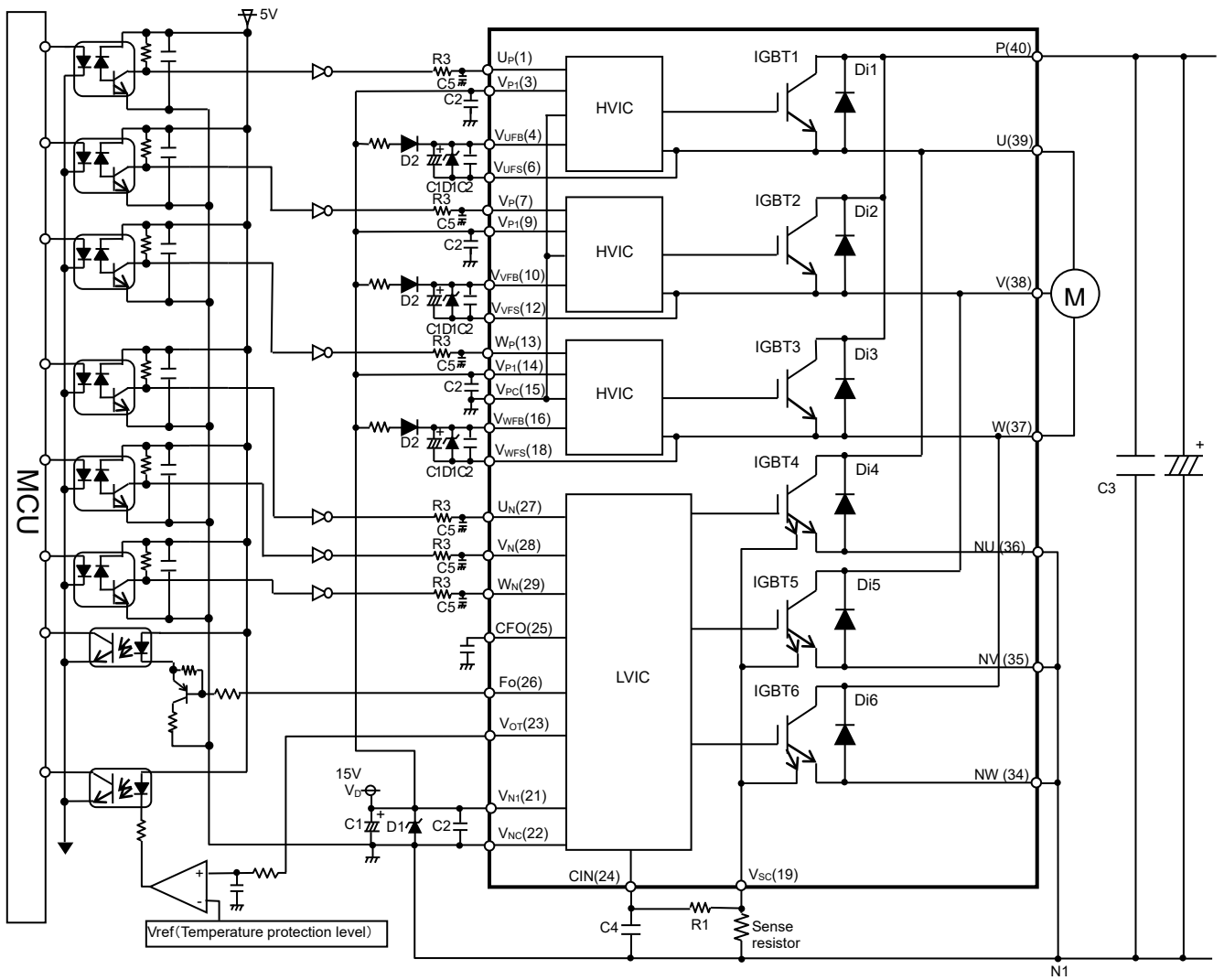


Fig.3-3 Interface circuit example with opto-coupler

Note:

- (1) High speed (high CMR) opto-coupler is recommended.
- (2) F_o terminal sink current is max.1mA. A buffer circuit will be necessary to drive an opto-coupler.
- (3) To prevent malfunction, it is strongly recommended to insert RC filter (e.g. R₃=100Ω and C₅=1000pF) and confirm the input signal level to meet turn-on and turn-off threshold voltage.
- (4) About comparator circuit at V_{OT} output, it is recommended to design the input circuit with hysteresis because of preventing output chattering.

1200V LARGE DIIPM Ver.4 Series APPLICATION NOTE

3.1.4 Circuits of Signal Input terminals and Fo Terminal

Large DIIPM Ver.4 is high-active input logic. A 3.3kΩ(min) pull-down resistor is built-in each input circuit of the DIIPM as shown in Fig.3-4, so external pull-down resistor is not needed.

When using same PCB for 600V large DIIPM Ver.4 PS21A7* series and 1200V series PS22A7* which have same package, it needs to give attention to the difference of input threshold voltage.

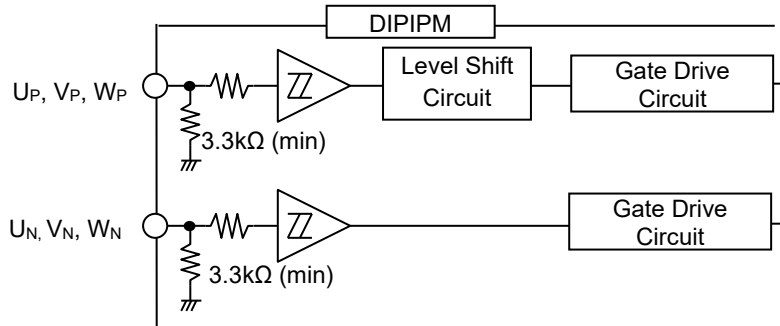


Fig.3-4 Internal structure of control input terminals

Table 3-1 Input threshold voltage ratings ($T_j=25^\circ\text{C}$)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn-on threshold voltage	$V_{th(on)}$	$U_P, V_P, W_P - V_{PC}$	-	-	3.5	V
Turn-off threshold voltage	$V_{th(off)}$	$U_N, V_N, W_N - V_{NC}$	0.8	-	-	

The wiring of each input should be patterned as short as possible. And more noisy in the application of using 1200V rating DIIPM, so it is strongly recommended to insert RC filter. There are limits for the minimum input pulse width in the DIIPM. DIIPM might make no response or delayed response, if the input pulse width (both on and off) is shorter than the specified value. (Refer Table 3-2)

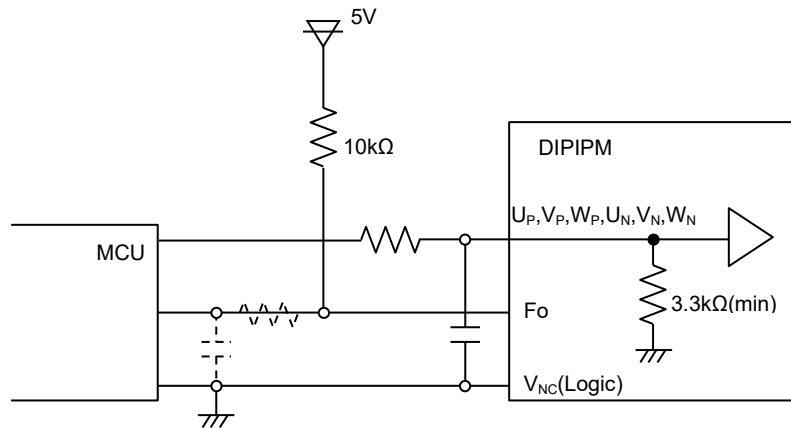


Fig.3-5 Control input connection

Note: Design for input RC filter depends on the PWM control scheme used in the application and the wiring impedance of the printed circuit board. But because more noisy in the application for 1200V, it is strongly recommended to insert RC filter. (Time constant: over 100ns. e.g. 100Ω, 1000pF)

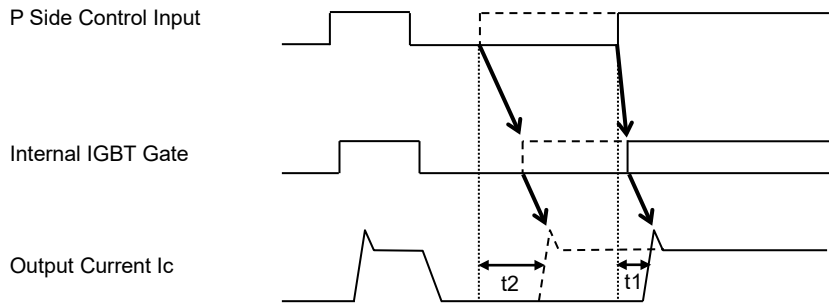
DIIPM input signal interface integrates a 3.3kΩ(min.) pull-down resistor. Therefore, when using RC filter, be careful to satisfy the turn-on threshold voltage requirement.

F_o output is open drain type. It should be pulled up to the positive side of 5V or 15V power supply with the resistor that limits F_o sink current I_{F_o} under 1mA. In the case of pulling up to 5V supply, over 5.1kΩ is needed. (10kΩ is recommended.)

Table 3-2 Allowable minimum input pulse width

	Symbol	Condition		PN	Minimum value	Unit
On signal	PWIN(on)	-		PS22A72	2.0	μs
				PS22A73	2.0	
				PS22A74	2.0	
				PS22A76	1.5	
				PS22A78-E	1.5	
				PS22A79	1.5	
Off signal	PWIN(off)	350 ≤ V _{CC} ≤ 800V, 13.5 ≤ V _D ≤ 16.5V, 13.5 ≤ V _{DB} ≤ 18.5V, -20 ≤ T _C ≤ 100°C, N line wiring inductance less than 10nH	Up to rated current	PS22A72	2.5	
				PS22A73	2.5	
				PS22A74	2.5	
				PS22A76	2.3	
			From rated current to 1.7x rated current	PS22A78-E	2.3	
				PS22A79	3.0	
				PS22A72	2.9	
				PS22A73	2.9	
			PS22A74	2.9		
			PS22A76	2.9		
			PS22A78-E	2.9		
			PS22A79	3.5		

*) Input signal with ON pulse width less than PWIN(on) might make no response.
 IPM might make delayed response or no response for the input signal with off pulse width less than PWIN(off).
 Refer Fig.3-6 about delayed response .



Real line: off pulse width > PWIN(off); turn on time t1
 Broken line: off pulse width < PWIN(off); turn on time t2
 (t1: Normal switching time)

Fig.3-6 Delayed response with shorter input off (P-side only)

1200V LARGE DIIPM Ver.4 Series APPLICATION NOTE

(2) Internal Circuit of Fo Terminal

F_O terminal is an open drain type, it should be pulled up to control supply (e.g. 5V) as shown in Fig.3-5. Fig.3-7 shows the typical V-I characteristics of Fo terminal. The maximum sink current of Fo terminal is 1mA. (I_{Fo} can be estimated from I_{Fo}=control supply voltage / pull up resistance approximately.) If opto-coupler is applied to this output, please pay attention to the opto-coupler drive ability.

Table 3-3 Electric characteristics of Fo terminal

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output voltage	V _{FOH}	V _{SC} =0V, F _o =10kΩ, 5V pulled-up	4.9	-	-	V
	V _{FOL}	V _{SC} =1V, F _o =1mA	-	-	0.95	V

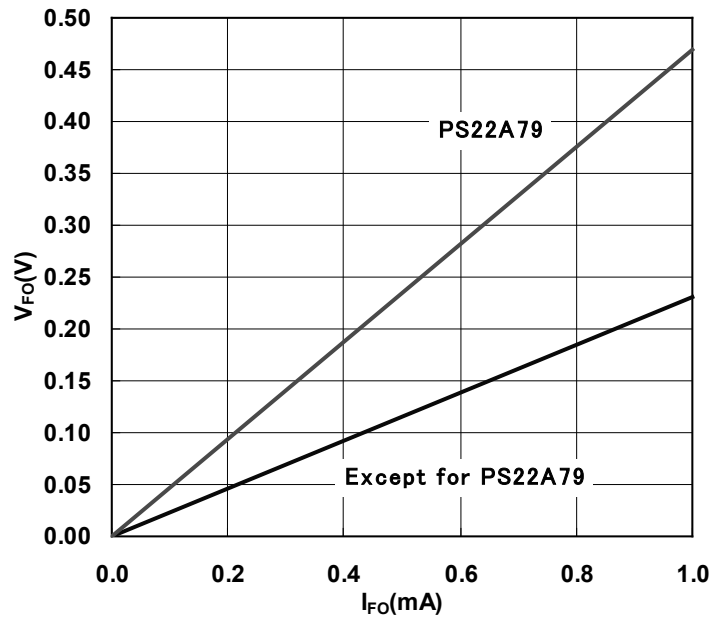


Fig.3-7 Fo terminal typical V-I characteristics (V_D=15V, T_j=25°C)

3.1.5 Snubber Circuit

In order to prevent DIIPM from the surge destruction, the wiring length between the smoothing capacitor and DIIPM P-N terminals should be as short as possible. Also, a 0.1μ~0.22μF/630V snubber capacitor should be mounted to the position between P and the connect point of NU, NV and NW terminals as close as possible as Fig.3-8.

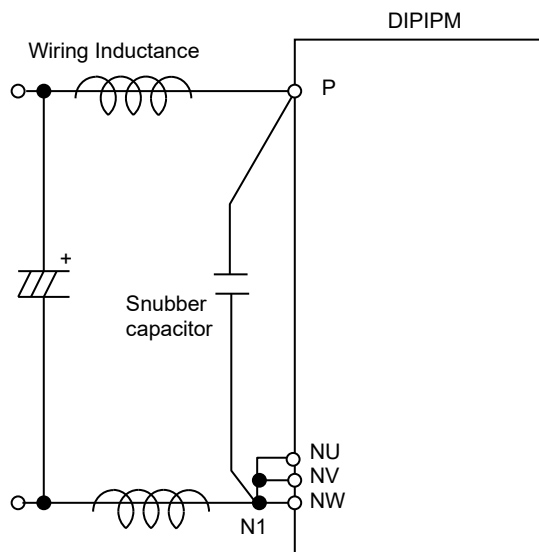


Fig.3-8 Recommended snubber circuit position

3.1.6 Influence of Wiring

Influence of pattern wiring around the sense resistor for SC protection and GND is shown below.

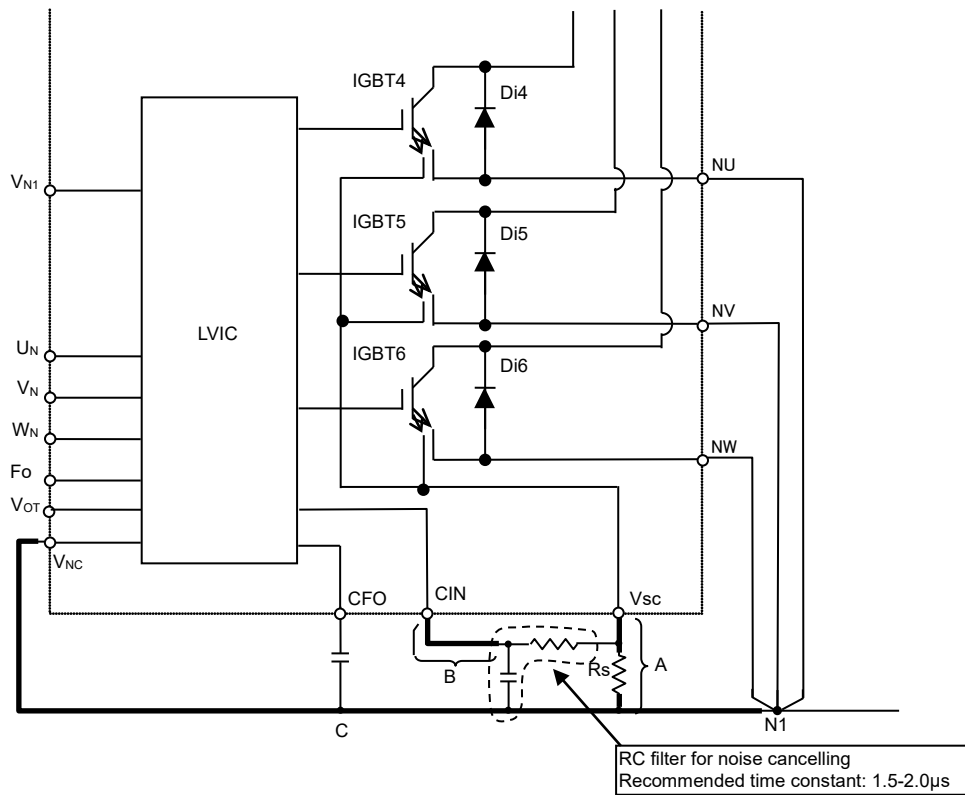


Fig.3-9 External protection circuit

(1) Influence of the part-A wiring

The part-A wiring affects SC protection level. SC protection works by judging the voltage of the CIN terminals. If part-A wiring is too long, extra surge voltage generated by the wiring inductance will lead to fluctuation of SC protection level. This wiring should be as short as possible for limiting the surge voltage.

(2) Influence of the part-B wiring pattern

RC filter is added to remove noise influence occurring on the sense resistor. Filter effect will drop down and noise will easily superimpose on the wiring, if part-B wiring (=after filtering part) is too long. Please install the RC filter near CIN, VNC terminals as close as possible.

(3) Influence of the part-D wiring pattern

Part-C wiring pattern gives influence to all the items described above, maximally shorten the GND wiring is expected. If control GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point at which NU, NV, NW are connected to power GND line.

3.1.7 Precaution for Wiring on PCB

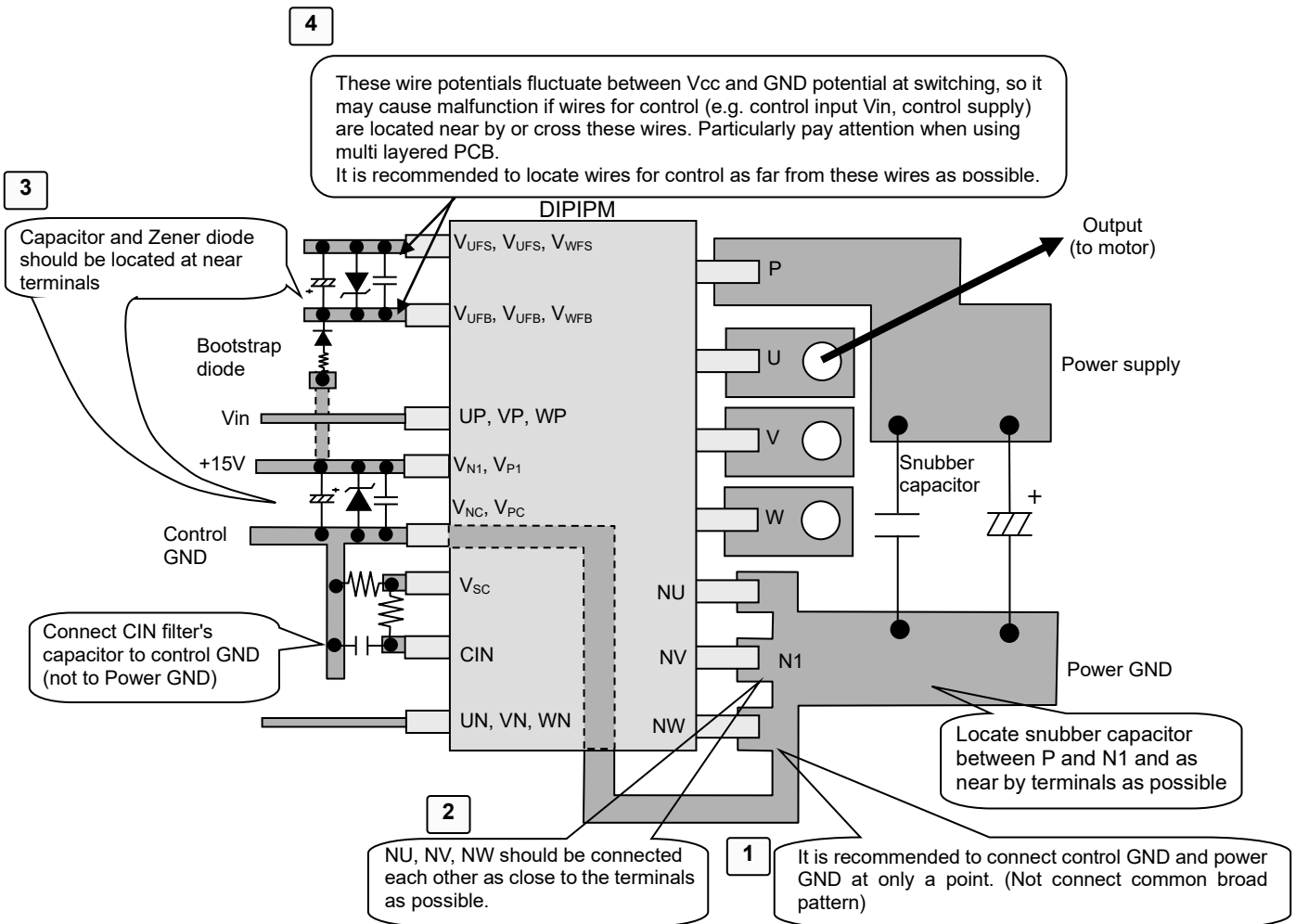


Fig.3-10 Precaution for wiring on PCB

The case example of trouble due to PCB pattern

	Case example	Matter of trouble
1	•Control GND pattern overlaps power GND pattern.	The surge, generated by the wiring pattern and di/dt of noncontiguous big current flows to power GND, transfers to control GND pattern. it causes the control GND level fluctuation, so that the input signal based on the control GND fluctuates too. Finally the arm short occurs.
	•Ground loop pattern exists.	Stray current flows to GND loop pattern, so that the control GND level and input signal level (based on the GND) fluctuates. Then the arm short occurs.
2	•Long pattern between NU, NV, NW terminals and N1	Long wiring pattern has big parasitic inductance and generates high surge when switching. This surge causes the matter as below. •HVIC malfunction due to VS voltage (output terminal potential) dropping excessively. •LVIC surge destruction
3	Capacitors or zener diodes are nothing or located far from the terminals.	IC surge destruction or malfunction occurs.
4	The input lines are located parallel and close to the floating supply lines for P-side drive.	Cross talk noise might be transferred through the capacitance between these floating supply lines and input lines to DIIPM. Then incorrect signals are input to DIIPM input, and arm short (short circuit) might occur.

3.1.8 SOA of DIIPM

The following describes the SOA (Safety Operating Area) of DIIPM.

- V_{CES} : Maximum rating of IGBT collector-emitter voltage
- V_{CC} : Supply voltage applied on P-N terminals
- $V_{CC(surge)}$: The total amount of V_{CC} and the surge voltage generated by the wiring inductance and the DC-link capacitor.
- $V_{CC(PROT)}$: DC-link voltage that DIIPM can protect itself.

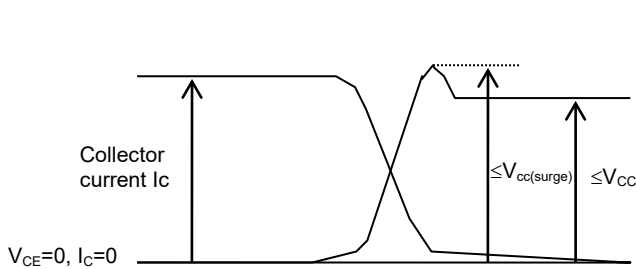


Fig.3-11 SOA at switching mode

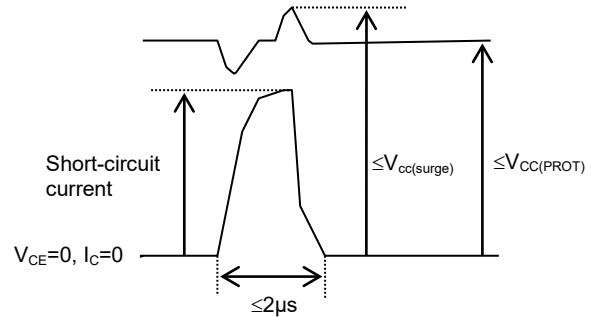


Fig.3-12 SOA at short-circuit mode

In case of switching

V_{CES} represents the maximum voltage rating (1200V) of the IGBT. By subtracting the surge voltage (200V or less) generated by internal wiring inductance from V_{CES} is $V_{CC(surge)}$, that is 1000V. Furthermore, by subtracting the surge voltage (100V or less) generated by the wiring inductor between DIIPM and DC-link capacitor from $V_{CC(surge)}$ derives V_{CC} , that is 900V.

In case of Short-circuit

V_{CES} represents the maximum voltage rating (1200V) of the IGBT . By Subtracting the surge voltage (200V or less) generated by internal wiring inductor from V_{CES} is $V_{CC(surge)}$, that is, 1000V. Furthermore, by subtracting the surge voltage (200V or less) generated by the wiring inductor between the DIIPM and the electrolytic capacitor from $V_{CC(surge)}$ derives V_{CC} , that is, 800V.

1200V LARGE DIIPM Ver.4 Series APPLICATION NOTE

3.1.9 SCSOA

Fig.3-13 ~ Fig.3-18 show the typical SCSOA performance curves of each 1200V Large DIIPM Ver.4 products.
Conditions: $V_{cc}=800V$, $T_j=125^{\circ}C$ at initial state, $V_{cc}(\text{surge})\leq 1000V(\text{surge included})$, non-repetitive, 2m load.

In the case of PS22A72 (5A rating) it means DIIPM can shutdown maximum 65A(@ $V_D=16.5V$) short circuit current safely if IGBT turn on period is within 6 μs (typical).

Since the SCSOA operation area will vary with the control supply voltage, DC-link voltage, and etc, it is necessary to set time constant of RC filter with a margin.

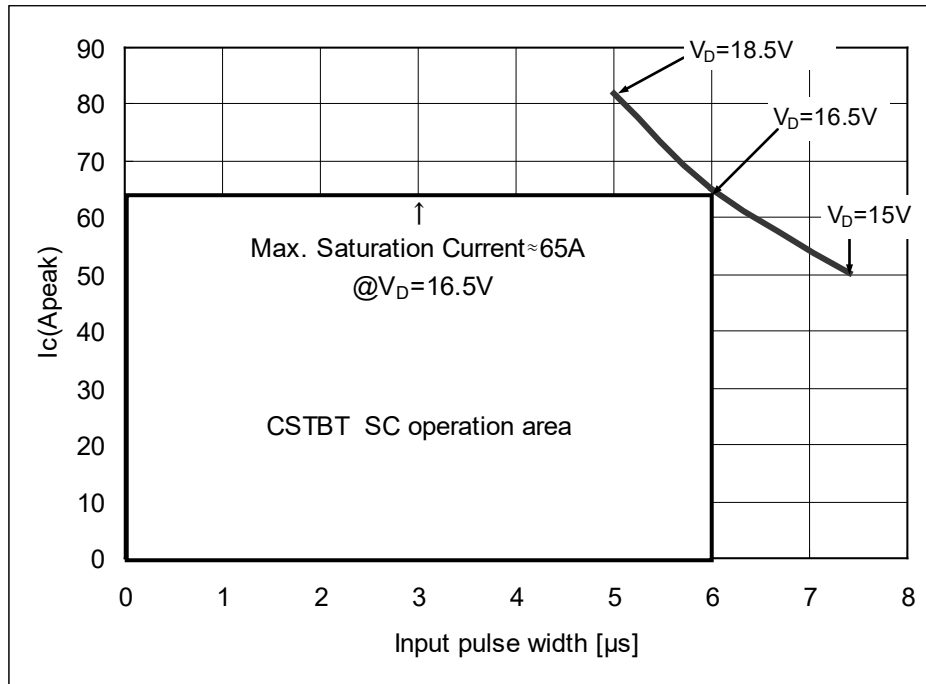


Fig.3-13 PS22A72 typical SCSOA curve

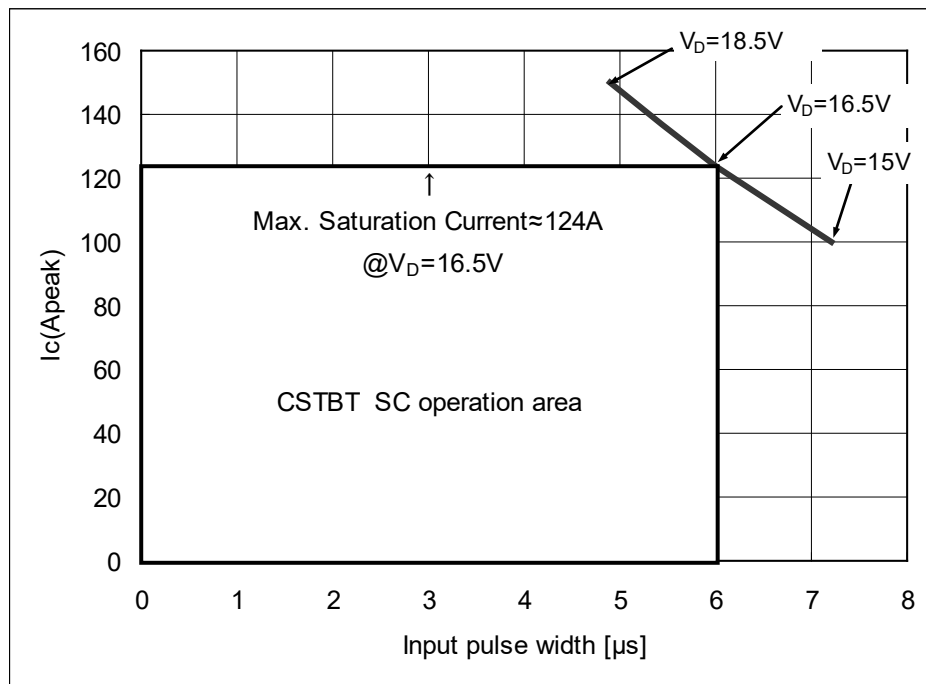


Fig.3-14 PS22A73 typical SCSOA curve

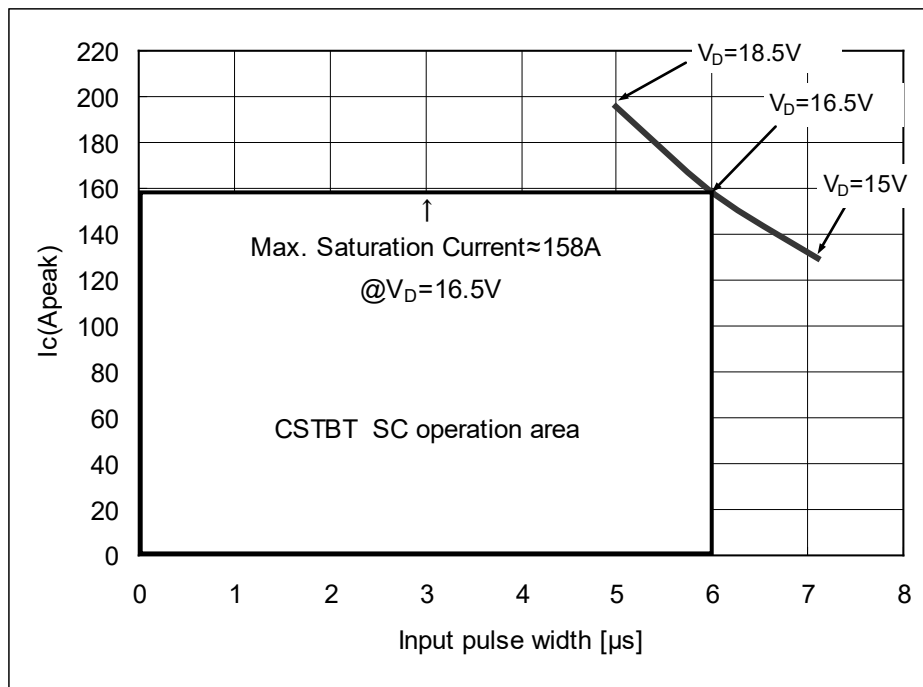


Fig.3-15 PS22A74 typical SCSOA curve

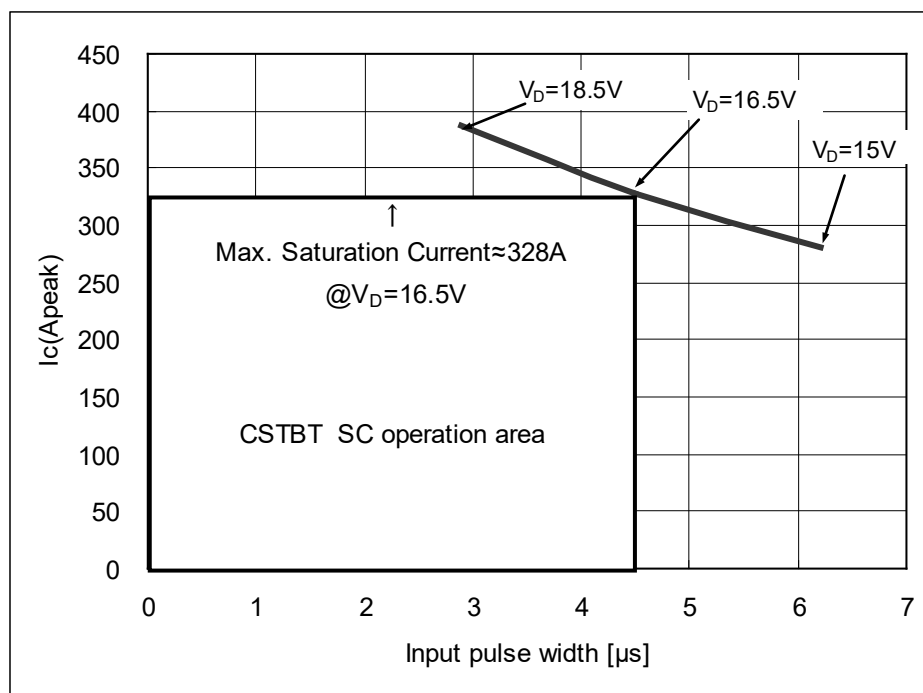


Fig.3-16 PS22A76 typical SCSOA curve

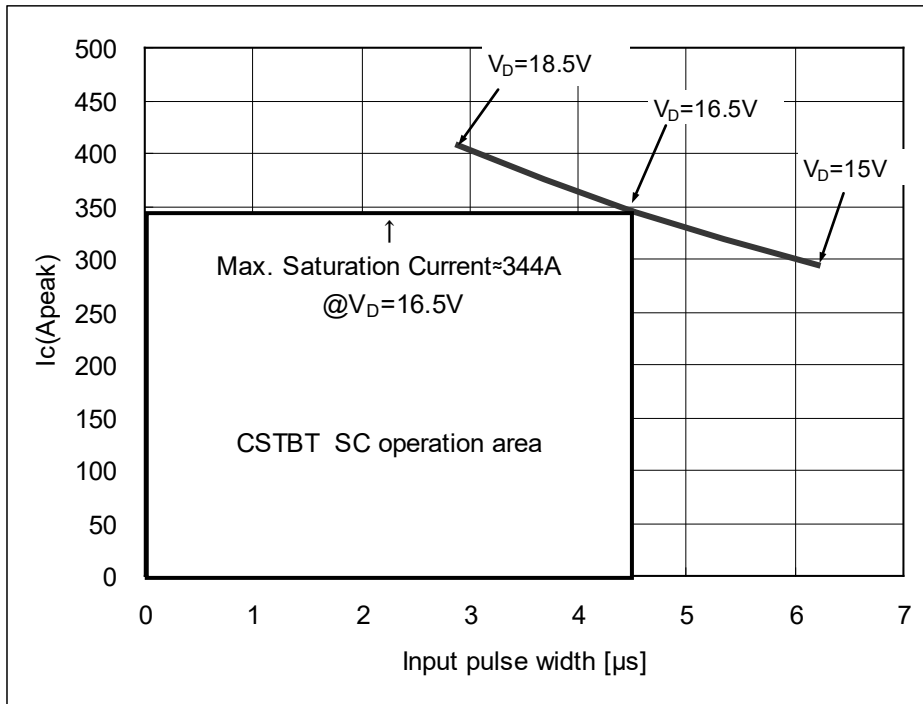


Fig.3-17 PS22A78-E typical SCSOA curve

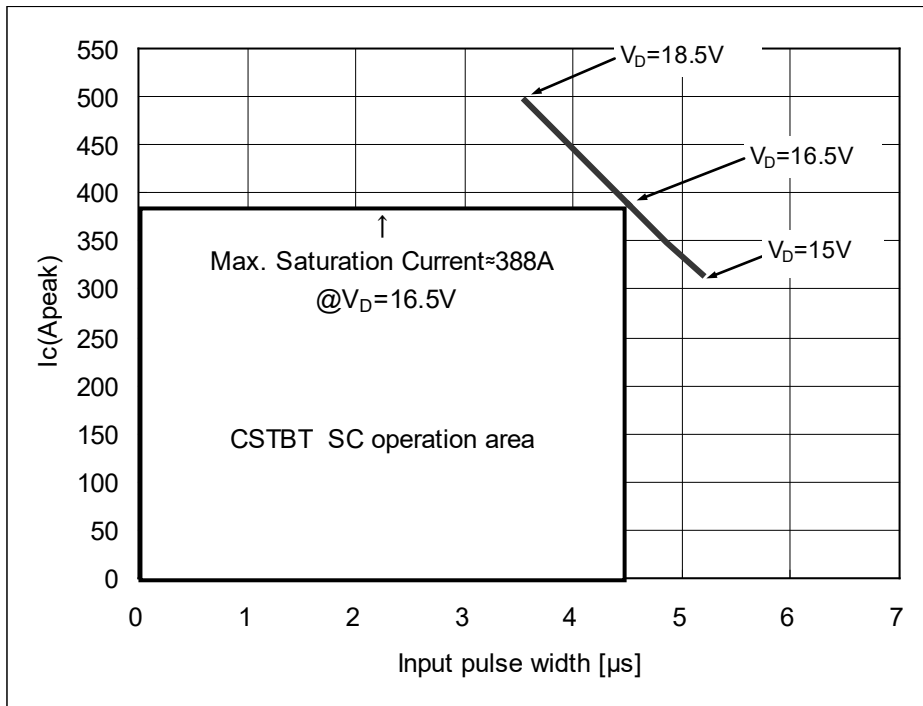


Fig.3-18 PS22A79 typical SCSOA curve

1200V LARGE DIIPM Ver.4 Series APPLICATION NOTE

3.1.10 Power Life Cycles

When DIIPM is in operation, repetitive temperature variation will happen on the IGBT junctions (ΔT_j). The amplitude and the times of the junction temperature variation affect the device lifetime.

Fig.3-19 shows the IGBT power cycle curve as a function of average junction temperature variation (ΔT_j).

(The curve is a regression curve based on 3 points of $\Delta T_j=46, 88, 98K$ with regarding to failure rate of 0.1%, 1% and 10%. These data are obtained from the reliability test of intermittent conducting operation)

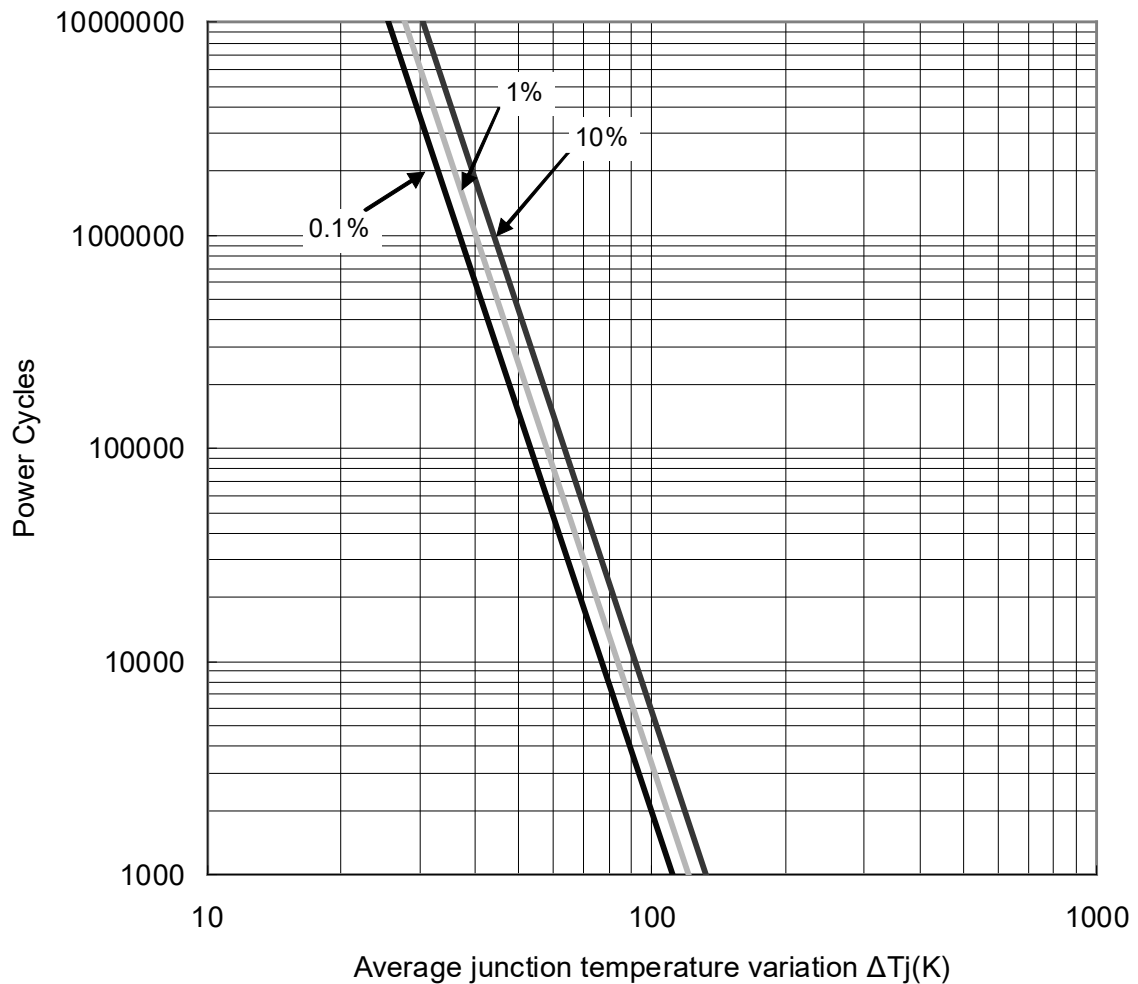


Fig.3-19 Power cycle curve

3.2 Power Loss and Thermal Dissipation Calculation

3.2.1 Power Loss Calculation

Simple expressions for calculating average power loss are given below:

- Scope

The power loss calculation intends to provide users a way of selecting a matched power device for their VVVF inverter application. However, it is not expected to use for limit thermal dissipation design.

- Assumptions

- (1) PWM controlled VVVF inverter with sinusoidal output;
- (2) PWM signals are generated by the comparison of sine waveform and triangular waveform.
- (3) Duty amplitude of PWM signals varies between $\frac{1-D}{2} \sim \frac{1+D}{2}$ (%/100), (D: modulation depth).
- (4) Output current varies with $I_{cp} \cdot \sin x$ and it does not include ripple.
- (5) Power factor of load output current is $\cos\theta$, ideal inductive load is used for switching.

- Expressions Derivation

PWM signal duty is a function of phase angle x as $\frac{1+D \times \sin x}{2}$ which is equivalent to the output voltage variation. From the power factor $\cos\theta$, the output current and its corresponding PWM duty at any phase angle x can be obtained as below:

$$\text{Output current} = I_{cp} \times \sin x$$

$$\text{PWM Duty} = \frac{1 + D \times \sin(x + \theta)}{2}$$

Then, $V_{CE(sat)}$ and V_{EC} at the phase x can be calculated by using a linear approximation:

$$V_{ce(sat)} = V_{ce(sat)}(@ I_{cp} \times \sin x)$$

$$V_{ec} = (-1) \times V_{ec}(@ I_{cp}(= I_{cp}) \times \sin x)$$

Thus, the static loss of IGBT is given by:

$$\frac{1}{2\pi} \int_0^{\pi} (I_{cp} \times \sin x) \times V_{ce(sat)}(@ I_{cp} \times \sin x) \times \frac{1 + D \sin(x + \theta)}{2} \bullet dx$$

Similarly, the static loss of free-wheeling diode is given by:

$$\frac{1}{2\pi} \int_{\pi}^{2\pi} ((-1) \times I_{cp} \times \sin x) ((-1) \times V_{ec}(@ I_{cp} \times \sin x) \times \frac{1 + D \sin(x + \theta)}{2}) \bullet dx$$

On the other hand, the dynamic loss of IGBT, which does not depend on PWM duty, is given by:

$$\frac{1}{2\pi} \int_0^{\pi} (P_{sw(on)}(@ I_{cp} \times \sin x) + P_{sw(off)}(@ I_{cp} \times \sin x)) \times f_c \bullet dx$$

FWDi recovery characteristics can be approximated by the ideal curve shown in Fig.3-20, and its dynamic loss can be calculated by the following expression:

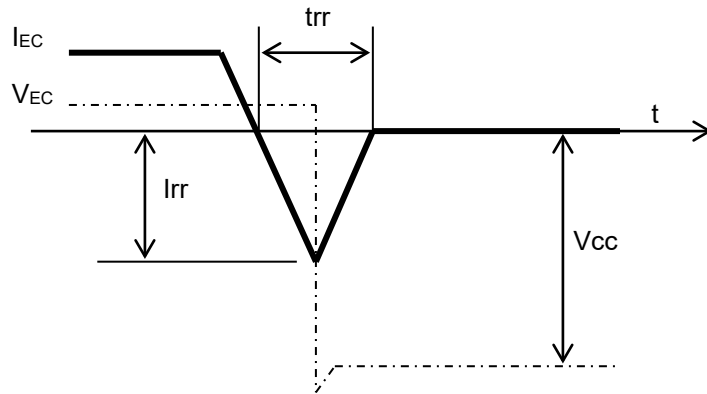


Fig.3-20 Ideal FWDi recovery characteristics curve

$$P_{sw} = \frac{I_{rr} \times V_{cc} \times t_{rr}}{4}$$

Recovery occurs only in the half cycle of the output current, thus the dynamic loss is calculated by:

$$\begin{aligned} & \frac{1}{2} \int_{\pi}^{2\pi} \frac{I_{rr}(@ I_{cp} \times \sin x) \times V_{cc} \times t_{rr}(@ I_{cp} \times \sin x)}{4} \times fc \cdot dx \\ & = \frac{1}{8} \int_{\rho}^{2\pi} I_{rr}(@ I_{cp} \times \sin x) \times V_{cc} \times t_{rr}(@ I_{cp} \times \sin x) \times fc \cdot dx \end{aligned}$$

- Attention of applying the power loss simulation for inverter designs
 - Divide the output current period into fine-steps and calculate the losses at each step based on the actual values of PWM duty, output current, $V_{CE(sat)}$, V_{EC} , and P_{sw} corresponding to the output current. The worst condition is most important.
 - PWM duty depends on the signal generating way.
 - The relationship between output current waveform or output current and PWM duty changes with the way of signal generating, load, and other various factors. Thus, calculation should be carried out on the basis of actual waveform data.
 - $V_{CE(sat)}$, V_{EC} and $P_{sw}(on, off)$ should be the values at $T_j=125^{\circ}C$.

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3.2.2 Temperature Rise Considerations and Calculation Example

Fig.3-21 shows the typical characteristics of allowable motor rms current versus carrier frequency under the following inverter operating conditions based on power loss simulation results.

Conditions: $V_{CC}=600V$, $V_D=V_{DB}=15V$, $V_{CE(sat)}=Typ.$, $P.F=0.8$, $Switching\ loss=Typ.$, $T_j=125^\circ C$, $T_c=100^\circ C$, $R_{th(j-c)}=Max.$, 3-phase PWM modulation, 60Hz sine waveform output

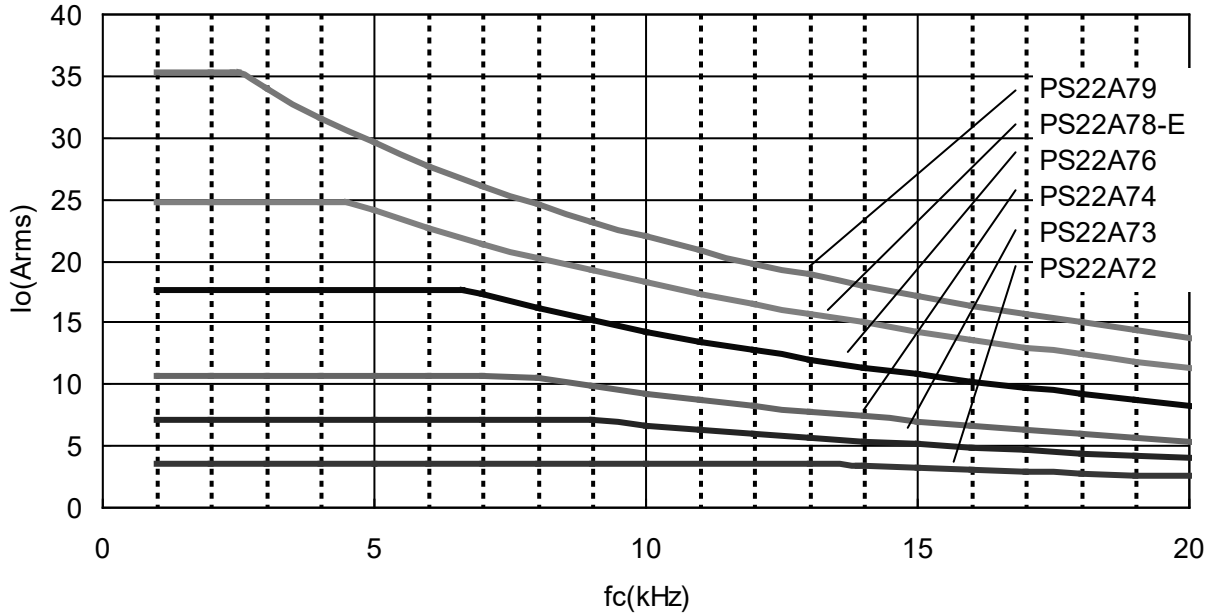


Fig.3-21 Effective current-carrier frequency characteristic

Fig.3-21 shows an example of estimating allowable inverter output rms current under different carrier frequency and permissible maximum operating temperature condition ($T_c=100^\circ C$ and $T_j=125^\circ C$). The results may change for different control strategy and motor types. Anyway please ensure that there is no large current over device rating flowing continuously.

The allowable motor current can also be obtained from the free power loss simulation software provided by Mitsubishi Electric on its web site. (URL: <http://www.mitsubishielectric.com/semiconductors/>)

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3.3 Noise and ESD Withstand Capability

3.3.1 Evaluation Circuit of Noise Withstand Capability

DIIPM have been confirmed to be with over +/-2.0kV noise withstand capability by the noise evaluation under the conditions shown in Fig.3-22. However, noise withstand capability greatly depends on the test environment, the wiring patterns of control substrate, parts layout, and other factors; therefore an additional confirmation on prototype is necessary.

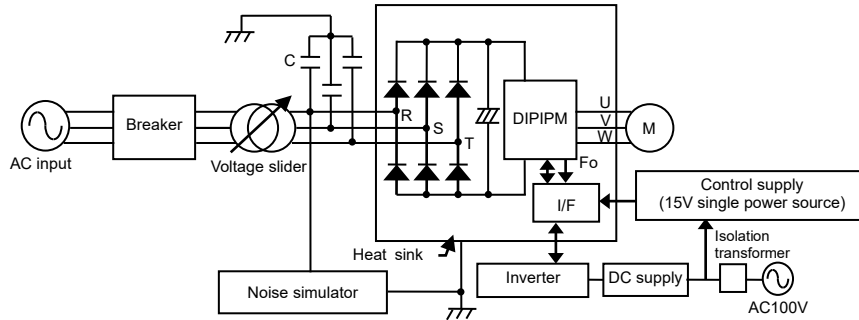


Fig.3-22 Noise withstand capability evaluation circuit

Note: C1: AC line common-mode filter 4700pF, PWM signals are input from microcomputer by using opto-couplers, 15V single power supply, Test is performed with IM

Test conditions

$V_{CC}=600V$, $V_D=15V$, $T_a=25^\circ C$, no load

Scheme of applying noise: From AC line (R, S, T), Period $T=16ms$, Pulse width $tw=0.05-1\mu s$, input in random.

3.3.2 Countermeasures and Precautions

DIIPM improves noise withstand capabilities by means of reducing parts quantity, lowering internal wiring parasitic inductance, and reducing leakage current. But when the noise affects on the control terminals of DIIPM (due to no good wiring pattern on PCB), the short circuit or malfunction of SC protection may occur. In that case, the countermeasures are recommended.

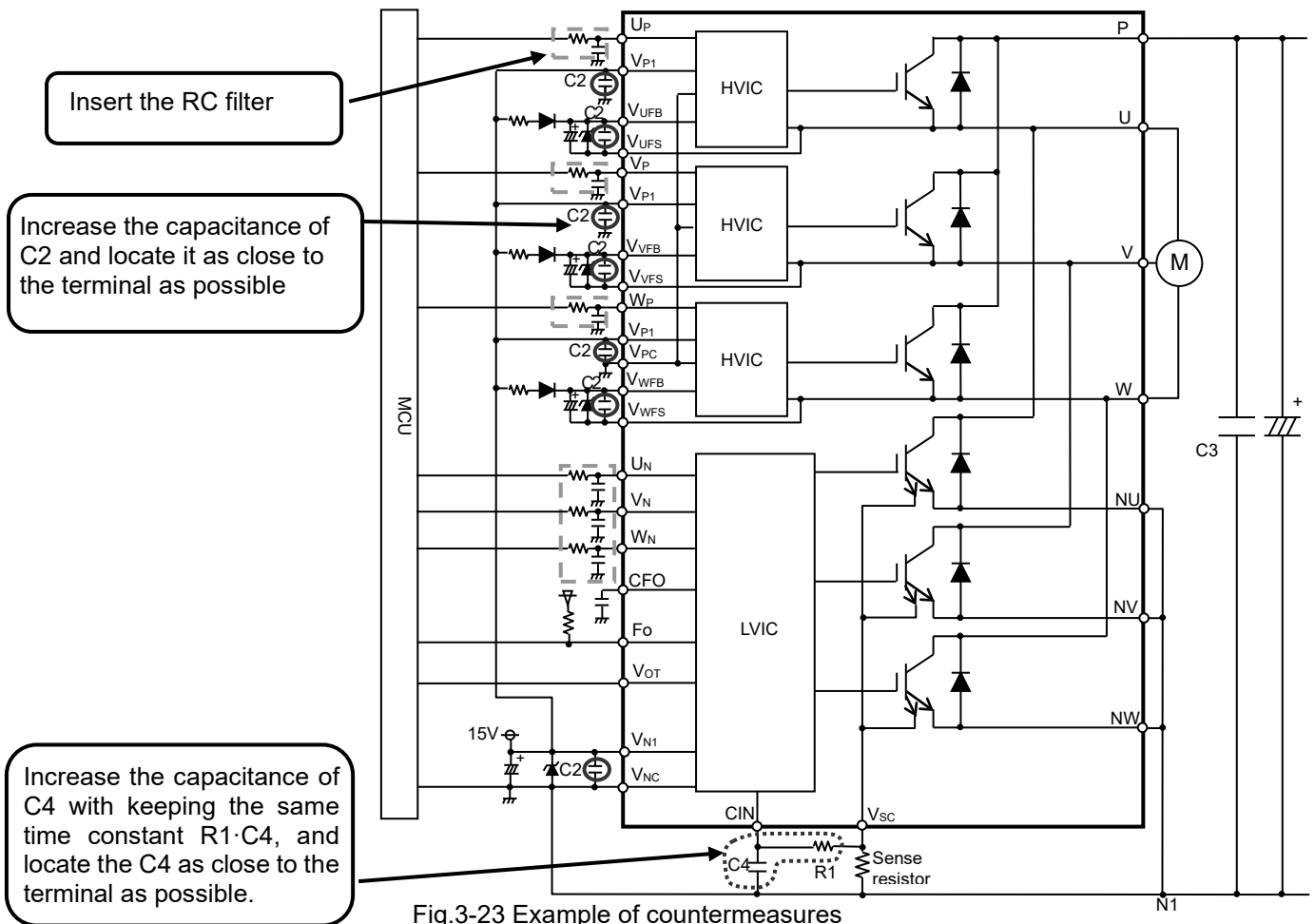


Fig.3-23 Example of countermeasures

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3.3.3 Static Electricity Withstand Capability

DIIPM has been confirmed to be with +/-200V or more withstand capability against static electricity from the following tests shown in Fig.3-24 and Fig.3-25. The results (typical data) are described in Table 3-4 and 3-5.

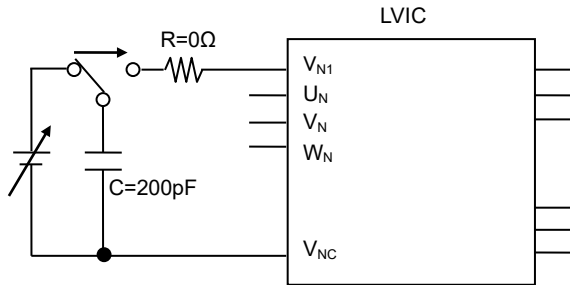


Fig.3-24 Surge test circuit example (V_{N1} terminal)

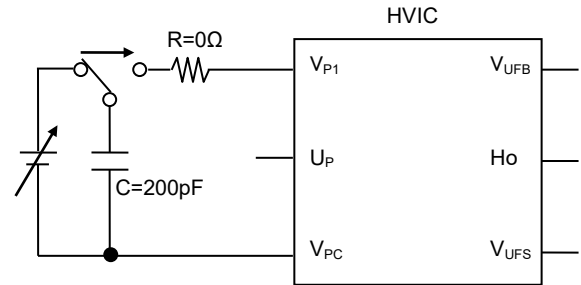


Fig.3-25 Surge test circuit example (V_{P1} terminal)

Conditions: Surge voltage increases by degree and only one-shot surge pulse is impressed at each surge voltage.
(Limit voltage of surge simulator: ±4.0kV, Judged by change in V-I characteristic)

Table 3-4 Typical ESD capability for PS22A72, PS22A73, PS22A74, PS22A76 and PS22A78-E

[Control terminal part]

For control part, since all models have same interface circuit on the control IC, they have same capability.

Terminals	+	-
UP, VP, WP-V _{NC}	0.7	2.1
V _{P1} - V _{NC}	0.4	2.0
V _{UFB} -V _{UFS} , V _{VFB} -V _{VFS} , V _{WFB} -V _{WFS}	0.5	1.9
UN, VN, WN-V _{NC}	0.8	1.5
V _{N1} -V _{NC}	4.0 or more	4.0 or more
CIN-V _{NC}	0.8	1.4
FO-V _{NC}	1.6	2.1
CFO-V _{NC}	1.4	1.6
V _{OT} -V _{NC}	1.5	2.0

[Power terminal part for PS22A72]

Terminals	+	-
V _{SC} -V _{NC}	0.5	0.3
P-NU, NV, NW	4.0 or more	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

[Power terminal part for PS22A73]

Terminals	+	-
V _{SC} -V _{NC}	0.5	0.5
P-NU, NV, NW	4.0 or more	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

[Power terminal part for PS22A74]

Terminals	+	-
V _{SC} -V _{NC}	0.6	0.5
P-NU, NV, NW	4.0 or more	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

[Power terminal part for PS22A76]

Terminals	+	-
$V_{SC}-V_{NC}$	0.3	0.3
P-NU, NV, NW	4.0 or more	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

[Power terminal part for PS22A78-E]

Terminals	+	-
$V_{SC}-V_{NC}$	0.3	0.3
P-NU, NV, NW	4.0 or more	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

Table 3-5 Typical ESD capability for PS22A79

[Control terminal part]

Terminals	+	-
UP, VP, WP- V_{NC}	0.8	1.1
$V_{P1}-V_{NC}$	1.3	1.2
$V_{UFB}-V_{UFS}$, $V_{VFB}-V_{VFS}$, $V_{WFB}-V_{WFS}$	1.9	2.4
UN, VN, WN- V_{NC}	0.9	1.4
$V_{N1}-V_{NC}$	4.0 or more	4.0 or more
CIN - V_{NC}	0.8	1.3
FO - V_{NC}	0.8	1.1
CFO - V_{NC}	0.7	1.3
$V_{OT}-V_{NC}$	0.9	1.6

[Power terminal]

Terminals	+	-
$V_{SC}-V_{NC}$	0.3	0.3
P-NU, NV, NW	4.0 or more	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

CHAPTER 4 Bootstrap Circuit Operation

4.1 Bootstrap Circuit Operation

For three phase inverter circuit driving, normally four isolated control supplies (three for P-side driving and one for N-side driving) are necessary. But using floating control supply with bootstrap circuit can reduce the number of isolated control supplies from four to one (N-side control supply).

Bootstrap circuit consists of a bootstrap diode(BSD), a bootstrap capacitor(BSC) and a current limiting resistor. It uses the BSC as a control supply for driving P-side IGBT. The BSC supplies gate charge when P-side IGBT turning ON and circuit current of logic circuit on P-side driving IC. (Fig.4-2) Since a capacitor is used as substitute for isolated supply, its supply capability is limited. This floating supply driving with bootstrap circuit is suitable for small supply current products like DIIPM.

Charge consumed by driving circuit is re-charged from N-side 15V control supply to BSC via current limiting resistor and BSD when voltage of output terminal (U, V or W) goes down to GND potential in inverter operation. But there is the possibility that enough charge doesn't perform due to the conditions such as switching sequence, capacitance of BSC, limiting resistance and so on. Deficient charge leads to low voltage of BSC and might work under voltage protection (UV). This situation makes the loss of P-side IGBT increase by low gate voltage or stop switching. So it is necessary to consider and evaluate enough for designing bootstrap circuit. For more detail information about driving by the bootstrap circuit, refer the DIIPM application note "Bootstrap Circuit Design Manual"

The circuit current characteristics in switching situation of P-side IGBT are described below.

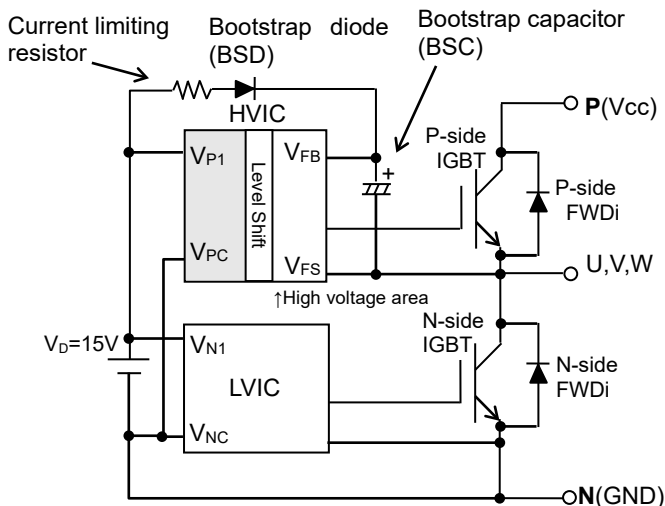


Fig.4-1 Bootstrap Circuit Diagram

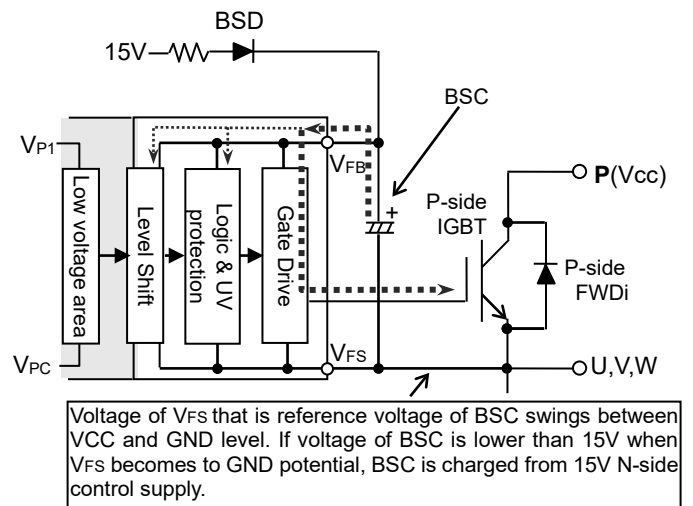


Fig.4-2 Bootstrap Circuit Diagram

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4.2 Bootstrap Supply Circuit Current at Switching State

Bootstrap supply circuit current I_{DB} at steady state is maximum 1.1mA for 1200V Large DIIPM Ver.4 series. But at switching state, because gate charge and discharge are repeated by switching, the circuit current will exceed 1.1mA and increases proportional to carrier frequency. For reference, Fig.4-3~4-8 show the circuit current I_{DB} for P-side IGBT driving supply - carrier frequency f_c typical characteristics for each products.
(Conditions: $V_D=V_{DB}=15V$, IGBT ON Duty=10, 30, 50, 70, 90%)

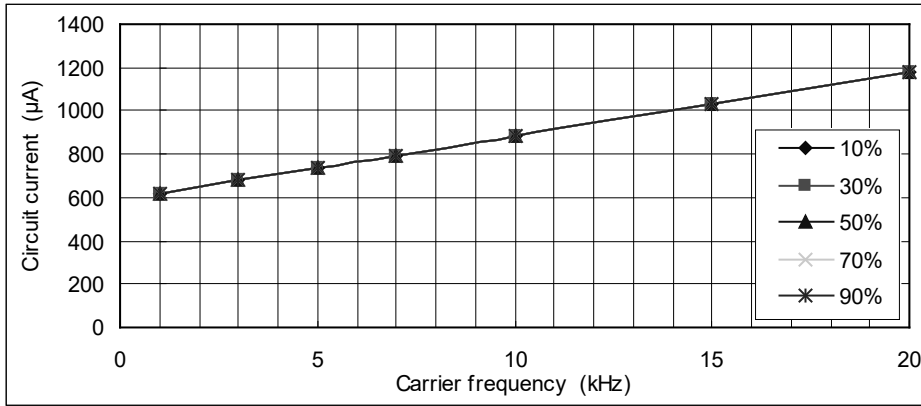


Fig.4-3 I_{DB} vs. Carrier frequency for PS22A72

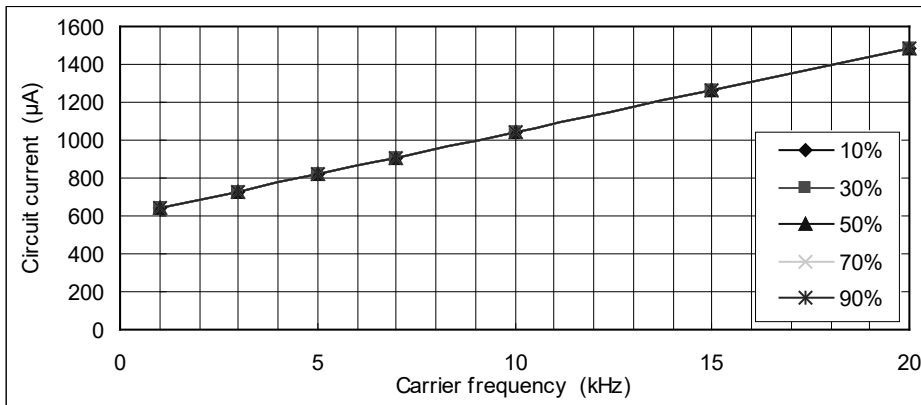


Fig.4-4 I_{DB} vs. Carrier frequency for PS22A73

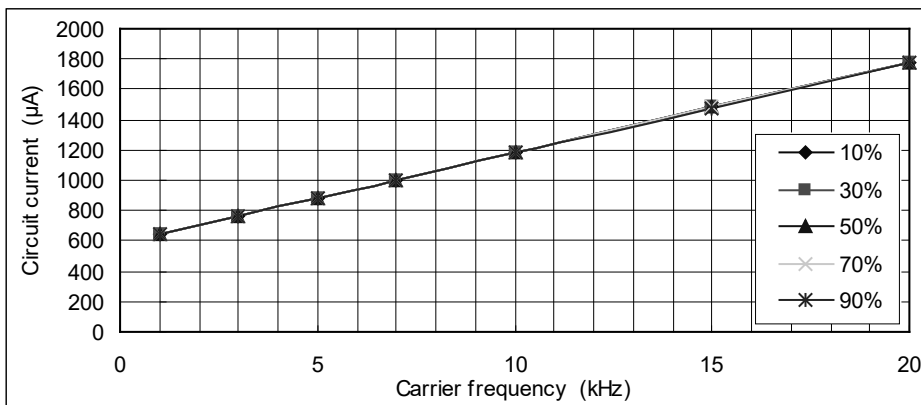


Fig.4-5 I_{DB} vs. Carrier frequency for PS22A74

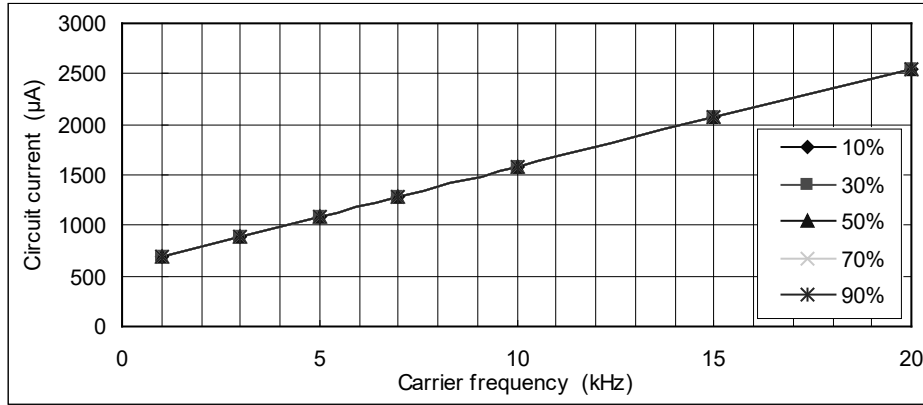


Fig.4-6 I_{DB} vs. Carrier frequency for PS22A76

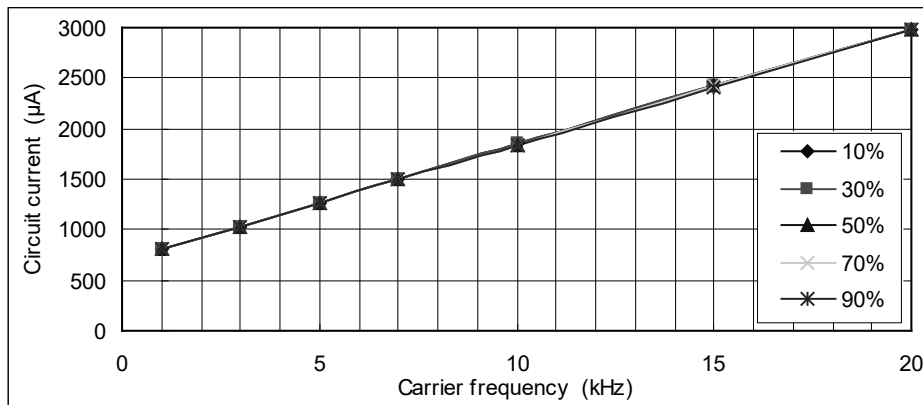


Fig.4-7 I_{DB} vs. Carrier frequency for PS22A78-E

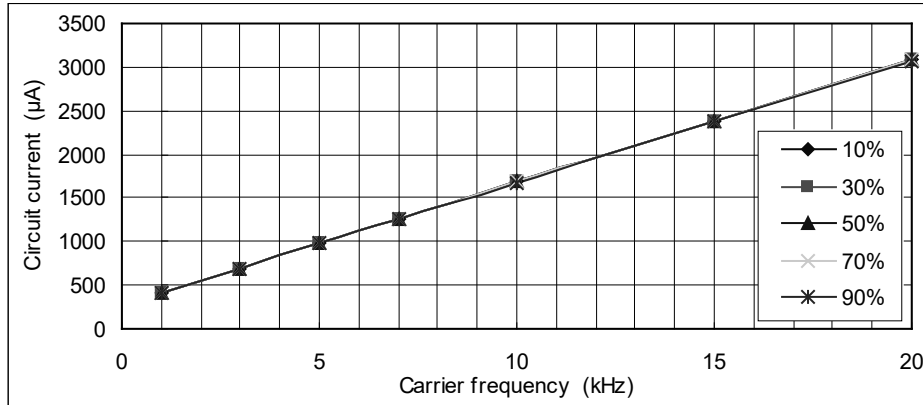


Fig.4-8 I_{DB} vs. Carrier frequency for PS22A79

4.3 Note for designing the bootstrap circuit

When each device for bootstrap circuit is designed, it is necessary to consider various conditions such as temperature characteristics, change by lifetime, variation and so on. Note for designing these devices are listed as below. For more detail information about driving by the bootstrap circuit, refer the DIIPM application note "*Bootstrap Circuit Design Manual*"

(1) Bootstrap capacitor

Electrolytic capacitors are used for BSC generally. And recently ceramic capacitors with large capacitance are also applied. But DC bias characteristic of the ceramic capacitor when applying DC voltage is considerably different from that of electrolytic capacitor. (Especially large capacitance type) Some differences of capacitance characteristics between electrolytic and ceramic capacitors are listed in Table 4-1.

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Table 4-1 Differences of capacitance characteristics between electrolytic and ceramic capacitors

	Electrolytic capacitor	Ceramic capacitor (large capacitance type)
Temperature characteristics (Ta:-20~ 85°C)	<ul style="list-style-type: none"> •Aluminum type: Low temp.: -10% High temp: +10% •Conductive polymer aluminum solid type: Low temp.: -5% High temp: +10% 	Different due to temp. characteristics rank Low temp.: -5%~0% High temp.: -5%~-10% (in the case of B,X5R,X7R ranks)
DC bias characteristics (Applying DC15V)	Nothing within rating voltage	Different due to temp. characteristics, rating voltage, package size and so on -70%~-15%

DC bias characteristic of electrolytic capacitor is not matter. But it is necessary to note ripple capability by repetitive charge and discharge, life time which is greatly affected by ambient temperature and so on. Above characteristics are just example data which are obtained from the WEB, please refer to the capacitor manufacturers about detailed characteristics.

(2) Bootstrap diode

It is recommended for BSD to have same or higher blocking voltage with collector-emitter voltage V_{CES} of IGBT in DIIPM. (i.e. 1200V or more is needed in the case of 1200V DIIPM.) And its recovery time t_{rr} should be less than 100ns. (Fast recovery type)

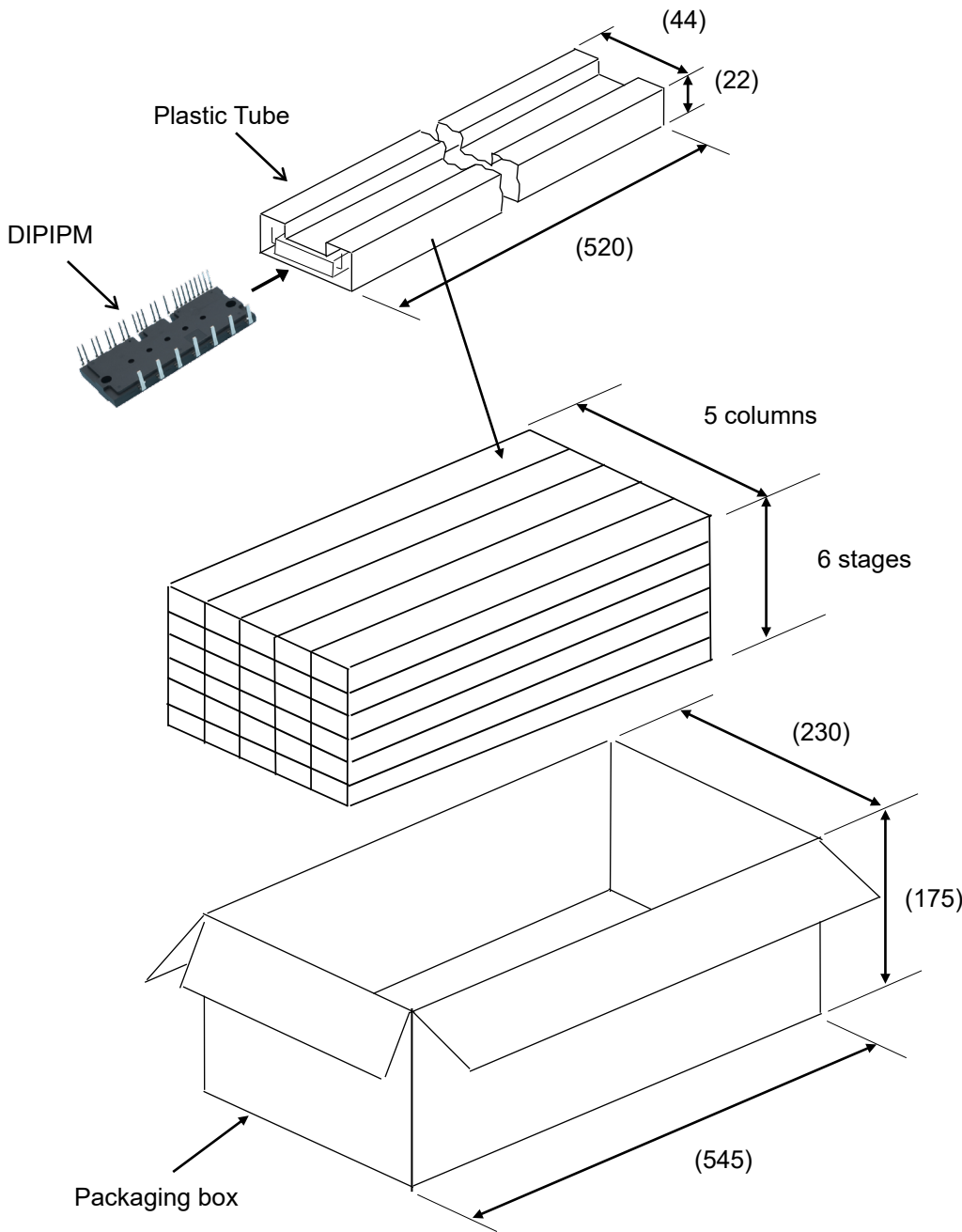
Also **it is highly recommended to apply the high quality product such as small variations of blocking voltage.** If BSD broke by impressed overvoltage and shorted, it leads to the control ICs over voltage destruction because DC-link voltage (V_{cc}) is impressed upon low voltage area of control ICs. Then DIIPM will lose various functions like protection and gate driving and it may lead to serious system destruction.

(3) Current limiting resistor

When designing limiting resistor, it is important to note its power rating, surge withstand capability (there is the possibility that surge may be impressed on the resistor when switching ON or OFF timing) and so on. Especially if small chip type resistor is applied, it is recommended to select anti-surge designed type. For detailed information, please refer to the resistor manufacturer.

CHAPTER5 PACKAGE HANDLING

5.1 Packaging Specification



Quantity:
6pcs per 1 tube

Total amount in one box (max):
Tube Quantity: 5 × 6=30pcs
IPM Quantity: 30 × 6=180pcs


When it isn't fully filled by tubes at top stage, cardboard spacers or empty tubes are inserted for filling the space of top stage.

Weight (max):
About 46g per 1pcs
About 380g per 1tube
About 13kg per 1box

Spacers are inserted into the top and bottom of the box. If there is some space on top of the box, additional buffer materials are also inserted.

Fig.5-1 Packaging Specification

5.2 Handling Precautions

 <h1>Cautions</h1>	
Transportation	<ul style="list-style-type: none">•Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged.•Throwing or dropping the packaging boxes might cause the devices to be damaged.•Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.
Storage	<ul style="list-style-type: none">•We recommend temperature and humidity in the ranges 5-35°C and 45-75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above.
Long storage	<ul style="list-style-type: none">•When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior.
Surroundings	<ul style="list-style-type: none">•Keep modules away from places where water (including dew condensation) or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems.
Flame resistance	<ul style="list-style-type: none">•The epoxy resin of case material is flame-resistant type (UL standard 94V-0), but they are not noninflammable.
Static electricity	<ul style="list-style-type: none">•ICs and power chips with MOS gate structure are used for the DIIPM power modules. Please keep the following notices to prevent modules from being damaged by static electricity. <p>(1)Precautions against the device destruction caused by the ESD The ESD of human bodies and packaging and/or excessive voltage applied across the gate to emitter may damage and destroy devices. The basis of anti-electrostatic is to inhibit generating static electricity possibly and quick dissipation of the charged electricity.</p> <ul style="list-style-type: none">*Containers that charge static electricity easily should not be used for transit and for storage.*Terminals should be always shorted with a carbon cloth or the like until just before using the module. Never touch terminals with bare hands.*Should not be taking out DIIPM from tubes until just before using DIIPM and never touch terminals with bare hands.*During assembly and after taking out DIIPM from tubes, always earth the equipment and your body. It is recommended to cover the work bench and its surrounding floor with earthed conductive mats.*When the terminals are open on the printed circuit board with mounted modules, the modules might be damaged by static electricity on the printed circuit board.*If using a soldering iron, earth its tip. <p>(2)Notice when the control terminals are open</p> <ul style="list-style-type: none">*When the control terminals are open, do not apply voltage between the collector and emitter. It might cause malfunction.*Short the terminals before taking a module off.

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