MITSUBISHI ELECTRIC

<IGBT Module>

J1 Series Application Note

Evaluation Kit: Water Jacket, DC-Link Capacitor, Gate Driver Board

Contents

1. Introduction

This kit is used to evaluate the electrical characteristics of the J1-Series IGBT Module. The kit is not meant to be used for reliability or field testing. For evaluation of reliability, vehicle tests or mass-production, the user must design their own driver board and water jacket and they must not use any part of this evaluation kit for these scenarios.

1.1. IGBT module Line-up for Evaluation kit

This evaluation kit uses some different parts depending on the J1-Series IGBT module being evaluated. Table 1 shows the parts needed based on the module selection.

Table 1: Power module and Evaluation kit list

IGBT module name	Rating	Number of IGBTs	Water Jacket Part #	DC-Link Capacitor Part #	Driver Board Part #
CT600CJ1A060-A	650V/ 600A	6	J1WJB	J1CP45060B	J1RB-5
CT700CJ1A060-A	650V/ 700A	6		J1CP85035B	

1.2. Features

The evaluation kit consists of a water jacket, a DC-Link capacitor, and a gate driver board.

a) Water Jacket

The water jacket assembly consists of the metal jacket and an O-ring. The water jacket is optimally designed to provide efficient direct cooling to the J1-Series IGBT Module. The water jacket cools the J1-Series IGBT Module uniformly across all chips at the same time and also has a very low pressure drop.

b) DC-Link capacitor

The evaluation kit's DC-Link capacitor is a large film capacitor that is mechanically designed to connect to the power terminals of the J1-Series IGBT Module. The DC-Link capacitors are available in 600A and 700A ratings.

c) Driver Board

The driver board uses an ASIC: M8160xJFP to provide the gate drive operation logic and protection functions for the IGBTs, such as under-voltage, over-temperature, and so on. The driver board also has DC/DC power supplies for driving the IGBT gates.

2. Water Jacket

2.1. Specifications

Type and specifications of the water jacket are shown below. Pressure drop characteristics is shown in Fig.1.

Type	Specifications
J1WJB	Recommended flow rate：~10L/min, material：A5052

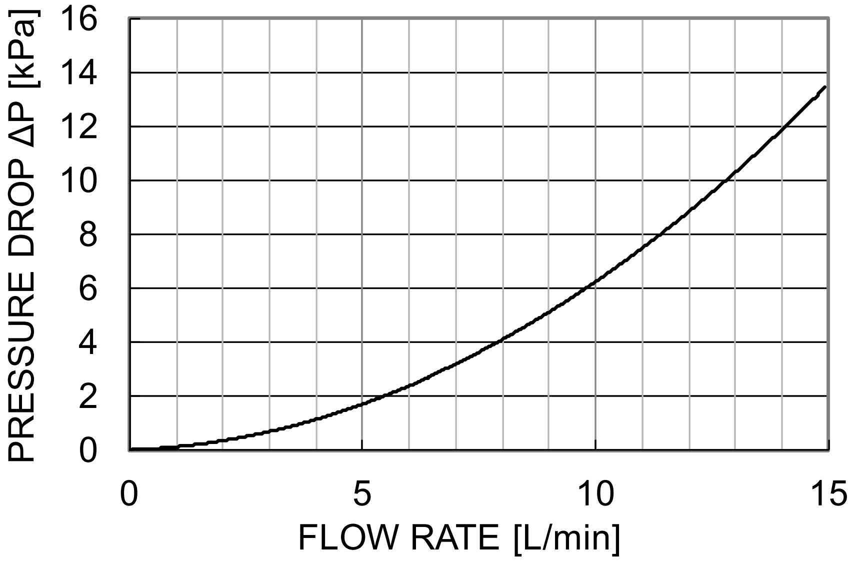


Fig.1 Pressure drop characteristics of J1WJB (representative example)

2.2. Application

This water jacket is used only for bench tests, nor for actual vehicle tests.

2.3. Package Outline

The outline of the water jacket is shown in Fig.2.
The surface gloss and model name printing (J1WJB) processing may change, but this does not affect the function.

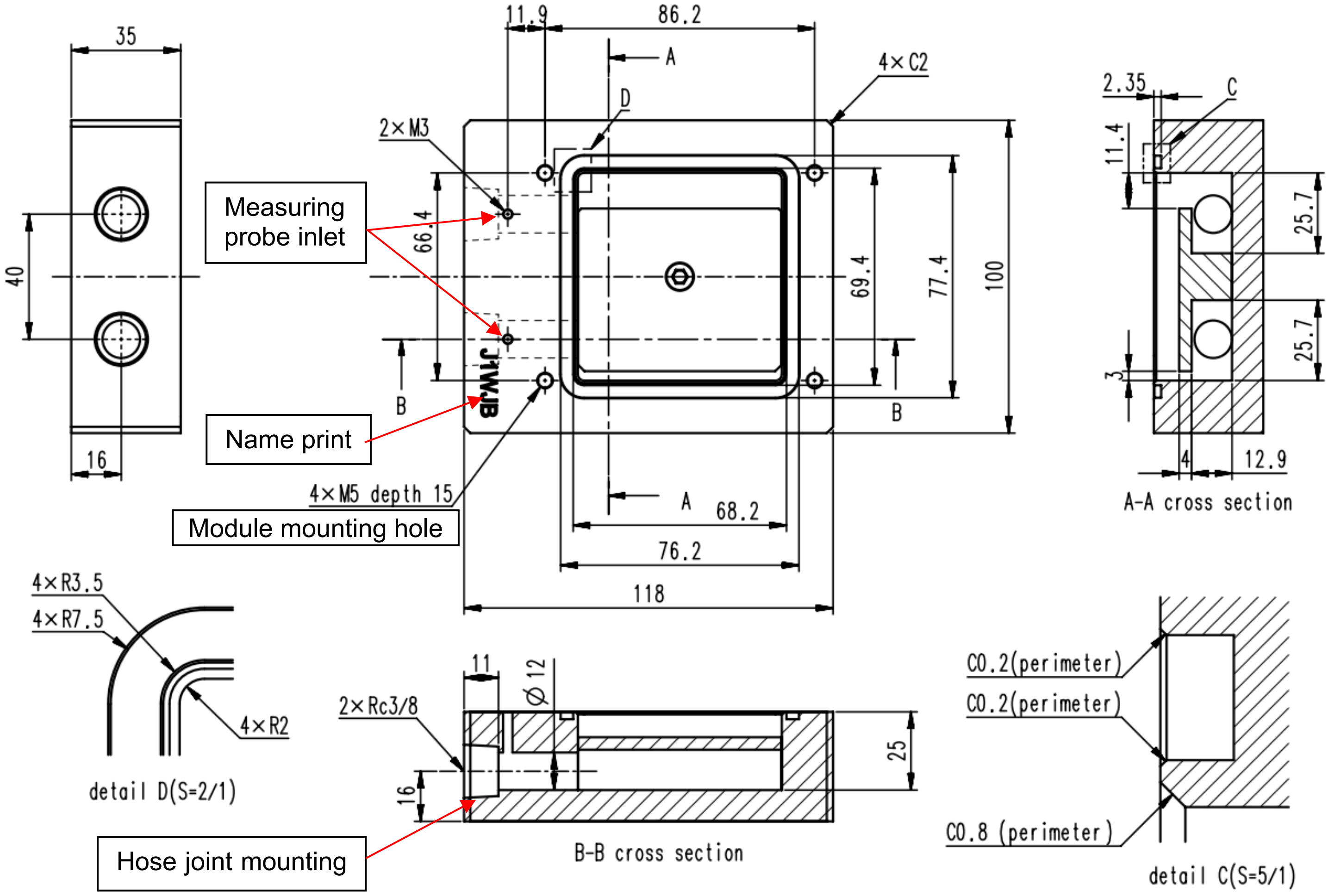


Fig.2 The outline of the water jacket

2.4. Usage

(1) Mounting method

Assembly image to mount the J1-Series IGBT module to the water jacket is shown in Fig.3. When mounting , tighten four counrers of the modules with M5 screws. Refer to each module data sheet for the tightening torque value(*). Mounting screws should be tightened in a diagonal sequence as shown in Fig.5 (A→B→C→D).

Temporary tightening should be done with 20% torque of the maximum rating torque, before the final tightening is done. M5 screws are to be supplied by our customers.

(*)The torque ratio depending on the screws used by the tightening environment. Please refer to Chapter 3 of JMH-00008 for the detailed tightening method.

(2) Setting of cooling water inlet/outlet

Inside diameter of cooling water inlet and outlet is Rc3/8. Fix hose joint wrapped by sealtape to inlet and outlet. Attached hose nipples are used as hosejoints in Fig.3. Please set water flow direction as shown in Fig.4.

[Caution]

1. In this jacket, there are holes made for a measureing probe such as a differential pressure guage, a theremocouple, etc.. Unless you use the measuring mechines, please fill the holes with screws wrapped by sealtape.
2. Don’t set water flow direction oppossite to that shown in Fig.4.

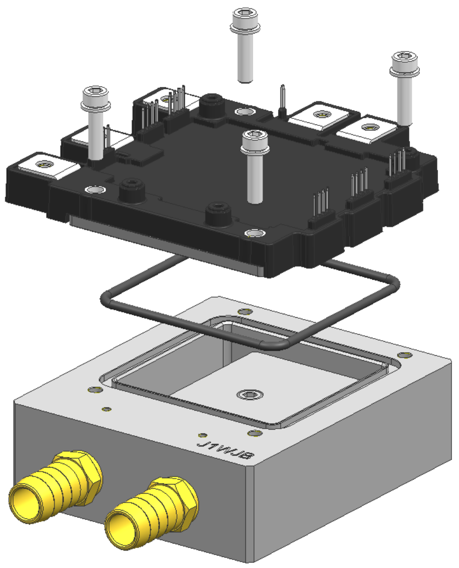


Fig.3 Assembly image

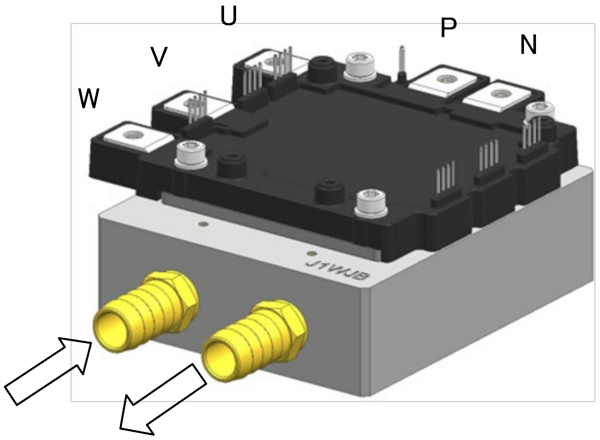


Fig.4 Flow direction of cooling water

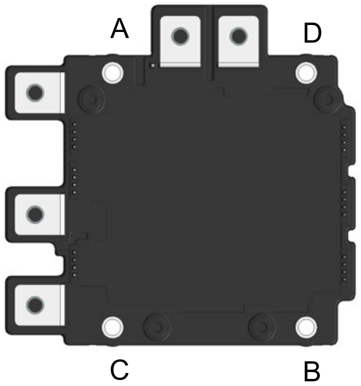


Fig.5 Mounting sequence of J1-seriese

2.5. Parts

The water jacket consists of these parts listed in Table1.

Table1 Parts list

No.	quantity	Name of parts	Note
1	1	Water jacket	—
2	1	O-ring（accessories）	Outline:Fig.6, Material:EPDM
3	2	Hose nipple(accessories)	Made by misumi corporation, HOSNS153

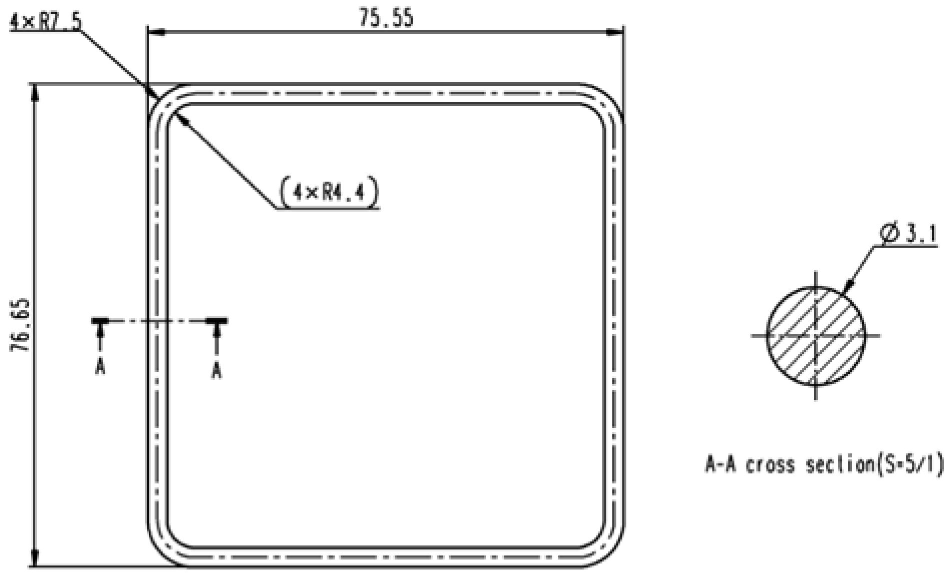


Fig.6 The outline of the O-ring

3. DC-Link Capacitor

3.1. Specifications

Specifications of the DC-Link capacitor are listed below.

Type	J1CP45060B	J1CP85035B
Rating Voltage	450VDC	850VDC
Rating Capacitance	600μF (100μF connected in parallel)	348μF (58μF connected in parallel)
Operating Temperature	-40~105°C	-40~105°C
ESL	15nH	15nH
Allowable ripple current	126Arms (21Arms × 6 : 10kHz, 70°C max)	108Arms (18Arms × 6 : 10kHz, 70°C max)

Fig.7 appearance

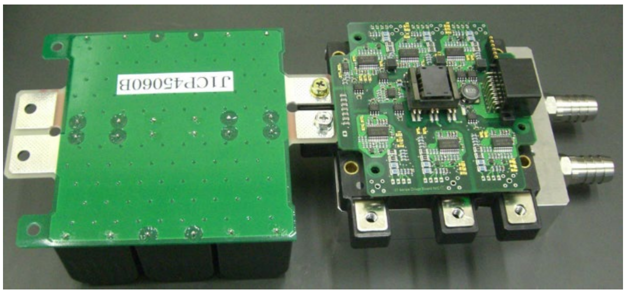


Fig.8 mounting image

3.2. Application

A three-phase inverter can be configured by combining the DC-Link capacitor with J1 series. The DC-Link capacitor is used only for bench tests, nor for actual vehicle tests.

3.3. Package Outline

Outlines of the DC-Link capacitor are shown in Fig.9.

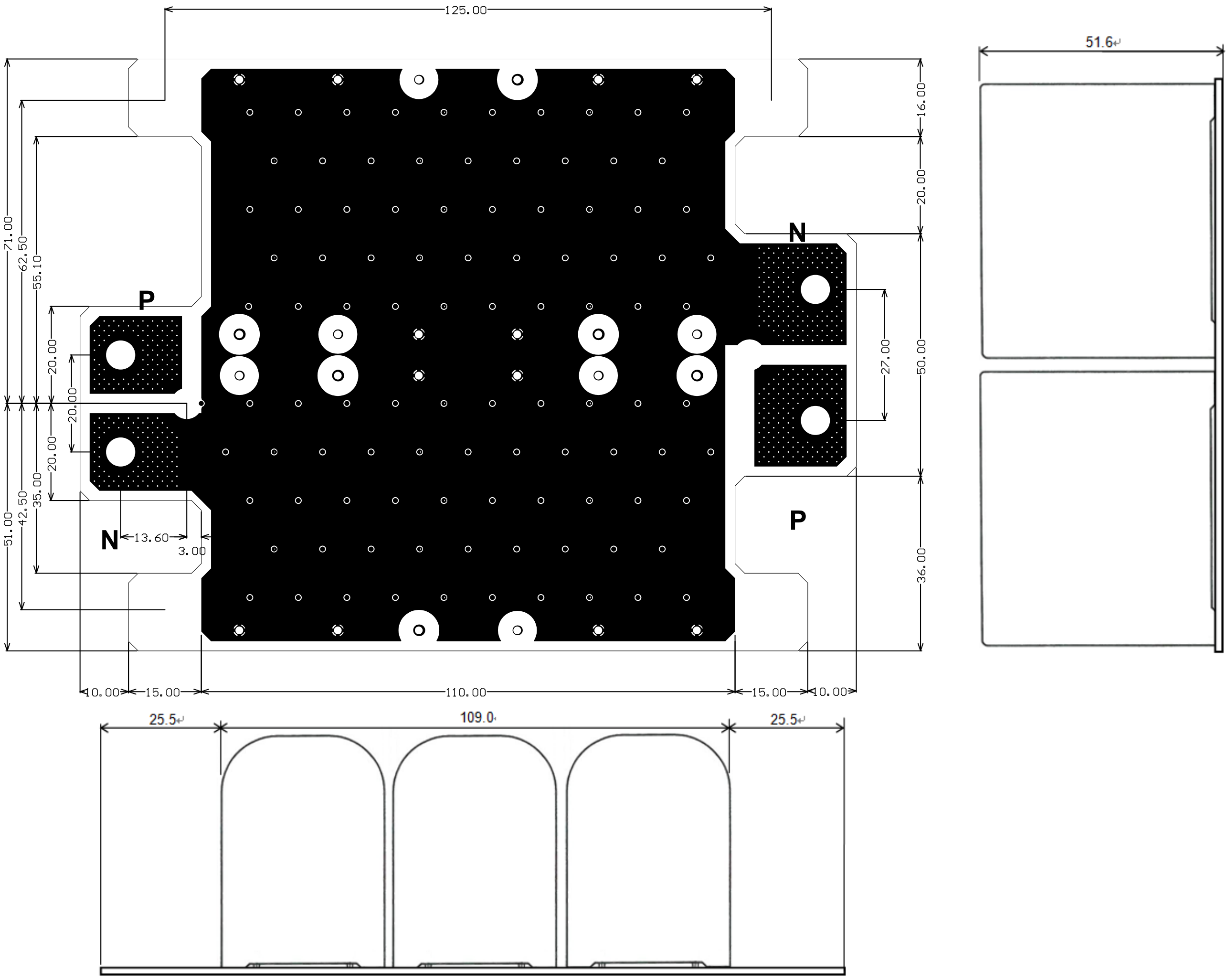


Fig.9 outline

4. Driver Board

4.1. Specifications

There are several different models of the driver board since each power module requires optimized driver and protection circuits. The driver board line-up is shown below in Table 1.

Table 1 Line-up of the driver board

Applicable Power module	Short-time short-circuit protection	
	Included	Not Included
CT600CJ1A060-A	J1RB-5␣610	J1RB-5␣620
CT700CJ1A060-A	J1RB-5␣611	J1RB-5␣621

4.2. Application

The driver board makes it possible to evaluate the electrical properties of the J1 series power modules.

The driver board can be used only for bench tests, not for actual vehicle tests. Component values mentioned in this application note such as resistors, capacitors, etc. are for basic tests and cannot be recommended for all applications. Therefore, it may be necessary to adjust the values according to the application.

There is no moisture-proof coating applied to the driver board so that components may be replaced if necessary. Before mounting the driver board to the IGBT module, please apply a moisture-proof coating if applicable.

4.3. Features

Features of the driver board are shown below.

- On-board Gate driver IC (M8160x[1]JFP) developed for J1 series power module
  The Gate driver IC (M8160xJFP) mounted on the driver board has several functions which maximize the performance of the J1 series IGBT Power Module by using the on-chip current sensor and on-chip temperature sensor. IGBT drive and protection functions performed by the IC are shown below.
  - Short-time short-circuit protection
    Protection from a short-time short-circuit(less than 1μsec) which has been caused by accidental turn-on of IGBT.
  - Short-circuit (SC) protection
    High speed protection against the arm-short, load-short, etc.
  - Over-current (OC) protection
    Protection circuit with accurate trip level around 1.2 ~ 2 times rated collector current.
  - Short-circuit (SC) current suppression
    Suppresses collector current when short-circuit occurs.
    Response time of the short-circuit (SC) protection circuit can be optimized by this function.
  - 2 types soft shutdown functions
    Short-circuit (SC) protection circuit and over-current (OC) protection circuit can use different soft-shutdown resistors for optimization.
  - Temperature compensation circuit for OC trip level
    Temperature characteristics of over-current (OC) trip level can be adjusted.
  - Switching of turn-off gate resistance.
    Smaller resistance is used for turn-off switching at high temperature.
  - Over-temperature (OT) protection
  - DC/DC power supply under-voltage (UV) protection

- P-N over-voltage protection.
  Over-voltage breakdown is prevented by cancelling the IGBT turn-on signal when a P-N over-voltage is detected.

- DC/DC power supply.
  DC/DC power supply supports the six gate drive power supplies (UH,VH,WH,UL,VL,WL)

- Gate drive signal interface.
  The driver board uses on-board magnetic couplers as isolators and can be driven by a TTL-level signal.

- Interlock function.
  Interlock function helps prevent High side IGBTs and Low side IGBTs from turning on at the same time.

- Dead-time control function.
  Dead-time is automatically expanded to prevent an arm-short, if the dead-time of the gate drive signal is shorter than the required dead-time under the each conditions.

[1] There are two types, M81603JFP and M81605JFP. Refer to datasheet for detail.

4.4. Accessories

In addition to a board-side connector for I/O terminal (CN1) on the driver board, a harness can be constructed from the following plugs and contact pins.

Table 2 Accessories

Accessories	Manufacturer : Product : Part Number	Note
Board-side connector	Tyco Electronics : 16 POS CAP HOUSING ASSY : C-175615 or Tyco Electronics : 28 POS CAP HOUSING ASSY : C-175976	Equipped on board
Plugs	Tyco Electronics : 16 POSITION PLUG HOUSING ASSEMBLY : C-175966 When C-175976 CAP HOUSING is equipped on board, below PLUG is attached. Tyco Electronics : 12 POSITION PLUG HOUSING ASSEMBLY : C-175965	
Contact pins	Tyco Electronics : 040 SERIES RECEPTACLE CONTACT : C-173681	

4.5. Block Diagram

Block diagram of the driver board is shown in Figure 10.

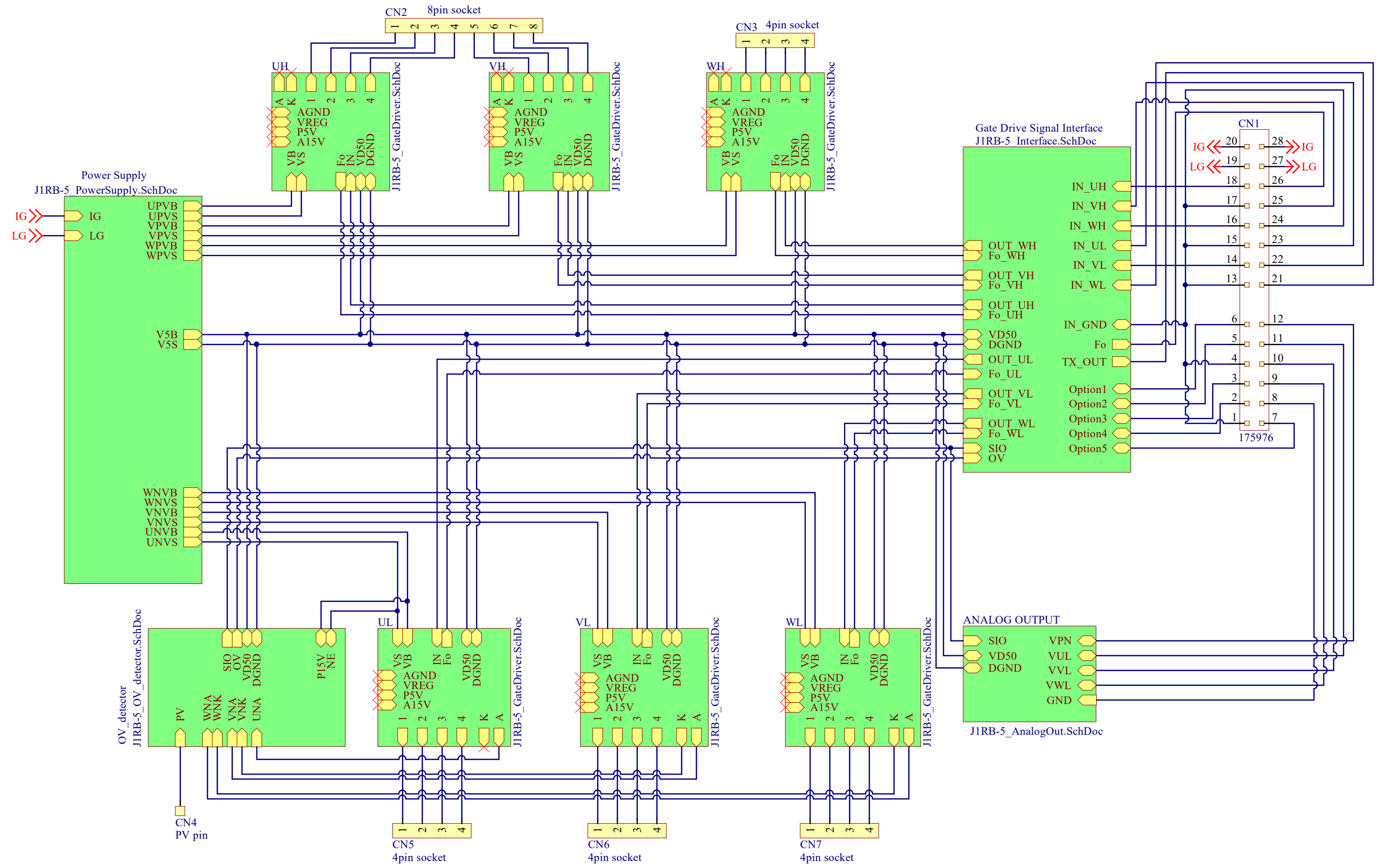


Figure 10. Block Diagram

4.6. Driver board outlines

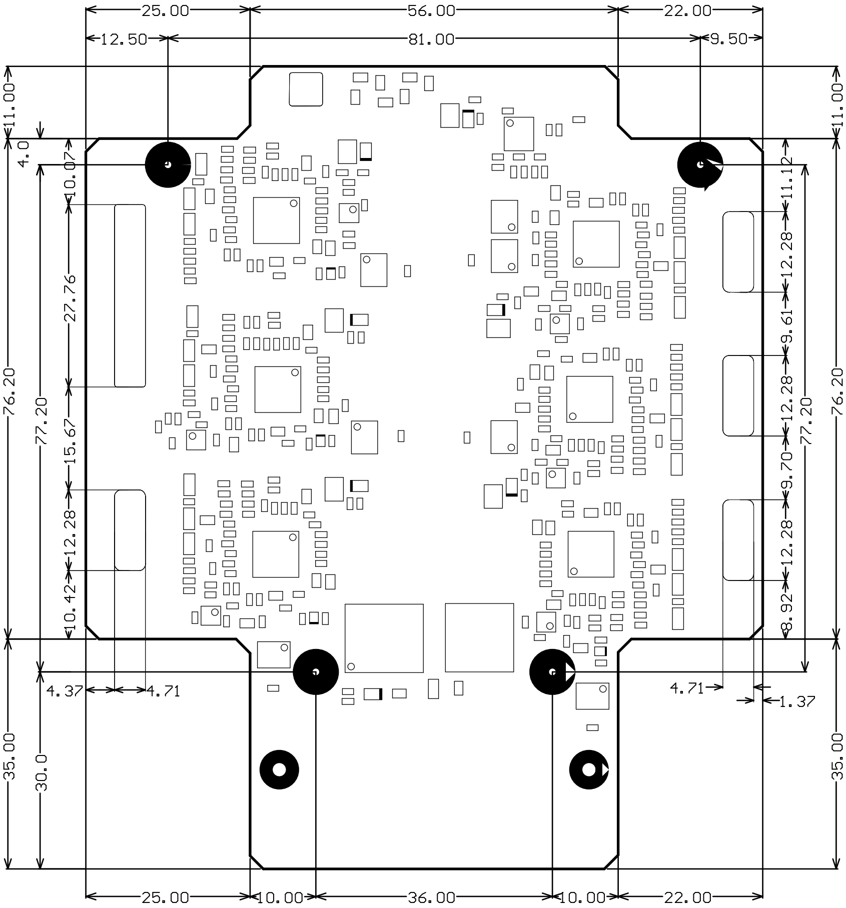


Figure 11. Driver board outline (unit: [mm])

4.7. Mounting

A driver-board mounting image is shown in Figure 12-1 and Figure 12-2.

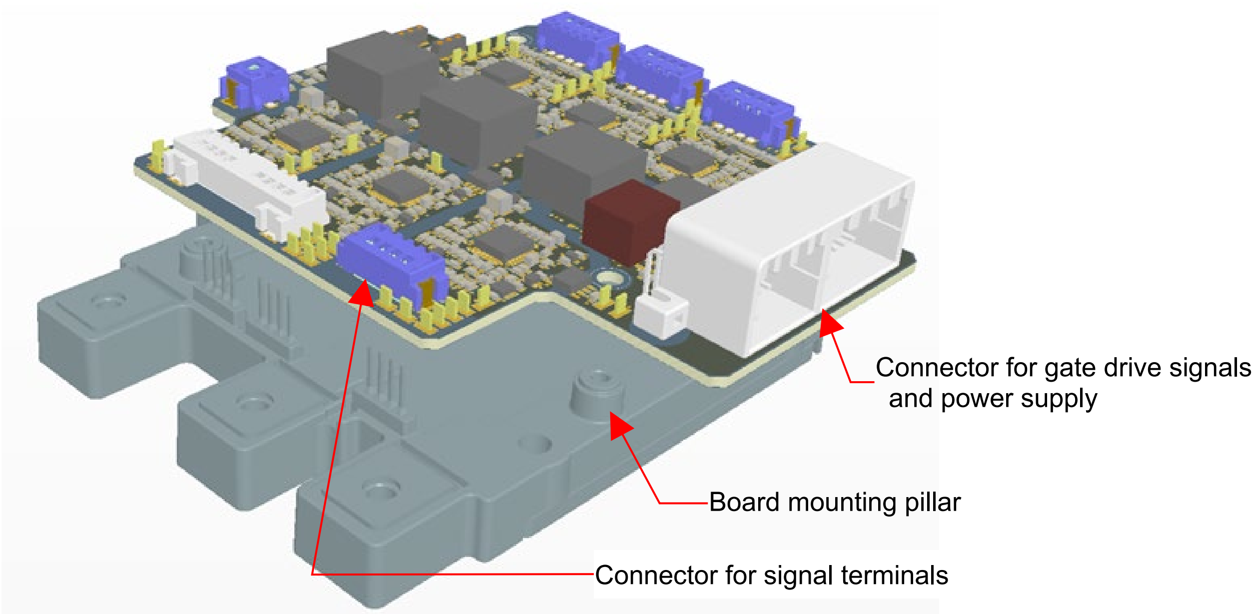


Figure 12-1 Mounting image

There are four pillars to fix the driver-board on the insert-case. A tapping screw is recommended to fix the driver-board on the pillars. A depth of hole in the pillars is 7±0.2mm. Recommended length of the screw is 6mm at the maximum so that it shouldn't touch the bottom of the hole when tightening. Please use appropriate screws by considering thicknesses of a PCB and a shield plate. 3.5×6mm screws are being used for our evaluation with a PCB of 1.6mm thickness.

It is important to set appropriate tightening torque for the tapping screw. The pillars may be broken if the tightening torque is too large. The driver-board cannot be fixed to the pillars if the tightening torque is too small.

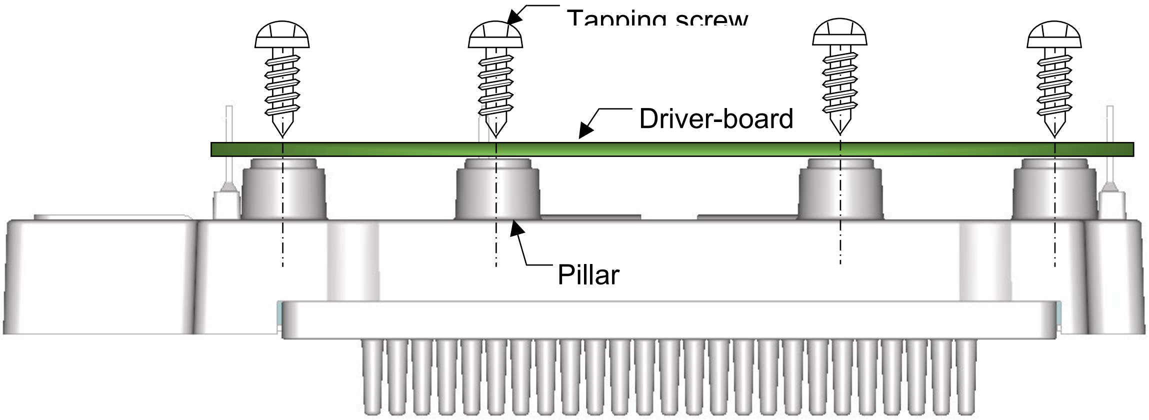
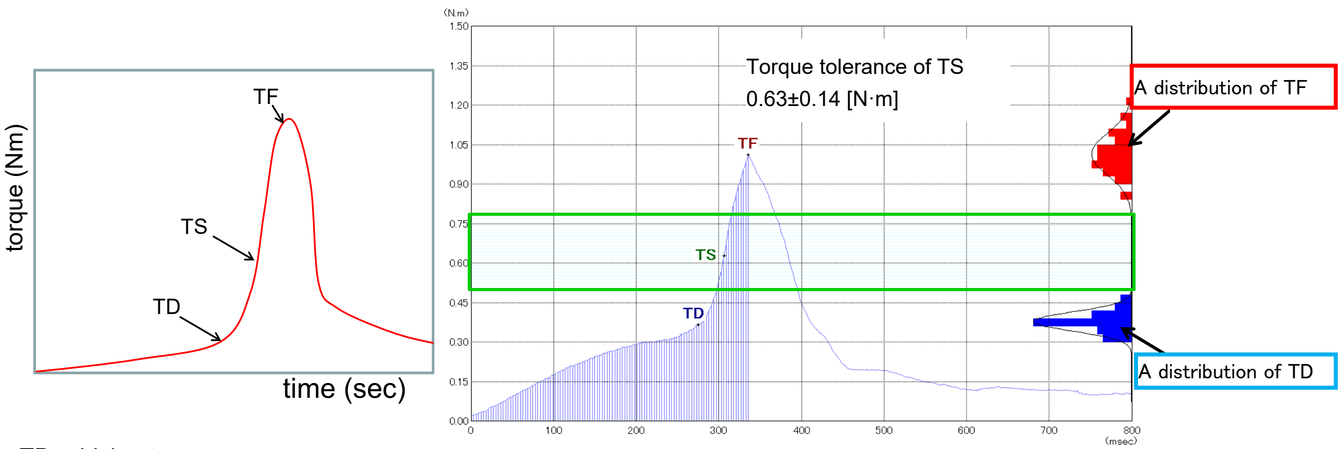


Figure 12-2 Driver-board mounting image

The way to evaluate appropriate tightening torque for the tapping screw is shown below. Figure 12-13 shows measured torque until a failure when tightening the tapping screw at a fixed rotation speed with a torque analyzer. Setting torque (TS) is calculated by measured driving torque (TD) and failure torque (TF). The evaluation was done with JIS Ⅱ grooved tapping screws (3.5×6) and PCB of 1.6mm thickness. The number of samples is 40. From the result, appropriate torque under our evaluation condition is calculated to be 0.63±0.14Nm.

According to the screw manufacturer, TF might improve by using the tapping screws designed especially for plastic (e.g. Delta PT® from EJOT, B-Tite screw, P-Tite screw, and PC screw). Please carefully choose appropriate tapping screws after consulting a screw manufacturer.



TD : driving torque
TF : failure torque
TS : setting torque, TS=(TD+TF)/2

Tapping screw : JIS Ⅱ grooved tapping screws (3.5×6), a number of sample = 40
Thickness of PCB : 1.6mm
Shield plate : Nothing

Figure 12-1 Outline of setting torque evaluation and measured results

4.8. I/O Terminal (CN1)

(1) I/O Terminal (CN1) Pins Layout

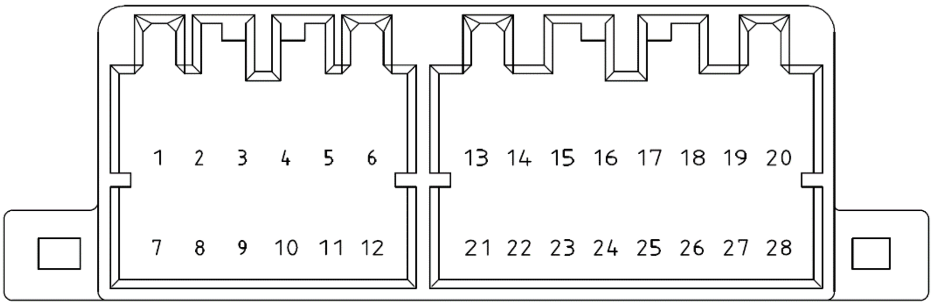


Figure 13 I/O Terminal (CN1) Pins Layout

Table 3 I/O terminal CN1 pins configuration (Active-Low)

Pin	Signal name	Note	Pin	Signal name	Note
20	IG DC Supply input (+)		28	IG DC Supply input (+)	
19	LG DC Supply input (-)	Connected to DGND via jumper J10	27	LG DC Supply input (-)	Connected to DGND via jumper J10
18	UH U-phase H-side gate drive signal	IGBT turns on when UH is Low	26	Fo	Fault output (Normally High, Low during Fault)
17	GND	Gate drive signal return	25	VH V-phase H-side gate drive signal	IGBT turns on when VH is Low
16	WH W-phase H-side gate drive signal	IGBT turns on when WH is Low	24	GND	Gate drive signal return
15	GND	Gate drive signal return	23	UL U-phase L-side gate drive signal	IGBT turns on when UL is Low
14	VL V-phase L-side gate drive signal	IGBT turns on when VL is Low	22	TX Serial output	P-N voltage, on-chip temperature sensor output
13	GND	Gate drive signal return	21	WL W-phase L-side gate drive signal	IGBT turns on when WL is Low
6	Option1	Optional output	12	VPN	Analog output option
5	Option2	Optional output	11	VUL	Analog output option
4	GND		10	VVL	Analog output option
3	Option3	Optional output	9	VWL	Analog output option
2	Option4	Optional output	8	GND	
1	GND		7	Option5	Optional output

(2) I/O terminals CN1 maximum ratings

Symbol	Parameter	Condition	Rating	Unit
IG	Power Supply input	LG level	(36)	V
UH	Gate drive signal U-phase H-side	GND level	-0.5~5.5	V
VH	Gate drive signal V-phase H-side	GND level	-0.5~5.5	V
WH	Gate drive signal W-phase H-side	GND level	-0.5~5.5	V
UL	Gate drive signal U-phase L-side	GND level	-0.5~5.5	V
VL	Gate drive signal V-phase L-side	GND level	-0.5~5.5	V
WL	Gate drive signal W-phase L-side	GND level	-0.5~5.5	V

(3) Electrical characteristics of I/O terminal CN1 (Ta=25°C)

Symbol	Parameter		Condition	Ratings			Unit
				Min.	Typ.	Max.	
IG	Supply input		LG level	8	-	24	V
VinL	Threshold voltage L of signal input for gate drive		GND level	0	-	0.8	V
VinH	Threshold voltage H of signal input for gate drive		GND level	2.0	-	5.0	V
Fo	Fo output	No Fault	GND level	2.4	-	5.0	V
		When Fault has occurred	GND level	0	-	0.5	V
TX	Serial output	L output	GND level	0	-	0.5	V
		H output	GND level	2.4	-	5.0	V

(4) Harness Construction Notes

When making harness, it is recommended to shield the entire harness or twist gate drive signal line and GND line in order to prevent noise interference.

4.9. Functions

Each gate drive function is explained in detail below.

(1) Gate drive signal input

The basic schematic of the gate drive signal input is shown in Figure 14.

The input to the CPLD is pulled-up internally. The gate drive circuit (High voltage side) is isolated from the gate drive signal (Low voltage side) by magnetic couplers. The output of a microcomputer or other controlling device can be used as the gate drive input.

The input logic polarity of the gate drive signal can be switched. By default, the input accepts active-low logic. In order to switch to active-high, remove R54 and mount R53.

When the P-N over-voltage protection circuit detects over-voltage between P-N terminals, the IGBT turn-on signal is cancelled. Refer section 0 for details.

This circuit has an interlock function to prevent P and N-side IGBTs from turning on at the same time (Figure 15). In order to disable the function for evaluation, remove R55 and mount R52 as shown in Figure .

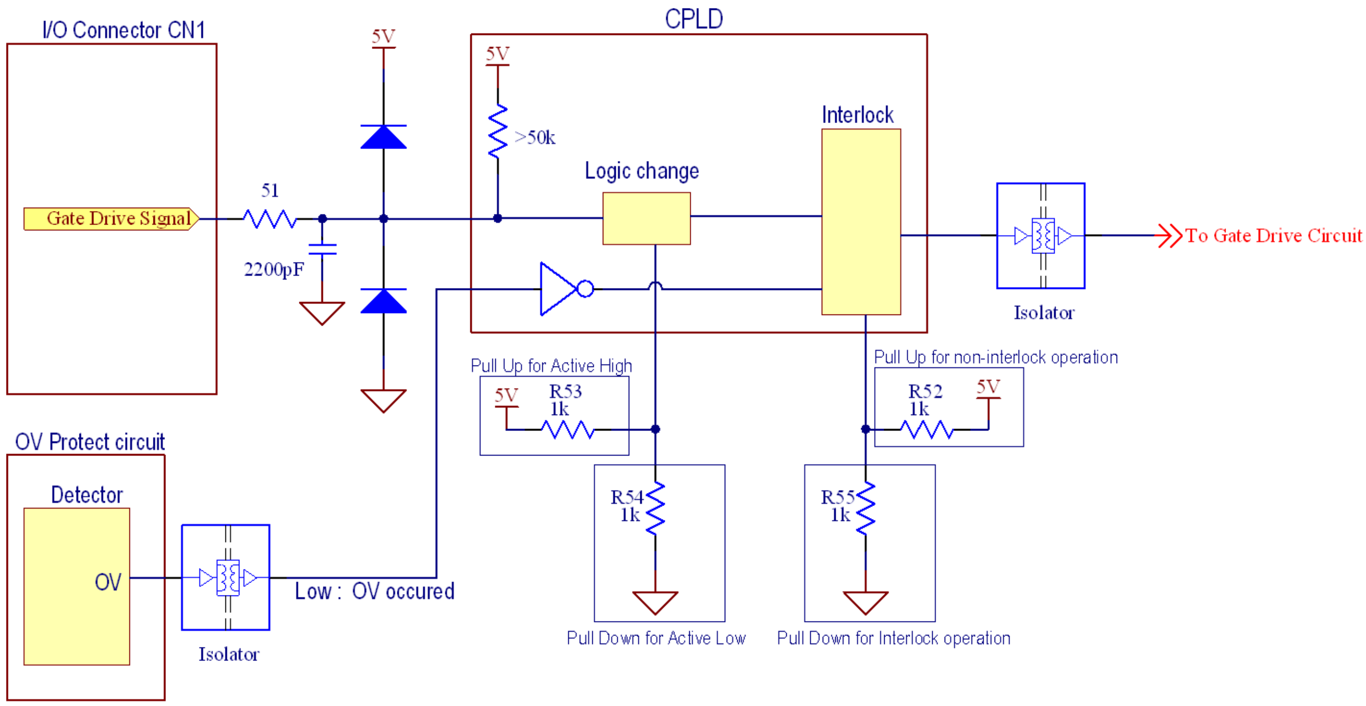


Figure 14 Diagram of signal input part for gate drive

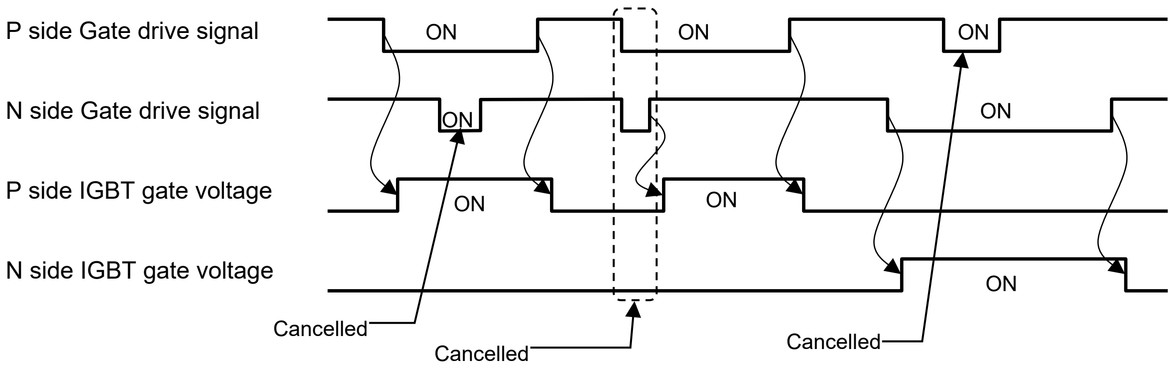


Figure 15 Gate drive signal interlock

(2) Fo output part

The outline of the fault output (Fo) circuit is shown in Figure 16. When any gate driver IC or over-voltage (OV) protection circuit senses a fault, fault output (Fo) pin of the I/O connector CN1 turns Low.

When a gate driver IC detects a short-circuit (SC) ,over-current (OC),over-temperature (OT) or power supply under-voltage (UV), its fault output (Fo) turns High and it turns off the corresponding IGBT using a soft-shutdown circuit.

When over-voltage (OV) is detected, the IGBTs are not turned off immediately. Refer section (9) for details.

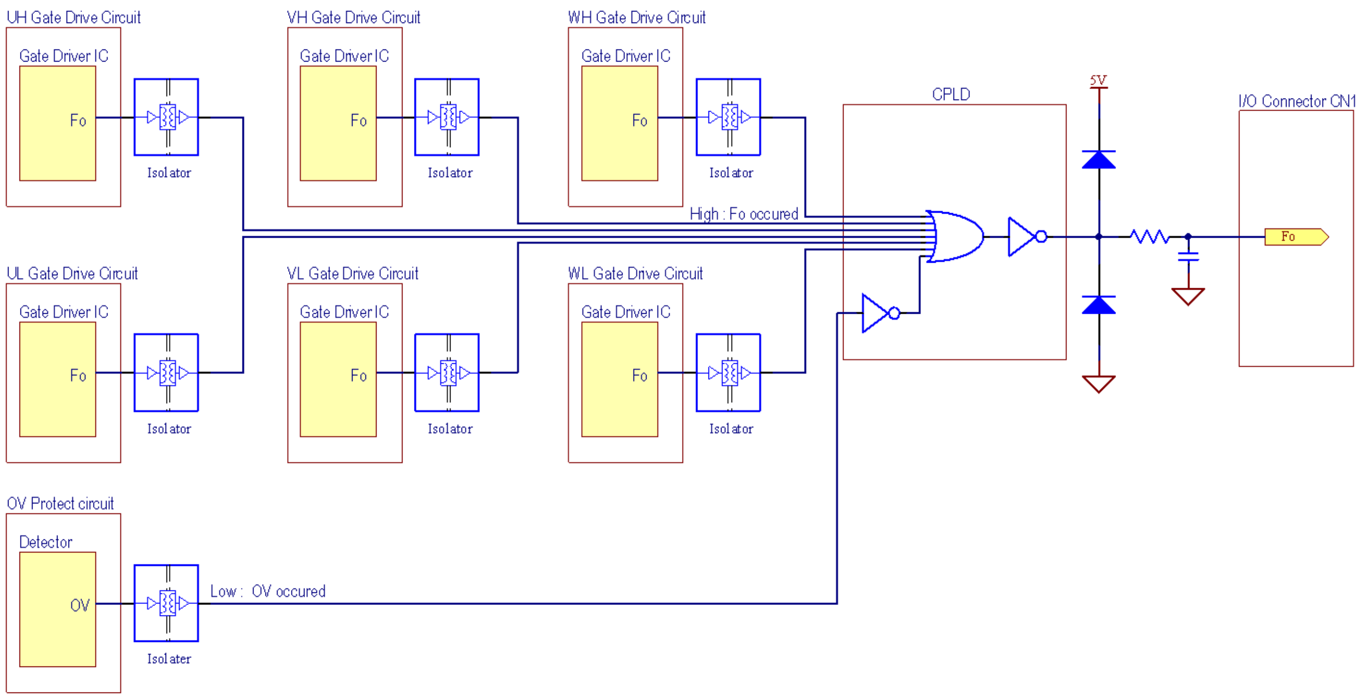


Figure 16 Outline of Fo output part

(3) Switch Mode Power Supply (SMPS)

The SMPS has six gate drive power supplies (UH,VH,WH,UL,VL and WL) and a 5V logic power supply for the I/O interface. The outline of the SMPS is shown in Figure .

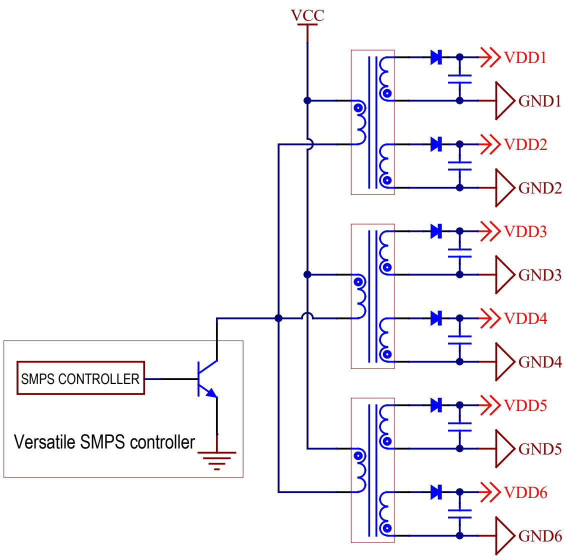


Figure 17 Outline of SMPS

(4) Gate drive and protection circuit part

The outline of the gate drive and protection circuits is shown in Figure 18. Please refer to the schematic "PEV-M2653 Schematic diagram" attached to this document for details of these circuits.

Because the gate drive current has high peak value of about 10A and it also has high frequency component, please take care to minimize fluctuations of the ground (PGND) potential on the gate drive circuit. In the driver board, the ground for the gate drive circuit and the ground for the protection circuit are separated as PGND and AGND. Both grounds are connected to each other near gate driver IC (M8160xJFP). The separation of the ground prevents malfunction of the protection circuit by suppressing fluctuations of the AGND potential.

The gate driver IC (M8160xJFP) outputs gate drive signal from Pin 21 (OUT1) in accordance with the input from Pin 27.

The J1-series IGBT module has an on-chip current sensor whose output is proportional to the collector current. The on-chip current sensor output is converted into a sense voltage by a sense resistor (R32 in Figure 18), and the sense voltage is fed to the SC and OC pin of the gate driver IC (M8160xJFP).

When detecting a short-circuit (SC), the OUT1 pin turns to a high-impedance state, and the IGBT gate is directly turned off by OUT2 on Pin 18. A soft-shutdown of the IGBT gate can be set by setting the resistance between the IGBT gate and OUT2 pin (R29 in Figure 18) larger than gate resistance for normal turn-off (R13 in Figure 18).

When detecting over-current (OC), OUT1 pin turns to a high-impedance state, and the IGBT gate is directly turned off by the OUT3 on Pin 17. A soft-shutdown of the IGBT gate can be set by setting the resistance between the IGBT gate and OUT3 pin (R31 in Figure 18) larger than gate resistance for normal turn-off (R13 in Figure 18).

The gate driver IC (M8160xJFP) has two soft shutdown circuits (OUT2, OUT3) for short-circuit (SC) and over-current (OC) respectively, so that each soft shutdown circuit can be individually optimized.

Please refer to the M8160xJFP datasheet for further information about its operation and function.

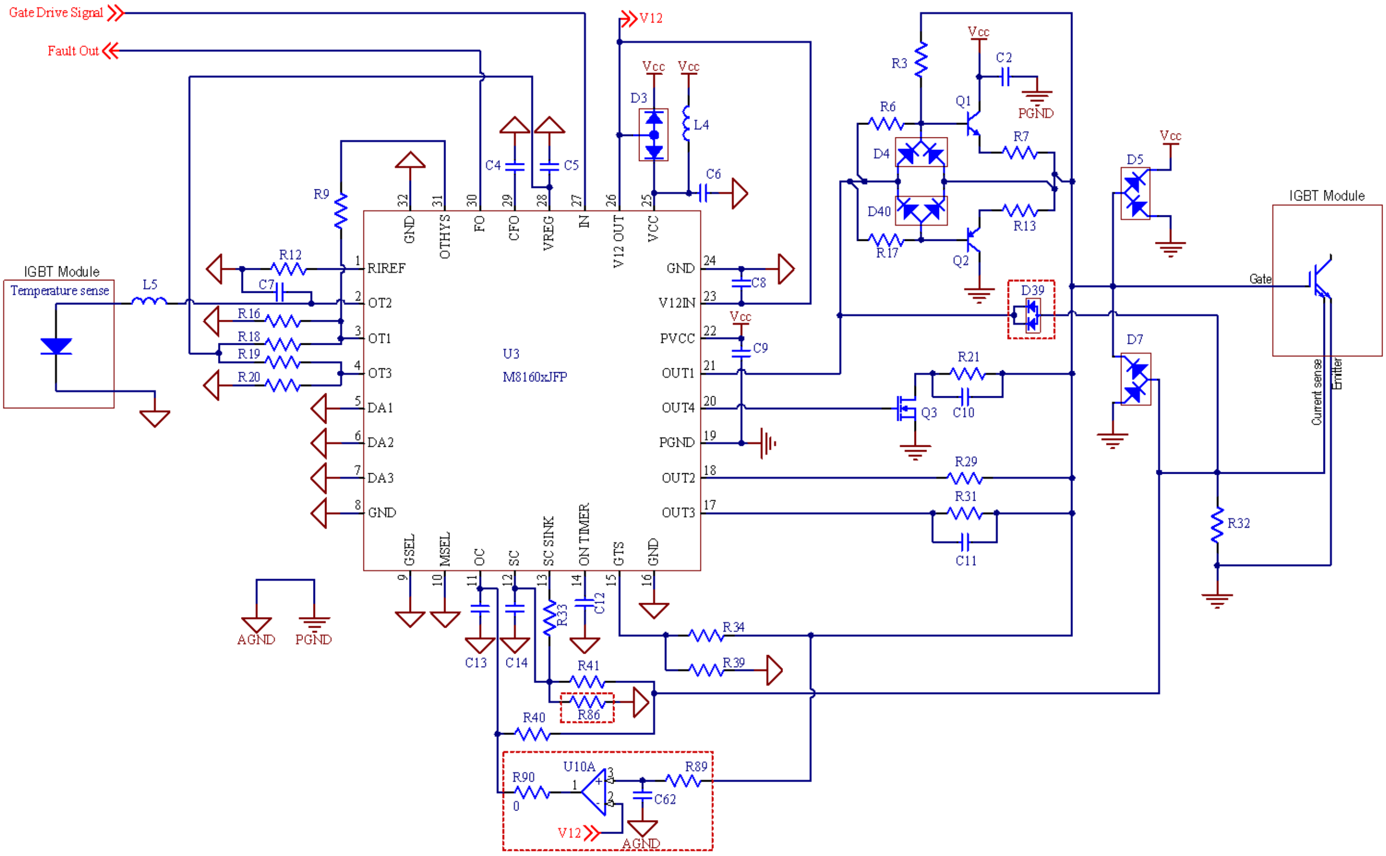


Figure 18 Outline of Drive and Protection circuit

(5) Gate Drive Buffer

The gate drive buffer for the driver board is shown in the left figure of Figure 2.

A conventional buffer is shown in the right figure of Figure 2. Transistor Q1 and Q2 are reverse biased at turn-on and turn-off of IGBTs shown in Figure 3. The base breakdown voltage of the transistors should be high so that their amplification characteristics are not degraded.

In the gate drive buffer on the driver board, diodes are connected between the base and the IGBT gate in order to reduce reverse bias to the bases of each transistor.

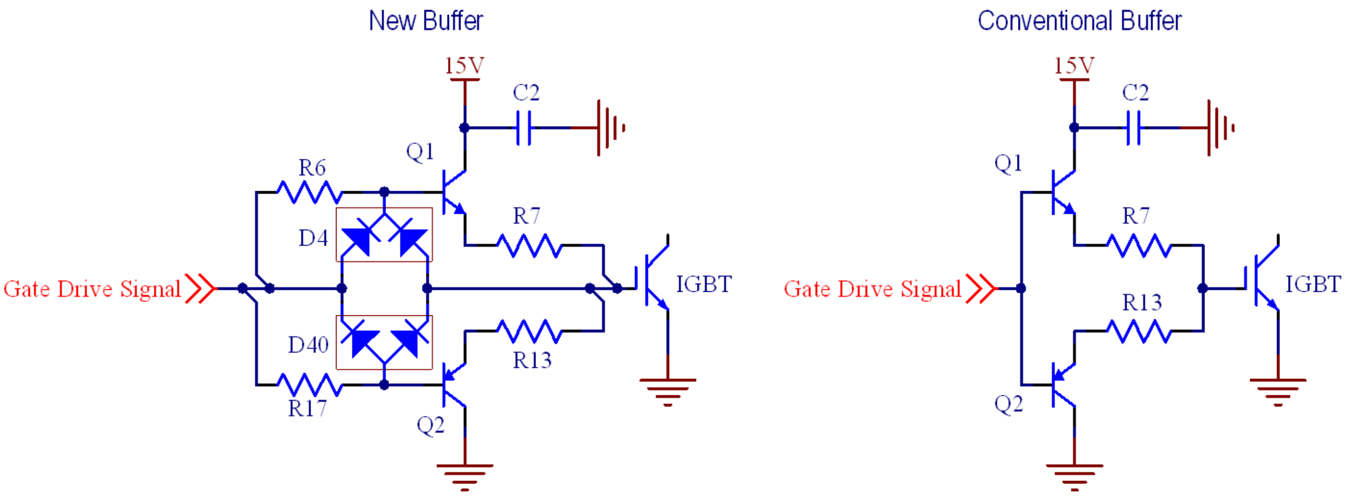


Figure 2 Gate Drive Buffer

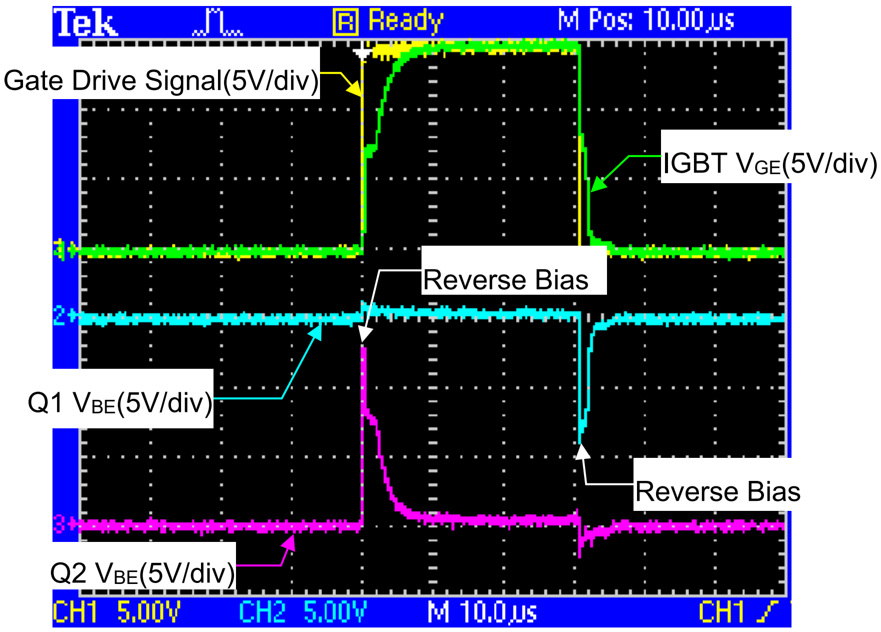


Figure 3 Measured waveforms of base voltage in conventional buffer circuit

(6) Short-circuit (SC) protection

The gate drive IC M8160xJFP has a short-circuit (SC) protection circuit which is independent of the over-current (OC) protection circuit. An on-chip current sensor output is fed into the short-circuit (SC) protection circuit. The threshold voltage of the circuit (SC trip level) is 1.0V. The sense voltage increases to 1.4V during the Miller period for example. In conventional protection circuits, a low pass filter is necessary to prevent the protection circuits from malfunction by this Vs increase. However, the low pass filter causes a delay of the short-circuit (SC) protection circuit.

The gate drive IC M8160xJFP has a function to divide the sense voltage fed into the short-circuit (SC) protection circuit during low level output duration ($t_{ONTIMER}$). By dividing the sense voltage with R41 and R33 connected to M8160xJFP Pin 13 during $t_{ONTIMER}$, a malfunction of the short-circuit (SC) protection can be prevented. Pin 13 (SCSINK) turns into a high-impedance state after $t_{ONTIMER}$, and non-divided sense voltage is fed into the short-circuit (SC) protection circuit, as seen in Figure 4. R86 in Figure 18 is an optional part used to increase short-circuit (SC) trip level after $t_{ONTIMER}$.

The voltage measured on Pin 12 (SC) is shown in Figure 22. While the sense voltage during the Miller period is about 1.4V, the sense voltage in Figure 22 is about 0.7V.

Since the driver board has a voltage divider circuit, as mentioned above, instead of a low pass filter, the delay of the short-circuit (SC) protection circuit can be minimized.

Although Pin 12 (SC) of the M8160xJFP has a low pass filter, its time constant is about 0.1μsec. Therefore there is little influence on the short-circuit (SC) protection circuit.

The protection characteristics can be optimized because the short-circuit (SC) protection circuit has a soft shutdown resistance independent of the soft shutdown resistance for the over-current (OC) protection circuit.

The arm-short waveform of the J1-series IGBT module CT600CJ1A060 using the driver board is shown in Figure 23. The short-circuit protection circuit softly shuts down the gate about 800nsec after the short-circuit. The collector current keeps rising for about 200nsec after the soft shutdown, and then decreases with -6.2kA/μsec slope.

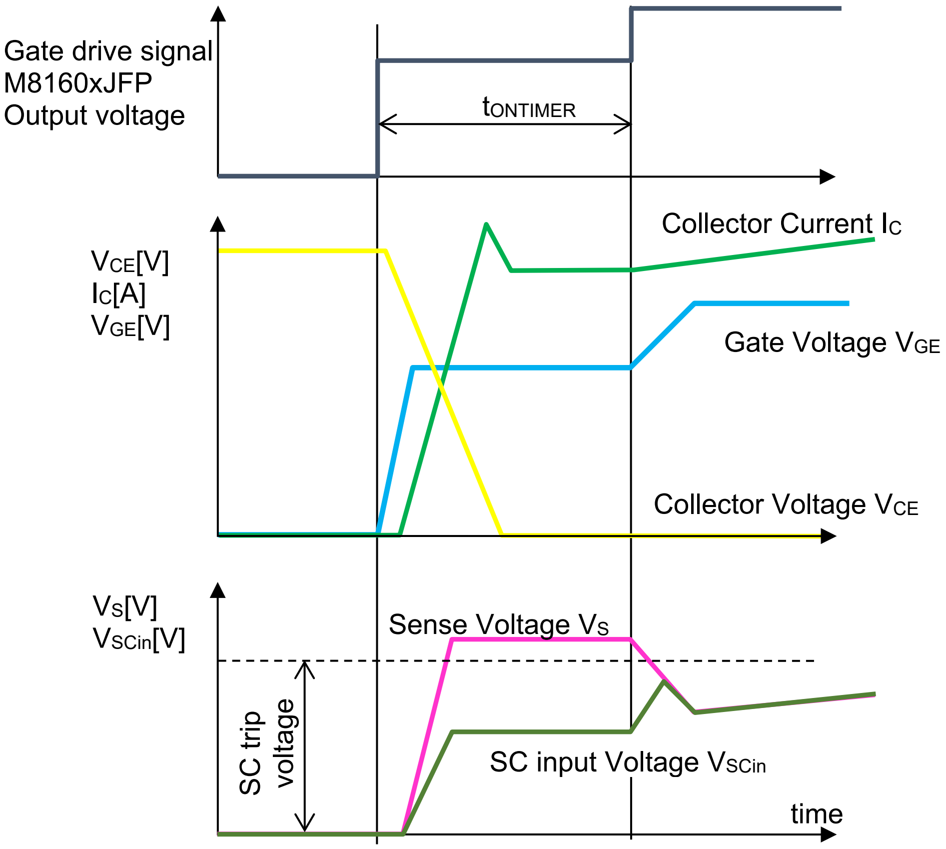


Figure 41 SC input voltage (V_{SCin})

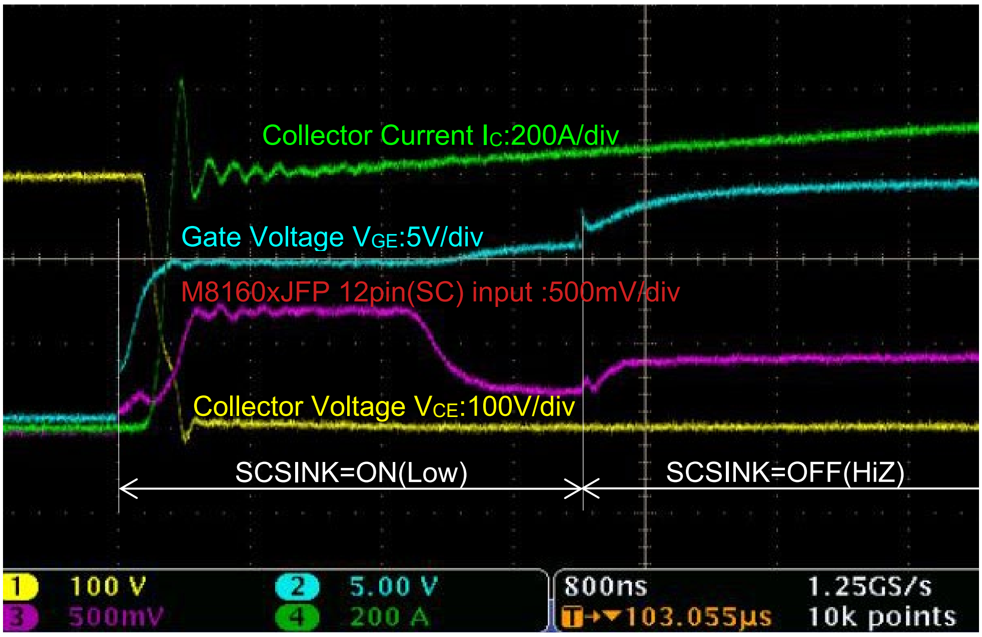
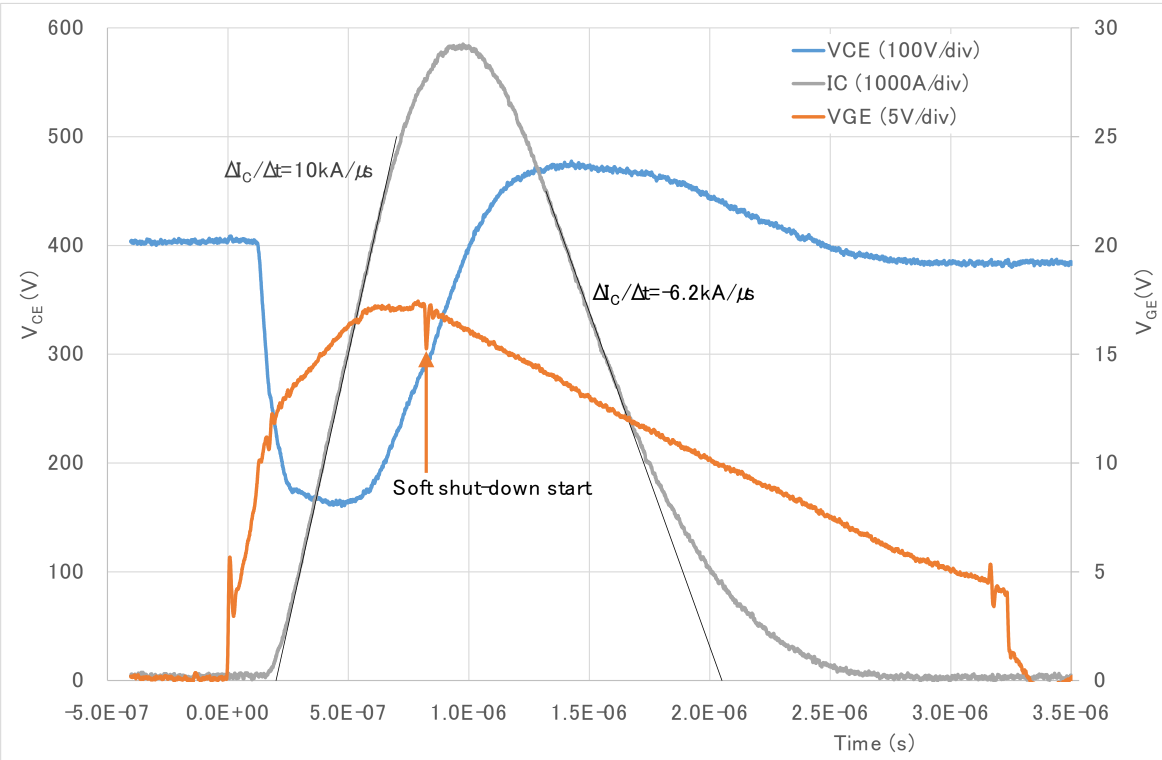


Figure 22 M8160xJFP 12pin(SC) input measurement waveform, CT600CJ1A060(ES1), Tj=25, RS=100Ω



$R_{G(on)}$=1.0Ω, DC-Link Capacitor=J1CP45060B(ESL=15nH), Ta=room temp., VPN=400V

Figure 23 Arm-short waveform, CT600CJ1A060 U phase low side

(7) Over-current (OC) protection

In general, the on-chip current sensor output has a positive temperature coefficient, and the on-chip current sensor output increases as the IGBT junction temperature increases. Therefore, the collector current level which starts the over-current protection (OC trip level) decreases at higher IGBT junction temperatures. The gate drive IC M8160xJFP has a temperature compensation function for the OC trip level so that OC trip level is maintained constant regardless of the IGBT junction temperature.

The block diagram of the M8160xJFP temperature compensation circuit for the OC trip level is shown in Figure 24. The on-chip temperature sensor output has a negative temperature coefficient, and decreases as the IGBT junction temperature increases. When GSEL is set Low, the VOT2 fed into the OT Pin 2 is inversely-amplified, and is fed to a comparator as VOC. VOC increases as the IGBT junction temperature increases, and the temperature characteristics of the on-chip temperature sensor output is compensated for.

Please set GSEL Low to enable the temperature compensation of the OC trip level. VOC is given by the following equation.

$$\mathrm{VOC} = \frac{30\mathrm{k}}{30\mathrm{k}+126\mathrm{k}} \times \left\{2.6 - \frac{112.5\mathrm{k}}{\mathrm{R}} \times (\mathrm{VOT2} - 2.6) - \frac{112.5\mathrm{k}}{112.5\mathrm{k}} \times (\mathrm{VDA} - 2.6)\right\},$$

R=99k where MSEL=Low, and R=198k where MSEL=High.

A 3bit D/A converter as shown in Figure 24 is used for offset correction of OC trip level,and the output of the converter is given by the following equasion.

$$\mathrm{VDA} = 2.86\text{-}0.13 \times [\mathrm{DA3.DA2.DA1}]$$

For example, VDA=2.86-0.13×010b=2.86-0.13×2=2.6V where DA3=L,DA2=H and DA1=L.

GSEL=Low, MSEL=Low and [DA3.DA2.DA1]=010b are set by default as shown in Figure 18. GSEL,MSEL and [DA3.DA2.DA1] are selectable by 0Ω resistor. Please refer to the circuit diagram attached to the application note for further information.

Please set GSEL high to disable temperature compensation. VDA and VOC is given by the following equation.

$$\mathrm{VDA} = 2.86 - 0.13 \times 101\mathrm{b} = 2.86 - 0.13 \times 2 = 2.6[\mathrm{V}]$$

$$\mathrm{VOC} = \frac{30\mathrm{k}}{30\mathrm{k}+126\mathrm{k}} \times \left\{2.6\text{-}\frac{112.5\mathrm{k}}{199\mathrm{k}} \times (2.6\text{-}2.6)\text{-}\frac{112.5\mathrm{k}}{112.5\mathrm{k}} \times (2.6\text{-}2.6)\right\} = \frac{30\mathrm{k}}{30\mathrm{k}+126\mathrm{k}} \times 2.6 = 0.5[\mathrm{V}]$$

,where GSEL=High, MSEL=High, and [DA3,DA2,DA1]=010b. Then Over-current protection threshold voltage is then 0.5V and the IC can be used like the conventional gate drive IC M81741JFP.

The protection characteristics can be optimized because the over-current (OC) protection circuit has a soft shutdown resistance independent of the resistance of the short-circuit (SC) protection circuit.

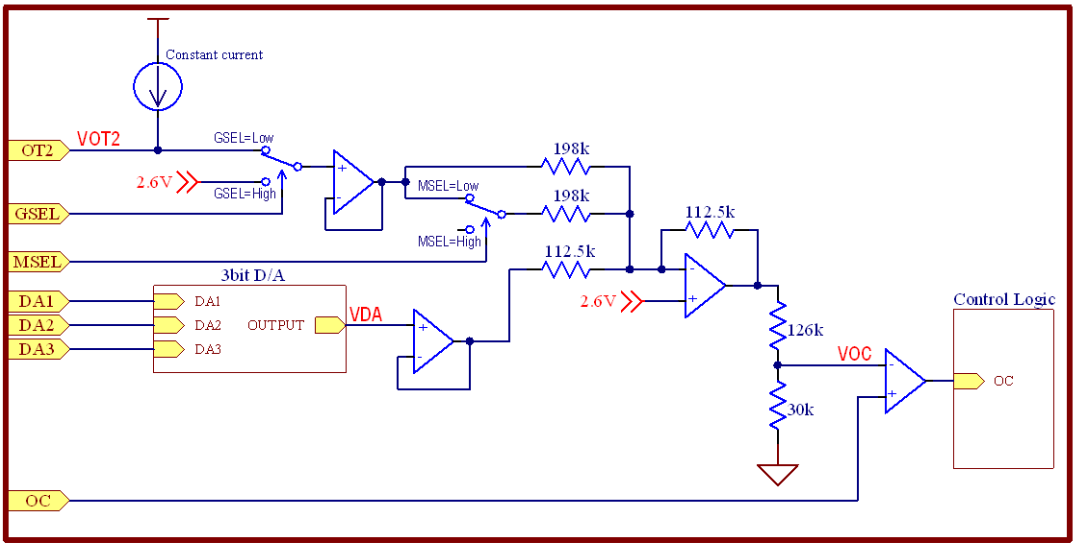


Figure 24 Block diagram of M8160xJFP temperature compensation circuit for OC trip level

(8) Over temperature (OT) protection

The driver board has a bias current source for the on-chip temperature sensor. Each phase of the driver board has over-temperature protection which utilizes the on-chip temperature sensor.

The over-temperature (OT) protection circuit diagram and its operation are shown in Figure , Figure 5 respectively. The bias current for the on-chip temperature sensor is determined by a resistance connected to Pin 1 of the gate driver IC M8160xJFP (R12 in25). Current output I_F from OT2 is represented by $I_F = \frac{2.35}{R12} \times 4$. In the driver board, R12=47kΩ and $I_F = \frac{2.35}{47k} \times 4 = 200\mu A$.

The over-temperature (OT) protection circuit is operated as a hysteretic comparator, the OT trip level and OT reset level differ from each other. When the On-chip temperature sensor output fed to Pin 2(OT2) falls below the OT trip level, over-temperature (OT) protection circuit turns off the IGBT. Over-temperature (OT) protection is cancelled when the on-chip temperature sensor output exceeds the OT reset level.

The on-chip temperature sensor outputs for phase U,V and W low side IGBTs are sent out as a serial output in an asynchronous NRZ (Non Return to Zero) signal from the connector CN1. The on-chip temperature sensor output is also used for switching the turn-off gate resistances and compensating temperature characteristics of the OC trip level.

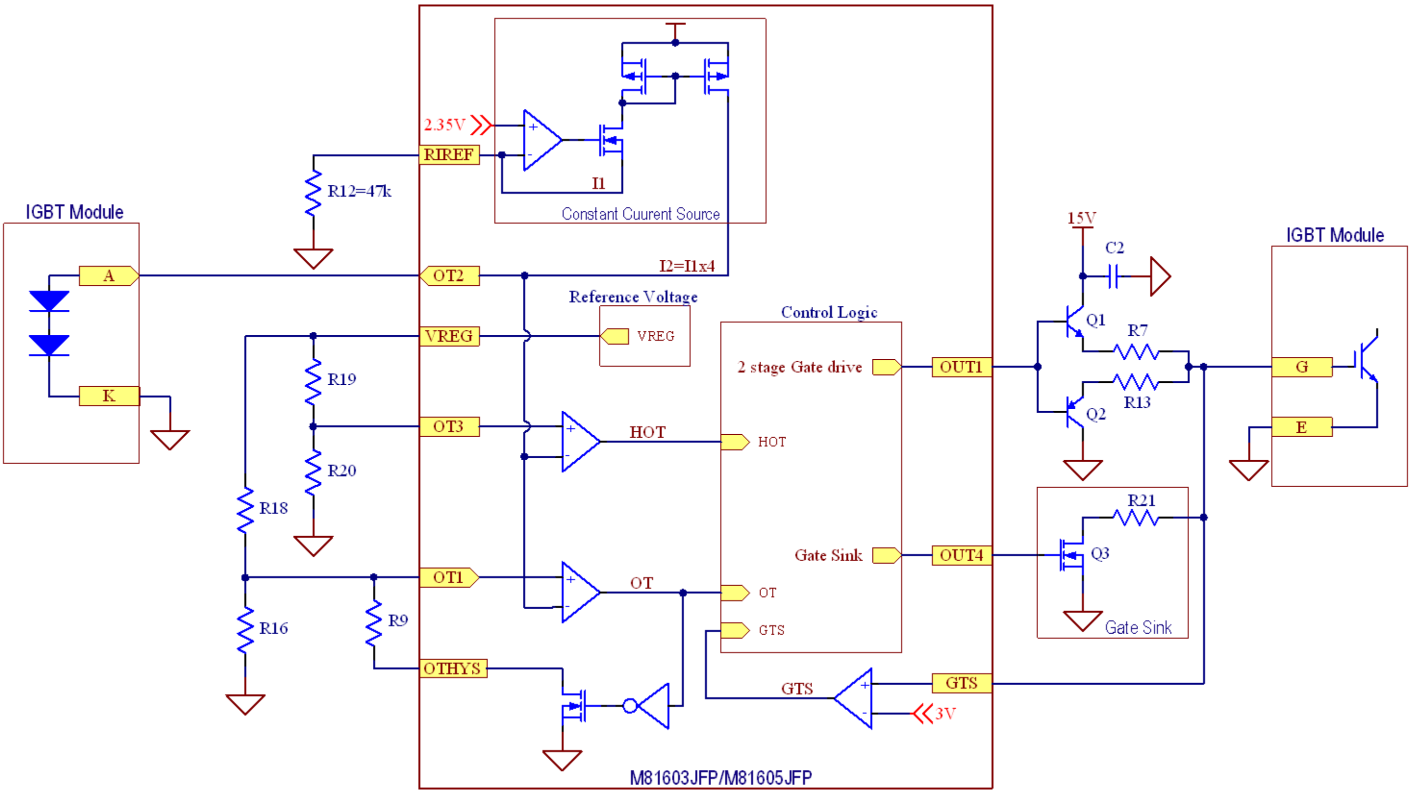


Figure 25 Over-temperature circuit diagram

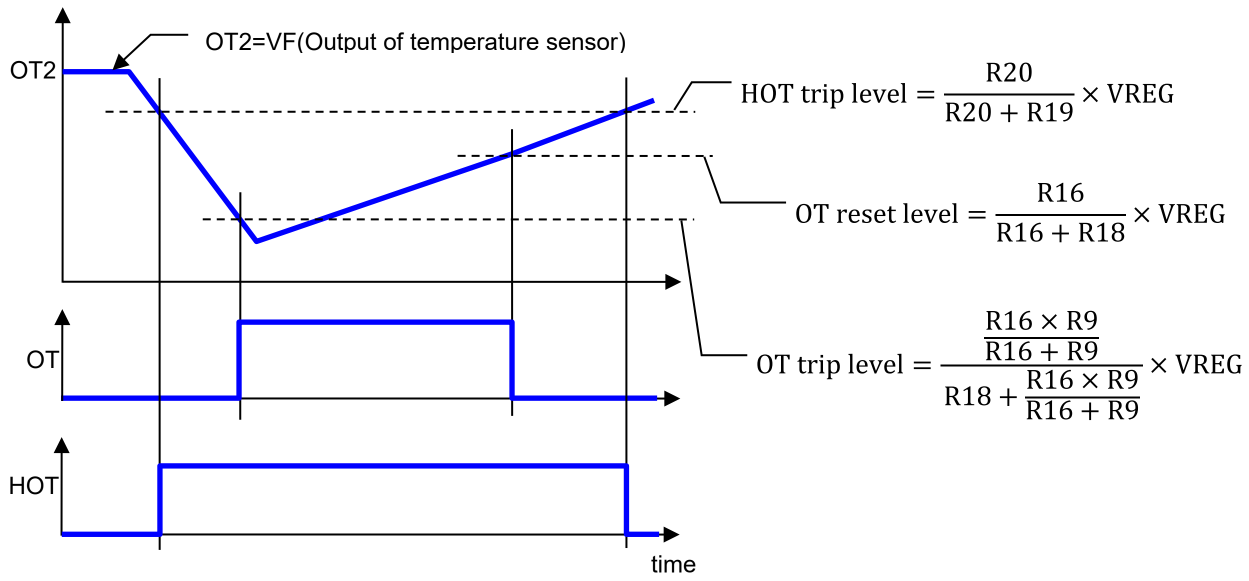


Figure 5 Over-temperature hysteresis operation

(9) Over-voltage (OV) protection

The over-voltage (OV) protection circuit detects the P-N voltage between the PV pin and the emitter control pin (UNE) of the U phase. When the P-N voltage exceeds the OV trip level, the IGBT that has been already on state keeps on state. And it turns off according to state of other protection circuit when the gate-drive signal turns off. If the IGBT is off state when OV occurs, it keeps off state during OV fault although the gate-drive signal turns on.

The GND of the over-voltage (OV) protection circuit is connected to the GND of the gate drive and protection circuit. The P-N voltage is monitored by the 1chip micro controller. The OV trip level is determined by the rating voltage of the J1-series power module.

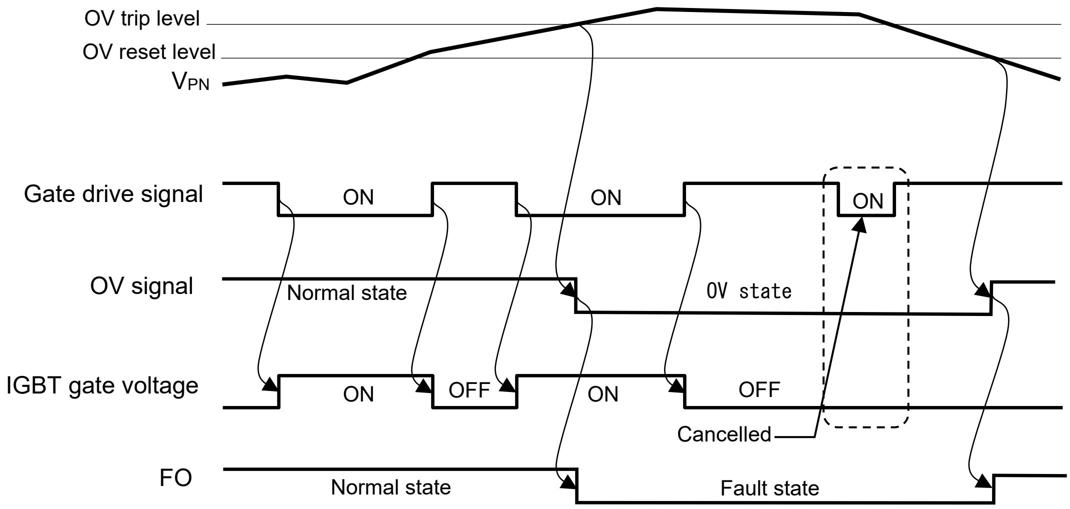


Figure 276 OV protection timing chart

Table 4 Over-voltage (OV) protection level

Item	Specifications	
#610, #620, #611, #621	Trip level	500 (V)
	Reset level	450 (V)

(10) Test Points

Test points are provided to monitor IGBT gate voltage, current sense, temperature sense and ASIC main terminal signals, such that each signal can be measured easily.

Table 5 Test point

No.	Signal name	Phase	Test point	Note
1	OUT1	U-phase H-side	TP1_UH	
		V-phase H-side	TP1_VH	
		W-phase H-side	TP1_WH	
		U-phase L-side	TP1_UL	
		V-phase L-side	TP1_VL	
		W-phase L-side	TP1_WL	
2	OUT2	U-phase H-side	TP2_UH	
		V-phase H-side	TP2_VH	
		W-phase H-side	TP2_WH	
		U-phase L-side	TP2_UL	
		V-phase L-side	TP2_VL	
		W-phase L-side	TP2_WL	
3	OUT3	U-phase H-side	TP3_UH	
		V-phase H-side	TP3_VH	
		W-phase H-side	TP3_WH	
		U-phase L-side	TP3_UL	
		V-phase L-side	TP3_VL	
		W-phase L-side	TP3_WL	
4	OUT4	U-phase H-side	TP4_UH	
		V-phase H-side	TP4_VH	
		W-phase H-side	TP4_WH	
		U-phase L-side	TP4_UL	
		V-phase L-side	TP4_VL	
		W-phase L-side	TP4_WL	
5	IGBT gate voltage(V_{GE})	U-phase H-side	TP5_UH	
		V-phase H-side	TP5_VH	
		W-phase H-side	TP5_WH	
		U-phase L-side	TP5_UL	
		V-phase L-side	TP5_VL	
		W-phase L-side	TP5_WL	
6	PGND	U-phase H-side	TP6_UH	
		V-phase H-side	TP6_VH	
		W-phase H-side	TP6_WH	
		U-phase L-side	TP6_UL	
		V-phase L-side	TP6_VL	
7	SC Input voltage	U-phase H-side	TP7_UH	
		V-phase H-side	TP7_VH	
		W-phase H-side	TP7_WH	
		U-phase L-side	TP7_UL	
		V-phase L-side	TP7_VL	
		W-phase L-side	TP7_UH	
8	FO	Low voltage side	TP6	Use TP7 as a GND of probe.
9	GND	Low voltage side	TP7	
10	VPN	P-N Voltage	TP8	Use TP6_UL as a GND of probe.

(11) Temperature sensor and P-N voltage digital output

The On-chip temperature sensor output and the P-N voltage are A/D converted by a 1chip micro controller and it is fed to CN1 as a serial output (asynchronous, Non-Return-to-Zero method). The timing, specifications and data format of the serial output are shown in Figure 28, Table 6, and Table 7 and respectively.

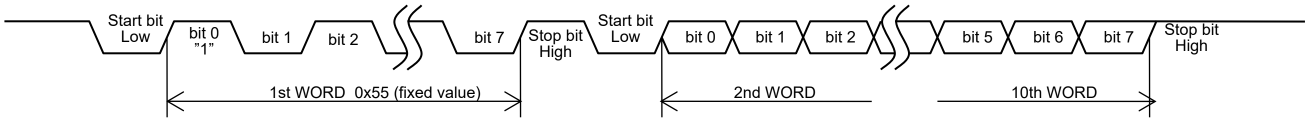


Figure 28 Timing chart of serial output

Table 6 Specifications of serial output

Item	Specifications
baud rate	115200 baud
character length	8bit
Parity	none
Start bit	”0” Low
Stop bit	”1” High, length1bit
Flow control	none

Table 7 Data format of serial output

No.	Data	Note
1st	0x55	Fixed data
2nd	0x55	Fixed data
3rd	P-N voltage upper 8bit	1LSB=1.096V FSR=1121.2V
4th	P-N voltage lower 8bit	
5th	U phase at low side temperature sensor output upper 8bit	1LSB=1mV FSR=4.095V
6th	U phase at low side temperature sensor output lower 8bit	
7th	V phase at low side temperature sensor output upper 8bit	
8th	V phase at low side temperature sensor output lower 8bit	
9th	W phase at low side temperature sensor output upper 8bit	
10th	W phase at low side temperature sensor output lower 8bit	

(12) Temperature sensor and P-N voltage analog output

The on-chip temperature sensor output and the P-N voltage are A/D converted by a 1chip micro controller mounted at the high voltage side. These signals are fed to connector CN1 as a digital serial signal.

Another 1chip micro controller mounted at the low voltage side receives this digital serial signal and converts to an analog signal, then outputs it as an analog signal from connector CN1.

Table 8 Temperature sensor and P-N voltage analog output

Signal name	CN1 Pin No.	Electrical characteristics	Note
VPN	12	Typical resolution = 1/32 Typical output voltage step=4.096/32=0.128 (V) Typical output voltage range=0～3.968(=0.128×31) (V) Output voltage ratio=(P-N voltage)/VPN=1121.2/3.968 (V/V)	P-N voltage
VUL	11	Typical resolution =1/1024 Typical output voltage step=4.096/1024=4 (mV) Typical output voltage range=0～4.092(=0.004×1023) (V) Output voltage ratio=(Sensor output)/VUL=1.0 (V/V)	U phase at low side temperature sensor output
VVL	10	Typical resolution =1/1024 Typical output voltage step=4.096/1024=4 (mV) Typical output voltage range=0～4.092(=0.004×1023) (V) Output voltage ratio=(Sensor output)/VUL=1.0 (V/V)	V phase at low side temperature sensor output
VWL	9	Typical resolution =1/1024 Typical output voltage step=4.096/1024=4 (mV) Typical output voltage range=0～4.092(=0.004×1023) (V) Output voltage ratio=(Sensor output)/VUL=1.0 (V/V)	W phase at low side temperature sensor output
GND	8		

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