

High-Speed Motion Controller “Q17nD Series”

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1. Introduction

Today's global market requires not only better CPUs to boost the functionality, performance and cost efficiency of components, but also higher throughput of entire systems. We have therefore developed a high-performance motion controller with multiple CPU high-speed transmission (Fig. 1).

2. Features of Motion Controller “Q17nDCPU”

We have developed a multiple CPU high-speed bus for data transmission between the motion controller and programmable controller to realize maximum data transmission of 14 kW at intervals of 0.88 ms. With a new architecture for the motion controller hardware, the improved performance allows up to 6 axes to be controlled at an operation cycle of 0.44 ms.

CPUs at a fixed cycle (0.88 ms; “multiple CPU high-speed transmission cycle” hereafter).

In the data transmission of a conventional Q Series motion controller, the device data on the motion controller side is set in the shared CPU memory at the main cycle intervals of the motion controller, then fed to the programmable controller by the END processing in the sequence program. On the other hand, with the newly developed multiple CPU high-speed bus, the data is transmitted to the programmable controller at the multiple CPU high-speed transmission cycle and read out by the sequence program, by setting the device data on the motion controller side to the shared multiple CPU memory (Fig. 2).

As a result, the device data is updated at high speed without the influence of the motion main cycle or the scan time of the sequence program.

3. Multiple CPU High-Speed Transmission

3.1 Outline of multiple CPU high-speed transmission

Multiple CPU high-speed transmission refers to a data transmission function executed between multiple

Existing system (Auto refresh)

(1) Device ON

Device reflection time

Device reflection time

(8) Device ON

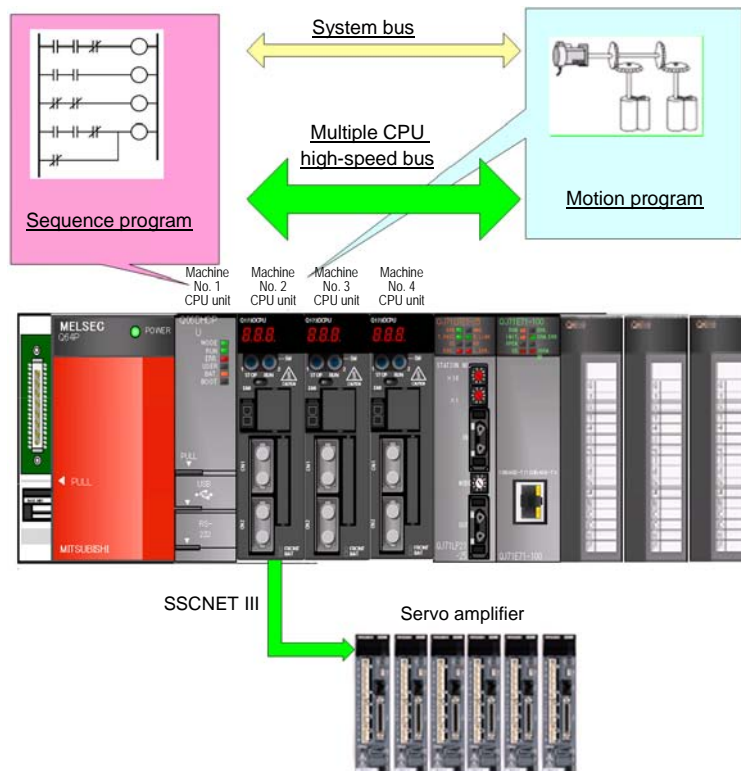


Fig. 1 Overall system configuration

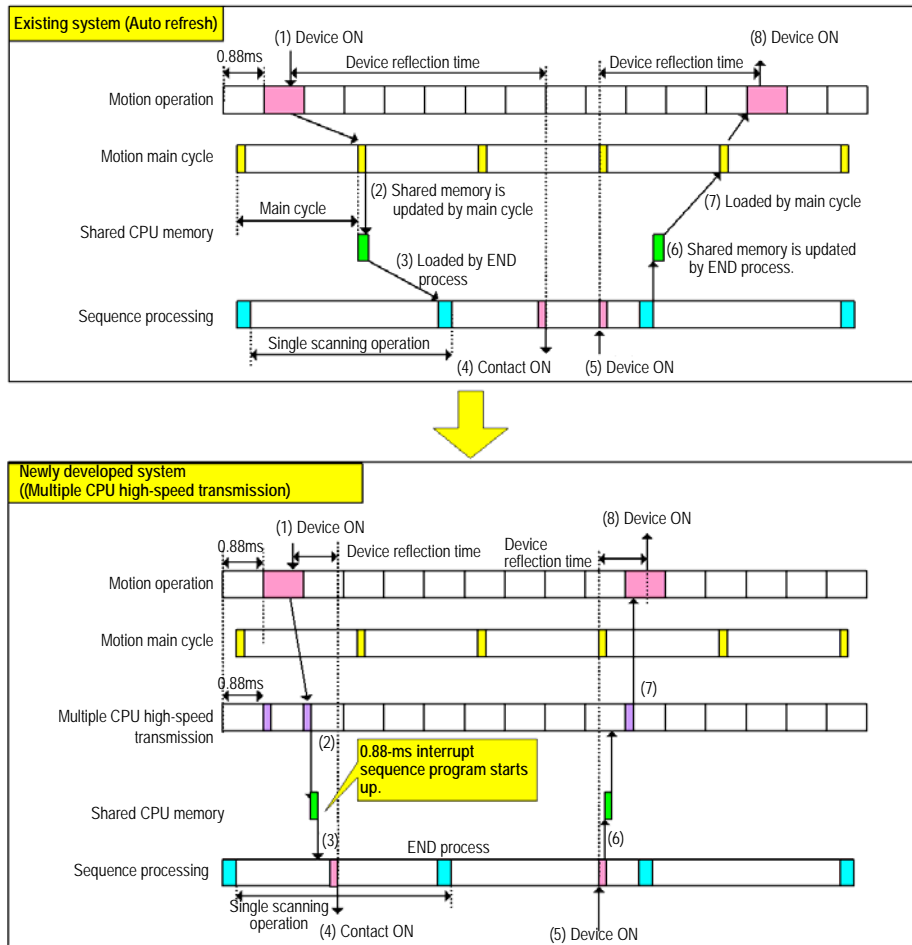


Fig. 2 Data transmission (Schematic diagram)

3.2 Technologies employed in multiple CPU high-speed transmission and their features

(1) The conventional Q Series motion controller uses only the system bus for data transmission between all units. Consequently, as the number of units increases while large volumes of data are periodically transmitted between CPUs, the required data transmission time inconveniently increases. Therefore, we have provided a multiple CPU high-speed bus exclusively for transmission between the CPUs, which enables high-speed data transmission regardless of the number of CPU units or the volume of data. With this multiple CPU high-speed bus, large volumes of data, a maximum of 14 kW, are refreshed at high speed for each multiple CPU high-speed transmission cycle to allow high-speed data sharing between the CPUs, increasing the data volume to almost 3.5 times the conventional transmission. Since the multiple CPU high-speed transmission is synchronized with the operation cycle of the monitor controller, data transmission involves no inefficient latency. In addition, data transmission on the programmable controller is also synchronized;

synchronized data transmission is secured between the programmable controller and the motion controller. Furthermore, since the communication with the servo amplifier is synchronized with the operation cycle of the motion controller, synchronized data transmission is achieved throughout between the programmable controller, motion controller, and servo amplifier. Thus, the data transmission has no latency and can process the data at high speed, resulting in a remarkable reduction in tact time.

- (2) Refresh device range settings are now increased from 4 types to 32 types for more flexible setting of the command and monitoring devices between the CPUs. As a result, the user can assign devices as desired, increasing the degree of freedom in programming.
- (3) A free area is newly provided in the shared CPU memory (Fig. 3). In this area, the user can specify the same devices in the sequence program, motion sequential function chart (SFC) program and servo program and easily understand the interrelationship between the programs, thus improving the program readability of the system.
- (4) Sequence instructions for the motion controller

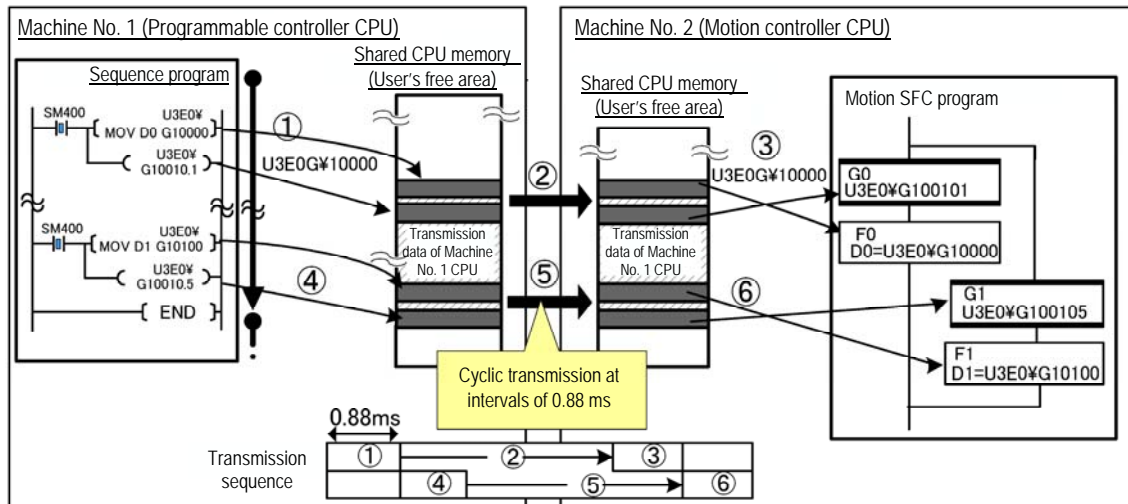


Fig. 3 Shared CPU memory

only are modified so that “complete device” or “device for storing complete status” can be omitted. This improvement simplifies sequence program execution while motion controller instructions are being used.

On the other hand, the conventional Q Series motion controller can perform sequence instructions for the motion controller only once during a single scanning operation. With this new series, multiple sequence instructions for the motion controller can be executed at the same time (a maximum of 32 times per single scanning operation).

- (5) Interrupt sequence programs synchronized to the operation cycle of the motion controller can be described; sequence processing synchronized with the motion control is now available. As a result, the high-speed servo control function uses information received from the units under the control of the programmable controller (high-speed counter module and analog-digital converter module) and the information can also be used in various applications mainly related to the sequence.

4. High-Speed and High-Performance Operation with Motion Control

The hardware architecture of the Motion Controller Q17nDCPU has been significantly improved compared to the conventional ones; performance is almost double and an operation cycle of 0.44 ms/6 axes has been realized (Table 1).

Table 1 List of operation cycles

Q173DCPU	Q172DCPU
0.44 ms / 1–6 axes	0.44 ms / 1–6 axes
0.88 ms / 7–18 axes	0.88 ms / 7–8 axes
1.77 ms / 19–32 axes	

The processing speed of motion SFC instructions has also been increased to almost three times that of the conventional series on a 32-bit addition basis.

This development enhances the overall performance of Mitsubishi FA products. As a total FA equipment supplier, we will continue developing products by focusing on the importance of total optimization.