The enhancement of properties toward low loss, low radiation noise, wide safe operating area (SOA), and high reliability is demanded of Si power devices considering the increasing range of application. The present Si power devices, on which much research has been conducted, are approaching their limit in terms of physical properties. However, we believe that there is still room to enhance the value of Si power devices through sophisticated design that allows such measures as optimization for specific uses and improvement in usability. With the aim of reducing steady-state loss and switching loss in insulated-gate bipolar transistors (IGBTs) and diodes, Mitsubishi Electric has made efforts to evolve IGBTs to planar type, trench type, and carrier-stored trench-gate bipolar transistor (CSTBT) type IGBTs. For diodes, we have evolved diffusion wafer diodes to thin wafer diodes. This article describes our successful initiative to improve the existing technologies, and to develop 7th generation IGBTs and diodes as IGBT modules for industrial use.

1. 7th Generation IGBTs

1.1 Enhancement of IGBT performance

From the 5th generation IGBTs, we started using trench-gate IGBTs in our own CSTBT structure in which a carrier-stored layer (CS layer) is formed. The CS layer allowed a significant reduction in the junction field-effect transistor (JFET) resistance, which constitutes the highest resistance in a cell. For the 6th generation, we narrowed the trench-gate pitch, thereby enhancing the carrier storing effect. The 7th generation successfully attained high performance and high drive controllability through ultra-thin wafer processing and improvement in the MOS and backside structure.

The performance of an IGBT is discussed in terms of the figure of merit (FOM)\(^2\). This is a numerical value expressed by Equation (1) using the values of the collector current density \(J_c\) (A/cm\(^2\)), the saturation voltage between the collector and emitter \(V_{CE_{sat}}\) (V), and the turn-off switching loss \(E_{off}\) (mJ/A).

\[
FOM = \frac{J_c}{V_{CE_{sat}} \times E_{off}} \quad \text{......................... (1)}
\]

While the FOM of a 5th generation IGBT is 1 in a 1,200 V IGBT for industrial use, the FOM of the 6th and 7th generation IGBT is 1.25 and 1.32, respectively. We have thus succeeded in upgrading the performance for each new generation. In addition, we have taken various measures for improving the MOS and backside structures and shrinking the termination structure in response to the demand for low cost, operability under high temperature, high SOA capability, and other properties.

1.2 Features of the 7th generation IGBT structure for industrial use

Figure 1 shows a schematic cross-sectional view of a 7th generation IGBT for industrial use together with its features. The 7th generation IGBT has a light punch-through (LPT) structure formed by using ultra-thin wafer processing technology, thereby reducing the loss. While the thin wafer process is effective for improving electrical properties, there have been issues such as a reduction in SOA capability due to decreased heat capacity of the chip and variations in electrical properties caused by mechanical stress. The 7th generation 1,200 V IGBTs for industrial use have secured the current capability and SOA capability through optimization of the area ratio between the \(n^+\) emitter layer and \(p^+\) layer in the MOSFET. Secondly, a

Fig. 1 Cross-sectional view of the structure of a 7th generation IGBT for industrial use and its features

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stress relief processing technology for the thin wafer that does not impose mechanical stress on the chips has been developed through optimization of the processing conditions in the grinding and thermal process, etc. Furthermore, as a result of optimizing the gate capacitance (between the gate emitter and collector) by adjusting the ratio between the active and non-active states of the trench gate in 7th generation IGBTs, the current dependence of the reverse recovery \( \frac{dv}{dt} \) (hereafter referred to as “dv/dt”) when turning on has been improved, thus realizing high dv/dt controllability.

### 1.3 Electrical properties of a 7th generation IGBT for industrial use

Figure 2 shows the waveform of the short-circuit safe operating area (SCSOA) of a 7th generation IGBT for the use of industrial IGBT modules. Thinning of a wafer reduces the thermal capacitance, which causes a decline in the SCSOA. However, the saturated current \( I_{sat} \) (voltage between the gate and emitter \( V_{GE} = 14 \text{ V} \), temperature at the connection \( T_j = 150^\circ\text{C} \); rated current \( \times 2 \)) and the latch-up endurance \( T_j = 175^\circ\text{C} \); rated current \( \times 2 \)) have been retained through optimization of the area ratio between the \( n^+ \) emitter layer and \( p^+ \) layer. As a result, the 7th generation IGBT remained unbroken during measurement up to the pulse width of 10.5 \( \mu\text{s} \), under measuring conditions of \( V_{CE} = 800 \text{ V} \), \( V_{GE} = 15 \text{ V} \sim 15 \text{ V} \), and \( T_j = 150^\circ\text{C} \), thus achieving the current capacity and high SOA capability that satisfy the product requirements.

Moreover, wafer thinning may cause mechanical stress that is imposed on a chip and causes the properties to fluctuate, which makes the stress relief during wafer processing very important. It was the key to focus particularly on the processing conditions for the grinding, electrode formation, and thermal processing as the optimization to realize an ultra-thin wafer process not only for small-capacity chips but also for large-capacity chips.

Figure 3 shows surface photographs of a small-capacity chip with a rated voltage of 600 V and rated current of 20 A, and a large-capacity chip with a rated voltage of 650 V and rated current of 200 A using ultra-thin wafers, and the in-plane variation of the threshold voltage \( V_{GE(th)} \) between the gate and emitter.\(^{(3)}\)

The area of the chip in Fig. 3(b) is approximately 20 times that in Fig. 3(a). The threshold voltage \( V_{GE(th)} \) of MOSFET portion is characterized by the carrier mobility, which is sensitively affected by the mechanical stress. For this reason, the in-plane variation of \( V_{GE(th)} \) is useful as an index for confirming the mechanical stress caused by warpage of the chip. Figure 3(c) and (d) shows the difference in variation of wafer in-plane \( V_{GE(th)} \). In-plane variation \( V_{GE(th)} \) in each case does not exceed \( \pm 0.2 \text{ V} \), showing no significant difference between (c) and (d). This suggests that the wafer was thinned without the excessive stress to cause the fluctuation of the characteristic.
junction; the emitter and collector. So the rate control easiness of this voltage raising and descending of dv/dt are preferable from the users’ point of view. When this dv/dt exceeds the reference value (e.g., 20 kV/μs), radiation noise is generated, leading to malfunction in a motor, etc. For this reason, the gate resistance Rg \((on)\) is adjusted to a value large enough to reduce the dv/dt so as not to exceed the reference value in the current range used. On the other hand, when the dv/dt is too small compared to the reference value, the switching will be slow. This causes the switching energy \(E_{on}\) to increase when turning on. Accordingly, the current dependence of dv/dt is preferable to be as small as possible along the entire current range of usage.

Figure 4 shows the diode’s reverse recovery dv/dt during IGBT’s turn-on dependency of the 6th generation and 7th generation IGBTs on the collector current \(I_c\). Both IGBTs use a chip with a rated voltage of 1,200 V and rated current of 110 A, under switching conditions of \(V_{CE} = 600 \text{ V}, V_{GE} = 15 \text{ V/–15 V}, T_j = 25^\circ \text{C}\), gate resistance \(R_g (on) = 10 \Omega\), and the collector current in a range of 5 to 110 A is allocated. The dv/dt value of the 6th generation IGBT when \(I_c = 5\text{ A}\) is increased by about 2.2 times when \(I_c = 110\text{ A}\). On the other hand, the dv/dt of the 7th generation IGBT when \(I_c = 5\text{ A}\) is increased by about 1.6 times when \(I_c = 110\text{ A}\), showing the ability to maintain an almost constant switching speed in the allocated current range. As described above, optimization of the gate capacitance has improved controllability for the dv/dt of the 7th generation IGBT.

2. 7th Generation Diode

2.1 Enhancement of diode performance

An effective means for enhancing the performance of a diode is reduction of the forward drop voltage \(V_F\) by making the wafer thinner. However, reducing chip thickness increases the risk of destruction due to high voltage peak (snap-off) during the reverse recovery, i.e., the SOA degradation. To solve this problem, we have developed RFC diodes adopting a new backside structure technology. In the RFC diode structure, a p layer is partially formed on the cathode side and holes are injected from the p layer avoiding a carrier-empty state during reverse recovery action. As a result, the electric field on the cathode side is relaxed and the snap-off voltage is suppressed.

To date, we have applied the RFC diode structure, in addition to the thinned wafer, to our 7th generation diodes of 1,200 V class or above.\(^{(4)(5)}\) The following sections present the results of trial manufacture and evaluation of a 650 V 7th generation diode for industrial use.

2.2 Features of the 7th generation (RFC) diode structure

Figure 5 shows the cross-sectional structure of a conventional diffusion wafer diode and a 7th generation diode. The thickness of the 650 V 7th generation diode has been reduced to about one-third of the thickness of the conventional diffusion wafer diode by means of ultra-thin wafer processing technology. Furthermore, an \(n^+\) cathode layer/p layer structure has been formed on the backside through a backside patterning process.

2.3 Electrical properties of 7th generation diodes

Figure 6 shows the reverse recovery waveform of a 7th generation diode chip. It is reported that the oscillation phenomenon becomes significant under conditions of high power-supply voltage (\(V_{cc}\)), high wiring inductance (\(L_s\)), low operation temperature, and other factors of hard recovery. To optimize the RFC diode parameters, we conducted the evaluation using the chip with a rated voltage of 650 V and rated current of 100 A under conditions in which the oscillation
phenomenon was likely to occur. As described above, hole injection from the p layer on the backside produces a moderate reverse recovery waveform (soft recovery) for an RFC diode. This means that adjusting the concentration and layout of the p layer in accordance with the wafer thickness and usage conditions allows control of the hole injection.

The snap-off of voltage and subsequent oscillation were observed with the chip prior to the optimization of conditions. However, optimization of the parameters made it possible to suppress the snap-off so as not to exceed 650 V, thus achieving SOA capability equivalent to that of the conventional diode.

Thanks to the RFC structure, the 7th generation diode has better tradeoff relationship between $V_F$ and $E_{rec}$ than the conventional diffusion wafer diode, as shown in Figure 7. Accordingly, with the 7th generation diodes, we reduced $E_{rec}$ by 30% with the same $V_F$ comparing to the conventional diffusion wafer diode. In addition, the FOM of the 7th generation diode, which can be expressed by Equation (2), was increased by 50%.

$$FOM = \frac{J_A}{V_F \times E_{rec}}$$  \hspace{1cm} (2)

$J_A$: Anode current density ($A/cm^2$)
$V_F$: Forward direction voltage drop at 125°C (V)
$E_{rec}$: Reverse recovery loss at 125°C (J/A per pulse)

As described above, the 7th generation diodes with the low loss but the wide SOA capability are suitable to a wide variety of conditions for industrial use.

3. Conclusion

Focusing on the improvement of usability for industrial use, we have developed 7th generation IGBTs and diodes with high performance and high SOA capability through the new technologies such as ultra-thin wafer processing and the backside doping profile designing. As a result, we succeeded in realizing 7th generation IGBTs with the higher controllability of dv/dt through optimization of the MOS structure, and with suppression of oscillation through optimization of the backside structure.

The ultra-thin wafer processing technology has been used for IGBTs and diodes of 600 V to 1,400 V. In addition, this backside designing of diodes are also applied to the entire voltage classes up to 6,500 V. Going forward, we will strive to develop 8th generation Si power chips with enhanced performance, controllability, and quality in response to market demands.

References