

7th Gen. IGBT and Diode Chipset Enabling Highest Performance Power Modules

Various application fields of power electronics require semiconductors with low losses, high reliability and good controllability. The 7th gen. IGBT which is based on the carrier stored trench bipolar transistor CSTBT™ technology is developed to address these requirements in the blocking voltage classes of 650V, 1200V and 1700V. A new corresponding freewheel diode is developed based on the new relaxed field of cathode technology.

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Introduction

Industrial IGBT Modules are used in a various field of applications. All this applications require semiconductors with low losses to develop modules and systems which have higher efficiency and higher power density. On the other hand a wide SOA (safe operation area) and good controllability of switching behavior are requested to achieve high reliability and cover the EMI conditions. The trade-off of these contrary requirements for the chip design are improved and optimized with the 7th gen. IGBT.

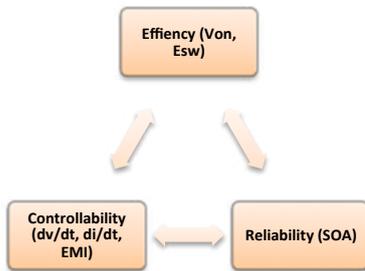


Figure 1: Trade-off of IGBT chip design requirements

IGBT chip design

The IGBT chip design of the 7th gen. IGBT is based on the CSTBT™ technology. This structure is also applied for the 6th gen. IGBT. The result of an additional carrier store layer is higher and homogeneous concentration of carrier's through the IGBT chip which provides lower on state voltage drop. Further optimizing of the cells, reduction of wafer thickness and advanced processes offer further improvements of the total IGBT performance.

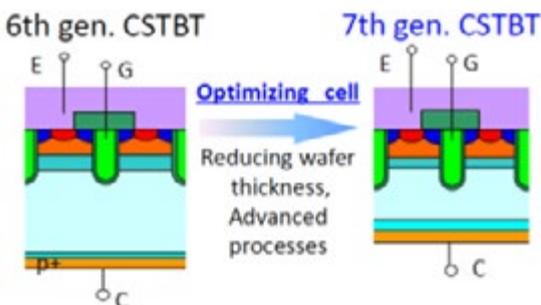


Figure 2: Evolution of IGBT Chip structures

The IGBT chip is divided in active and passive area. The passive area at the termination of the chip is used to expand the electrical field. This passive area does not contribute by the actual current conduction. To minimize the passive area new termination structure is introduced. By this method the IGBT chip size can be reduced without reduction of the active area. Therefore electrical performance of the IGBT is not influenced by this passive edge termination reduction. On the other hand the active IGBT chip area can be enlarged if the total chips size is kept. The result of the enlarged active area is a further reduction of the on state voltage drop. So enlarging active area enables either the reduction of the on state voltage drop or the compact package design with high current density As conclusion the new termination structure enable to design a more compact IGBT chips with higher efficiency.

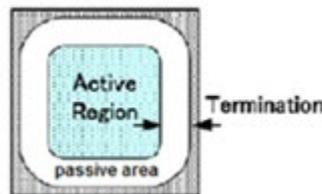


Figure 3: IGBT chip areas

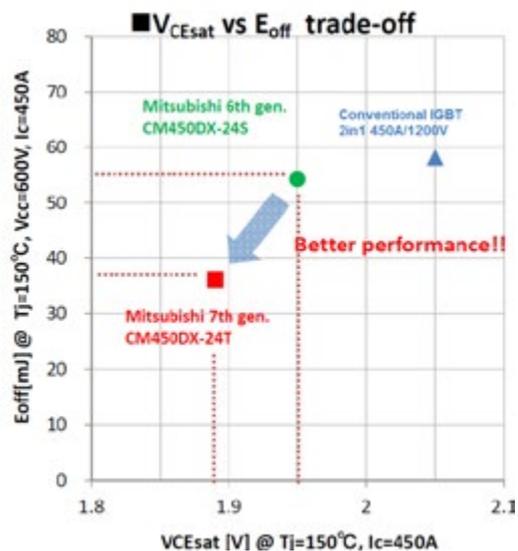


Figure 4: VCE(sat)- Eoff tradeoff of 1200V/450A Modules

By the new structures combined with the reduced wafer thickness and advanced process the $V_{CE(sat)}$ - E_{off} trade-off could be essentially improved as shown in Figure 4. The turn-off losses are reduced by approx. 30% simultaneously with the reduction of $V_{CE(sat)}$ of more than 50mV. By comparing the turn-off switching waveforms in Figure 5 the E_{off} reduction is the result of the reduced current tail.

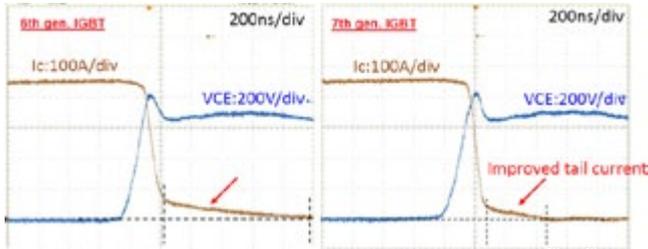


Figure 5: turn-off waveform comparison 6th, 7th gen. 1200V/450A Modules.

From another important point of view, the IGBT power loss performance has trade-off relationship with SCSOA (Short Circuit Safe Operation Area). By improving process, the maximum short-circuit current magnitude is reduced. In addition optimization of CS layer and unit cell design succeeded in obtaining more than 10 μ s short circuit withstands time without sacrificing IGBT power loss performance. In case of 1200V class IGBT 10 μ s withstand time is valid under the condition which are the dc link voltage of 800V and short circuit starting temperature of 150°C.

The unit cell design is optimized for the purpose of improving the trade-off relationship between E_{on} and maximum recovery dv/dt . Reducing the dv/dt has an effect on suppressing the EMI irradiation

noise to the equipment's. If one needed to reduce the EMI irradiation noise, the dv/dt would be reduced by increasing the gate resistance (R_G). Hence, reducing the dv/dt will increase the turn-on energy E_{on} due to slower switching. In the 7th generation IGBT chip, an optimization of the unit cell design is improving this trade-off, resulting in lower turn-on energy E_{on} than previous generation when these are evaluated at same dv/dt condition.

Diode chip design

The requirements as low switching and on state losses and wide SOA are also desired to the free feeling diode. To reduce the forward voltage drop V_F and the charge Q_{rr} the wafer thickness is reduced as shown in Figure 6. The thinner n-drift layer tends to cause a snap-off and oscillation behavior due to strong electric field when the depletion layer reach to the cathode layer. To solve this problem, in 7th generation diode, N+/P cathode structure is applied. This new diode is called RFC (Relaxed Field of Cathode) diode.

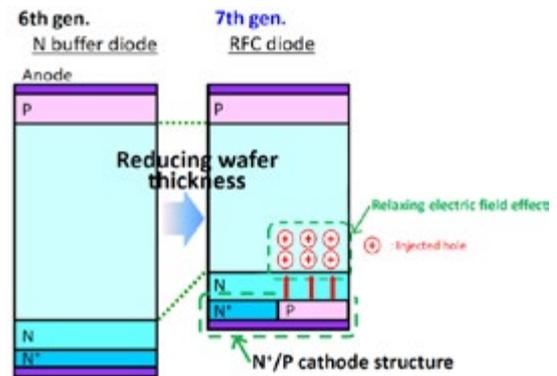


Figure 6: crosssection of 6th and 7th gen diode structure

This is a unique structure in cathode side of the diode chip. P layers are inserted partially and alternately into the N+ layer. This shallow P and N+ alternating layer can relax the expansion of the depletion layer in n- layer by holes injection from P layer. As result RFC diode can minimise snap-off and oscillation. The new diode has improved the trade-off relationship between the forward voltage (VF) and the reverse recovery charge (Qrr) which is shown in Figure 7. The reduction of the reverse recovery charge has two positive impacts. At first the reverse recovery energy is reduced which minimize the diode switching losses. And the second impact is a reduction of the turn-on energy of the IGBT due to the reduced recovery current.

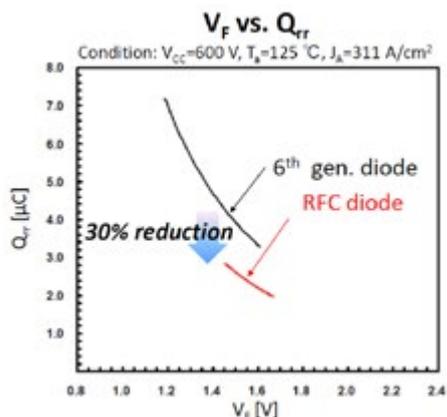


Figure 7: Qrr vs VF tradeoff of 1200V diodes

Inverter operation with 7th gen IGBT

The performance of the IGBT / diode chipset must be assessed under conditions of the application. One of the typical application of those IGBTs and diodes is a motor control inverter with a configuration of three half bridges. For this typical motor control application the losses are calculated as shown in Figure 8. A sinusoidal modulation is considered. To benchmark the real chipset technology performance the simulation is based on the same chip size for 6th and 7th gen. IGBT. The gate resistors are adjusted to the same max. dv/dt of 10kV/µs to have comparable EMI conditions.

As result the 7th gen. IGBT achieved a reduction of 15% total IGBT Module losses compared to the previous 6th gen. IGBT. As shown a

major part of this loss reduction is caused by the better dynamic performance of RFC freewheeling diode. But also the dynamic and static IGBT characteristics contribute to the loss reduction.

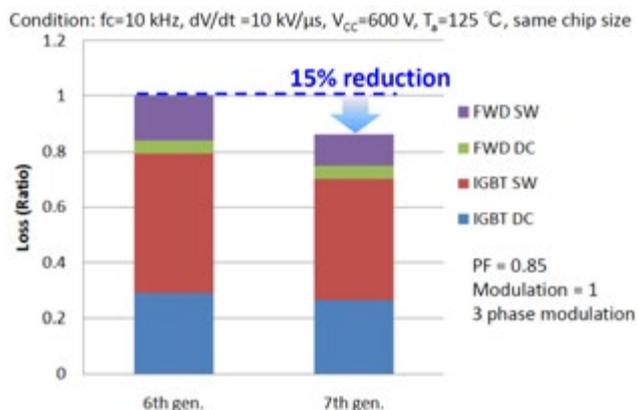


Figure 8: Loss simulation result of 7th and 6th gen IGBT under inverter mode operation conditions

Conclusion:

The 7th gen IGBT and diode technology provide a chipset for a power Module design which could improve the total losses by inverter mode operation by 15%. This has been achieved without sacrificing the reliability and SOA. The switching speed controllability by RG and trade-off of dv/dt and switching losses is improved which resulting in an excellent EMI performance.

These improvements are verifying that the 7th gen. is able to cover the rising requirements of a wide field of power electronics applications.

References

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- [2] PCIM2014 7th Generation IGBT Module for Industrial Applications
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