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CHAPTER 1  PRODUCT OUTLINES

1.1 Applications and Features

DIP-PFC (Dual In Line Package Power-Factor-Correction) is an IPM used for the power factor correction of AC-DC-AC inverter systems such as inverter air-conditioners, general-purpose inverters, etc. It is a highly integrated power module manufactured by the means of transfer mold technology, and featured with the following advantages:

1. Compact Structure
   DIP-PFC realizes a very compact active converter structure by integrating a conventional AC/DC converter, and high speed switching elements IGBT in one package, which contributes to a perfect system solution of with small size, simplification, high reliability and low cost.

2. Transfer Mold Package
   DIP-PFC is manufactured by using the transfer mold technology, which realizes smaller size, lower cost and improved productivity. Furthermore, by mounting a DIP-PFC on the same control board with DIP-IPM, minimum wiring and share of one heat sink can be easily realized.

3. Lower Power Loss
   DIP-PFC employs the low loss IGBT and Diode chips. The total power loss is reduced by about 10% comparing to traditional products, which contributes to an improved system efficiency.

4. Excellent Performance
   By combined utilization with the application specific control IC, the output voltage can be controlled in a wider range, and the high order current harmonic problem can be completely cleared which leads to a high power factor over 99%.

5. Abundant Protective Functions
   DIP-PFC and the control IC are designed with various protective functions for the prevention of module destruction against steep variation of load and various abnormal operations, which improves the reliability of the total system.

1.2 Products Line-up

<table>
<thead>
<tr>
<th>Table 1  DIP-PFC family</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Rating ( V_i )</td>
</tr>
<tr>
<td>-------------------------</td>
</tr>
<tr>
<td>PS51277-A</td>
</tr>
<tr>
<td>PS51259-A</td>
</tr>
</tbody>
</table>

1.3 Structure and Functions

1.3.1 Module Structure

Fig.1(a) and (b) show the DIP-PFC package photograph and its cross-section diagram, respectively. In order to avoid erroneous installation with DIP-IPM, some pins are specially treated, such as lead cut and with wider width.
1.3.2 Internal Circuitry Topology

Fig. 2 shows the internal circuitry of DIP-PFC, which consists of a full-wave diode rectifier bridge and two IGBT elements parallel connected to the negative-side of the diode bridge, and an LVIC for drive of the IGBTs.

1.3.3 Built-in Functions

(a) AC/DC conversion: Converting commercial single phase AC input into DC output.
(b) IGBT drive and protection: The built-in LVIC provides the functions of IGBT gate drive and control supply under voltage (UV) protection.

PFC operation becomes unstable and easy to cause malfunction if control supply is below a certain level. It is necessary to block IGBT operation immediately if UV happens.

(Note): LVIC inside the DIP-PFC only provides the function of IGBT gate drive and UV protection, the DIP-PFC control circuitry and OV/OC protective functions are not built-in. Therefore, a set utilization of the control IC with the DIP-PFC is necessary.
CHAPTER 2 ELECTRIC CHARACTERISTICS

2.1 Static Characteristics

Table 2  Typical static characteristics of DIP-PFC

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameters</th>
<th>Condition</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{CES}$</td>
<td>Collector-emitter shut-down current</td>
<td>$V_{CE}=600V, T_j=25^\circ$</td>
<td>1.0mA(max.) 1.0mA(max.)</td>
</tr>
<tr>
<td>$V_{CE(sat)}$</td>
<td>Collector-emitter saturation voltage</td>
<td>$V_D=15V, V_{CIN}=5V,T_j=25^\circ$ (Note 1)</td>
<td>2.0V(Typ.) 1.8V(Typ.)</td>
</tr>
<tr>
<td>$V_F$</td>
<td>Diode Forward voltage drop</td>
<td>$T_j=25^\circ, V_{CIN}=5V$ (Note 2)</td>
<td>1.6V(Typ.) 2.1V(Typ.)</td>
</tr>
<tr>
<td>$I_r$</td>
<td>Diode Recovery current</td>
<td>$V_{CC}=300V,V_D=15V, T_j=25^\circ$ (Note 3)</td>
<td>13A(Typ.) 13A(Typ.)</td>
</tr>
</tbody>
</table>

Note 1  PS51277-A @ $I_c=30A$, PS51259-A @ $I_c=50A$
Note 2  PS51277-A @ -$I_c=30A$, PS51259-A @ -$I_c=50A$
Note 3  PS51277-A @ $I_c=20A$, PS51259-A @ $I_c=30A$

2.2 Switching Characteristics

Table 3  Typical switching characteristics of DIP-PFC

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{on}$</td>
<td></td>
<td>$V_{CC}=300V, V_D=15V, T_j=125^\circ$</td>
<td>0.23us(Typ.) 0.29us(Typ.)</td>
</tr>
<tr>
<td>$t_{off}$</td>
<td>Switching time</td>
<td>$V_{CC}=300V, V_D=15V, T_j=125^\circ$</td>
<td>0.23us(Typ.) 0.17us(Typ.)</td>
</tr>
</tbody>
</table>

Note 4  PS51277-A @ $I_c=20A$, PS51259-A @ $I_c=30A$

2.3 Recommended Operation Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC input voltage</td>
<td>$V_{CC}$</td>
<td>Between S-R terminals</td>
<td>90 – 264 V_rms</td>
<td></td>
</tr>
<tr>
<td>Control Supply</td>
<td>$V_D$</td>
<td>Between $V_D$ - GND terminals</td>
<td>13.5 15.0 16.5 V</td>
<td></td>
</tr>
<tr>
<td>PWM Carrier Frequency</td>
<td>$f_{PWM}$</td>
<td>$T_c\geq100^\circ C, T_j\geq125^\circ C$</td>
<td>– 20 – kHz</td>
<td></td>
</tr>
<tr>
<td>Input on voltage</td>
<td>$V_{IN(ON)}$</td>
<td>Between $V_{IN}$ - GND terminals</td>
<td>4.0~$V_D$ V</td>
<td></td>
</tr>
<tr>
<td>Input off voltage</td>
<td>$V_{IN(OFF)}$</td>
<td>Between $V_{IN}$ - GND terminals</td>
<td>0~1.0 V</td>
<td></td>
</tr>
</tbody>
</table>

2.4 Waveforms of Input Current/Voltage and Current Harmonic

![Fig.3 Input current/voltage wave of PS51259-A](image1)
Condition: $V_i=200V$, $I_i=15.732A$, $V_o=275.6V$, P.F=99.9%

![Fig.4 Current harmonic of PS51259-A](image2)
Condition: $V_i=200Vrms$, 60Hz, $V_o=370V$, $f_{sw}=20kHz$
CHAPTER 3  PACKAGE

3.1 Package Outline Drawing

![Package Outline Drawing](image1)

Fig. 5 Package Outlines

3.2 Laser Marking

Fig. 6 shows the laser marking range of DIP-PFC. Mitsubishi mark, type name(area A), lot number(area B) are marked in an area of 42.5~8mm, positioned 38mm far away from the right edge of the package.

![Laser Marking](image2)

Fig. 6  Laser marking
3.3 Description of Input/Output Terminal

Table 4  Description of input/output terminal

<table>
<thead>
<tr>
<th>No.</th>
<th>symbol</th>
<th>Terminal Name</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>N2</td>
<td>Output Terminal of PFC</td>
<td>· Connected with the minus side of the converter.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>· A shunt resistor is inserted between N2 and N terminals to detect DC bus current.</td>
</tr>
<tr>
<td>14</td>
<td>GND</td>
<td>GND of Control Supply</td>
<td>· This is the GND of DIP-PFC.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>· In order to avoid the GND potential variation due to IGBT switching, please add a fast clamp diode between this GND and the N terminal.</td>
</tr>
<tr>
<td>15</td>
<td>VD</td>
<td>Control Supply (+ )</td>
<td>· The positive terminal of the 15V supply of LVIC.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>· Please add a noise filter with good temperature and frequency characteristics near the terminal to prevent DIP-PFC malfunction from noise interference.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>· Please ensure the voltage ripple within the specifications.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>· Please add a Zener diode(24V/1W) between the control supply terminals to protect LVIC from surge destruction if the surge voltage is large.</td>
</tr>
<tr>
<td>16</td>
<td>V_in</td>
<td>Control Input</td>
<td>· Input terminal of LVIC. Please connect it to the output terminal of the control IC. If the signal is affected by noise, please add a noise filter with good temperature and frequency characteristics near the input terminal.</td>
</tr>
<tr>
<td>17</td>
<td>GND</td>
<td>GND</td>
<td>· The input signal GND, connected to the control supply GND inside.</td>
</tr>
<tr>
<td>22</td>
<td>P</td>
<td>Output Terminal of PFC</td>
<td>· Connected with the positive side of internal converter.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>· Connect to the positive polarity of inverter input terminal.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>· An electrolytic condenser should be mounted as closely as possible to the P&amp;N terminals so as to suppress surge voltage. In addition, a film condenser with good frequency characteristics is also necessary.</td>
</tr>
<tr>
<td>23</td>
<td>S</td>
<td>AC Input Terminal</td>
<td>· Connect to commercial AC supply via ACL.</td>
</tr>
<tr>
<td>24</td>
<td>R</td>
<td>AC Input Terminal</td>
<td>· Connect to commercial AC supply via ACL.</td>
</tr>
<tr>
<td>25</td>
<td>N</td>
<td>IGBT Emitter</td>
<td>· In order to measure the bus line current, please insert a shunt resistor between N and N2 terminals.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>· The two IGBTs’ terminals are connected inside DIP-PFC.</td>
</tr>
<tr>
<td>26</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: No. 3—13,18—21pins are dummy pins, therefore, should not be connected to PCB pattern

3.4 Function Description

Table 5  Function description

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Operation</td>
<td></td>
<td>· The input drive logic is high-active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>· IGBT turns on if the input signal voltage level is higher than $V_{th(on)}$, and IGBT turns off if the signal level is lower than $V_{th(off)}$.</td>
</tr>
<tr>
<td>Control Supply Under Voltage</td>
<td>UV</td>
<td>· The LVIC monitors the control supply voltage. If there is an under voltage happens within a certain period of time, IGBT gate will be interrupted immediately, and the control input will be suspended.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>· The UV state is defined to be the period from the time the control supply drops below the UV trip level to it rises again to the UV reset level.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>· The control input will be released in the next pulse soon after the control supply rises over the UV reset level.</td>
</tr>
</tbody>
</table>
3.5 Installation Guidelines

Fastening a module to a heat sink with excessive uneven stress might cause devices to be damaged or degraded because over stress will apply to the internal silicon chips. An example of recommended fastening order is shown in Figure 7. Approximately, set the temporary fastening torque to be 20~30% of the maximum rating.

![Recommended Fastening Order of Mounting Screws](image)

Table 6. Mounting Torque and Heat Sink Flatness Specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mounting torque</td>
<td>Mounting screw :</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>M4</td>
<td>0.98</td>
<td>1.18</td>
<td>1.47</td>
<td>N·m</td>
</tr>
<tr>
<td></td>
<td>Recomended 1.18N·m</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Recomended 12 kg·cm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DIP-PFC flatness</td>
<td>-</td>
<td>-50</td>
<td>+100</td>
<td></td>
<td>um</td>
</tr>
<tr>
<td>Heat sink flatness</td>
<td>-</td>
<td>-50</td>
<td>+100</td>
<td></td>
<td>um</td>
</tr>
</tbody>
</table>

![Flatness measurement point of heat sink](image)

Fig. 8 Flatness measurement point of heat sink.

**Tightening torque test**

Tightening torque test is to investigate the maximum allowable tightening torque under which DIP-PFC package will not broke or voltage endurance; inserting a 100um thickness gauge between DIP-PFC and Heat-sink, tightening DIP-IPM gradually to the heat-sink with 0.098N·m (1kg·cm) unit from 1.18Nm (12kg·cm).

Tightening torque is confirmed to be more than 0.98N·m (10kg·cm), even in the worst condition.

Heat sink flatness is prescribed as shown in Figure 8. For most effective heat-radiation it is necessary to enlarge as much as possible, the contact area between the module and the heat sink to minimize the contact thermal resistance. According to the heat sink flatness (surface warp/concavity and convexity) on the module installation surface (refer to Figure 9). Also, the surface finishing-treatment should be less than 12um.

Evenly apply 100um~200um grease with good thermal-conductivity over the contact surface between a module and a heat sink. It is also helpful for preventing the contact surface from corrosion. Further more, use grease with stable quality within the operating temperature range and have long endurance. Use a torque wrench to fasten up to the specified torque. Exceeding the maximum torque limitation might cause...
the modules to be damaged or degraded as the above mentioned fastening with uneven stress. Please pay attention not to remain any ash on the contact surface of the module and the heat sink.

3.6 Temperature measurement of DIP-PFC Case and Heat Sink

The heat sink should be such designed to have enough thermal dissipation capability that the case temperature and IGBT junction temperature of DIP-PFC would not exceed the maximum ratings even at the worst condition. If the DIP-PFC operates at a temperature over the specification, it will possibly lead to a thermal destruction.

Therefore, please select the heat sink on the basis of a careful thermal calculation. In addition, it is also necessary to confirm the effect by a prototype evaluation.

Please measure the case temperature at the position as shown in Fig. 10.

![Fig. 10 Case temperature measurement point](image-url)
CHAPTER 4  SYSTEM APPLICATIONS

4.1 System Connections

![System connection block diagram]

Note:
2. To operate the DIP-PFC properly and make full use of its excellent performance, it is necessary that the DIP-PFC should be used together with its control IC and DIP-IPM.
3. It is necessary to operate DIP-PFC, the control IC, DIP-IPM and MCU on the same GND stage. This GND is usually set to the DIP-PFC N terminal.
4. A large charge current of the electrolytic condenser will flow on the DIP-PFC when applying AC supply, which might cause destruction. Therefore, an Inrush current prevention circuit shown in Fig. 10 is necessary. Open the relay when condenser Co is initially charged, and close it after the charge is over.
5. Large surge voltage is easily produced between P&N terminals when switching large current at a high frequency. The countermeasure to the surge is to shorten the DC-link bus wiring between DIP-PFC and the DIP-IPM as possible as you can. Also, the capacitance of the electrolytic condenser should be large enough to absorb the surge voltage generated both by DIP-PFC and DIP-IPM. In addition, it is necessary to mount a condenser with good high frequency characteristics, such as polypropylene film condenser closely to the P and N terminals of DIP-PFC.
6. In case of mounting the DIP-PFC on the same heat sink as that of DIP-IPM, please make sure that the mounting height and grease thickness of the two modules are the same, so as to minimize the contacting thermal resistance of both modules.
7. Recommendation: ACL: 1mH,
   Co: Electrolytic condenser suitable for high frequency, 1000~2000uF/450VDC,
   Co': Polypropylene film Condenser suitable for high frequency, 0.22uF / 630VDC

* Concerning DIP-IPM, please refer to its application note DPH-0352-B.

4.2 Recommended system Composition

<table>
<thead>
<tr>
<th>PFC</th>
<th>Control IC</th>
<th>IPM</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>PS51277-A</td>
<td>M81012FP*</td>
<td>PS21865, PS21245-E</td>
<td></td>
</tr>
<tr>
<td>PS51259-A</td>
<td>M63914FP</td>
<td>PS21867, PS21246-E</td>
<td></td>
</tr>
</tbody>
</table>

(*) Under Development
DIP-PFC Wiring Guidelines

Because DIP-PFC switches large current at a very high speed, considerable large surge voltage is generated easily between P and N terminals. Please pay attention to the following items:

- The area of P-Co-N shown in Fig. 12 should be as small as possible because the rectangle shaped switching current flows on this route. In addition, please add a bypass condenser Co' with good frequency response such as a polypropylene film condenser closely to the P and N terminals.

- The two IGBT emitters are connected to the VNO terminal of LVIC inside the DIP-PFC. If the internal wiring inductance shown as L1 and L2 in Fig. 13 is too large, large surge voltage will be generated by di/dt. Especially, the lower the temperature, the faster the switching speed, therefore the larger the di/dt. This surge voltage applies to the VNO and N terminals, which is possible to destruct LVIC.

- In order to suppress the surge voltage, the external wiring method shown in Fig. 13 is recommended. To reduce the parasitic wiring inductance, the wiring of the external terminals of N(N-1) and N(N-2) should be made as short as possible.

- Please mount a fast clamp diode (EG01Y@Sanken) between N and control GND terminals to prevent control GND potential variation from the minus voltage of N terminal.

---

Fig. 12 DIP-PFC Interface

![Fig. 12 DIP-PFC Interface](image)

Fig. 13 Recommended wiring method

![Fig. 13 Recommended wiring method](image)
4.4 DIP-PFC Operation Sequence

Control Input

IGBT gate signal

IGBT collector current

Fig. 14 DIP-PFC operating sequence

4.5 Start-up and Stop Operation Sequence of AC Supply, Control Supply and Control Signal

Please follow the sequence shown in Fig. 15 to start-up and stop PFC so as to avoid malfunction or abnormal destruction due to noise or other disturbance at start-up and stop operation. The DC voltage control signal Vctrl should be activated after the ON/OFF switch is turned on.

AC Supply Input

Control Supply Voltage

ON/OFF signal

DC Voltage Control Signal

0 V

0 V

ON

OFF

>= 3 V

0 V

(a) Start-up sequence

(b) Stop sequence

Fig. 15 Start-up and stop operation sequence

There are possibility that the LVIC output will not be ON when the VD is in rising state from 0 V even the ON/OFF signal is set to ON level.

This phenomenon is understood that the initial state of the internal protective circuit is not stable (Hi or Lo) at the control voltage rising period. In this case, please turn off the ON/OFF signal to reset the IC. In addition, even if the IC output can set to ON state, the IGBT gate might be blocked due to abnormal input such as noise.

To avoid such problem, please set the ON/OFF signal after the VD has completely established.
4.6 Noise Withstand Capability

The noise withstand capability of DIP-PFC is carried out under the following conditions, from which over 2.0kV withstand capability has been confirmed. However, noise withstand capability greatly depends on the test conditions, such as the wiring patterns of control substrate, parts layout, and motor type etc., therefore the actual system test should be performed. Fig. 16 shows the evaluation system.

(1) Common noise test condition:
- \( V_i = 200 \text{V}, V_D = 15 \text{V}, T_a = -20\text{°C} \rightarrow 80\text{°C} \)
- Line noise pulse width \( t_w = 1 \mu \text{s} / T = 16 \text{ms} \), Amplitude = \( 2 \text{kV} \)
- Continuous pulse input with pulse width 15 \( \mu \text{s} / T = 50 \text{s} \) to DIP-PFC input terminals.

(2) Thunder surge test condition:
- \( V_i = 200 \text{V}, V_D = 15 \text{V}, T_a = 25 \text{°C} \)
- Thunder surge pulse width \( t_w = 1.2 \mu \text{s} / T = 50 \text{s} \), Amplitude = \( 7 \text{kV} \)
- Continuous pulse input with pulse width 15 \( \mu \text{s} / T = 50 \text{s} \) to DIP-PFC input terminals.

**Fig. 16 Common noise evaluation circuit**

**Fig. 17 Thunder surge evaluation circuit**
CHAPTER 5 ADDITIONAL GUIDELINES

5.1 Packaging Specifications

Per tube
6 pieces of DIP-PFC per tube

Per package box (Max.)
Total number of tubes is 30.
(5 columns x 6 rows)
Total number of DIP-PFC is 180.
(30 tubes x 6 pieces)

Weight
Approximately 54g / Per DIP-PFC
Approximately 420g / Per tube
Approximately 14kg / Per package

The above weights are ones when the maximum number of DIP-PFC is packaged.

Fig. 18 DIP-IPM Packaging Specification
5.2 Handling Precautions

Transportation
- Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged.
- Throwing or dropping the packaging boxes might cause the devices to be damaged.
- Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.

Storage
- We recommend room temperature and humidity in the ranges 5~35°C and 45~75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above.

Long storage
- When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior.

Surroundings
- Keep modules away from places where water or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems.

Disposal
- The epoxy resin and the case materials are made of approved products in the UL standard 94-V0, still they are incombustible.

Static electricity
- Exclusive ICs of MOS gate structure are used for the DIP-PFC power modules. Please keep the following notices to prevent modules from being damaged by static electricity.
  (1) Notice of breakdown by static electricity
  Excessively high voltage (over the Max. rated input terminal voltage) resulting from the static electricity of human bodies and packaging materials, might cause the modules to be damaged if applied on the control terminals. For countermeasures against static breakdown, it is important to control the static electricity as much as possible and when it exists, discharge it as soon as possible.
  * Do not use containers which are easy to be electro-statically charged during transportation.

  * Be sure to short the control terminals with carbon cloth, etc. just before using the module. Also, do not touch between the terminals with bare hands.
  * During assembly (after removing the carbon cloth, etc.), earth machines used and human bodies. We suggest putting a conductive mat on the surface of the operating table and the surrounding floor.
  * When the terminals on the printed circuit board with mounted modules are open, the modules might be damaged by static electricity on the printed circuit board.
  * When using a soldering iron, earth its tip.
  (2) Notice when the control terminals are open
  * When the control terminals are open, do not apply voltage between the collector and emitter.
  * Short the terminals before taking a module off.
Appendix

Specific Control IC for DIP-PFC

A.1 M81012FP (Under Development)

A.1.1 Introduction

M81012FP is an integrated circuit specially developed for the control of DIP-PFC. It is designed in a standard 24-pin SSOP outline as shown in Fig. 19.

A.1.2 Feature

- Automatically synchronizing to the AC input supply, and generating referenced sinusoidal current waveform (50/60Hz);
- Voltage over-shot restraint function in light load (OV1);
- Soft start function
- Built-in protective function
  - Over Voltage protection (OV2)
  - Over Current protection (OC) by using external shunt resistor

A.1.3 Pin Arrangement and Description

<table>
<thead>
<tr>
<th>No.</th>
<th>Symbol</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CT</td>
<td>The oscillator frequency is determined by the potential of middle point of RC, the frequency can be set in the range of 10 kHz~50 kHz</td>
</tr>
<tr>
<td>2</td>
<td>RT</td>
<td>Current error amplifier output</td>
</tr>
<tr>
<td>3</td>
<td>IAOUT</td>
<td>Current error amplifier output</td>
</tr>
<tr>
<td>4</td>
<td>IA+</td>
<td>Current error amplifier input, referenced current signal</td>
</tr>
<tr>
<td>5</td>
<td>IA-</td>
<td>Current error amplifier input, actual current signal</td>
</tr>
<tr>
<td>6</td>
<td>SOUT</td>
<td>Referenced standard sinusoidal current</td>
</tr>
<tr>
<td>7</td>
<td>0cross</td>
<td>Zero cross signal input, synchronized to AC voltage</td>
</tr>
<tr>
<td>8</td>
<td>NC</td>
<td>Null</td>
</tr>
<tr>
<td>9</td>
<td>VDD</td>
<td>Positive terminal of 5V power supply</td>
</tr>
<tr>
<td>10</td>
<td>NC</td>
<td>Null</td>
</tr>
<tr>
<td>11</td>
<td>DGND</td>
<td>GND terminal of IC, please make it short circuit to the GND (No.12 pin)</td>
</tr>
<tr>
<td>12</td>
<td>GND</td>
<td>GND of 5V power terminal</td>
</tr>
<tr>
<td>13</td>
<td>SS</td>
<td>Terminal for setting soft start time</td>
</tr>
<tr>
<td>14</td>
<td>V-LMT</td>
<td>Terminal for setting current limit in soft start operation</td>
</tr>
<tr>
<td>15</td>
<td>NC</td>
<td>Null</td>
</tr>
<tr>
<td>16</td>
<td>VAOUT</td>
<td>Voltage error amplifier output</td>
</tr>
<tr>
<td>17</td>
<td>VA-</td>
<td>Voltage error amplifier input, from DC output voltage signal</td>
</tr>
<tr>
<td>18</td>
<td>OV1</td>
<td>Voltage over-shot restraint at light load, from DC output voltage signal</td>
</tr>
<tr>
<td>19</td>
<td>OV2</td>
<td>Over Voltage protection terminal, from DC output voltage signal</td>
</tr>
<tr>
<td>20</td>
<td>CIN</td>
<td>Over current protection terminal, input from shunt voltage signal</td>
</tr>
<tr>
<td>21</td>
<td>ON/OFF</td>
<td>Input terminal of ON/OFF signal for DIP-PFC start/stop control</td>
</tr>
<tr>
<td>22</td>
<td>CFO</td>
<td>Fault signal output pulse width setting terminal</td>
</tr>
<tr>
<td>23</td>
<td>Fo</td>
<td>Fault signal output terminal</td>
</tr>
<tr>
<td>24</td>
<td>OUT</td>
<td>PWM output for IGBT gate drive, connected to DIP-PFC Vin Terminal</td>
</tr>
</tbody>
</table>
A.1.4 Maximum Ratings (Ta=25°C)

<table>
<thead>
<tr>
<th>No.</th>
<th>Item</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD Supply Voltage</td>
<td>VDD</td>
<td>0.3 V</td>
<td>VDD</td>
<td>(Typ.)=5V</td>
</tr>
<tr>
<td>2</td>
<td>Input Operating Voltage</td>
<td>Vi</td>
<td>-0.3 V</td>
<td>VDD</td>
<td>±0.3 V</td>
</tr>
<tr>
<td>3</td>
<td>Output Voltage</td>
<td>VO</td>
<td>-0.3 V</td>
<td>VDD</td>
<td>±0.3 V</td>
</tr>
<tr>
<td>4</td>
<td>OSC Frequency Capability</td>
<td>†OSC</td>
<td>100 kHz</td>
<td>Typical value=20kHz</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Fo Output Current</td>
<td>IFO</td>
<td>+15 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Operating Temperature</td>
<td>Toper</td>
<td>-20°C</td>
<td>80°C</td>
<td></td>
</tr>
</tbody>
</table>

A.1.5 Interface Circuit Example

Fig. 20  Example of evaluation circuit using M81012FP
A.2 M63914FP

A.2.1 Introduction

M63914FP is a semiconductor integrated circuit specifically developed for the control of active filter. Fig. 19 shows its package outline of 36-pin SSOP.

A.2.2 Features

- Voltage overshot restraint function (OV1)
- Soft start function (SS1)
- Built-in protective functions
  - Over voltage protection (OV2)
  - OC/SC protection by using external shunt resistor
  - Control voltage under voltage protection (UV)
  - Over temperature (OT)

A.2.3 Terminal Arrangement and Description

<table>
<thead>
<tr>
<th>No.</th>
<th>Symbol</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ON/OFF</td>
<td>Input terminal of DIP-PFC operation start signal</td>
</tr>
<tr>
<td>2</td>
<td>TEST</td>
<td>Test terminal, please shorten it to the GND in actual use</td>
</tr>
<tr>
<td>3</td>
<td>Vcc</td>
<td>15V control supply</td>
</tr>
<tr>
<td>4</td>
<td>NC</td>
<td>Null</td>
</tr>
<tr>
<td>5</td>
<td>NC</td>
<td>Null</td>
</tr>
<tr>
<td>6</td>
<td>PVcc</td>
<td>Power supply terminal for control output</td>
</tr>
<tr>
<td>7</td>
<td>OUT</td>
<td>PWM Output terminal for IGBT gate drive</td>
</tr>
<tr>
<td>8</td>
<td>P-GND</td>
<td>Shorten to GND</td>
</tr>
<tr>
<td>9</td>
<td>S-GND</td>
<td>Shorten to GND</td>
</tr>
<tr>
<td>10</td>
<td>S-GND</td>
<td>Shorten to GND</td>
</tr>
<tr>
<td>11</td>
<td>Cin</td>
<td>Over current protection terminal, input from shunt voltage signal</td>
</tr>
<tr>
<td>12</td>
<td>OV2</td>
<td>Over Voltage protection terminal, from DC output voltage signal</td>
</tr>
<tr>
<td>13</td>
<td>OT</td>
<td>Output terminal for over temperature</td>
</tr>
<tr>
<td>14</td>
<td>Vreg</td>
<td>IC internal regular supply</td>
</tr>
<tr>
<td>15</td>
<td>CFO</td>
<td>Fault signal output pulse setting terminal</td>
</tr>
<tr>
<td>16</td>
<td>VA+</td>
<td>Voltage error amplifier input, reference voltage</td>
</tr>
<tr>
<td>17</td>
<td>VA-</td>
<td>Voltage error amplifier input, from DC output voltage signal</td>
</tr>
<tr>
<td>18</td>
<td>VAOUT</td>
<td>Voltage error amplifier output, connected to the multiplier input</td>
</tr>
<tr>
<td>19</td>
<td>lac</td>
<td>Multiplier input, actual current signal</td>
</tr>
<tr>
<td>20</td>
<td>MPOUT</td>
<td>Multiplier output, connected with IA+ terminal</td>
</tr>
<tr>
<td>21</td>
<td>IA+</td>
<td>Current error amplifier input, Referenced sinusoid current signal</td>
</tr>
<tr>
<td>22</td>
<td>IA-</td>
<td>Current error amplifier input, Actual current signal</td>
</tr>
<tr>
<td>23</td>
<td>IAOUT</td>
<td>Current error amplifier output</td>
</tr>
<tr>
<td>24</td>
<td>OV1+</td>
<td>Voltage error amplifier input, form DC output voltage</td>
</tr>
<tr>
<td>25</td>
<td>OV1-</td>
<td>Voltage error amplifier input, form DC output voltage</td>
</tr>
<tr>
<td>26</td>
<td>OV1OUT</td>
<td>Voltage error amplifier output, used for voltage overshot control</td>
</tr>
<tr>
<td>27</td>
<td>S-GND</td>
<td>Connect to GND</td>
</tr>
</tbody>
</table>

Fig. 21 Pin Arrangement of M63914FP
A.2.4 Maximum Ratings (Ta=25°C)

<table>
<thead>
<tr>
<th>No.</th>
<th>Item</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Supply Voltage</td>
<td>VDD</td>
<td>1 VDD</td>
<td>V</td>
<td>DD</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(Typ.)=15V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Supply Voltage</td>
<td>PVDD</td>
<td>-0.2 V DD</td>
<td>V</td>
<td>DD</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>-0.2 V DD</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Output Voltage</td>
<td>VOUT</td>
<td>-0.2 V DD</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>-0.2 V DD</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Output Current</td>
<td>IOUT</td>
<td>≤1 A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>OSC Frequency</td>
<td>'†OSC</td>
<td>50 ‘Hz</td>
<td>Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Typical value=20kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Fo Output Current</td>
<td>IFO</td>
<td>+15 mA</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Operating Temperature</td>
<td>Topr</td>
<td>-20°C to 80°C</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

A.2.5 Interface Circuit Example

Fig. 22  Example of evaluation circuit using M63914FP
A.3 Protective Function (M81012FP, M63914FP)

(1) Voltage Overshot Control Function (OV1)
Generally, the output voltage of a boost type active filter will rise greatly at a light load. OV1 is designed to restrain the overshoot of the output voltage. When the voltage exceeds the defined value by about 20V, IGBT gate input will be blocked so that the further voltage rise can be restrained. OV1 protection can be released automatically if the output voltage drops below the OV1 trip level.

(2) Over Voltage Protection (OV2)
IGBT gate input will be interrupted if the DC bus voltage exceeds the OV2 trip level. This can prevent the over voltage applying to the DC smoothing condenser and the load.

(3) Over Current / Short Circuit Protection (OC/SC)
The DC bus current is detected by using an external shunt resistor. If the current exceeds the SC trip level, IGBT gate input will be blocked to prevent DIP-PFC from over current destruction.

(4) Soft Start Function (SS)
This function is used to start the PFC softly so as to restrain the over current at start-up.

A.4 Fault Output Condition and Its Timing (M81012FP, M63914FP)
The control IC will assert an Fo signal when the following abnormal state is detected

- Over Voltage
Fault signal will output if the output voltage exceeds the OV2 trip level, and at the same time, IGBT operation will be stopped. Over voltage protection cannot be released automatically. To activate the DIP-PFC from an OV2 protection, please reset the ON/OFF signal once again.

- Over Current
Fault signal will output if the bus current exceeds the OC/SC trip level, and at the same time, IGBT operation will be stopped. Over current protection cannot be released automatically. To activate the DIP-PFC from an OC/SC protection, please reset the ON/OFF signal once again.

Note: For UV protection, IGBT gate will be interrupted when control voltage drops below the UV trip level, and the protection will be released automatically if the control voltage recovers to the UV reset level. Because UV protection is realized by the LVIC instead of the control IC in M81012FP, Fo signal will not be asserted by the control IC. However, Fo will be asserted by M63914FP.

Fig.23 Fault output timing chart.
A.5 Example of Interface Circuit Design

(1) PFC ON/OFF Circuit (M81012FP, M63914FP)

The start-up and stop operation of DIP-PFC is controlled by the ON/OFF command usually from a MCU. The ON/OFF control is high active. Fig. 24 shows an interface circuit. It consists of two transistors for level shift. Also, a hard interruption circuit is realized synchronously to the Fo signal coming from DIP-IPM. It is necessary to consider the parameter dispersion of the total resistors in designing the circuit.

![Fig. 24 ON/OFF circuit](image)

- **ON**
  - The internal circuit of ON/OFF terminal connecting to a comparator, therefore, current cannot flow into this terminal. Hence, the collector current of DTC2 can only flow on the resistor R3. Please control the DTC2 base current so that the voltage drop of R3 is within the IC on threshold range of 2.4—2.6 V.

- **OFF**
  - To stop PFC, the base of DTC1 should be set to low by the MCU. In addition, if the Fo output of DIP-IPM becomes low, the base of DTC1 will also become low due to clamp of the diode D1. Therefore, DTC1 as well as DTC2 will be turned off, and PFC will be stopped.

(2) Carrier Frequency Setting Circuit (M81012FP, M63914FP)

The carrier frequency of the IC can be arbitrary set by using the external resistor Rt and the condenser Ct. To make the PFC work most effectively, it is recommended that the carrier frequency to be set to 20—25 kHz. Carrier frequency can be determined as follows:

\[
 f_{\text{WM}} = \frac{1}{\text{Ton} + \text{Toff}} \cdot \frac{1}{\text{Vrt} \cdot \text{Vrt}}
\]

Where Ict is the current flows on the condenser, and Vrt the reference voltage of internal oscillator.

The ON and OFF time can be calculate by using the upper and lower threshold value Vo sch and Vo sc, of the oscillator,

\[
 \text{Ton} = \text{Toff} = (\text{Vosch} - \text{Vosc}) \cdot \text{Ct} \cdot \text{Ict}
\]

Therefore, the carrier frequency can be got from

\[
 f_{\text{WM}} = \frac{1}{\text{Ton} + \text{Toff}}
\]

As for MP81012FP, Vr=1.73V, Vosch=3.0V, Vosc=1.7V.

Suppose RT=100 kΩ, CT=330PF, then

![Fig. 25 Carrier frequency setting circuit](image)
\[ T_{on} = T_{off} = (0.0 - 1.7) \times 330P / (0.73 / 100k) = 24.8 \text{ (sec)} \]
\[ f_{\text{WM}} = \frac{1}{T_{on}+T_{off}} \]

(3) Soft Start Setting Circuit (M81012FP, M63914FP)

The DC voltage will be overshot easily if starting-up the PFC at the condition of a very low bus voltage. To restrain the peak value of voltage overshot, the control IC provide the soft start function, which starts the PFC slowly so that the voltage rises softly to the demand value. The soft start time is determined by the condenser connected to the SS terminal as shown in Fig. 26. The relationship between the soft start time and the capacitance is as follows:

\[ T_s = 3.25 \times 10^5 \times C_s \text{ (s) for } M81012FP \]
\[ T_s = 1.83 \times 10^5 \times C_s \text{ (s) for } M63914FP \]

For your reference, from the internal circuit constant, the voltage overshot becomes zero if the DC voltage control signal varies from 5V (PFC off) to 1.14V (300V) within 500ms. In actual use, the capacitance should be determined by according to the allowable maximum overshot and available mounting space for the condenser of the application system.

(4) Current Limitation Setting Circuit (M81012FP)

The control IC provide the current limitation function for soft start operation. The demanded current level can be set by the reference voltage of the V-LMT terminal, as shown in Fig. 27.

\[ \text{Limited current (A )} = V_{(V-LMT)} \times 20 \text{ (A/V) } \]

Note 1: The control IC might not make response if the V-LMT voltage is under 1.0V.

Note 2: If the referenced voltage is obtained by using resistor division, please pay attention to the resistance dispersion and temperature characteristics of the resistors.

(5) DC Voltage Control Circuit (M81012FP, M63914FP)

Because DIP-PFC is a boost type active converter, it is necessary to ensure the DC bus line voltage to be higher than the maximum peak value of the AC input voltage with a merging of about 30V. The DC output voltage is set by a microprocessor or a hardware circuit instead of the control IC. Figure 28 shows the relationship of DC output voltage versus the voltage command value. For reference, \[ V_{dc}=300@V_{ctrl}=1.04V. \] The maximum DC voltage should not be larger than the over voltage trip level.

The DC voltage setting circuit is shown in Fig. 29. The desired voltage is kept by the voltage feedback to the error amplifier in the control IC.

The DC voltage can be calculated as follows:

\[ V_{dc} = V_{ctrl} + \frac{(V_{reg} - V_{ctrl}) \times R_1 + R_2)}{R_1} \]
**APPLICATION NOTE**

(V23/27)

Vdc

RAOUT

Vctrl

To current-limit circuit

Control IC

Vreg.

Fig. 29 DC output voltage setting circuit

(6) Zero Cross Capturing Circuit (M81012FP)

The control IC captures the zero cross point of AC input voltage, and generates the referenced sinusoidal current waveform with the internal digital/analog circuit. Figure 30 shows the zero cross capturing circuit. Opto-coupler is used to isolate the power side and the control side. The zero cross input to the control IC is pulse signal.

When a forward AC voltage is applied, PC1 turns on and current flows on the primary side. DTC1 also turns on because its base becomes low due to pull-down of R2. The 0cross input becomes high due to the R4.

On the other hand, when a reverse AC voltage is applied, the current is bypassed by diode D1, and the opto-coupler turns off. DTC1 also turns off, which leads to a low input to the 0cross terminal.

Therefore, it is understood that a high level zero cross signal corresponds to the positive waveform, and a low signal corresponds to a negative waveform of the AC input voltage.

The zero cross pulse signal might be not so precisely synchronized to the AC input voltage because of the on/off threshold value of the opto-coupler and the inherent delay of the circuit. Please make compensation to the delay if necessary.

(7) Referenced Sinusoidal Current Generating Circuit (M81012FP)

The control IC generates the referenced sinusoidal current waveform by the internal digital/analog circuit based on the detected zero cross signal and the demand current amplitude.
Note: The PWM on pulse width becomes small when the AC input current phase is near 90°. The output of the voltage error amplifier comes to the peak values of the triangular carrier, as shown in Fig. 33. Therefore, IGBT on pulse is easily imposed by noise, which makes the output of SOUT unstable. If the output voltage of the error amplifier becomes smaller than the minimum value of the carrier, on pulse will not be generated and IGBT will not turn on. A countermeasure to the problem is to connect a bypass film condenser to the SOUT terminal to filter the noise.

For M63914FP, please input the AC current signal to Iac terminal (input of the multiplier) as shown in Fig. 22.

(8) Voltage Error Amplifier Interface Circuit (M81012FP, M63914FP)
The internal error amplifier compares the actual voltage Vdc and the demanded signal Vctrl, and regulate the PWM duty so as to keep the DC voltage to the demanded value. However, error might happens because of the dispersion of the circuit constants. Please make compensation if necessary.
(9) Current Error Amplifier Interface Circuit (M81012FP, M63914FP)

The internal error amplifier compares the actual bus current with the referenced sinusoidal current, and regulates the PWM duty so as to make the actual current follow the referenced one. The output of the error amplifier is compared to the triangular carrier wave, and the result is then sent to DIP-PFC control input. If the wiring of this signal line is too long, noise may be imposed on it, and result malfunction of DIP-PFC.

![Fig. 35 Current error amplifier circuit](image)

(10) Fault Output (Fo) Circuit (M81012FP, M63914FP)

The control outputs an Fo signal when there is a over voltage or over current in the DIP-PFC. Since Fo terminal is open collector type, it is necessary to pull it up to 5V logic supply through a resistor of about 4.7 kΩ. The electric characteristics of terminal is as follows:

<table>
<thead>
<tr>
<th>Item Code</th>
<th>Condition</th>
<th>Rating Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fo output voltage</td>
<td>V\text{FO(L)}</td>
<td>1.0max V</td>
</tr>
<tr>
<td></td>
<td>I\text{FO(L)} = 10mA in operation</td>
<td></td>
</tr>
</tbody>
</table>

Please ensure that I\text{FO(L)} will not exceed 10mA.

The operation of DIP-PFC will be interrupted by the circuit shown in Fig.24, however, to make the system fail-safe against noise, please also stop the PWM output of the microprocessor. In DIP-PFC/DIP-IPM system, although DIP-IPM can work with only a pure diode rectifier bridge, it is better to stop the total system by software in case there is Fo output either from DIP-PFC or DIP-IPM. In addition, a noise filter is recommended in the circuit. The time constant should be determined according to actual application condition.

The Fo output pulse width is determined by the condenser connected to the CFO terminal. (Example: C\text{FO}=22 \, \text{rF} \quad \text{t}_\text{p} = 1.8\text{ms (typ )})

![Fig. 36 Fo output circuit](image)

(11) Over Voltage detecting Circuit (M81012FP, M63914FP)

There are two over voltage control functions (OV1, OV2) in the control IC. OV1 is used for the restraint of voltage overshot in light load, it will not latch-up and can recover to normal state if the OV1 lock is released. OV2 is used for the protection DIP-PFC from over voltage destruction, it will stop the DIP-PFC and keep the latch-up state. The control IC outputs Fo only an OV2 failure is detected.

The over voltage detecting circuit of OV2 is shown in Fig.36. The DC bus voltage signal is obtained by the division of resistors, and is compared with the fixed reference voltage by the internal error amplifier. If the
DC voltage exceeds the setting value, the error amplifier will output a latch signal to the OV2 protection circuit to stop the DIP-PFC.

To prevent malfunction due to noise, a noise filter with a time constant of about 2 μs is recommended.

![Over voltage detecting circuit](image)

**Fig. 37 Over voltage detecting circuit**

(2) PFC Over Current Detecting Circuit (M81012FP, M63914FP)

The PFC DC bus line current is detected by using a shunt resistor. The detected current signal is transferred to the control IC with the circuit shown as Fig. 38

![Current detecting circuit](image)

**Fig. 38 Current detecting circuit**

The maximum value of over current should be set below the 1.7 times of the IGBT current rating. In addition, please set the RC filter constant to 1.5—2.0 μsec so as to shut down PFC quickly in case of a over current.
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