TECHNICAL BULLETIN

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[Title] Cautions when using the A1S66ADA analog to digital conversion function **[Date of Issue]** June, '03

[Relevant Models] A1S66ADA

Thank you for your continued support of Mitsubishi programmable logic controllers, MELSEC-A series.

This bulletin provides cautions when using the A1S66ADA analog to digital conversion (hereinafter referred to as A/D conversion) function.

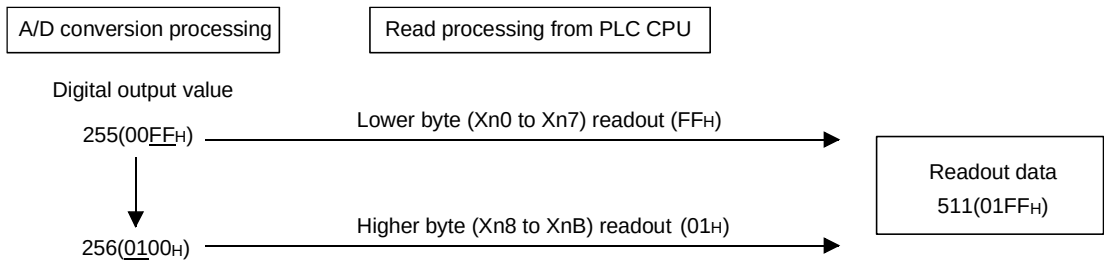
1. Caution

When a digital output value is read from the PLC CPU, an excessively large or small data value may be read out intermittently. To prevent this, create a sequence program that will mask these invalid values. Please refer to Section 3. Program example.

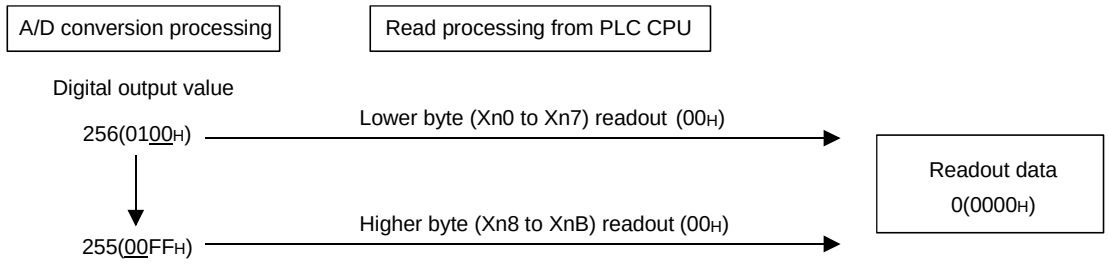
2. Detailed description

When a digital output value is read from the PLC CPU (while the A1S66ADA is performing A/D conversion), the lower byte (Xn0 to Xn7) and the higher byte (Xn8 to XnB) may be read at a different instance in time.
If this occurs, the old A/D conversion data of the lower byte and current A/D conversion data of the higher byte are stored as a 16bit value, which results in the value being incorrect. (An incorrect value is produced, when the value is incremented/decremented by 1.)

Example 1) A digital output value is read from the PLC CPU during A/D conversion of the A1S66ADA (when the value is incremented by 1).



Example 2) A digital output value is read from the PLC CPU during A/D conversion of the A1S66ADA (when the value is decremented by 1).



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3. Program example

The following is a program example for reading a digital output value A/D-converted through Channel 3.
At each scan, a read digital output value is compared with the one read at the preceding scan and only normal data are updated.
In the following program, an error of 100 or more in the digital value is determined as abnormal.
For the value used for the determination, set "(Input variation per scan) + (Digital error value 40)" or more.

(1) System configuration
Install the A1S66ADA to "slot 0" of the main base.

(2) Devices used by user
1) Digital output value read command signal..... M0
2) Digital output value read switch signal M1
3) Data read interlock signal for digital output value comparison M2
4) Data register for storage of digital output value comparison source data D0
5) Data register for storage of digital output value comparison data D1
6) Data register for storage of difference between D0 and D1..... D2
7) Data register for storage of normal digital output value D10