ISSN 1345-3041

Mar.2015 / Vol.149

Mitsubishi Electric

ADVANCE

Recent Development Results of Power Device

MITSUBISHI ELECTRIC
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Mar. 2015 / Vol. 149
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Mitsubishi Electric Advance is published on line quarterly (in March, June, September, and December) by Mitsubishi Electric Corporation.

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Technical Reports

Precis

Mitsubishi Electric offers a wide variety of power electronics products to satisfy various customer needs, ranging from home appliances to industrial, automotive and railway application products.

In addition, developments of new SiC devices together with new packaging technology are now intensively underway.

Overview

Author: *Gourab Majumdar**

Status Quo and Prospects of Power Semiconductor Technologies

With the increasing global population as well as economic development in emerging countries, the demand for energy continues to grow. The shale gas revolution in the United States may substantially help solve energy issues, but not global warming. Renewable energies such as wind and solar power are attracting attention, and the efficient use of energy is becoming ever-more important. Over 40% of secondary energy is widely used as electric power. Therefore, the development of power electronics (PE) technologies for converting power has become essential for effectively using electricity.

By supplying not only various PE devices and machinery which help save energy but also power semiconductors as the core of such PE devices and machinery, Mitsubishi Electric is promoting research and development with a view to the sustainable development of such devices and machinery. In particular, we are improving the performance and functions of insulated gate bipolar transistor (IGBT) modules and intelligent power modules (IPMs) that incorporate peripheral circuits having optimal protection and driving functions.

These power modules combine technological elements of not only the semiconductor chip structure and process design but also package technology to ensure high-temperature and high-reliability performance. Starting from a planar gate cell structure through a trench cell structure and CSTBTs (IGBTs forming carrier accumulation layers), Si-IGBT chip technology has now reached the seventh-generation CSTBTs in which high performance is achieved by using ultra-thin wafer technology.

In recent years, to create high-temperature, high-withstand voltage semiconductors having high-speed switching performance by replacing Si wafers with SiC (Silicon Carbide) wafers for semiconductor materials, Mitsubishi Electric has developed and commercialized power metal-oxide semiconductor field-effect transistors (MOSFETs), power modules and IPMs using power Schottky barrier diode (SBD) chips.

These new semiconductors have enabled dramatic reductions in power conversion losses as well as the size and weight of power modules and their application systems, leading to the further evolution of power electronics equipment.

This issue looks at our power semiconductors, and development examples of our IGBT modules, IPMs, SiC and device technologies in the fields of consumer applications, industry, automobiles and electric railways.

**Fellow, Semiconductor & Device Group*

Super Mini DIPIPM "Ver.6 Series"

Authors: *Shogo Shibata** and *Masahiro Kato**

This paper introduces the new Super Mini DIPIPM™ Ver.6 Series for air conditioners and other white goods applications.

The Ver.6 Series employs the seventh generation insulated-gate bipolar transistor (IGBT) configured in the carrier-stored trench-gate bipolar transistor (CSTBT) architecture to reduce the power consumption and cost of inverter systems. It also enables improved system design by offering an enhanced product lineup and expanded overload operating range.

1. Introduction

Mitsubishi Electric's Dual Inline Package Intelligent Power Modules, the DIPIPM series, are transfer-molded IPMs with integrated power chips and control IC chips containing drivers and protection circuitry. In 2004, Mitsubishi Electric commercialized the Super Mini DIPIPM Ver.4 Series configured with the fifth generation IGBT, and in 2011, the Super Mini DIPIPM Ver.5 Series with the sixth generation IGBT. These series have helped reduce the size and energy consumption of inverter units for air conditioners, washing machines, refrigerators and other white goods. This time, the "Super Mini DIPIPM Ver.6 Series" has been developed by incorporating Mitsubishi Electric's proprietary seventh generation IGBT. In 2013, this series was put into mass production and has contributed to the low power consumption of white goods. This paper describes the outline, features and key technologies of the Super Mini DIPIPM Ver.6 Series.

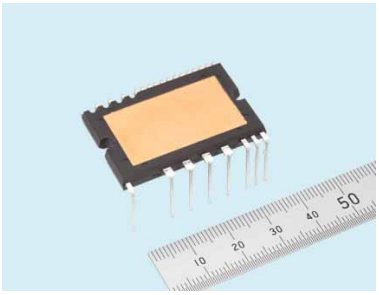

Fig. 1 External view of the Super Mini DIPIPM Ver.6 Series

2. Outline of the Super Mini DIPIPM Ver.6 Series

As shown in Fig. 2, the internal circuit of the Ver.6 Series is configured in the conventional manner, integrating a three-phase AC output power inverter and control circuit. The control integrated circuit consists of a high-voltage integrated circuit (HVIC), a low-voltage IC (LVIC) and bootstrap diodes (BSDs).

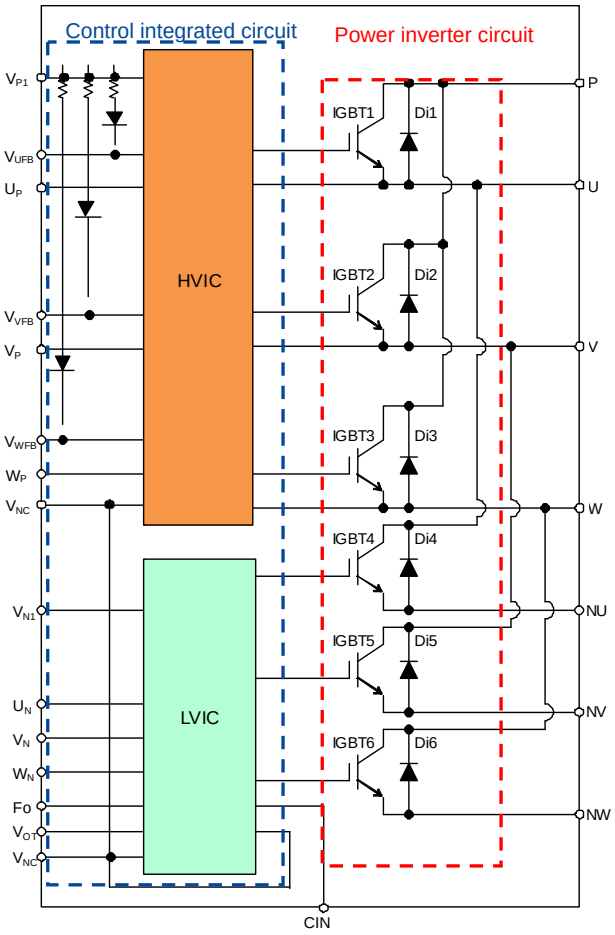

Fig. 2 Internal circuit diagram

2.1 Power inverter circuit

The three-phase AC output power inverter is configured with six IGBTs and six free-wheeling diodes (FWDs).

2.2 Control ICs

HVIC (one unit): The HVIC integrates the drive circuits for the P-side IGBTs, the high-voltage level shifter, and the undervoltage protection circuit for the floating power supply (UV, without Fo (full output)). A bootstrap circuit system is employed to enable driving with a single 15-V power supply.

LVIC (one unit): The LVIC integrates the drive circuits for the N-side IGBTs, the undervoltage protection circuit for the control power supply (UV), the short-circuit protection circuit (SC), and the

*Power Device Works

overtemperature protection (OT) or analog temperature output (VOT) circuit. The short-circuit protection circuit detects an overcurrent using an external shunt resistor, feeds it back to the LVIC to shut off the IGBTs, and outputs an error signal if the undervoltage protection circuit for the control power supply or the short-circuit protection circuit is active.

BSD (three units): Diodes for the bootstrap circuit (BSDs) are integrated with the current limiting resistors. They eliminate the need for external components and thus help reduce the board size. They also enable driving with a single 15-V power supply.

2.3 Internal structure

Figure 3 shows a cross-sectional diagram of the Super Mini DIPIPM Ver.6. The package size and terminal arrangement and layout remain the same as that of the previous Super Mini DIPIPM Ver.5. This minimizes the design and evaluation time for upgrading to the Ver.6 Series.

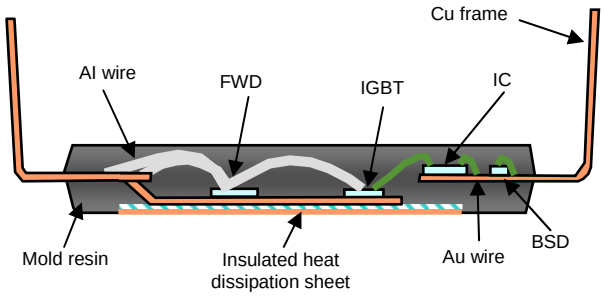

Fig. 3 Internal structural diagram

3. Features of the Super Mini DIPIPM Ver.6 Series

3.1 Seventh generation IGBT

The Super Mini DIPIPM Ver.6 Series adopts the seventh generation IGBT, which has improved the IGBT performance from the level of the Ver.5 Series. While the IGBTs of previous generations already employed Mitsubishi Electric's proprietary transistor structure, namely CSTBT, to achieve high energy saving performance, the seventh generation focuses on saving energy under low-load operating conditions. To this end, in the CSTBT structure as shown in Fig. 4, the seventh generation IGBT has drastically reduced the thickness of the p+ layer as well as optimizing the device structure.

In addition, it has also minimized the turn-off tail current and reduced the switching power loss. These improvements significantly reduce the power loss of air conditioners during rated operation.

3.2 Enhanced lineup

The previous Super Mini DIPIPM Series lineup has a maximum rated current of up to 30 A; and the BSD circuit is integrated in the 5 to 15-A models that have a high market demand. By employing the seventh generation IGBT, the Ver.6 Series has achieved a greater current carrying capacity per unit area. This makes it possible to add a new model with a rated current of 35 A to the lineup and the BSDs are now integrated in six models ranging from 5 to 35 A.

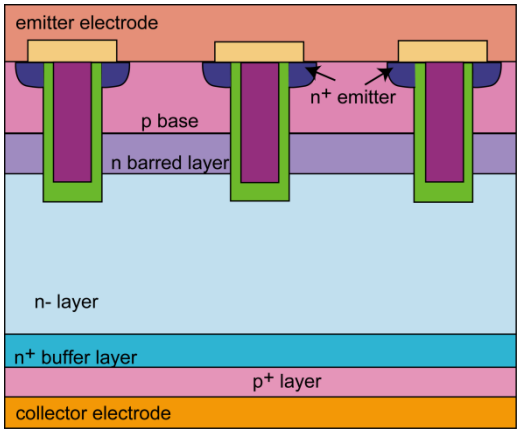

Fig. 4 CSTBT structure

3.3 Expanded overload operating range

The Ver.6 Series employs a trimming circuit to compensate the characteristics of the short-circuit protection function embedded in the LVIC. As a result, the variance in the detected voltage for short-circuit protection has been reduced from the conventional ±10% to ±5%. This improved accuracy allows 10% expansion of the inverter overload operating range, and increases the current carrying capacity for driving the system's motors.

3.4 Overtemperature protection/temperature detection function

Just like the previous Ver.5 series, the new Super Mini DIPIPM Series is available with overtemperature protection (OT) or analog temperature output that externally reports the module temperature as an analog voltage signal (VOT). Either model can be chosen according to the system requirements.

4. Performance/Characteristics of Super Mini DIPIPM Ver.6 Series

For the representative model of the Super Mini DIPIPM Ver.6 Series, PSS15S92E6-AG (15 A/ 600 V), Table 1 shows the electrical characteristics, and Fig. 5 shows the dependence of the temperature rise, $\Delta T(j-c)$, on the allowable effective current. When operated with a carrier frequency of 5 kHz at an effective current of 7.5 Arms, the rise in junction temperature remains below 25°C.

Table 1 Electrical characteristics of PSS15S92E6-AG

Item	Symbol	Conditions	Min.	Min.	Typ.	Max.	Unit
Collector-emitter saturation voltage	$V_{CE(sat)}$	V_D=V_{DB}=15V, I_C=15A, V_{IN}=5V	Tj=25°C	–	1.70	2.05	V
			Tj=125°C	–	1.90	2.25	
Forward voltage drop	V_{EC}	-I_C=15A, V_{IN}=0V		–	2.50	3.00	V
Switching time	t_{on}	V_{CC}=300V, V_D=V_{DB}=15V, I_C=15A, Tj=125°C, V_{IN}=0⇔5V, Inductive load		0.65	1.05	1.45	μs
	t_{rr}			–	0.30	–	
	$t_{c(on)}$			–	0.40	0.65	
	t_{off}			–	1.15	1.60	
	$t_{c(off)}$			–	0.15	0.30	

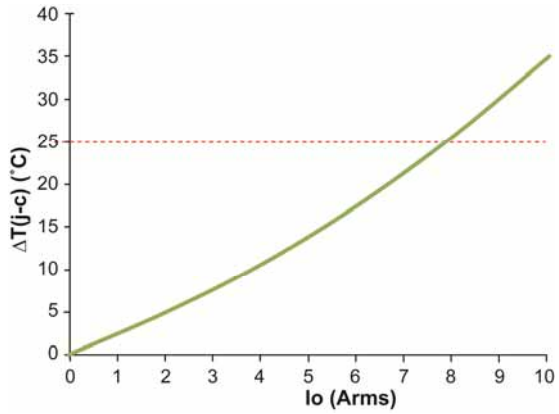

Fig. 5 Temperature rise – Allowable effective current characteristics of 15-A model of Super Mini DIPIPM Ver.6 Series (Conditions: Tj = 125°C, Vcc = 300 V, P.F. = 0.8, three-phase sinusoidal output)

5. Conclusion

This paper presented the functions and features of the newly developed/commercialized Super Mini DIPIPM Ver.6 Series. We will continue to use the key technologies of the Ver.6 Series to develop products that meet market needs, thus expanding the use of inverters in home appliances and industrial equipment and hence saving energy.

Reference

(1) Masataka Shiramizu, et al.: “Super Mini DIPIPM ‘Ver.4 New Series’ Development, Mitsubishi Denki Giho, 84, No. 4 (2010) (in Japanese).

Hybrid SiC Modules for High-Frequency Applications

Author: *Yuji Miyazaki**

1. Introduction

A high-frequency hybrid SiC power module reduces losses during operation in high-frequency regions. It increases the switching frequency of the equipment and thus enables the size, weight, and cost of the equipment to be reduced.

2. Increase in Switching Frequency

Power supply systems often employ AC reactors and/or filter circuits for suppressing harmonics, output transformers for power conversion, and DC reactors for voltage boosting circuits. These reactor components are generally bulky and thus occupy considerable space, particularly in a large-capacity system, making it difficult to reduce the size, weight and cost of power electronics devices and peripheral systems.

From the designer's standpoint, it is advantageous to increase the switching frequency of the power device, because higher frequency allows the use of smaller reactor components, thus reducing the size and cost of equipment as well as potentially creating new added value such as the integration of external reactors and improved filter performance. Since 2004, Mitsubishi Electric has provided the fifth generation insulated-gate bipolar transistor (IGBT) optimized for high-frequency switching, namely the carrier-stored trench-gate bipolar transistor (CSTBT). These have been commercialized as the "NFH Series" high-frequency IGBT modules, which are widely used for uninterruptible power supply (UPS), power conditioners for solar power generation, medical power units and other equipment that runs at a high switching frequency.

3. Development of Hybrid SiC Module

3.1 Features

As the successor of the "NFH Series", our newly developed high-frequency hybrid SiC module employs a silicon carbide Schottky barrier diode (SiC-SBD) to meet the requirements for increasing the power system frequency. The SiC-SBD is expected to exhibit much higher performance than the silicon diode (Si-Di). Figure 1 compares the turn-on current waveforms of the Si-Di and SiC-SBD. Inside the Si-Di, which is a bipolar device with a PN junction, minority carriers (holes) are accumulated during the conduction period, and then are discharged by the electric field applied during the switching period. Consequently, a spike-like transient current (recovery current) appears and acts as a factor to increase the switching power loss. In contrast, the SiC-SBD operates as a unipolar device and thus generates no recovery current. There is only a small charge current due to the parasitic capacitance of the device, resulting in an extremely small switching loss.

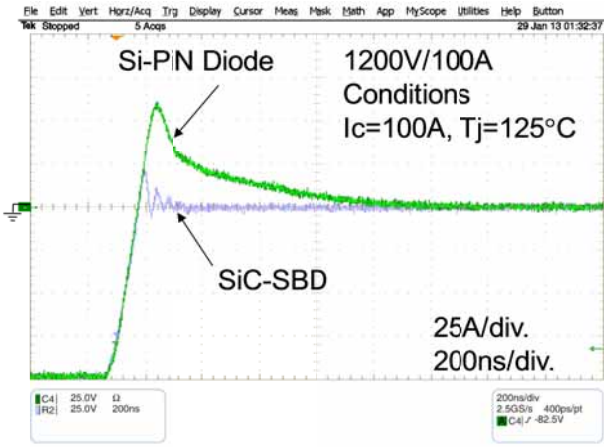

Fig. 1 Comparison of turn-on waveforms

In contrast, it is less meaningful for the transistor switch to employ a SiC – metal oxide semiconductor field effect transistor (MOSFET) to reduce conduction loss, because the conduction loss accounts for a relatively small percentage of the applied equipment's total loss. Considering cost effectiveness too, we adopted a well-proven Si-IGBT device for the NFH Series. In response to the market demand, we have developed a product lineup with a rated voltage and current of 1,200 V and 100 to 600 A (Table 1). The packages are fully compatible with those of the conventional NFH Series and so the existing devices can be easily replaced. In addition, since the IGBT

Table 1 Product lineup

Type name	Voltage	Current	Circuit	Package
CMH100DY-24NFH	1200V	100A	2in1	A
CMH150DY-24NFH		150A		
CMH200DU-24NFH		200A		B
CMH300DU-24NFH		300A		
CMH400DU-24NFH		400A		C
CMH600DU-24NFH		600A		

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characteristics remain the same as those of the conventional products, the driving circuit requires no modification for the replacement.

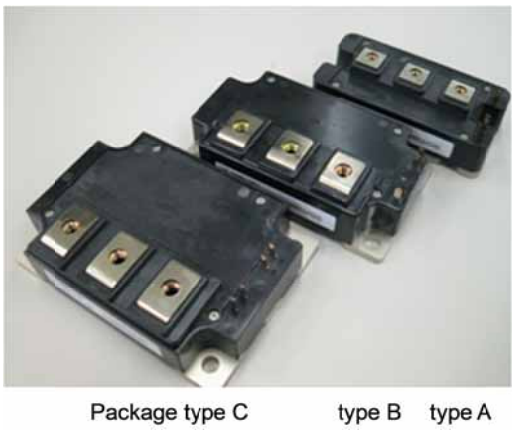

Fig. 2 External view of modules

3.2 Reduction in power loss and increase in Switching Frequency

Figure 3 shows the breakdown of the power loss per half module of the 1,200 V/100 A rated conventional and new power modules. Assuming application to a general-purpose power supply, the operating conditions are set to provide an output of 30-A sinusoidal current (effective value) at a switching frequency of 30 kHz. Under these operating conditions, the hybrid SiC module reduces the power loss by almost 40% compared with the conventional NFH Series. This is mainly attributable to the reduction in the diode switching loss. This reduction level is sufficient to improve the total power conversion efficiency of the power electronics system. As an alternative, the reduction in power loss can be used for increasing the switching frequency. Figure 4 compares the power loss – switching frequency relationship at varying switching frequencies, otherwise under the same operating conditions as those of Fig. 3. According to the results, if the power loss is kept equal, the switching frequency of the hybrid SiC module can be doubled from that of the conventional NFH Series.

4. Conclusion

The combined technologies of the existing Si device and advanced SiC device have achieved a much higher performance than that of the conventional high-frequency NFH Series module. By increasing the equipment operating frequency, it is possible to reduce the size of reactor components, and hence reduce the size, weight, and cost of the equipment. In response to diversified user needs, we will continue to develop high value-added products.

References

(1) Mitsuharu Tabata, et al.: "The NF Series: New Trench-type IGBT Modules with Low Power Drive", Mitsubishi Denki Giho, 77, No. 9, 563–566 (2003) (in Japanese).
(2) Yuuji Miyazaki, et al.: "IGBT Module "NFM Series for High Frequency Application", Mitsubishi Denki Giho, 80, No. 6, 411–414 (2006) (in Japanese).

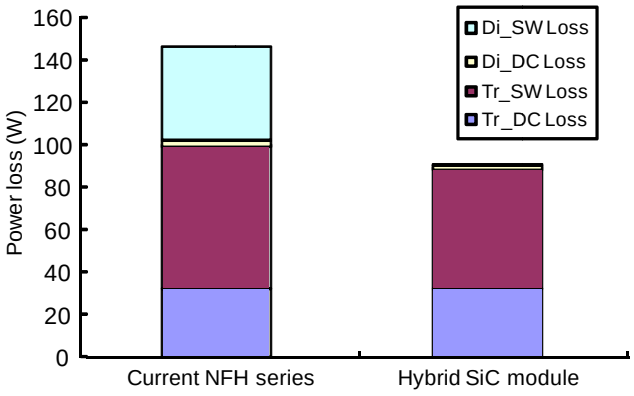

Fig. 3 Power loss (30 kHz)

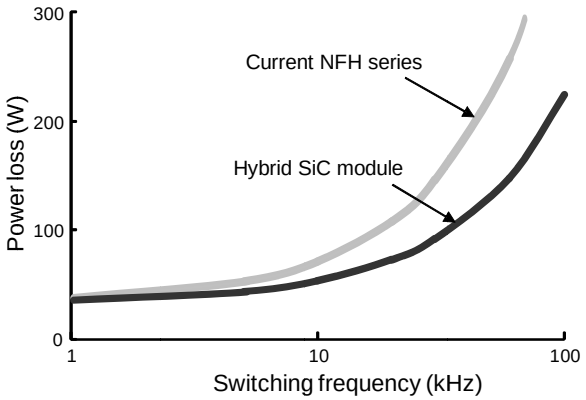

Fig. 4 Frequency dependence of power loss

Next-Generation Power Module for Automotive Applications – J1-Series

Authors: *Mikio Ishihara** and *Kazuaki Hiyama**

In recent years, electric vehicles (EVs) and hybrid electric vehicles (HEVs) have evolved remarkably, and in turn, there is a growing demand for higher performance, smaller, and lighter power modules as key components.

In response to these market needs, the smaller, lighter, higher-performance "J1-Series" has been developed. A direct water-cooling structure was adopted to achieve 30% lower thermal resistance, 40% smaller footprint, and 76% lighter weight.

1. Outline of J1-Series Power Module

The J1-Series comprises automotive power semiconductor modules integrating six each of seventh generation insulated-gate bipolar transistors (IGBTs) and seventh generation diodes in a pin-fin type direct water-cooling package (Fig. 1).

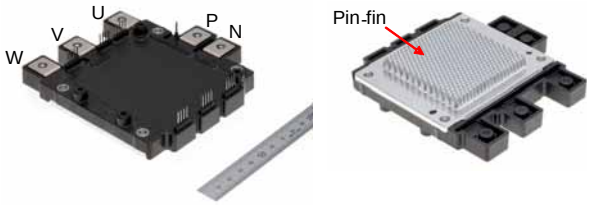

Fig. 1 External appearance of J1-Series power module

The product lineup covers various user needs by means of four models with the same outer dimensions and electrode layout, but with different ratings (Table 1).

Table 1 J1-Series Power Module Lineup

Model	Ratings (Ic/Vces)	Vce(sat) Typ. @Ic, 25°C	Package size (mm)
CT600CJ1A060	600A/650V	1.4V	120×115.2×31 (6-in-1)
CT400CJ1A090	400A/900V	1.7V	
CT300CJ1A120	300A/1200V	1.7V	
CT300CJ1A060	300A/650V	1.4V	

As shown in the circuit diagram (Fig. 2), the internal connection of the J1-Series uses a 6 in-1 configuration for size reduction and efficient installation at the user's site. In addition, each IGBT chip is provided with a current sensor for short-circuit protection as well as an on-chip temperature sensing diode for overtemperature protection, which is able to directly monitor the chip temperature.

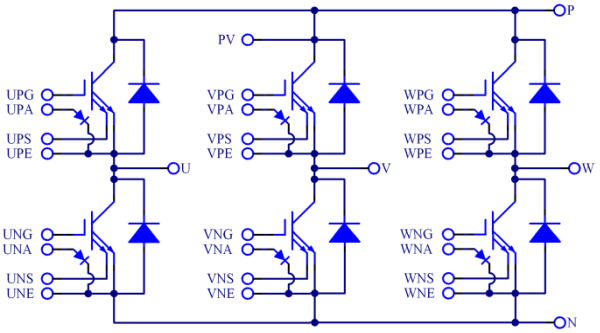

Fig. 2 Circuit diagram of J1-Series

2. New Package Structure

To implement the development concept, a new package structure has been developed for the J1-Series (Fig. 3).

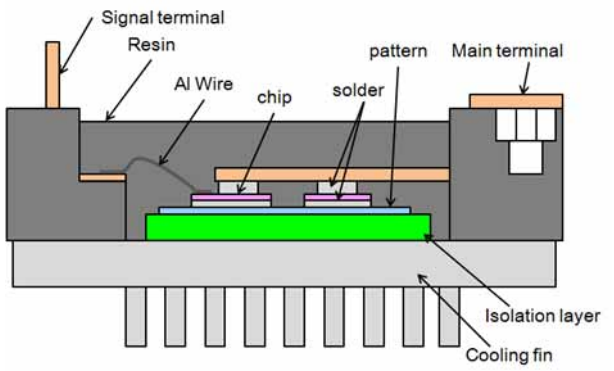

Fig. 3 Internal package structure of J1-Series

The J1-Series no longer uses heat sink grease as required by the previous structure; instead, it is equipped with a cooling fin integrated with the module to allow direct cooling and improve the cooling performance. In addition, by optimizing the shape and layout of the fin, and eliminating the solder layer beneath the isolation layer, the thermal resistance between the chip and the cooling water, $R_{th(j-w)}$, is reduced by more than 30% from the level of the conventional product that consists of three J-Series transfer-molded power modules (T-PMs) mounted on a Cu cooling fin with the heat sink grease between them (Figs. 4 and 5).

To increase the current carrying capacity and thus reduce the package size, a direct-lead-bonding (DLB)

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structure has been adopted (Fig. 6), where the upper surface of the chip is directly bonded to the Cu lead. Compared to the conventional wire bonding (WB) structure, the contact area can be expanded, and thus the current carrying capacity can be significantly improved. In combination with the previously described improved cooling performance, the DLB structure has successfully reduced the package size and hence the footprint by 40%[*1] (Fig. 7).

In addition, the DLB structure ensures more uniform chip temperature while power is supplied compared to the WB structure, and thus generates less thermal stress in the chip and improves the power cycle tolerance.

The J1-Series uses aluminum as the cooling fin material to provide high corrosion resistance against cooling water and to reduce the weight by 76%[*2] from the conventional product (Fig. 4).

As described above, the J1-Series is smaller and lighter, and has higher cooling performance and enhanced current carrying capacity.

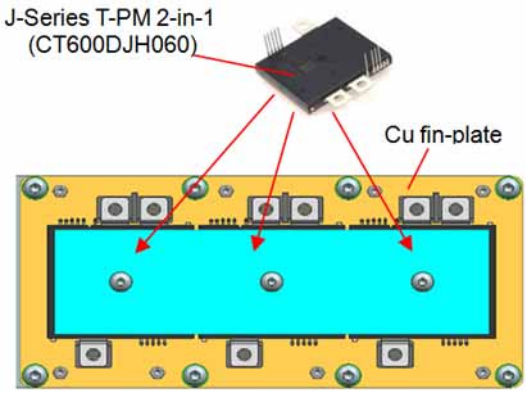


Fig. 4 Conventional product (J-Series T-PM with Cu fin)

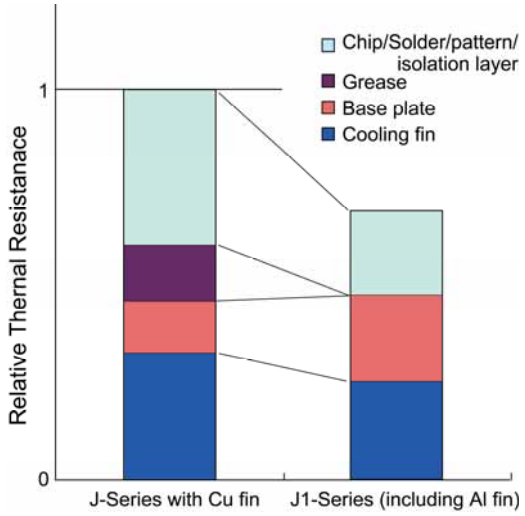


Fig. 5 Comparison of thermal resistance of J1-Series and conventional product

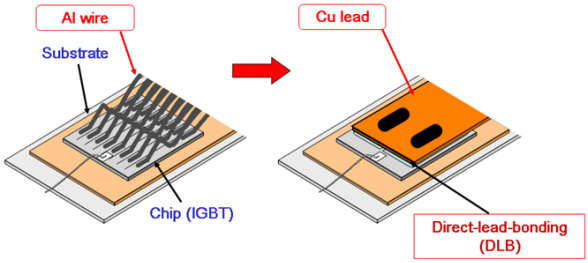


Fig. 6 Comparison of conventional WB and DLB structures

3. Evaluation Kit

To help the user evaluate the J1-Series, an evaluation kit has been newly designed and prepared as a support tool. The kit consists of a driver board, a DC-link capacitor and a water-cooling jacket. It is optimized to enhance the features of the J1-Series, that is, “higher performance” and “smaller and lighter”. The photo in Fig. 8 shows the J1-Series PM and driver board mounted on the water-cooling jacket.

The driver board is configured with an IGBT gate driver IC (M81603JFP), newly developed for the J1-Series PM.

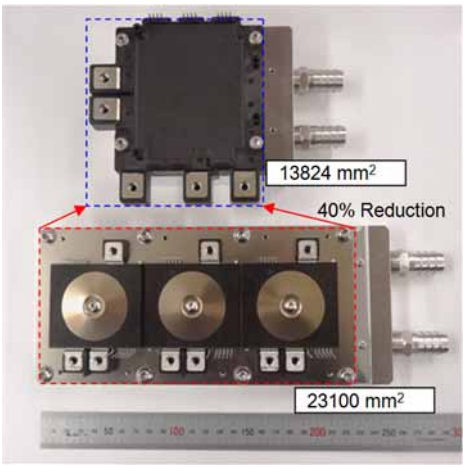


Fig. 7 Comparison of footprints of J1-Series and conventional product

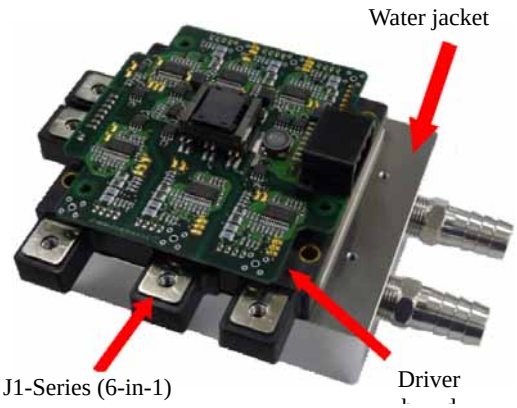


Fig. 8 Evaluation kit for J1-Series

[1] J1-Series 120×115 [mm²], Conventional product 220×105 [mm²]

[2] J1-Series 335 [g], Conventional product 1250 [g]

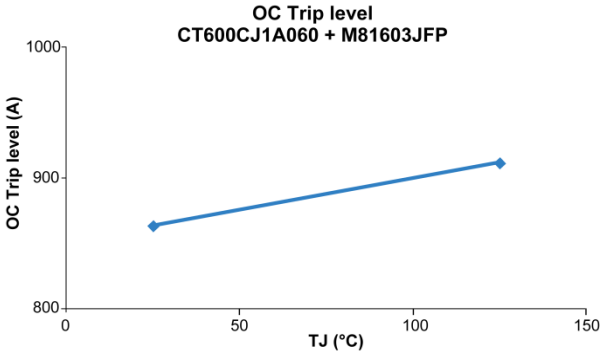


Fig. 9 OC trip level of J1-Series measured with evaluation kit

4. Gate Driver IC (M81603JFP)

In addition to the protection functions equivalent to those of the conventional intelligent power module (IPM), namely, short-circuit protection (SC), overtemperature protection (OT) and undervoltage protection (UV), the gate driver IC, M81603JFP, is equipped with the following additional gate driver and protection functions all integrated in a single IC package.

(1) By adding a function to switch the turn-off gate resistor according to the chip temperature, the IGBT switching loss is reduced by 20%.

(2) By adding a correction circuit for the temperature characteristics of the overcurrent protection (OC) function, it is possible to lower the level of OC sensitivity to the temperature and thus it is no longer necessary to consider the chip temperature margin in the product design. Figure 9 shows the measurement results for the OC trip level when the correction is used.

(3) By adding a circuit to switch the gate drive voltage from 12.7 V to VDD voltage[*3] during the turn-on period, the maximum short-circuit current is limited to below a certain level. In addition, the OC circuit is optimized to reduce the response time of the protection circuit at the time of short circuit. These additional features have reduced the power loss during the short-circuit period by 50%, and thus the product design no longer needs to consider the tradeoff between chip performance and short-circuit tolerance.

(4) By providing an independent soft shutdown gate resistor to each of the SC and OC circuits, the surge voltage in the case of a short circuit is halved and the delay time in the case of an overcurrent is also halved.

5. Verification of Current Carrying Capacity

We verified the current carrying capacity of the J1-Series by evaluating its electrical characteristics and thermal resistance. Under the conditions of carrier frequency fc = 5 [kHz], cooling water temperature Tw = 65 [°C], and cooling water flow rate = 10 [l/min], a current carrying capacity of 600 A (= 424 A rms) or higher was demonstrated even when the electrical parameters and thermal resistance were set to the maximum values.

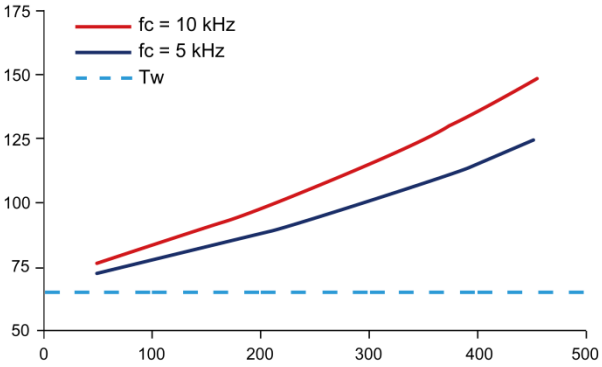


Fig. 10 Verification of current carrying capacity of CT600CJ1A060

6. Conclusion

In response to EV and HEV market needs, the new "J1-Series" of automotive power semiconductor modules has been developed along with an evaluation kit. The J1-Series achieves high performance, compact size and light weight compared with the conventional products, contributing to development of the automotive inverter system.

The evaluation kit was developed as a user support tool. It consists of a water-cooling jacket and a driver board that includes driving and protection circuits optimized for the J1-Series.

We will continue to work on mass-producing products, enhancing the product lineup and offering products to users.

[3] Power supply voltage of the IGBT driver circuit

Technologies for Seventh Generation High Performance, High Ruggedness Power Chips

Authors: *Kenji Suzuki** and *Fumihito Masuoka**

For the evolution of power electronics, it is essential to enhance the performance of Insulate Gate Bipolar Transistors (IGBTs) and diodes, both mounted on the power modules. Since the late 1980s, Mitsubishi Electric has been developing low-loss structures for IGBTs such as by fine pattern processing and the CSTBT™[1-2]. Diode performance has also been improved by thin wafer processing and cathode profile optimization.

This paper presents the high performance and ruggedness (i.e., wide Safe Operating Area (SOA)) seventh generation IGBT and diode, which have been developed by employing an ultra-thin wafer process and newly optimized profiles in the backside doping layer.

1. Seventh generation IGBT

The first to third generation IGBTs were of the planar type structure, and their performance was improved by applying the conventional finer cell-pitch patterning technology. The fourth and later generations adopted a trench-type structure instead; and the fifth and later generations adopted the Mitsubishi Electric's proprietary CSTBT™ structure, where a Carrier-Stored (CS) layer is formed beneath the Channel Dope layer. Since the CS layer can enhance the electron injection efficiency to hold high enough holes on the emitter side during on-state, i.e. carrier storing effect, it is possible to reduce the on-state forward voltage drop V_{on}. The sixth generation IGBT employed the narrower trench-gate pitch to enhance the carrier storing effect and the performance was further improved. In addition, the high energy ion implantation was used to form the CS layer, and the variance in the threshold voltage was successfully reduced.

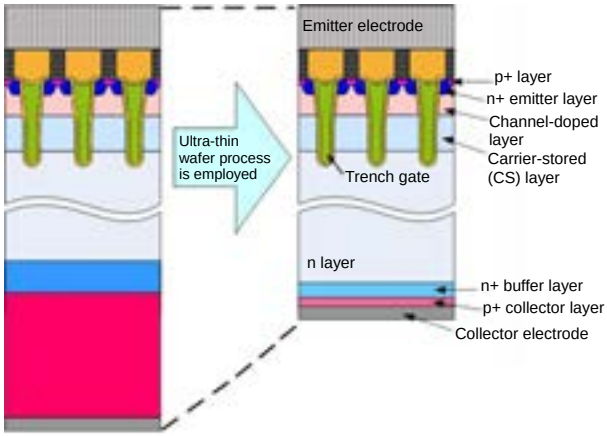
The performance of the IGBT is described by the Figure Of Merit (FOM) defined by:

$$FOM = \frac{J_C}{V_{CE(sat)} \times E_{off}} \quad (1)$$

where J_C (A/cm^2) is the collector current density, $V_{CE(sat)}$(V) is the collector-emitter saturation voltage (on-state voltage V_{on}), and E_{off} (mJ/cm^2/A/pulse) is the normalized turn-off energy loss.

The sixth generation IGBT achieved far higher performance than the first generation: the FOM of the 1200V class IGBT was increased by more than 10-fold from the first generation. Additional improvements have also achieved the required product characteristics of high reliability such as high temperature operation and high ruggedness, and those are based upon the improved termination and backside structures as well as the metal oxide semiconductor (MOS) structure.

Figure 1 shows the cross-sectional schematics of the sixth and seventh generation IGBTs. The 600V class seventh generation IGBT employs the Light Punch-Through (LPT) structure by using the ultra-thin wafer process to improve the trade-off between V_{on} and E_{off}. At the same time, the area ratio between the N$^+$ emitter and P$^+$ region of the gate structure as the MOS cell is also optimized to maintain the sufficiently low saturation current, thus ensuring the wide Short Circuit SOA (SCSOA)[3].



(a) Sixth generation IGBT (b) Seventh generation IGBT

Fig. 1 Cross-sectional schematics of the sixth and seventh generation IGBTs

Figure 2 shows the output V_{CE}-J_C characteristics of the sixth and seventh generation 600V class IGBTs. In the seventh generation IGBT, the LPT structure reduced the concentration in the P$^+$ collector and N$^+$ buffer layers, which keeps the built-in potential (voltage) lower than that of the sixth generation IGBT, and

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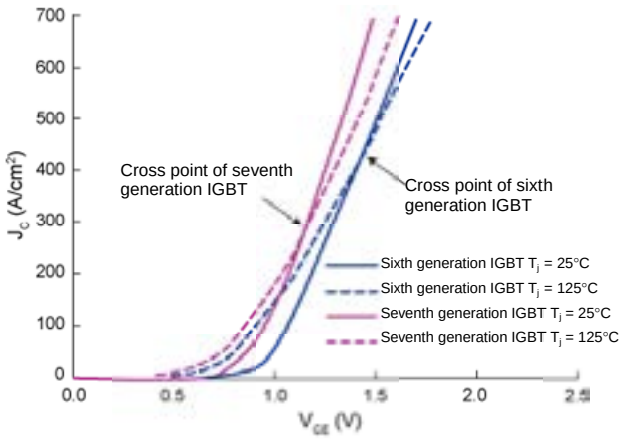


Fig. 2 Output characteristics of sixth and seventh generation IGBTs

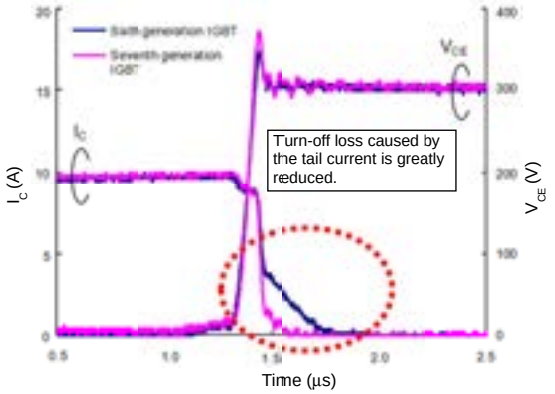


Fig. 3 Turn-off waveforms of sixth and the seventh generation IGBTs

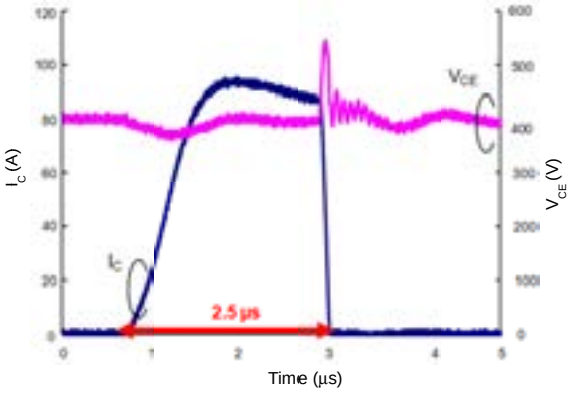


Fig. 4 SCSOA waveform of seventh generation IGBT

improved the more than 0.1V of V_{on} at or around the rated current density of 500A/cm^2. In addition in the seventh generation IGBT, the trade-off between the V_{on} and E_{off} has been adjusted by the backside P collector concentration, so as to exhibit a lower cross point of the V_{CE}-J_C curve suitable for parallel operation. The seventh generation IGBT requires no carrier lifetime control process such as electron beam irradiation. Therefore, it exhibits stable electrical characteristics for a long time, and is suitable for high temperature, large current operation.

Figure 3 shows the turn-off waveforms of the sixth and seventh generation IGBTs, both using 600V/10A rated power chips and measured under the following conditions: collector-emitter voltage V_{CE} = 300V, gate-emitter voltage V_{GE} = 15V/0V, collector current I_C = 10A, and temperature T_j = 125degC. The seventh generation IGBT has a lower tail current than that of the sixth generation and has reduced the turn-off loss by about 34%. Also, by optimizing the backside P-collector concentration, the seventh generation IGBT, just like the sixth, has successfully suppressed the oscillation in the turn-off waveform.

Figure 4 shows the waveforms of the seventh generation IGBT that demonstrate the characteristics of the SCSOA. As the described above, the optimized MOS structure maintained the saturation current sufficiently low to enhance the latch-up tolerance. As a result, a wide SCSOA that satisfies the product requirements is ensured up to a pulse width of 2.5µs under the conditions of V_{CE} = 400V, V_{GE} = 15V/0V, and Tj = 125degC.

So, the seventh generation IGBT has achieved the excellent performance with an FOM of 1.8 times of that of the sixth generation maintaining an even wider SCSOA.

2. Seventh generation diode

The free wheeling diode has reduced the forward voltage drop V_F by employing the thin wafer process and optimizing the cathode profile[4]. While the thin wafer process is effective for reducing the V_F for both the IGBT and diode, it in turn reduces the margin against a snap-off voltage endurance during the reverse recovery time period, and hence increases the risk of device breakdown. This time, the thin wafer process has been employed together with a new backside cathode doping profile to develop the seventh generation diode[5].

Figure 5 shows the cross-sectional schematics of the conventional and seventh generation diodes. In the seventh generation diode, there are partial P type regions on the cathode side. This structure avoids carriers from an absence time period around the cathode even under the depletion severely hitting the cathode conditions during the reverse recovery mode operation. As a result, the electric field on the cathode side is relaxed and thus the oscillation phenomenon is prevented.

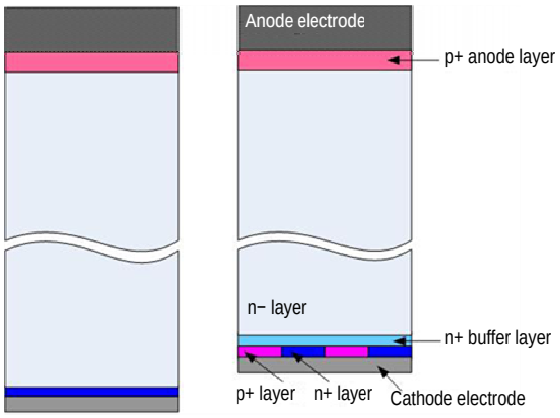
Figure 6 shows the output V_{AK}-J_A characteristics of 1200V class conventional and seventh generation diodes. Maintaining the low V_F characteristics, the seventh generation diode has reduced the cathode electron injection efficiency to keep a low current level of the cross point between the V_{AK}-J_A curves at room

and high temperatures. This tends to reduce the unexpected current increase when the temperature rises at or around the rated current, and thus the seventh generation diode is suitable for the chip parallel operation of the high power module.

Figure 7 shows the reverse recovery waveforms of conventional and seventh generation diodes, both using 1200V/10A rated power chips and measured under the conditions of V_{AK} = 800V, I_A = 0.6A, and Tj = 25degC, in which condition the conventional diode tends to cause oscillation. The conventional diode generates a high voltage peak (snap-off) when the tail current is sharply shut off, as depicted by broken circles in Fig.7. In contrast, with the seventh generation diode, almost no voltage surge is observed and the snap-off is successfully prevented. This peak voltage, defined as the snap-off voltage $V_{snap\text{-}off}$, was measured with increasing V_{cc} applied during the reverse recovery time period. The result revealing the ultimate characteristics is shown in Fig. 8. The $V_{snap\text{-}off}$ of the conventional diode is heavily dependent on the V_{cc}, and the $V_{snap\text{-}off}$ exceeds the rated breakdown voltage at V_{cc} = 800V, and at V_{cc} = 900V the chip was destroyed. On the other hand, the seventh generation diode effectively suppresses the $V_{snap\text{-}off}$. This suppression effect is more conspicuous with increasing V_{cc}, and allows the recovery operation even at V_{cc} = 1000V without any breakdown.

Consequently, the seventh generation diode makes it possible to reduce the wafer thickness by about 21% from the sixth generation level without emerging oscillation phenomenon, resulting in the reduction of V_F and reverse recovery loss E_{rr}.

The FOM of the diode is also defined by Eq. (1), where the collector current density J_C (A/cm^2) is replaced with the anode current density J_A (A/cm^2), the collector-emitter saturation voltage $V_{CE(sat)}$ (V) that determines the steady-state loss with the forward voltage drop at 125degC V_F (V), and the turn-off loss E_{off} (mJ/cm^2/A/pulse) with the reverse recovery loss at



(a) Conventional diode (b) Seventh generation diode

Fig. 5 Cross-sectional schematics of conventional and seventh generation diodes

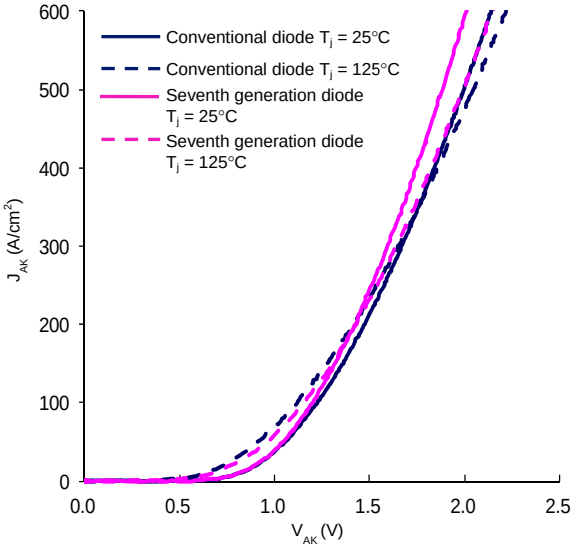


Fig. 6 Output characteristics of conventional and seventh generation diodes

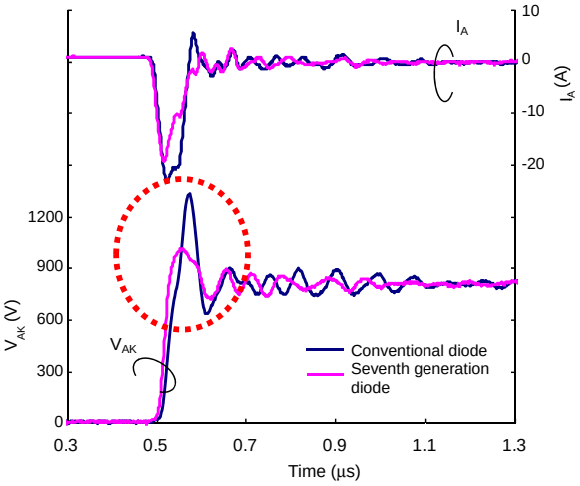


Fig. 7 Reverse recovery waveforms of conventional and seventh generation diodes under oscillation-prone conditions

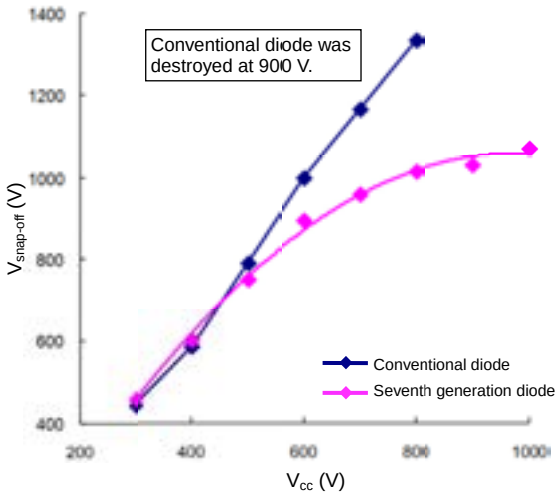


Fig. 8 V_{cc} – $V_{snap\text{-}off}$ relationship of conventional and seventh generation diodes under oscillation-prone conditions

125degC E_{rr} (mJ/cm^2/A/pulse). In terms of the FOM, the seventh generation diode has achieved a drastic improvement, 2.7 times higher than that of the conventional diode.

We are currently developing a 1200V class IGBT and diode that employ the new ultra-thin wafer process and the backside doping profile already applied to 600V class devices. In addition, we plan to apply the seventh generation technologies to all the diodes with a higher breakdown voltage including the 6500V class chips. We will continue to serve a series of high performance and high quality Si power chips to all the applications of the markets.

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Low On-Resistance SiC-MOSFET with a 3.3-kV Blocking Voltage

Authors: *Kenji Hamada*, Shiro Hino** and *Takeshi Kitani***

An SiC-MOSFET with a 3.3-kV blocking voltage has been developed by using Mitsubishi Electric's proprietary low on-resistance technology that partially increases the doping concentration at the surface of the n-SiC drift layer. By optimizing the cell structure parameters and ion implantation conditions, the new MOSFET has achieved a specific on-resistance of 14 mΩcm^2 and an avalanche breakdown voltage of 3.9 kV.

1. Background

Silicon carbide (SiC) is attracting attention as a new semiconductor material expected to replace silicon (Si) material. SiC enables the fabrication of low-resistance, high-voltage power devices surpassing Si power devices. Mitsubishi Electric is currently working on reducing the power loss, enhancing the performance, and increasing the current of the SiC metal oxide semiconductor field effect transistor (SiC-MOSFET) and SiC Schottky barrier diode (SiC-SBD), which are both SiC unipolar devices having a blocking voltage in the range of 600 V to 1.7 kV. In parallel, Mitsubishi Electric has also been developing application technologies such as employing SiC power devices in inverter applications, and has demonstrated improved efficiency and downsizing of the equipment.

The SiC unipolar devices are also applicable to industrial and railway vehicle power modules, which require an even higher blocking voltage. Mitsubishi Electric has integrated SiC-SBDs and Si insulated-gate bipolar transistors (Si-IGBTs) to fabricate a prototype hybrid SiC module with a 3.3-kV blocking voltage, and demonstrated its 1.5 kV/ 2 kA switching operation.(1) To increase the efficiency of the module even further, the Si-IGBT needs to be replaced with an SiC switching device. Therefore, an SiC-MOSFET with a blocking voltage of 3.3 kV has been strongly desired. This paper describes the development of Mitsubishi Electric's SiC-MOSFET with a 3.3-kV blocking voltage.

2. Fabrication of SiC-MOSFET with a 3.3-kV Blocking Voltage

2.1 Device structure

The basic structure of the SiC-MOSFET developed by Mitsubishi Electric is of a double diffused MOSMET (DMOSFET), which is widely adopted for Si power MOSFETs. The SiC-MOSFET with a 3.3-kV blocking voltage was fabricated on a 30-μm-thick n-SiC drift layer epitaxially grown on an n-type 4H-SiC substrate and having a doping concentration of 3×10^{15}/cm^3. As the termination structure, the uniquely developed field limiting ring (FLR)(2) was adopted to allow an avalanche breakdown to occur in a stable manner at a drain voltage of about 4 kV. The SiC-MOSFETs were fabricated with the following cell structure parameters: channel length = 0.4–1.6 μm, length of junction field effect transistor (JFET) = 1.6–3.6 μm, cell pitch = 11 μm, and active area = 4.8×10^{-5} to 9.0×10^{-2} cm^2. Annealing for the activation of ion implanted impurities was performed at 1700°C. A 50-nm-thick gate oxide was formed by the thermal oxidation and nitridation processes. Ni silicide was formed for the source and drain contact electrodes.

2.2 Reduction in on-resistance of MOSFET (JFET doping)

The 3.3-kV SiC-MOSFET is designed to have a relatively low doping concentration in the drift layer, which is likely to increase the resistance of the JFET region. To reduce the JFET resistance, it is effective to extend the JFET length and increase the doping concentration in the JFET region (JFET doping). However, both of these methods in turn increase the electric field of the gate oxide and cause a negative effect on the long-term reliability and the MOSFET's blocking voltage. Thus there is a tradeoff between the JFET resistance and the gate oxide electric field, and the optimum design of both the JFET length and JFET doping conditions is extremely important.

This time, by utilizing the process/device simulation technique, the JFET doping parameters have been optimized to a doping concentration of 1×10^{17}/cm^3 and a thickness of about 1 μm. JFET doping was performed by multiple ion implantation of nitrogen atoms as the n-type impurity, while the surface region of the drift layer was not doped to avoid any negative impact on the MOSFET's channel characteristics or the gate oxide electric field.

3. Electrical Characteristics of 3.3-kV SiC-MOSFET

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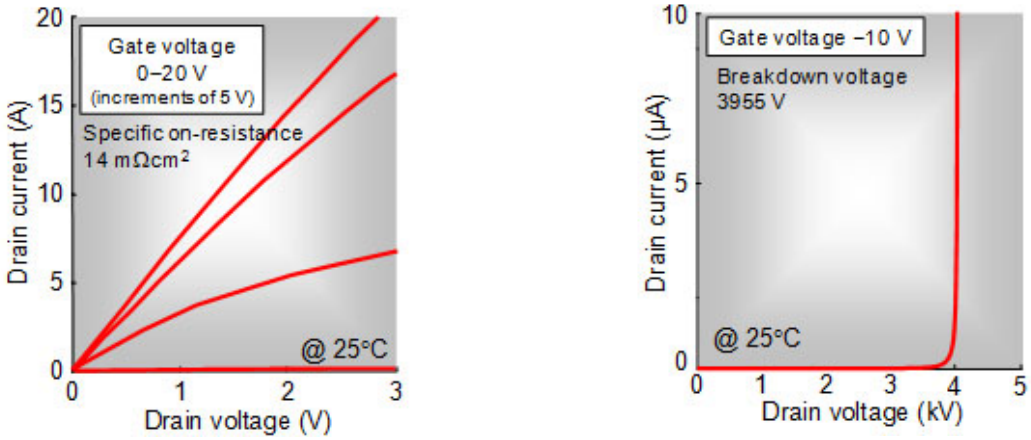
3.1 Cell structure dependence of static characteristics

Figure 1 shows the output and the blocking characteristics of the SiC-MOSFET with an active area of 9.0×10^{-2} cm^2. A specific on-resistance of 14 mΩcm^2 was obtained at a gate voltage of 15 V and a drain current density of 100 A/cm^2. An avalanche breakdown voltage of about 3.9 kV was obtained at a gate voltage of −10 V.

Figure 2(a) shows the channel length dependence of the specific on-resistance of SiC-MOSFETs both having an active area of 2.0×10^{-3} cm^2. The specific on-resistance decreases monotonically with shrinking channel length regardless of the JFET doping. The device with JFET doping has a specific on-resistance that is 8 to 12 mΩcm^2 lower than that of the SiC-MOSFET without JFET doping. Either device exhibits an effective channel mobility of about 22 cm^2/(V·s). Figure 2(b) shows the JFET length dependence of the specific on-resistance. The specific on-resistance remarkably increases with shrinking JFET length regardless of the JFET doping. The SiC-MOSFET with JFET doping exhibits a specific on-resistance relatively less dependent on the JFET length, which suggests that the depletion in the JFET region may have a significant impact on the specific on-resistance.

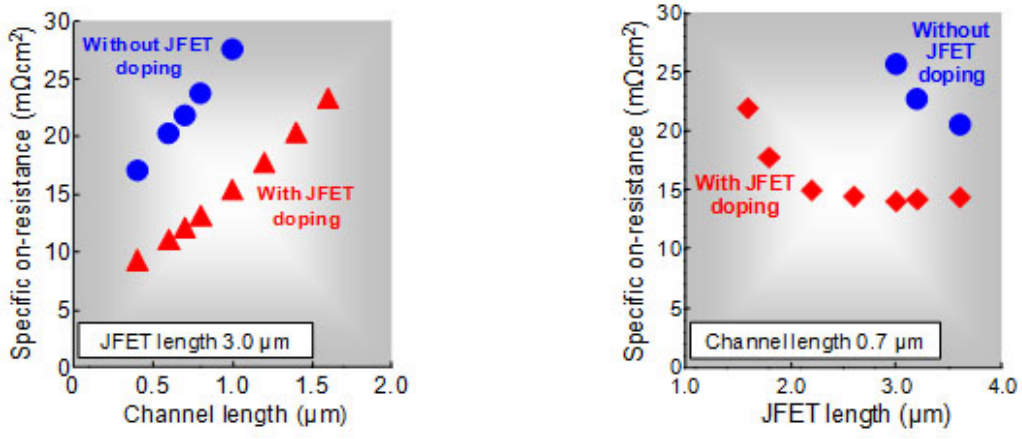
Figure 3 shows the analysis of the specific on-resistance. The channel resistance decreases with shrinking channel length regardless of the JFET doping. This is due to the increase in the channel width density. On the other hand, the JFET resistance and drift resistance increase with shrinking JFET length; in particular, the SiC-MOSFET without JFET doping shows a remarkable increase. To reduce the total resistance of the 3.3-kV SiC-MOSFET, it is quite effective to reduce the JFET resistance by means of JFET doping.

Figure 4 shows the JFET length dependence of the avalanche breakdown voltage at a gate voltage of −10 V. In the case of the SiC-MOSFET with JFET doping, the breakdown voltage decreases with increasing JFET length, which is caused by an increasing electric field at the edge of the p-well. In



(a) Output characteristics (b) Blocking characteristics

Fig. 1 Output characteristics and blocking characteristics



(a) Channel length dependence (b) JFET length dependence

Fig. 2 Channel length and JFET length dependence of specific on-resistance

Drain current(A)

order to achieve both a low specific on-resistance and a high blocking voltage, optimum design of both the JFET length and the JFET doping conditions is crucial.

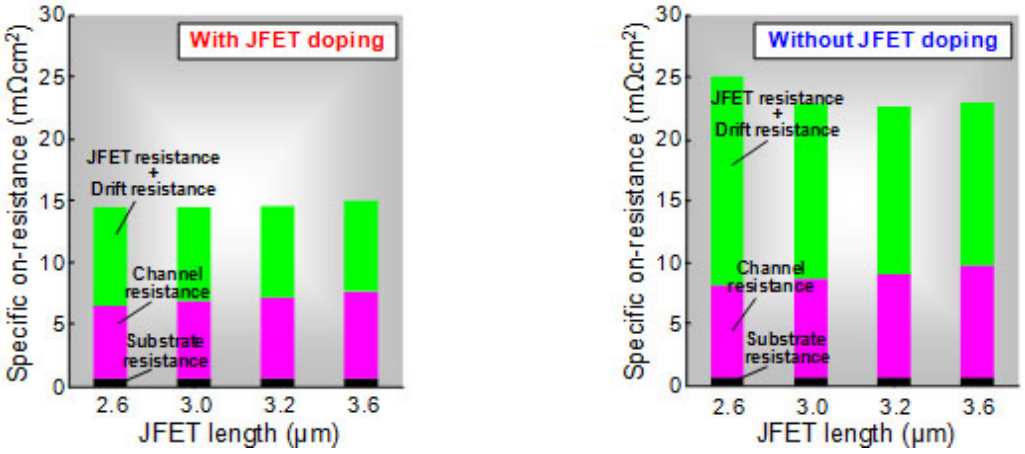
3.2 Temperature dependence of specific on-resistance

Figure 5 shows the temperature dependence of the specific on-resistance of the SiC-MOSFET having a channel length of 0.7 μm, a JFET length of 3.0 μm, and an active area of 4.8×10^{-5} cm^2. The MOSFET with JFET doping exhibits a smaller change in the specific on-resistance than that without JFET doping, namely, an increase from 12 to 23 mΩcm^2 with increasing temperature from room temperature to 175°C. This is due to the decrease in the temperature dependence of the electron mobility in the JFET region, which results from an increased influence of ionized impurity scattering due to the JFET doping. The SiC-MOSFETs have a threshold voltage of about 2 V at room temperature and about 1 V at 175°C, both at a drain voltage of 10 V and regardless of the JFET doping. The JFET doping is a highly effective technique for reducing the MOSFET's on-resistance over a wide temperature range from room to high temperatures.

4. Conclusion

Mitsubishi Electric has developed an SiC-MOSFET with a 3.3-kV blocking voltage to further improve the efficiency of existing industrial and railway vehicle power modules. By means of the JFET doping technique and optimizing device structural parameters, the specific on-resistance has been drastically reduced over a wide temperature range from room to high temperatures. By utilizing these technologies, Mitsubishi Electric has commercialized the world's first railway inverter systems for 1500-V DC catenaries that incorporate 1500-A-rated, high-capacity all-SiC power modules.

Part of this research work was conducted under the "Novel Semiconductor Power Electronics Project Realizing a Low Carbon-Emission Society" commissioned by the New Energy and Industrial



(a) With JFET doping (b) Without JFET doping

Fig. 3 Analysis of specific on-resistance

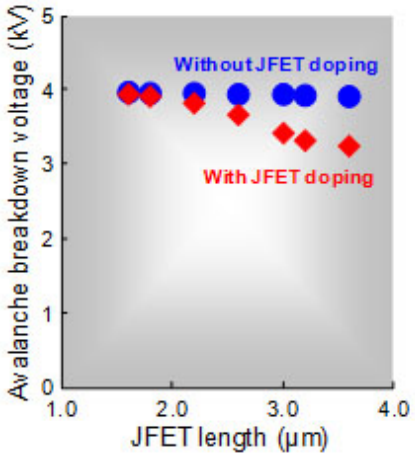


Fig. 4 JFET length dependence of avalanche breakdown voltage

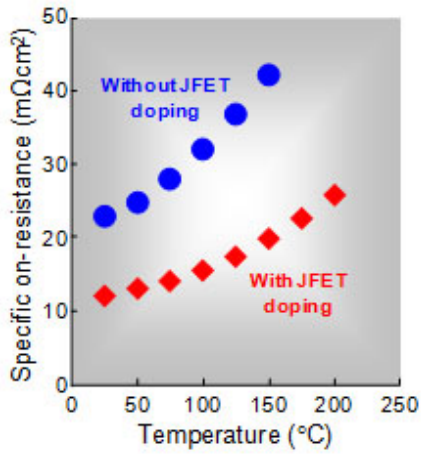


Fig. 5 Temperature dependence of specific on-resistance

Technology Development Organization (NEDO), Ministry of Economy, Trade and Industry.

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Packaging Technologies for High-Temperature Power Semiconductor Modules

Authors: *Yasunari Hino*, Nobuo Yokomura*** and *Hiroaki Tatsumi****

1. Introduction

With growing awareness of the environment and energy saving, power electronics are being applied in increasingly diverse fields, ranging from consumer and industrial inverters to electric railways, automobiles, and solar and wind power generation systems. As the key components of power electronics, power semiconductor modules are required to efficiently control the current, enhance the durability and reduce the size under harsh operating conditions.

Silicon carbide (SiC) devices can operate at high speed with low power loss, making it possible to drastically improve the module performance. In addition, since such devices can also operate at high temperatures, the cooling structure and hence the power semiconductor module can be made smaller.

However, the high-temperature operation of power semiconductor modules imposes a significant engineering challenge for realizing not only high-temperature operation of the chips, but also durability of the materials and package structure at high temperatures.

With this background, Mitsubishi Electric is focusing on developing the packaging structure, materials, and their component technologies toward the launch of high-temperature power semiconductor modules. This paper describes the enhancement of high-temperature durability of bonding materials, as well as the improvement of bonding reliability and service life especially against temperature cycles, both required for the high-temperature operation of power semiconductor modules.

2. Component Technology of Packaging—Sintering Bonding

Since conventional tin (Sn) solder material is expected to exceed the limit at a certain high operating temperature for power semiconductor modules, we examined the sintering bonding technique that utilizes nanosized metal particles covered with organic protective coating and the “depression of melting point” phenomenon, where the melting point lowers as the particle size becomes smaller.

The bonding material consists of silver (Ag) nanoparticles covered with organic protective coating and several solvents determined by considering the sintering dispersibility, viscosity, and drying resistance. When heated, the solvents vaporize and the organic protective coating is thermally decomposed, then the Ag nanoparticles come into contact, and are sintered and bonded together at a temperature that is lower than the Ag’s melting point. Consequently, the bonded zone becomes highly heat resistant, having the intrinsic melting point of metal. This time, we used nanosized Ag particles, which allows the bonding to be completed at a heating temperature similar to that of the conventional Sn solder material, while the bonded zone has a melting point over 900°C.

2.1 Ag Nanoparticle Sintering Bonding Process

As illustrated in Fig. 1, the pasty material that contains dispersed Ag nanoparticles is screen printed on the substrate. The chips are then mounted in place and hot pressed to complete the sintering bonding. Note that we have developed and built prototype chip mounting and hot press machines, which are dedicated

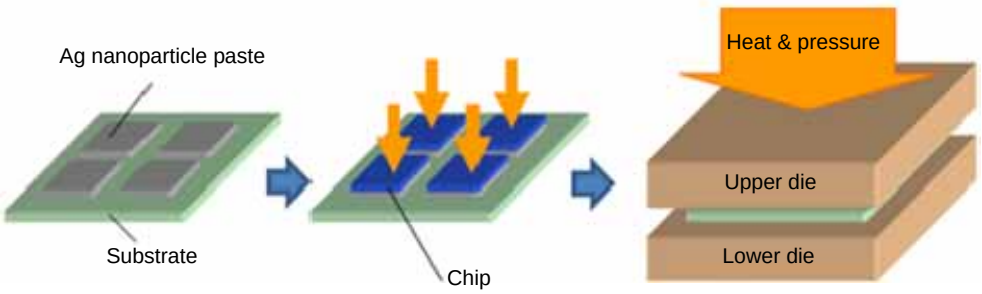

Fig. 1 Ag sintering bonding process

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to the sintering bonding process and capable of mounting and hot pressing multiple chips simultaneously.

Based on the above bonding process steps, basic evaluation samples were fabricated (Fig. 2), and the reliability was verified on the sintering bonding using Ag nanoparticles.

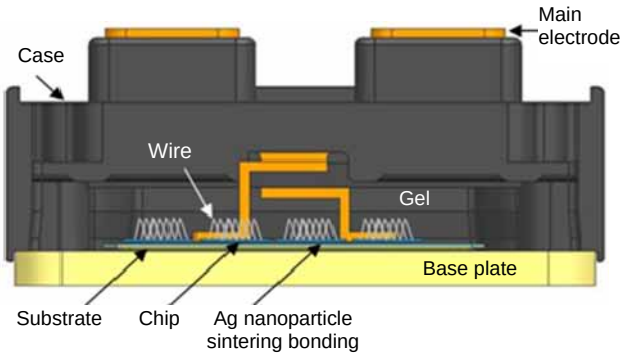


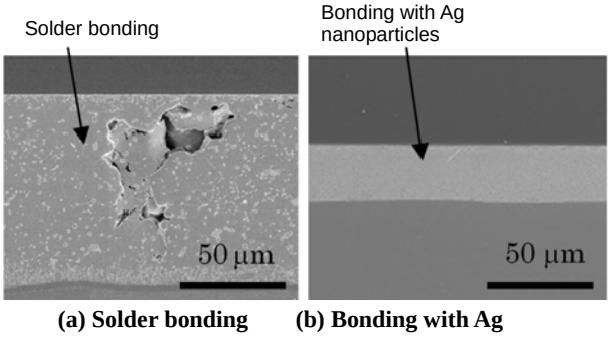
Fig. 2 Structure of high-temperature power semiconductor modules

2.2 Reliability Test

When power semiconductor modules are used for electric railways, automobiles and other applications under severe temperature conditions, cracks may occur in the bonded zone caused by the thermal stress arising from a difference in the thermal expansion of the materials inside the package. Therefore, we have conducted power cycle and temperature cycle reliability tests.

(1) Power cycle test

In addition to the evaluation samples with the Ag nanoparticle material, we have also fabricated reference samples using an Sn-Ag-Cu-Sb solder material. The power cycle tests were conducted on both samples at Tjmax = 175°C and ΔTj = 90 K. As a result, the Ag sintering bonded sample exhibited a power cycle life about 5 times longer than that of the solder-bonded reference sample. After the power cycle test, the bonded zone was examined by cross-sectional observation as shown in Fig. 3. Reticulated cracks can be seen in the solder bonded area, whereas the sintering bonded area remains in a good condition without any crack development. This result indicates that the Ag nanoparticle sintering bonding will not be a controlling factor of the power cycle life.

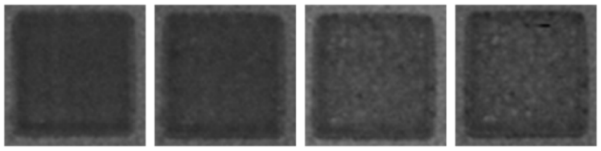


(a) Solder bonding **(b) Bonding with Ag nanoparticles**

Fig. 3 Cross sections after power cycle test

(2) Thermal cycle test

Crack development in the Ag sintering bonded area was examined through the thermal cycle test with a temperature change between −40 and 175°C (ΔT = 215 K). Figure 4 shows the images taken by scanning acoustic tomography (SAT) before the test, and after 300, 600, and 900 cycles. With increasing cycles, very small white regions are observed, but no obvious exfoliation is found in the bonded area. Figure 5 shows the cross-sectional view of the sample after the thermal cycle test (900 cycles). Any noticeable exfoliation developed in the Ag sintering bonded area.



(a) 0 (b) 300 (c) 600 (d) 900 (cycles)

Fig. 4 SAT images after thermal cycle test

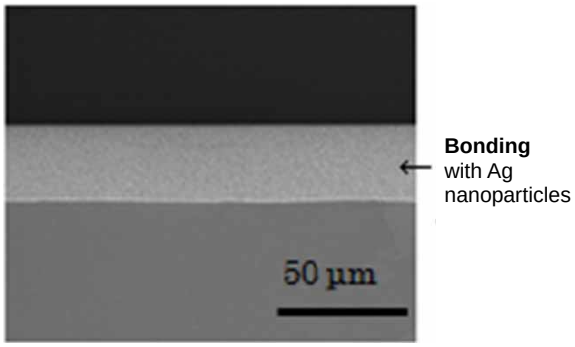


Fig. 5 Cross-section after thermal cycle test

3. Conclusion

This paper has described a bonding technology that utilizes the low-temperature sintering characteristics of nanosized Ag particles. It is a packaging component technology that enables power semiconductor modules to operate at high temperatures. This sintering bonding technology has been verified to exhibit high temperature resistance, high reliability, and long service life. In addition to the Ag sintering bonding technology, it is necessary to develop innovative packaging design, material and manufacturing processes for the commercialization of high-temperature power semiconductor modules.

Based on Mitsubishi Electric's long-accumulated component technologies of packaging and mass production, we will speed up the development toward the launch of next-generation, high-temperature power

semiconductor modules, striving to contribute to environmental protection and energy conservation.

References

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