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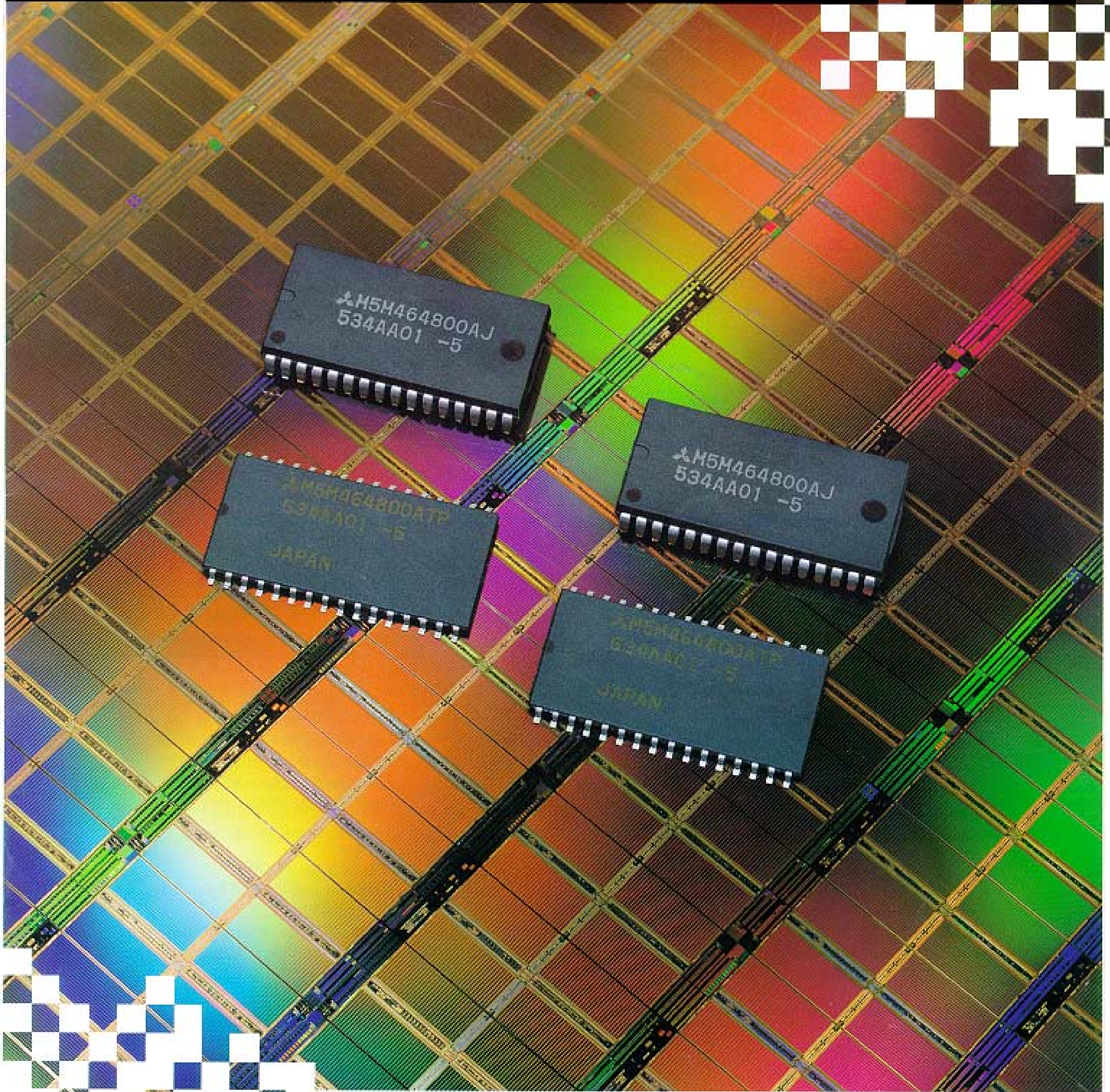
MITSUBISHI ELECTRIC ADVANCE

Semiconductors Edition



MITSUBISHI ELECTRIC

A Quarterly Survey of New Products, Systems, and Technology

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Semiconductors Edition

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MITSUBISHI ELECTRIC OVERSEAS NETWORK

Our cover photograph shows typical semiconductor products arranged on an eight-inch wafer used for 64Mb DRAM devices. The rainbow colors are the result of the regular fine pattern (0.3µm rule), which acts as a diffraction grating. This technology has an important role to play in packing the enormous number of transistors needed to implement systems-on-chip products.

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Vol. 75 Feature Articles Editor

Tsuyoshi Toyama

Editorial Inquiries

Masaaki Udagawa
Planning and Administration Dept.
Corporate Engineering, Manufacturing & Information Systems
Mitsubishi Electric Corporation
2-3-3 Marunouchi
Chiyoda-ku, Tokyo 100, Japan
Fax 03-3218-2465

Product Inquiries

Tsuyoshi Uesugi
Strategic Marketing Dept.
Global Operations Group
Mitsubishi Electric Corporation
2-2-3 Marunouchi
Chiyoda-ku, Tokyo 100, Japan
Fax 03-3218-3597

Orders:
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Foreword

To the Special Edition on Semiconductors

*Dr. Shoji Hirabayashi**

This issue of *Advance* is a special edition devoted to semiconductors, and introduces the latest and most advanced semiconductor devices developed by Mitsubishi Electric. These devices include new products that demonstrate the corporation's technological leadership, including a programmable realtime MPEG2 video decoder and a 2.5Gbps laser modulator, and the technologies used to implement them.

Looking back over the 50 years or so since the invention of the transistor, we see the spectacular growth of a new industry that in recent years has contributed to the downsizing of computers, huge increases in the capacity and speed of communications, and the addition of electronic "intelligence" to a wide range of products. The world is now witnessing the development of a new industrial revolution—a revolution in information-processing technology, exemplified by the dawn of the multimedia age.

Mitsubishi Electric is responding to these dramatic changes in the marketplace by splitting its semiconductor business into four business units: memory devices; microcomputers and ASICs; radio-frequency and optical devices; and power devices. This major reorganization integrates all the necessary functions, from research and development, through production, to marketing, into the four individual business units. Its purpose is to meet market requirements by research and development that rapidly and accurately reflect the trends and changes in customer needs. Our active commitment to the internationalization of development and production is demonstrated in the current program of establishing development and production centers not only in Japan but also in the United States, Europe and Asia, including China.

We trust that our many customers will continue to use and benefit from a succession of new Mitsubishi Electric semiconductor products that will address the widest possible range of application areas. ❑

**Dr. Shoji Hirabayashi (Senior Managing Director) is with the Semiconductor Group.*

An Overview of System LSI Concepts and Technologies

*by Dr. Heihachi Matsumoto**

With five years left in this century, the personal computer market is expanding rapidly, finding new applications in business, home and mobile environments. Computers joined by high-capacity networks will be the basis of the next generation of multimedia communication services. Software and hardware for such systems are already in the prototype stage. This article surveys current trends in the the semiconductor industry, and introduces new concepts in system LSI and system-on-chip technologies.

Semiconductor Devices and System Products

Constant technical advances have made it possible to implement electronic system products that offer high performance, excellent reliability and moderate cost. The relationship between systems and semiconductors is mutually beneficial: Innovative system products boost demand for semiconductors, while performance improvements and functional enhancements in semiconductor devices boost demand for system products.

In the 1990s, personal computers have moved into first place as the number one growth industry as demand for consumer television and VCR equipment has leveled off due to market saturation, and the mainframe market has been shaken by downsizing trends throughout the business world. Cellular phones and other mobile communication products form another major growth industry.

Continued rapid growth is expected in both computers and cellular phone systems, with annual demand for each anticipated to reach 100 million units by the year 2000. These markets will overtake consumer VCR sales, reaching a volume comparable with that of color televisions.

An increasing proportion of electronic products will incorporate semiconductor devices due to the growing popularity of digital processing, increased use of electronic data resources, the ability to reduce equipment dimensions and the development of high-performance mechatronics systems.

Semiconductor Technology Trends

Supported by generous demand for system products, semiconductor products have improved continuously. DRAM devices have been the first to benefit from new manufacturing technologies. For a quarter century, DRAM capacities have quadrupled approximately every three years due to improvements in photolithography resolution. DRAM speed has also improved. Advanced wafer-processing technologies pioneered for DRAM have been subsequently applied to microprocessors and ASICs, microwave devices, optical devices and power devices in a kind of ripple effect. Modern device technologies are gradually making it possible to implement entire electronic systems on a single silicon chip. We refer to this capability as "system-on-chip" technology.

System-On-Chip Development Issues

As device integration scales grew through the 1980s, the enhanced performance of memory, microprocessors and logic devices boosted the performance of the systems they constituted. However, performance increases in larger systems were hampered by speed limitations associated with the long and numerous interconnects between devices. Closely related system functions must be combined on a single chip to eliminate this bottleneck and take full advantage of improvements in transistor switching speeds and higher integration scales. This is precisely the capability that system-on-chip technology provides.

Many technologies must be combined to implement a system-on-chip product: systems and semiconductors, and within semiconductors, fabrication processes for memory, microprocessors and logic. Functions have to be implemented in an optimal way across the fields of software and hardware.

Designing such systems is an immensely complicated task that requires numerous levels of performance qualification. Advances in design, CAD, simulation and testing technologies, and the effective integration of all these technologies are the key to successfully implementing system-on-chip products.

**Dr. Heihachi Matsumoto is with the System LSI Development Division.*

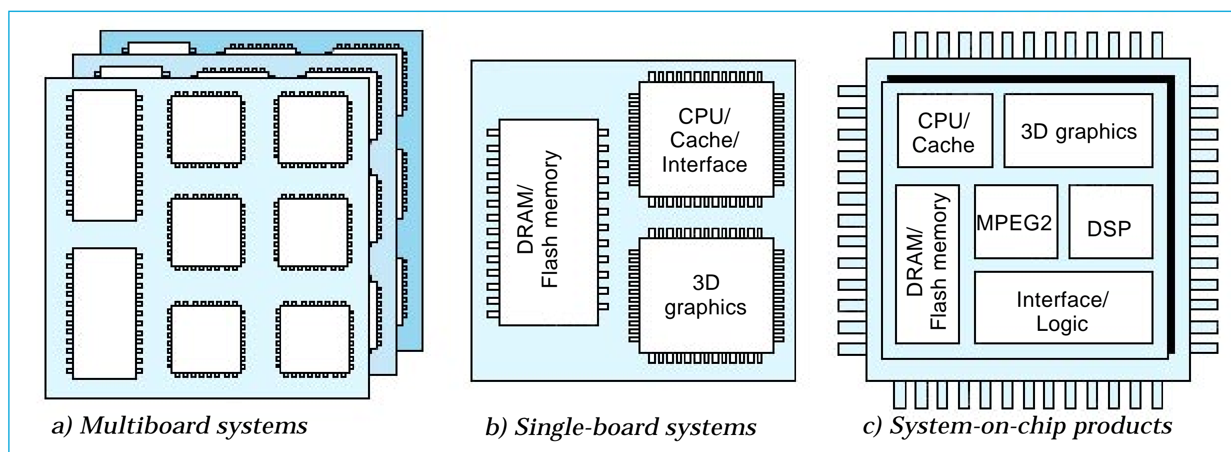


Fig. 1 Evolutionary stages of system-on-chip products.

System LSI Development

System LSI products—chipsets that implement systems as several LSIs—offer an excellent intermediate solution, with performance and cost-effectiveness approaching that of system-on-chip products. Optimally partitioning functions among several devices is a key design issue, and solutions developed for system LSIs will also apply to the design of future system-on-chip products.

Fig. 1 illustrates the evolutionary stages toward system-on-chip products. Vigorous demand for multimedia applications provides much of the incentive for system LSI development.

Hardware manufacturers and service providers are working toward realizing interactive multimedia services that link personal computers and networks and allow people to communicate freely and seamlessly by whatever media is appropriate—voice, text, data, images or full-motion video.

Table 1 lists semiconductor technologies that multimedia-capable systems will require. It is particularly worth noting that network technologies—digital signal compression and decompression, error correction and encryption—will be needed to supplement the computer technologies central to current multimedia applications. Semiconductor devices will be called on to transport digitized audio and video information through telecommunication networks.

Fig. 2 illustrates a systems project underway at Mitsubishi Electric. The Personal Handyphone System (PHS), which offers personal telephone services, was inaugurated in 1995. The corporation has developed a chipset that implements the functionality required for PHS handsets, and in the future, the same functional partitioning will serve as the basis for system-on-chip implementation.

Fig. 3 shows the block diagram of a three-dimensional (3D) graphic processing chipset which will provide functionality for an add-in graphic adapter for desktop personal computers. The 3D graphics processor chipset is piloting technologies for future multimedia graphic applications such as virtual-reality travelogues and high-performance car-navigation systems, as well as arcade games and other educational and entertainment applications.

While semiconductor manufacturers focused on mass production of memory and other com-

Table 1 Multimedia Products and Their Component Semiconductor Devices

Products		Semiconductor devices
Next-generation AV equipment Interactive TV, Digital satellite broadcasts		High-performance, cost-effective microprocessors RISC microprocessors
Personal terminals Personal digital assistants (PDAs), PHS personal cellular phones		Digital signal processors Codecs, Error correcting and encryption products
Prepackaged media CD-ROMs, Digital video discs (DVDs)	➡	High-speed, cost-effective graphic memory CDRAM, SDRAM, 3D-RAM
Other Car navigations systems, TV-based games and educational products		High-capacity, non-volatile memory Flash EEPROM
		Ultrahigh-speed telecommunication networks ATM devices, MMICs, LDs

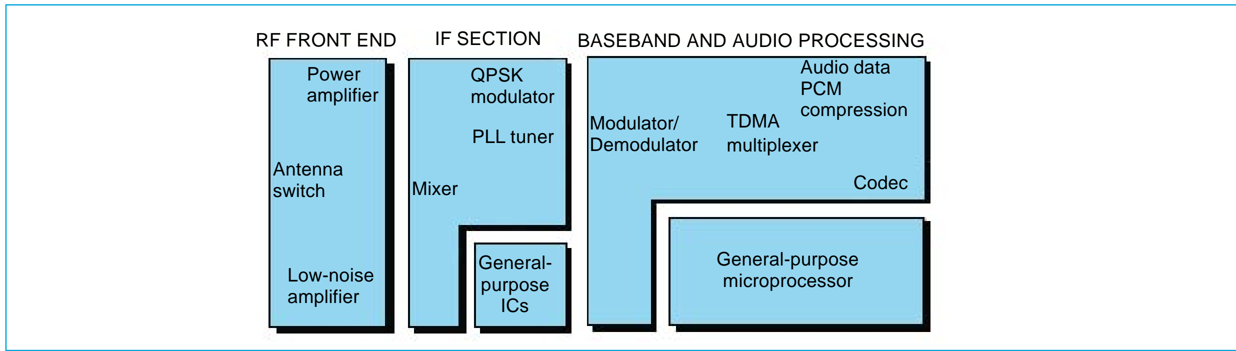


Fig. 2 Functional partitioning of a PHS chipset.

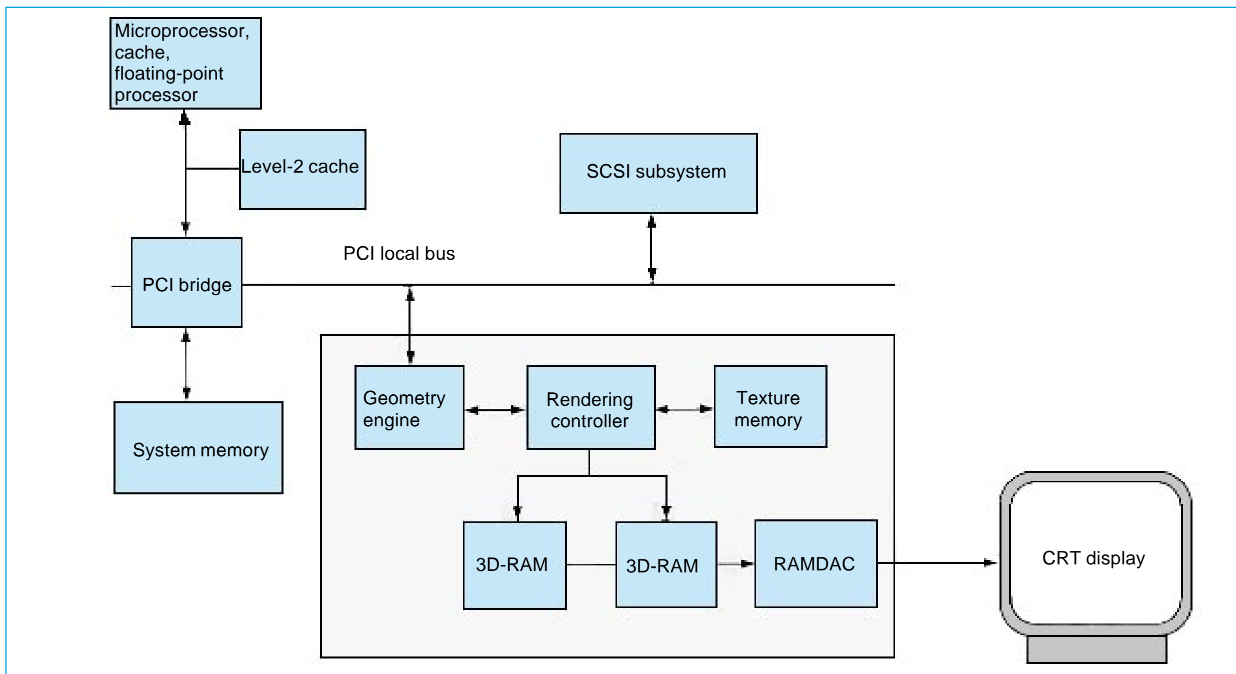


Fig. 3 A 3D graphic system for a desktop computer.

modity devices in the 1980s, the focus has shifted toward the intellectual property value of microprocessors, establishing *de facto* standards for personal computers and their peripherals, and utilizing the enormously powerful integration technologies now becoming available to create truly intelligent subsystems in silicon. If consumers are to accept the next generation of multimedia technologies, products and services, manufacturers will have to create innovative semiconductor devices and system products that provide convenient services of genuine value.

System LSIs and their system-on-chip successors represent an evolutionary step in technology, from semiconductors as commodity devices to semiconductors as a repository, for both hardware and software functions primary to virtually all future electronic equipment. As the possibilities that these technologies offer are explored, the lessons learned will enable the design and implementation of tomorrow's sophisticated electronic system products almost entirely in silicon.

Although system LSIs are only one category among a sometimes bewildering array of semiconductor products, Mitsubishi Electric believes that the evolution of system LSIs will set the future direction of the semiconductor industry. This special issue of *Advance* introduces these and other state-of-the-art semiconductor products, in an excellent sampling of the corporation's comprehensive semiconductor capabilities. ❑

A 256Mb DRAM

by Masaki Tsukude, Takahisa Eimori and Dr. Kazutami Arimoto

The authors have test manufactured a 256Mb dynamic random-access memory (DRAM) device with a 0.25μm design rule. The device features a hierarchical bit-line architecture that dramatically reduces die area. To ensure adequate cell read voltage, it employs a planar stacked-capacitor memory cell with a high-dielectric film in place of conventional silicon-oxide film. The refresh characteristics have been markedly improved by a boosted-sense-ground (BSG) scheme in which the low level of the memory cell is raised slightly above ground.

This article reports on the features of the new DRAM device, as well as the simplified production process and reduced chip area that contribute to lower manufacturing costs.

Development Background

The capacity of DRAM devices has been quadrupling approximately every three years while high-resolution lithography and mass production techniques have brought ever lower costs. DRAMs are a major factor in the reduced size and increased capabilities of current information equipment. DRAMs of 4 and 16Mb capacities are currently under mass production, while at the R&D level, several 256Mb devices were announced at the 1993 IEEE International Solid-State Circuit Conference (ISSCC).[1-3]

When the capacity of DRAM devices is increased, the memory cells must be scaled down in size and require tighter mask alignment, both of which adversely affect the refresh rate. At the same time, equipment manufacturers are demanding memory devices with less exacting refresh requirements. Personal data assistants (PDAs) and notebook computers, for example, require low-power memory with a longer refresh interval.

In general, a higher integration scale reduces the cost per unit memory; however, the manufacture of submicron devices requires a huge investment in production facilities that raises the manufacturing cost. Cost savings are therefore a high priority.

The authors have addressed these issues in the 256Mb device presented here. A low refresh rate has been achieved by employing a high-dielectric film in the memory cells that ensures adequate capacitance and by adopting a BSG scheme.[4] To lower the cost per device, production processes have been simplified by the use of a planar stacked memory cell array. A hierarchical bit-line configuration reduces the die area.

Planar Stacked Memory Cells

The 256Mb DRAM is based on a 0.25μm CMOS process, in which a memory cell with an area of 0.72μm² must provide a capacitance of greater than 25fF. Three-dimensional memory-cell designs with cylindrical or fin shapes are unsuited for this purpose because sufficient capacitor area would require an impractically large number of these shapes or use of thick films in the length direction. The additional processes needed to fabricate these structures would produce steps and edges requiring extremely tight manufacturing tolerances. To ensure adequate alignment in a finer design rule, the photolithography process must keep these steps and other surface irregularities extremely small.

Our planar stacked memory-cell architecture and a high-dielectric film make it possible to manufacture the device with relatively few processes and wide manufacturing tolerances, which contribute to high yields.

High-Dielectric-Constant Film Technology

Fig. 1 shows the construction of a planar memory cell with high-dielectric-constant film. We employed $(Ba,Sr)TiO_3$ (or BST) as the dielectric film. The compound has a dielectric constant of approximately 300 and is free of the high temperature degradation that impairs the performance

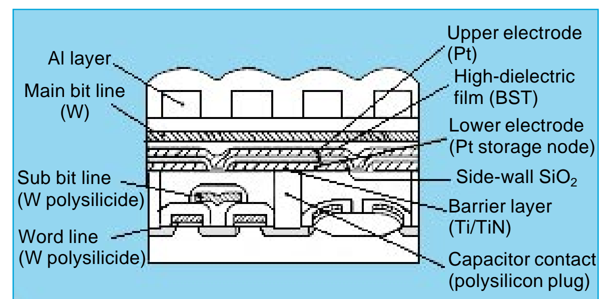


Fig. 1 Cross section of a planar memory cell.

**Masaki Tsukude, Takahisa Eimori and Dr. Kazutami Arimoto are with the ULSI Laboratory.*

of silicon-dioxide film dielectrics.

Thin films are vulnerable to large leak currents that arise from crystal grain effects. We developed a film with both granular and columnar grains that achieves high capacitance combined with low leakage currents. BST films were used to achieve the high-capacitance low-leak performance for our 256Mb DRAM.[5] The capacitor plates are platinum, the lower one deposited over a silicon-dioxide diffusion barrier. We developed appropriate etching technologies for the plate and BST materials.

Boosted-Sense Ground

Two leak paths are the primary determinants of the memory cell refresh characteristics. The first is the leak current through the *pn* junction formed by the storage node's *n* region and the *p* region that is held at the substrate voltage (V_{bb}). It is typically minimized by lowering the substrate voltage, and by reducing the concentration of *p*-type impurities near the junction.

The second is the subthreshold leak current that flows in the channel direction of the memory cell access transistor when the word line is not selected (low level). It is typically minimized by increasing the substrate voltage and by using higher channel doping concentrations to boost the threshold voltage of the access transistor.

Since these mutually exclusive solutions allow little fundamental improvement, we developed an alternative solution, called *boosted-sense ground* in which the low level of the bit lines is raised slightly above the level of the unselected word lines (which are typically at ground level). It is easily implemented by the addition of a simple circuit that raises the sense ground level (see Fig. 2).

Fig. 3 illustrates the basic operating principles. When the word line is not selected in a conventional memory cell, both the source voltage of the memory cell access transistor (the low-level bit line) and the gate voltage with respect to the source (V_{gs}) are 0V (Fig. 3b, A).

The source voltage in the BSG scheme is slightly higher, so that V_{gs} drops to –0.5V (Fig. 3b, B). This reduces the subthreshold leak current without deepening the substrate potential or increasing the channel doping.

To reduce junction leak current, suppose that we use a shallower substrate potential and decrease the doping with *p*-type impurities. This causes the access transistor drain current curve in Fig. 3b to shift from the solid line to the broken line. V_{gs} would be at 0V in a conventional memory cell, and the transition from A to C would cause the subthreshold leak current to increase. In the BSG scheme, the same change in parameters would cause a transition from B to D, holding the threshold leak current constant while reducing the junction leak current. Actual measurements on test devices show that these measures bring a threefold improvement in refresh characteristics.

The BSG scheme also serves to reduce the

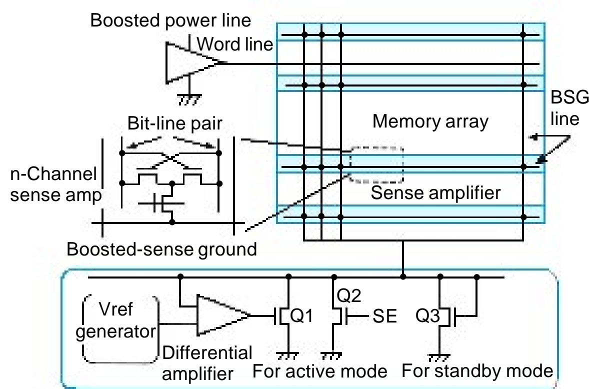


Fig. 2 Boosted-sense ground scheme.

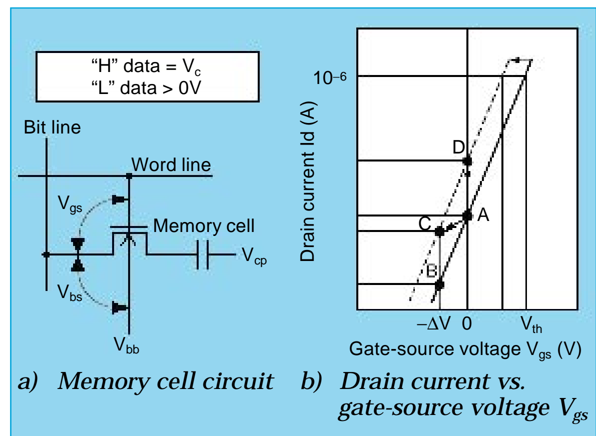


Fig. 3 Principles of boosted-sense ground scheme.

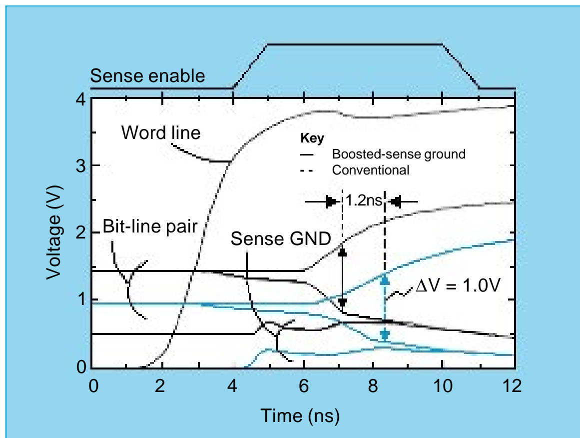


Fig. 4 Simulated waveforms during sensing period.

sensing time because 1.2ns less time is required to build up a 1.0V potential difference between bit lines (Fig. 4). When the sense operation begins, it enters an overdrive state, driving directly to the external ground level.

Hierarchical Bit-Line Architecture

The die area occupied by the sense amplifier is a major factor in 256Mb DRAM design because the number of sense amplifiers increases with the storage capacity and the number of memory cells that can be connected to one bit line is limited by a bit line's parasitic capacitance. We overcame this limitation by developing a hierarchical bit-line architecture that dramatically reduces the number of sense amplifiers and the die area they occupy. Fig. 5 shows the hierarchical bit-line configuration used in our 256Mb DRAM. The main bit lines and sense amplifier are linked in a shared sense amplifier configuration. The main bit-line pair is connected to the sub bit lines through a switching transistor controlled by the block selection signal. Each sub bit line is connected to 32 memory cells to form a sub block. The main bit-line pairs connect to 32 sub blocks, and therefore reach 1,024 memory cells. The number of sense amplifiers is reduced to one-fourth of the number in a 256b/bit-line configuration, which corresponds to a 10% reduction in die area. The total bit-line capacitance (Cb), including the sense amplifier region, is approximately 150fF. This is six times

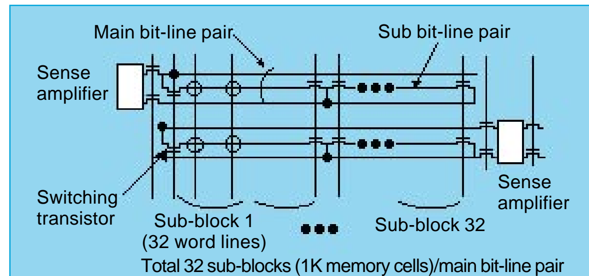


Fig. 5 Hierarchical bit-line architecture.

the 25fF memory cell capacitance (Cs), which leaves ample potential difference for reading the memory cell.

Test Results

Fig. 6 shows a micrograph of a test-manufac-

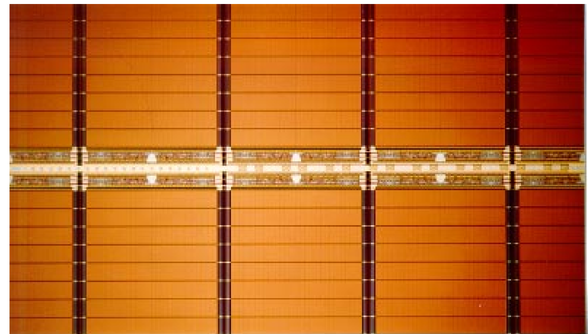


Fig. 6 Micrograph of a 256Mb DRAM.

Table 1 Device Specifications

Fabrication process	0.25μm CMOS with KrF excimer laser
Isolation	Modified LOCOS
Memory cells	
Planar cell size	0.6 x 1.2μm (0.72μm²)
Cell dielectric film	$(Ba,St)TiO_3$
Characteristics	C_s = 25fF, T_{eq} = 0.47nm, leakage current < 2×10^{-7}A/cm²
Interconnections	2 polysilicide, 1 Al
Die size	13.32 x 22.84mm (304mm²)
Power supply	3.3V external, 2.5V for peripheral circuits, 2.0V for memory array
Access time	t_{RAC} = 34ns with V_{cc} = 3.3V, RT Active current 62mA (tc 90ns)
Standby current	60μA
Refresh cycles	16,384

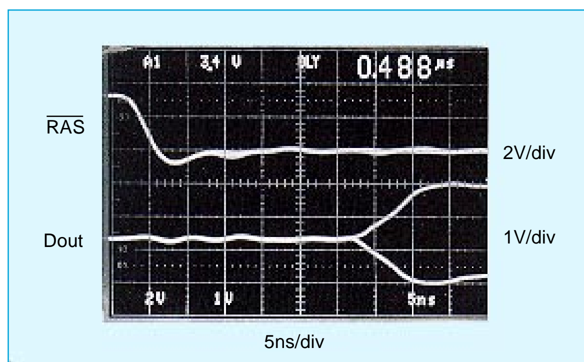


Fig. 7 Operating waveforms.

tured 256Mb DRAM. It is divided into eight 32Mb blocks arranged in two rows of four blocks separated by the row decoder, a configuration that reduces the interconnect length. Due to the hierarchical bit-line architecture, the overall die size is reduced to just 304mm² despite use of a standard 0.72µm² memory cell. The 3.3V external power supply is reduced to the 2.5V operating voltage by an internal regulator. The BSG scheme means that the memory cell array operates at 2.0V, which lowers power consumption without sacrificing operating speed. Table 1 lists the principal specifications. Fig. 7 shows output waveforms during operation at 3.3V and 25°C.

A trio of innovations—the boosted-sense ground scheme, hierarchical bit-line architecture and an improved high-dielectric planar stacked memory cell capacitor—make this 256Mb DRAM amenable to mass production at high yield and relatively low cost. Economic advantages of a small die area and simplified manufacturing process are accompanied by improved refresh characteristics that guarantee a market for this innovative device.❑

References

1. Hasegawa, T., Takashima, D., Ogiwara, R., Ohta, M., Shiratake, S., Hamamoto, T., Yamada, T., Aoki, M., Ishibashi, S., Oowaki, Y., Watanabe, S. and Masuoka, F. "An Experimental DRAM with a NAND-Structure Cell." ISSCC Digest of Technical Papers, pp. 46 – 47, 1993.
2. Kitsukawa, G., Horiguchi, M., Kawajiri, Y., Kawahara, T., Akiba, T., Kawase, Y., Tachibana, T., Sakai, T., Aoki, M., Shukuri, S., Sagara, K., Nagai, R., Hasegawa, N., Yokoyama, N., Kisu, T., Yamashita, H., Kure, T. and Nishida, T. "256Mbit DRAM Technologies for File Applications." ISSCC Digest of Technical Papers, pp. 48 – 49, 1993.
3. Sugibayashi, T., Takeshima, T., Naritake, I., Matano, T., Takada, H., Aimoto, Y., Furuta, K., Fujita, M., Saeki, T., Sugawara, H., Murotani, T., Kasai, N., Shibahara, K., Nakajima, K., Hada, H., Hamada, T., Aizaki, N., Kunio, T., Kakehashi, E., Masumori, K. and Tanigawa, T. "A 30ns 256Mbit DRAM with a Multi-Divided Array Structure." ISSCC Digest of Technical Papers, pp. 50 – 51, 1993.
4. Asakura, M., Ohishi, T., Tsukude, M., Tomishima, S., Hidaka, H., Arimoto, K., Fujishima, K., Eimori, T., Ohno, Y., Nishimura, T., Yasunaga, M., Kondoh, T., Satoh, S., Yoshihara, T. and Demizu, K. "A 34ns 256Mbit DRAM with a Boosted-Sense Ground Scheme." ISSCC Digest of Technical Papers, pp. 140 – 141, 1994.
5. Eimori, T., Ohno, Y., Kimuta, H., Matsufusa, J., Kishimura, S., Yoshida, A., Sumitani, H., Maruyama, T., Hayashide, Y., Moriizumi, K., Katayama, T., Asakura, M., Horikawa, T., Shibano, T., Itoh, H., Sato, K., Namba, K., Nishimura, T., Satoh, S. and Miyoshi, M. "A Newly Designed Simple-Stacked Capacitor Cell with High-Dielectric Constant Film for 256Mbit DRAMs." IEDM Digest of Technical Papers, pp. 631 – 634, 1993.

A Second-Generation 1Mb Synchronous Burst SRAM

*by Ryuichi Kosugi and Minoru Senda**

Mitsubishi Electric has developed a second-generation 1Mb synchronous burst SRAM for applications with high-speed, low-voltage microprocessors. It is configured as 32K x 32b, operating on a 3.3V power supply with 2.5 or 3.3V I/O buffers. It is implemented in 0.4µm CMOS and operates at speeds up to 150MHz with low maximum power dissipation of 290mA.

General Description

All I/O registers are internal to enable pipelined operation. Capabilities include simultaneous 32b write, 8b write, linear and interleaved burst sequences, power-down by snooze and chip select, and power-down on suspend-burst operation of read cycle. The 100-pin QFP/LQFP package has a body size of 14.0 x 20.0mm with a 0.65mm lead pitch.

Process Technology

The device is implemented in a 0.4µm CMOS process with three layers of polysilicon and two of aluminum. The first Al layer is used for the memory cell bit lines, giving the device low-resistance, high-speed data-transfer capabilities. The CMOS transistor employs a 10nm gate oxide layer and a 0.4µm gate length. Its high drive capability and reduced gate capacitance support high-speed operation.

Layout

Fig. 1 shows a block diagram. Sixteen data I/O circuits flank the left and right sides of the device, while blocks for address and control circuitry are placed above and below the memory cell array. Each of the four, 256Kb memory blocks is configured as 512 rows x 512 columns. Separate power supplies are provided for the I/O buffers and the internal circuitry. Noise immunity is enhanced by providing a separate power supply circuit for each of the four I/O buffer circuits.

Memory Cell Data Bus

P-channel transistors supply V_{cc} to bit lines to ensure operation under low-voltage power supply. In addition, we have made the memory-cell sense operation faster by using switching transistors to equalize complementary bit lines immediately prior to read, and by lowering the parasitic capacitance, which we accomplished by separating the write driver output lines from the sense amplifier input lines.

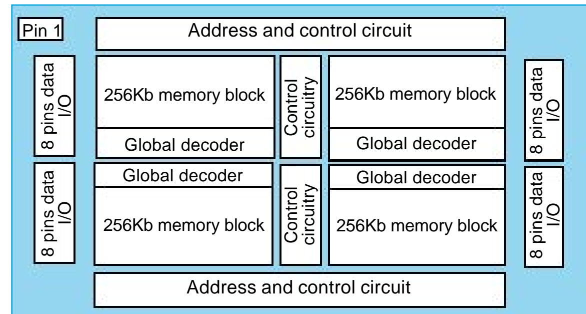


Fig. 1 Circuit block layout.

Decoder Method

We employed an original divided word-line configuration for word-line selection. This system dramatically lowers the column current by reducing the number of word lines active at any one time. We placed the input register circuit in the predecoder circuit in order to optimize the setup and hold time with respect to the clock signal of each input signal. The lowest address (which has a low load) is used, speeding operation of the burst-mode counter circuit.

I/O Buffers

The back gates of the p-channel transistors on the input buffer and the pull-up side of the output buffer are connected to V_{ccQ}, the I/O buffer power supply. This reduces the effective gate capacitance so that high-speed switching is possible even with a low V_{ccQ} value.

Applications

Fig. 2 shows a 256KB cache system using two of the new 1Mb SRAMs. No external burst counter is needed, allowing the address lines to be tied directly to the CPU. This has the effect of lowering the component count and reducing power dissipation. Fig. 3 shows the timing diagram. A conventional SRAM requires nine clock cycles (3-2-2-2) per burst operation, while the synchronous burst SRAM accomplishes the transfer in just six clock cycles (3-1-1-1), a time savings of 33%.

**Ryuichi Kosugi and Minoru Senda are with the Memory IC Division.*

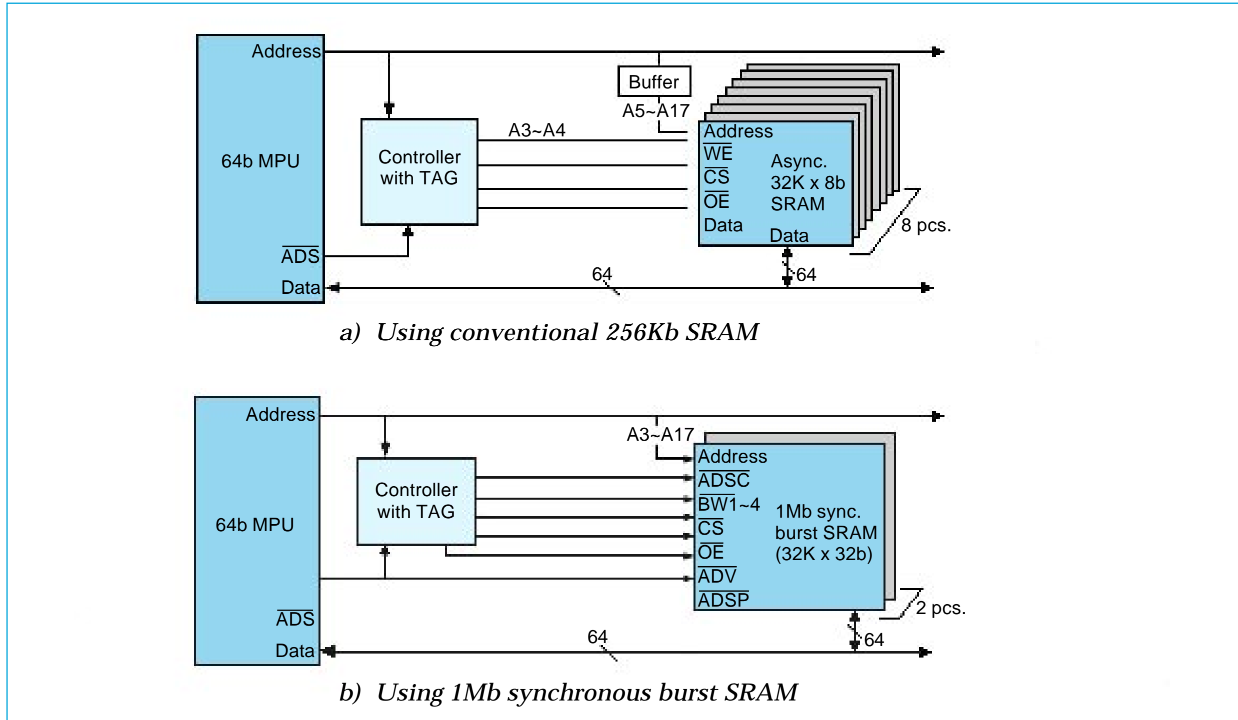


Fig. 2 Typical cache systems.

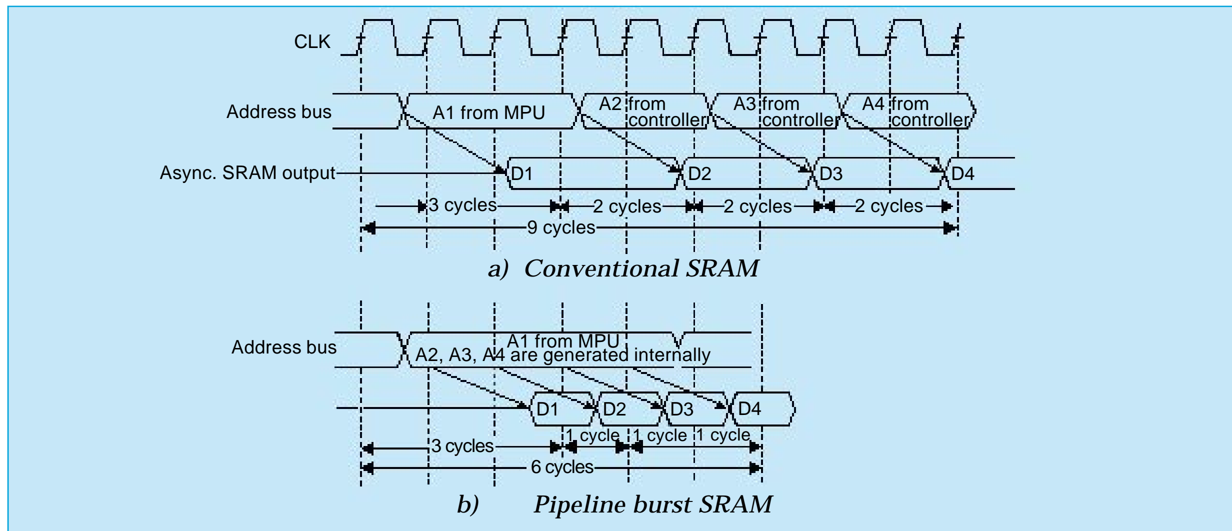
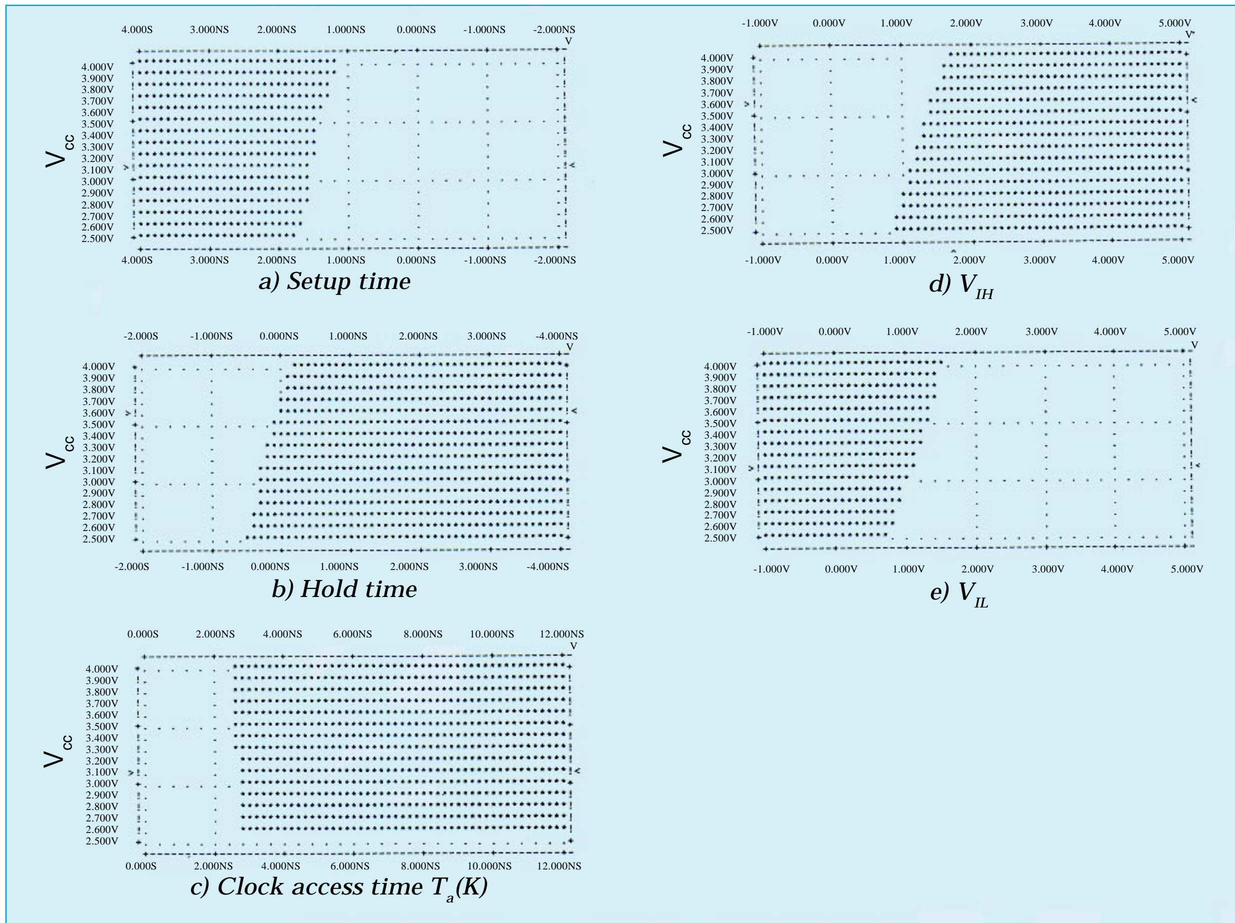


Fig. 3 Timing diagrams.

Electrical Characteristics

Fig. 4 shows the effect of supply voltage on the device characteristics. When V_{ccQ} is 2.5V, the setup time is 1.6ns, the hold time 0.0ns and the clock access time 2.8ns, providing an adequate speed margin for direct coupling to a 150MHz micro-processor. Input voltage levels V_{IH} and V_{IL} of 1.4 and 1.2V, respectively, satisfy the requirements of the 2.5V I/O interface.



a) Setup time

b) Hold time

c) Clock access time $T_a(K)$

d) V_{IH}

e) V_{IL}

This second-generation synchronous burst SRAM offers ease-of-use and enhanced performance in addition to a higher integration scale that allows two of these devices to replace eight 256Kb SRAMs. ❑

The M32R/D, A 32b RISC Microprocessor with 16Mb Embedded DRAM

*by Hideo Tsubota and Toshifumi Kobayashi**

Mitsubishi Electric has developed an original 32b RISC microprocessor core (M32R) with digital signal processing (DSP) capabilities, as well as a monolithic device for "system-on-chip" multimedia applications (M32R/D) that combines the M32R processor with 16Mb of on-chip DRAM. By combining processor and memory functions, the M32R/D achieves enhanced performance, low cost and low power consumption.

Background

Microprocessor applications in multimedia equipment are growing rapidly, including digital satellite broadcast terminals, personal digital assistants (PDAs), car navigation systems, Internet terminals and digital still cameras. These embedded applications demand low power consumption alongside high-performance processing. Cost-effective single-chip application-specific standard product (ASSP) solutions to the processing requirements of these applications (also called "system-on-chip" solutions) require a compact microprocessor core.

The M32 Series

Fig. 1 shows the processing capabilities of the M32R, and future processors and application targets for these chips. The M32RX will be of the dual-issue type, and the M32S will integrate a multiprocessor on a single chip.

The M32R/D is the world's first device to integrate a high-performance microprocessor with a large-capacity 16Mb DRAM, a 2KB cache and a memory controller. Instead of peripheral circuits providing application-specific capabilities, the M32R/D provides all relevant capabilities, including large memory capacity, on a single chip. Table 1 lists the specifications of this innovative device.

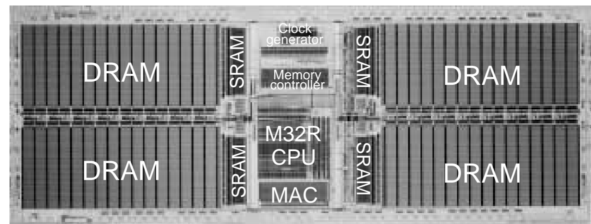
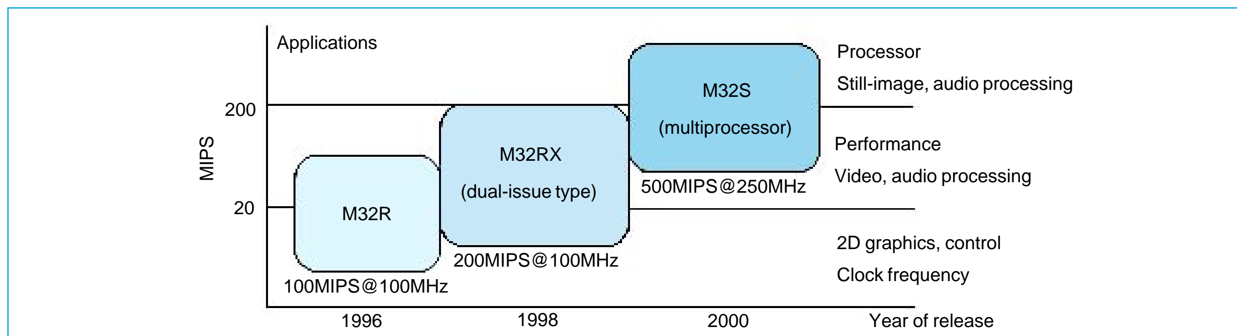


Fig. 2 Die photograph.

Table 1 M32R/D Overview

CPU core	32b RISC
Performance	52.4MIPS at 66.7MHz, Dhrystone V2.1
Instruction	83 including 16 and 32b lengths
General-purpose registers	32b x 16
Pipeline	5-stage
Clock	66.7MHz internal, 16.7MHz external
Memory	16Mb DRAM, 2KB cache
Internal memory bus	128b, operates at clock frequency
Peripheral circuits	32 x 16b multiply and accumulator, memory controller
External bus	24b address, 16b data
Power supply	3.3V
Die size	19.9 x 7.7mm
Transistors	343,000 (not including DRAM)
Process	0.45µm CMOS, 4 polysilicon, 2 metalization
Package	80-pin plastic QFP



*Hideo Tsubota is with the System LSI Laboratory and Toshifumi Kobayashi with the Microcomputer & ASIC Division.

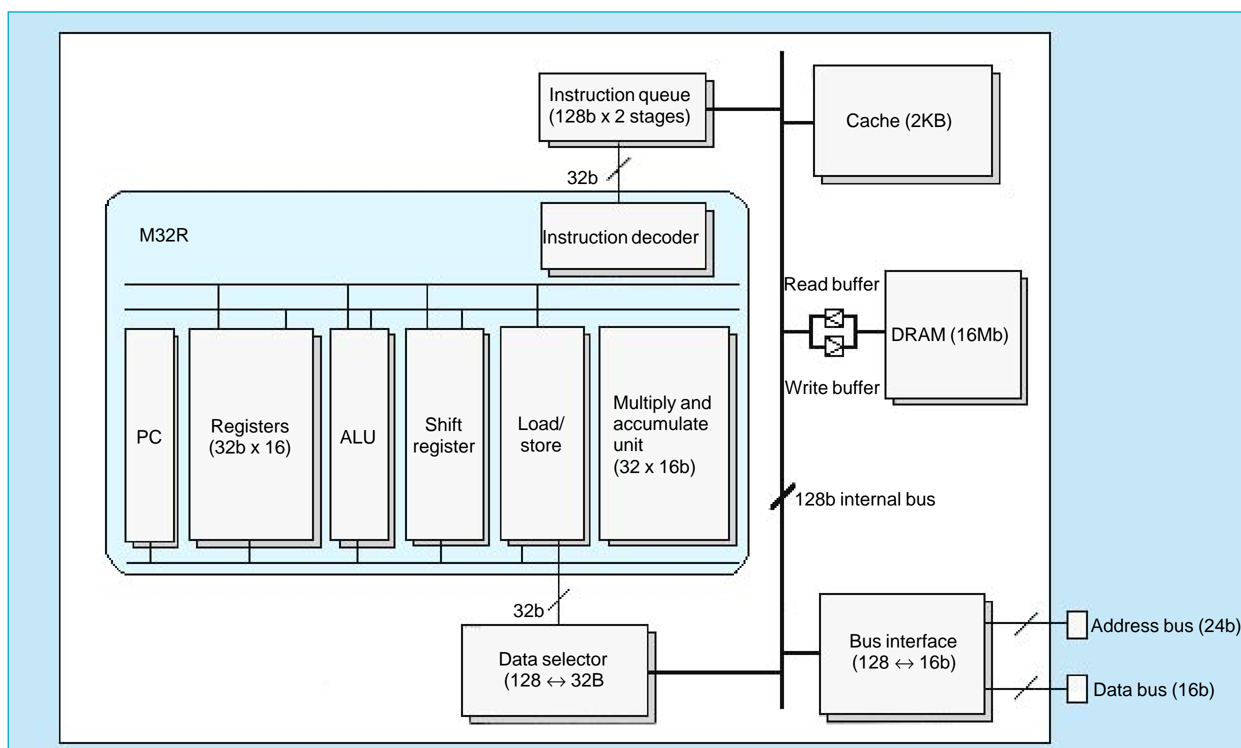


Fig. 3 M32R/D block diagram.

Die Layout

Fig. 2 shows a micrograph of the M32R/D die. The 19.9 x 7.7mm die includes 343,000 transistors in addition to 16Mb of DRAM. To keep inter-connects short, the M32R microprocessor, multiply and accumulate unit, bus interface, clock generator and other peripheral circuits are placed in the center, surrounded by four banks of byte-organized DRAM and SRAM cache.

HIGH-PERFORMANCE 128b INTERNAL BUS. As shown in Fig. 3, the single-chip design of the M32R/D allows use of a 128b data bus between the microprocessor, DRAM and cache, which eliminates memory-access bottlenecks. This design also allows both the microprocessor and bus to operate at a high frequency of 66.7MHz, giving the device an outstanding 52.4MIPS performance using the Dhrystone V2.1 benchmark.

LOWER POWER CONSUMPTION WITH 16b EXTERNAL BUS. Since the DRAM necessary for any application is on-chip, the external bus is needed only for connecting to ROM and ASICs. This 16b data bus operates at one-fourth the internal clock frequency, which lowers the power consumption required for driving the I/O lines. External memory accesses are also few, so that much less power is consumed than in a conventional configuration consisting of separate microprocessor, cache and DRAM chips. The on-chip DRAM also features a self-refresh mode that operates when the microprocessor is in sleep mode.

TWO CACHE MODES FOR VARIOUS MEMORY CONFIGURATIONS. The on-chip cache provides on-chip DRAM access in one clock cycle for cache hits and five clock cycles for cache misses. The direct-mapped cache has two operating modes.

1. The on-chip DRAM caching mode assumes that the on-chip DRAM is utilized as the main memory, and caches instructions and data from the on-chip DRAM. The cache operates as stored-in cache for data, thus minimizing traffic between cache and DRAM.
2. The external ROM caching mode assumes that external ROM is utilized for program memory and on-chip DRAM for data memory, and caches instructions from the external ROM. The bus interface unit has a 128b buffer for burst transfers, allowing rapid transfers when burst-mode ROM is used.

The M32R Microprocessor Core

A RISC architecture provides high performance in a compact die area, leaving sufficient area to integrate 16Mb of DRAM on the chip. Memory access is accomplished by load and store instructions, and all arithmetic is performed using registers. There are 83 basic instructions, and 16, 32b general-purpose registers.

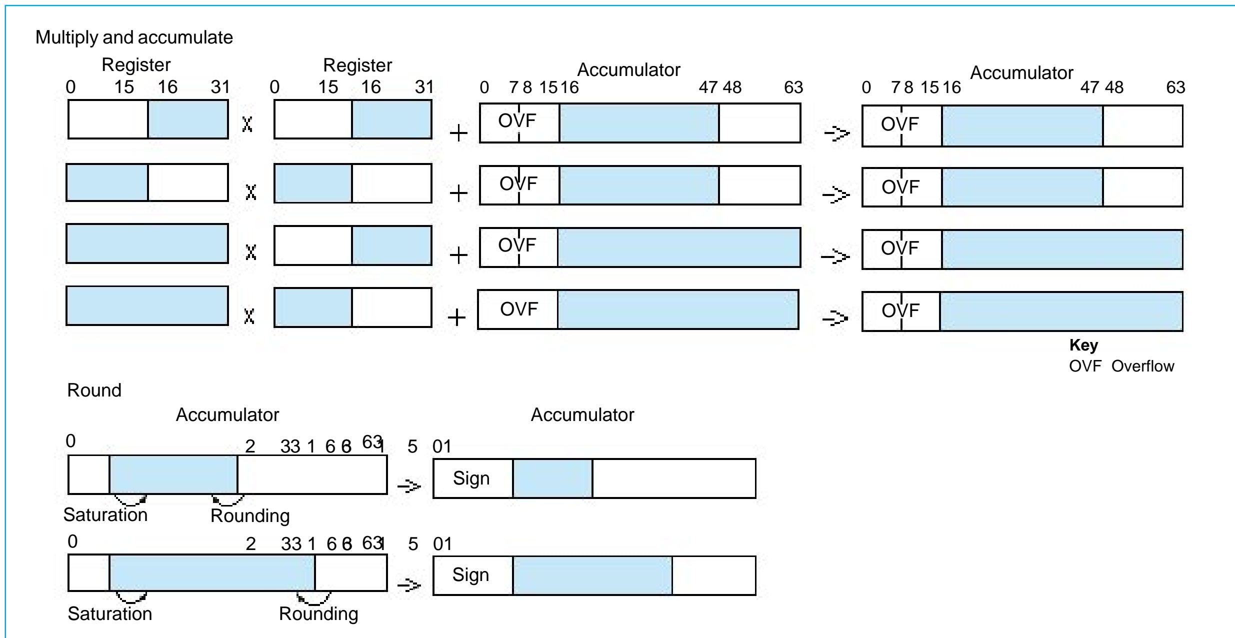


Fig. 4 Multiply and accumulate instructions.

CODING EFFICIENCY. The M32R supports 16 and 32b instruction formats. The 16b format results in more compact code. Instructions are executed in 32b units with considerations that will enable future devices to execute two 16b instructions in parallel. Data transfers are accelerated by compound instructions such as "load and update address" and "store and update address" that execute in a single step.

FIVE-STAGE PIPELINE. The M32R employs a five-stage pipeline for retrieve, decode, execute, memory access and write back. Not only load/store and register arithmetic, but almost all instructions, including compound instructions, are executed in a single clock cycle. Instructions reach the execute stage in the order they are retrieved. However, memory access can introduce wait states that delay subsequent register arithmetic. This penalty is eliminated by providing a capability for out-of-order completion that allows register arithmetic to take priority.

MULTIPLY AND ACCUMULATE. Multimedia applications require DSP capabilities. The M32R provides this high-speed processing through two special functions. A high-speed 32 x 16b multiplier combined with a 56b accumulator enables the M32R to complete 32b integer multiplication in just three clock cycles. Fig. 4 shows four multiply and accumulate functions available for 56b data and instructions for rounding the accumulator result to 16 or 32 bits. All of these instructions execute in a single cycle. These fast-executing functions, combined with the compound instructions for load/store and address update, provide the performance needed for high-speed data encoding and decoding, filtering, and other typical DSP tasks.

Optimizing C Compiler

An optimizing C compiler was developed in parallel with the microprocessor, and utilized to evaluate the instruction set. The results were then applied to architecture design. This allowed a reduction in microprocessor size without degrading performance.

INSTRUCTION ALIGNMENT. While the 16b instructions result in more compact code, the need to simplify the instruction decoder led us to require that 32b instructions be aligned at word boundaries. Fig. 5 shows how the compiler minimizes the penalty associated with this design. For word alignment of instructions, a null instruction (NOP) should be inserted following the SLLI instruction. A compiler changes the execution order of the SLLI and LD24 instructions, which eliminates the NOP instruction

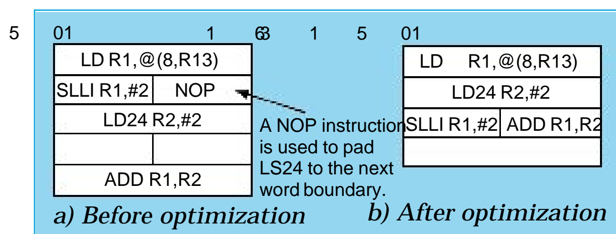


Fig. 5 Instruction scheduling for word alignment.

and yields more compact code.

INSTRUCTION SCHEDULING. If a memory load/store instruction is delayed, the M32R will usually execute a subsequent register arithmetic instruction out of sequence. However, if the following instruction involves one of the operands loaded by the previous instruction, the pipeline will be stalled until the memory access is complete. When an LD instruction is followed by an SLLI instruction without optimization (Fig. 6a), all subsequent processing must wait until data is loaded into register R1. The compiler minimizes this delay by scheduling in ADD and LD24 instructions that can be performed in the interim (Fig. 6b), thereby minimizing the cost of long-latency instructions. The scheduling algorithm is executed in a code unit with only one entry point and one exit point.

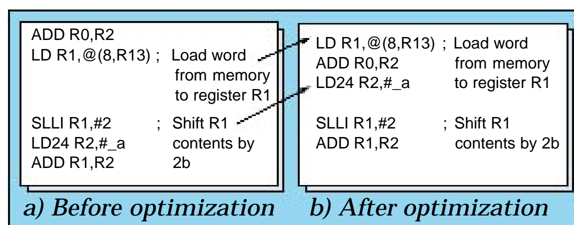


Fig. 6 Instruction scheduling for load latency.

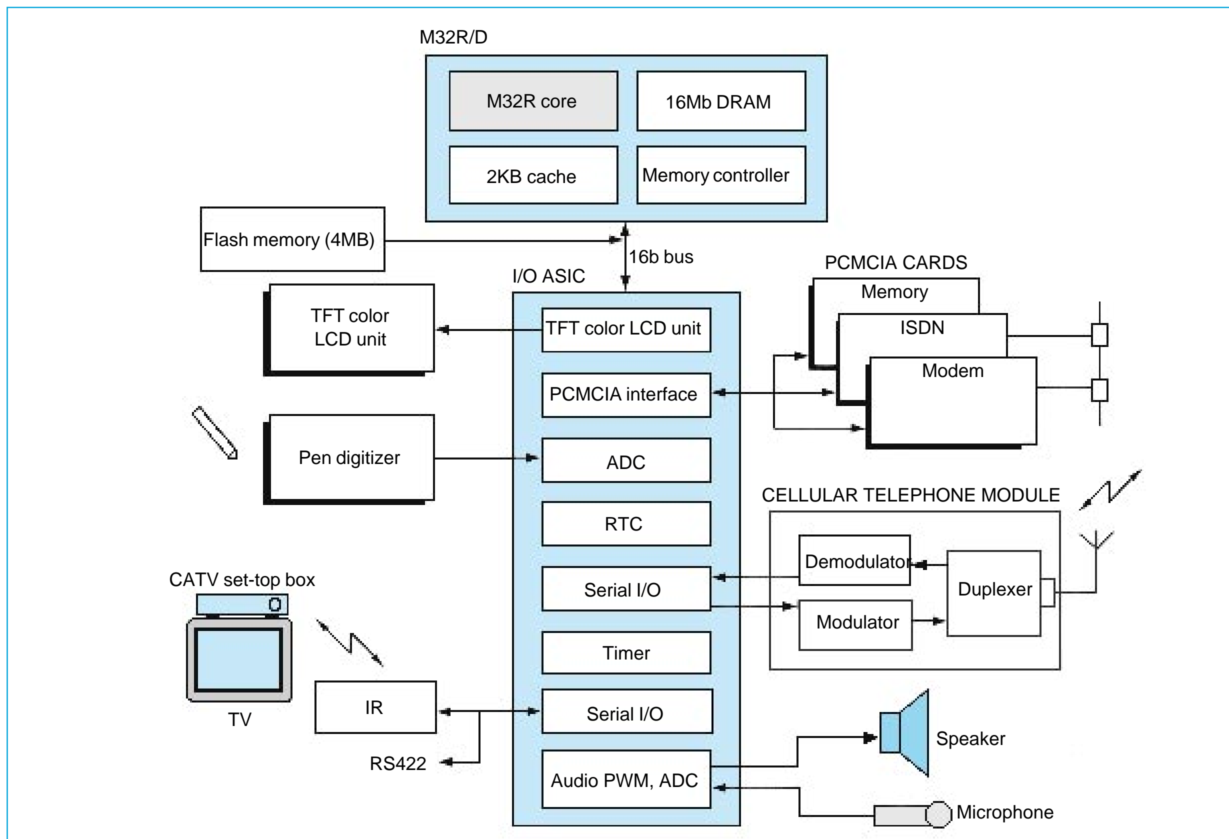


Fig. 7 A typical PDA application.

Application

Fig. 7 shows an application of the M32R/D in a PDA. No external memory or memory controller is required. The entire application can be implemented by just three devices: the M32R/D, a program ROM and an ASIC with peripheral circuitry for the LCD controller, PCMCIA interface and timer functions.

By combining a microprocessor with large-capacity DRAM on a single chip, the M32R/D simultaneously realizes high performance, lower power dissipation and low cost. With these advantages, the M32R/D and its successors promise to play a major role in the multimedia revolution❑

New M16C Series 16b Microcomputers

*by Takashi Yamasaki and Kazuo Nakamura**

The new M16C/60 Series microcomputers use a new architecture featuring powerful arithmetic processing capabilities, efficient ROM use and powerful, advanced noise-immunity. We report on these features and the first product in the series, the M30600M8-XXXFP.

Development Objectives

The M16C/60 Series was developed to offer users the following features: a new instruction set with enhanced arithmetic processing abilities; improved C execution efficiency; low-voltage, low-power operation; enhanced noise immunity; reduced radiated noise emissions; debugging support; and competitive pricing.

General Description

The M30600M8-XXXFP/GP is a monolithic microcomputer incorporating a M16C CPU as its core. Fig. 1 shows a die micrograph and Table 1 the main specifications. The device operates at $f_{(Xin)}$ = 10MHz max. over V_{cc} = 4.0 ~ 5.5V and 7MHz (with 1 wait) over V_{cc} = 2.7 ~ 5.5V. Although the operating frequency is not high, more processing is accomplished per clock cycle, giving the device about six times the processing power of 7700 Series microcomputers operating at the same frequency.

The device includes 64KB of ROM and 10KB of RAM. The large RAM capacity was selected to suit one of our first applications, a minidisc player. The internal timers and serial I/O support are based on the proven peripheral circuits of 7700 Series microcomputers with some improvements. The 10b analog-to-digital converter (ADC) has sample and hold functions, and can complete a conversion in 3.3μs at 10MHz while performing successive comparison approxima-

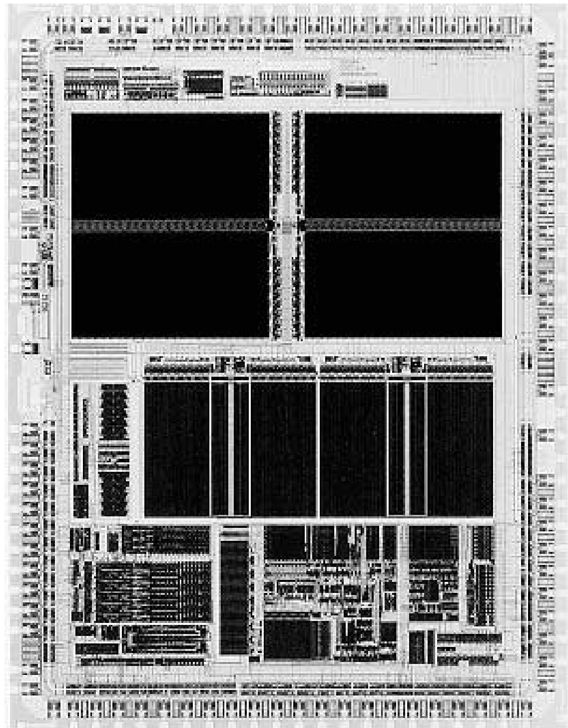


Fig.1 The M30600M8 die.

Table 1 M30600M8-XXXFP/GP Specifications

CPU core	Original 16b microprocessor
Memory	64KB ROM, 10KB RAM
Basic instructions	91
Instruction execution time	100ns min. at 10MHz
Power supply	10MHz, no wait at 4.0 ~ 5.5V; 7MHz, 1 wait at 2.7 ~ 5.5V
Power dissipation	22mW typ. at Vcc = 3V, 7MHz, 1 wait
Interrupts	17 internal, 5 external, 7 priority levels, non-maskable interrupt, Key-on wake up
General-purpose 16b timers	5+3
UARTs	2 (also support synchronous operation)
CRC calculation circuit	CCITT compliant 10b
ADC	(8+2) channel input 8b
DAC	2 channels
DMA controller	2 channels, 15 request sources
Watch dog timer	Provided
Programmable I/O	88 (one is input only)
Memory expansion	Up to 1MB
Chip-select outputs	4
Clock generator circuit	2 built-in (require external ceramic or quartz crystal resonator)
Operating temperature	–40 ~ 85°C
Fabrication process	CMOS
Package	100-pin plastic-molded QFP (FP: 0.65mm pitch, GP: 0.5mm pitch)

**Takashi Yamasaki and Kazuo Nakamura are with the Microcomputer & ASIC Division.*

tion. The peripheral functions have been further enhanced with the addition of a two-channel direct memory access (DMA) controller.

Seven interrupt levels are provided, including such new functions as a key-on-wakeup interrupt and an address-match interrupt. The address-match interrupt is an important innovation because it allows a faulty mask ROM program to be corrected with external EEPROM. A number of design improvements have led to extremely low 6mA power dissipation when the microcomputer operates at 3V and 7MHz with wait states. The device package is a 100-pin quad flat package (QFP) with a 0.65mm lead pitch. A similar package with a 0.5mm lead pitch will also be available.

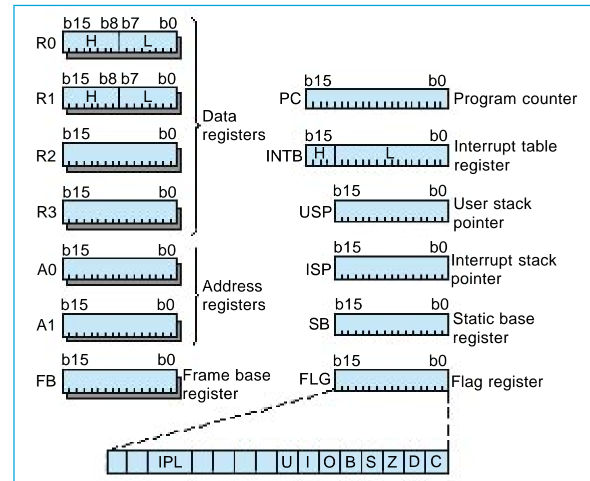


Fig. 2 Register set. Note that registers R0 ~ R3, A0, A1 and FB are duplicated in two banks.

CPU Architecture

REGISTERS. Fig. 2 shows the M16C register set. The M16C has six general-purpose registers (R0 ~ A1), two base registers (SB, FB) and six dedicated registers. The general-purpose registers can be used to hold operands for arithmetic operations, and A0 and A1 can be used as address registers. The 16b registers R0 and R1 can be handled as four 8b registers (R0L, R0H, R1L, R1H).

SB is used as a static base register for data, so that each program module can define static data and access it with a small displacement. The 20b program counter gives programs a 1MB linear address space.

FB is provided as a stack-frame base register. EXNTR and EXITD instructions are provided to create and remove stack frames, enabling efficient access to local variables in subroutines in C and other high-level languages.

USP is the user stack pointer, and ISP the interrupt stack pointer. When an interrupt occurs, PC and FLG are saved on the stack and ISP is used as the stack pointer. INTB specifies the base address of the interrupt vector table, allowing the table to be placed at any location in ROM or RAM.

The C, Z, S and O bits in the FLG register are flags for carry, zero and overflow. O allows comparison of both signed and unsigned integers. The D bit is the flag for the single-step interrupt. I is the interrupt mask bit, and IPL is three bits defining the interrupt priority level.

Two banks of registers are provided for R0 ~ A1 and FB. The B bit in the FLG register selects the bank in use. This speeds processing for the highest priority interrupts. The U bit selects between ISP and USP when no interrupt is set.

OP CODES AND ADDRESSING. Fig. 3 shows the four types of OP codes and addressing modes of the M16C. Types 1 and 2 are 8b instructions. While they have only limited addressing modes, they offer efficient ROM access during port control and other 8b operations. Type 1 codes specify R0L and R0H as the destination, and R0L/R0H or memory as the source. In Type 2 codes, the source is an immediate value and the destination is R0L, R0H or memory. These instructions handle only 8b operands. However, since the OP code size is 8b, program ROM efficiency is enhanced such as port manipulation processing.

Types 3 and 4 support 8 and 16b operations. Type 3 codes can specify general-purpose registers or memory for source and destination. In Type 4 codes, the source is an immediate value and the destination is a general-purpose register or memory. Since there is no need to load memory in the genral-purpose register when

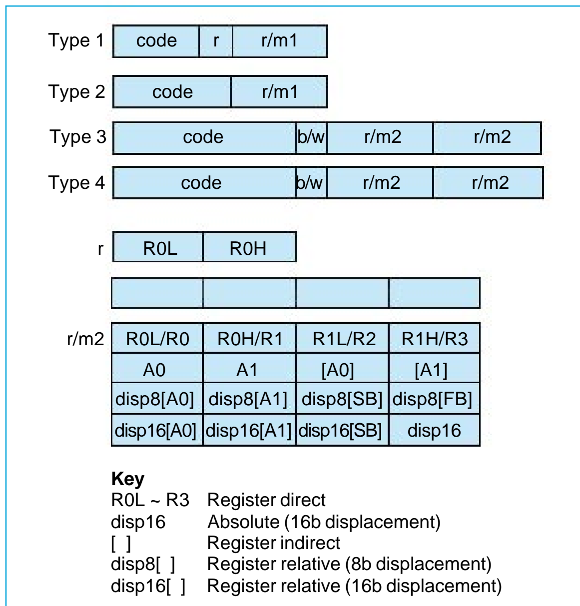


Fig. 3 OP codes and addressing modes.

using these instructions to process memory, ROM efficiency and speed are improved.

INSTRUCTION SET ENHANCEMENTS. The M16C can perform 1, 4, 8 and 16b operations. On 8b and 16b operands, it can perform signed and unsigned addition, subtraction, multiplication and division, the logical operations AND, OR, XOR and shift, and decimal addition and subtraction. Two signed division instructions are provided, allowing the remainder sign to be matched to either the divisor or to the dividend as needed for correct rounding. The DIVX instruction, which matches the remainder sign to that of the divisor, is used in graphics processing where rounding needs to be carried out in the direction of $-\infty$ rather than zero.

To facilitate 4b operations, instructions are provided for transferring the upper or lower four bits of R0L to or from other general-purpose registers or memory. This enhances RAM efficiency by allowing two decimal digits to be packed in each byte of memory. Bit operations include set, reset, negate and test, as well as logic operation with the C flag and loading such conditions as greater-than/less-than as a result of the preceding instruction. These capabilities are extremely useful in control applications involving complicated conditions.

There are also PUSHM and POPM instructions that allow push and pop to be performed on any number of registers in R0 ~ A1, SB and FB. In CPUs with a number of registers, push and pop often cause losses in speed and ROM efficiency, but with the M16C, PUSHM and POPM can push or pop any register in two clock cycles using a 16b instruction.

Noise Considerations

Noise must be considered in designing embedded microcomputers due to the smaller circuit geometries and higher operating frequencies of modern devices. Two important indices of noise performance are electromagnetic susceptibility (EMS) and electromagnetic interference (EMI) radiated by oscillator circuits and other circuit elements.

In this section we introduce two of the M16C's many noise-immunity enhancements. First, the pin layout provides noise protection while simplifying PCB design. Noise at the clock input (X_{in}) and output (X_{out}) is a common cause of misoperation, so we have surrounded them by the V_{cc}, V_{ss} and RESET lines, which are held at stable voltages and serve as a noise barrier. X_{in} and X_{out} are separated by V_{ss}, which simplifies connecting a three-pin oscillator circuit. By having the power-supply pin near V_{cc} and V_{ss}, it is also easier to connect a decoupling capacitor. V_{cc} (AV_{cc}) and V_{ss} (AV_{ss}) are separated to reduce the likelihood of power-supply shorts.

Second, we have taken steps to prevent noise-induced changes to the internal control registers. Internal registers control the processor mode and clock switching, and therefore should not be changed accidentally. In the M30600M8, we avoid this possibility by including a protect register and requiring the programmer to set the appropriate bit before altering the registers that control processor mode or clock switching. We tested the noise immunity of the device after each stage of noise-prevention design. Fig. 4 shows the results.

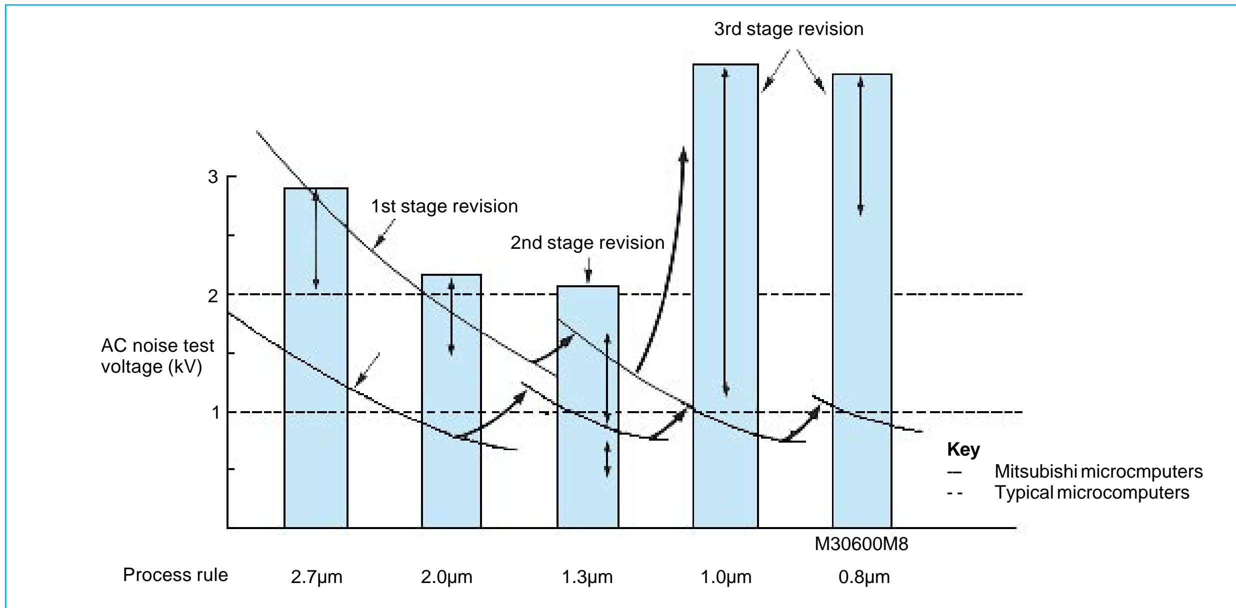


Fig. 4 Noise immunity.

The X_{in}-X_{out} circuit has two output levels: high power is supplied after a reset until the oscillator stabilizes, then low power is used to minimize spurious emissions and reduce power consumption.

Development Environment

Mitsubishi Electric Semiconductor Software Corp. is already shipping the AS30 assembler, NC30 C compiler and MR30 realtime OS for the M16C/60. As of February 1996, we are shipping engineering samples of the XDB30 and WDB30 debugger packages, which operate on NEC PC9801, IBM PC, HP9000 and Sparc workstations. Engineering samples of emulator boards are also available, with mass production scheduled to begin in mid April. Third-party developers have already released debuggers and C compilers.

Future Developments

We are already developing a second M16C product. This, the M30612M4, includes a universal asyncronous receiver/transmitter (UART) that is compliant with the smart-card interface specification.

We have also begun developing variations of the M30612M4: the M30610M16 with 128KB ROM and 10KB RAM, and the M30612M8 with 64KB ROM and 3.5KB RAM. Additional planning includes the development of internal flash memory and low-voltage versions. ❑

A Single-Chip Picture-in-Picture IC with Field Buffer Memory

*by Shigehiro Tamaki and Kenji Murakami**

The picture-in-picture (PIP) function is especially useful to CATV, VCR and Laserdisc users, because it allows them to monitor one video source while viewing another. Mitsubishi Electric is developing a single-chip PIP implementation that will make this function available to users of mass-market TVs at a modest price. This article discusses the evolution of this device, its specifications and signal processing capabilities.

Background

About 10~15% of the 24 million television sets sold annually in North America have a picture-in-picture (PIP) function that allows the user to view TV broadcasts concurrently with VCR or Laserdisc reproduction. A cost-effective LSI implementation of the PIP function will help the corporation stay competitive in this market by making it possible to equip moderately priced sets with this attractive feature.

The corporation developed one of the first PIP-capable TV sets in 1990, and since then has taken advantage of advances in fine-patterning technology to gradually reduce the number of ICs used to implement this function. A single-chip PIP implementation is currently under development.

Development History

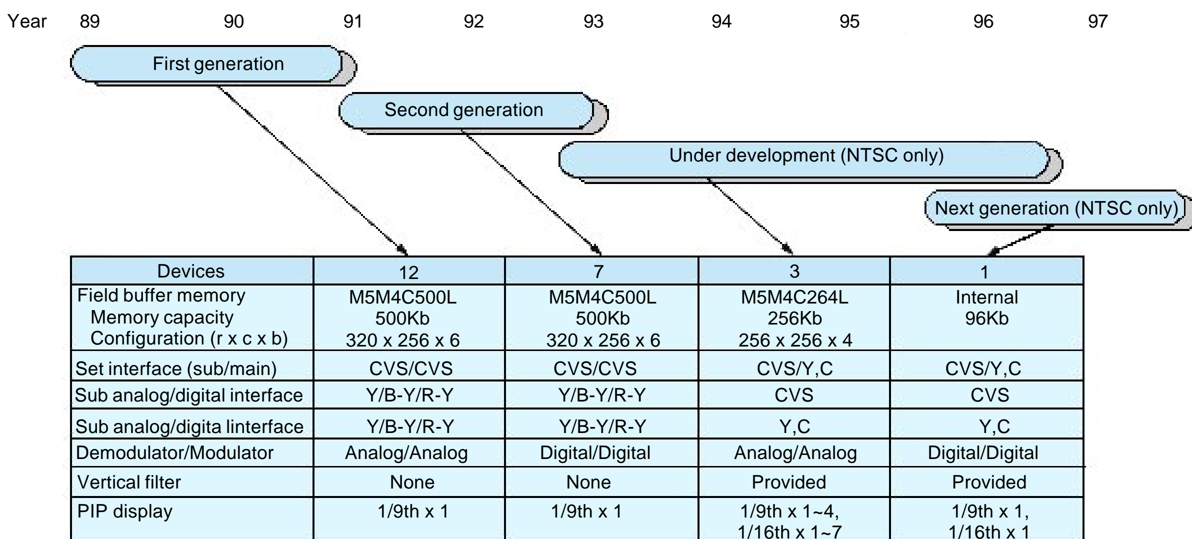
The 1990 implementation consisted of 12 ICs, all of which were analog except for the field memory and control circuitry. The next implementation was basically identical, with greater integration of the analog circuitry (Fig. 1). In the 1993 implementation, which is used in our current mass production TVs, most of the analog signal processing has been replaced by digital circuitry, reducing the chipset to three LSIs, a digital video processor, a 256Kb buffer memory and analog circuitry (Fig. 2).

The single-chip implementation currently under development includes all required memory for a single PIP screen, thus completing the integration process. It is also designed to be adjustment free. The following sections describe its operation.

Functions and Signal Processing

Table 1 lists the specifications, and Figs. 3 and 4 show the functions and signal processing.

SUB-PICTURE SIGNAL PROCESSING. The TV set provides the composite video signal selected for the sub-picture. A clamp circuit performs a sync-tip clamp on this signal, which is digitized at a subcarrier frequency (fsc) sampling rate of four (14.318MHz). An additional sync-tip-level slice is performed to detect the composite sync signal (Fig. 5). The digital signal is now separated into lumi-



Devices	12	7	3	1
Field buffer memory Memory capacity Configuration (r x c x b)	M5M4C500L 500Kb 320 x 256 x 6	M5M4C500L 500Kb 320 x 256 x 6	M5M4C264L 256Kb 256 x 256 x 4	Internal 96Kb
Set interface (sub/main)	CVS/CVS	CVS/CVS	CVS/Y,C	CVS/Y,C
Sub analog/digital interface	Y/B-Y/R-Y	Y/B-Y/R-Y	CVS	CVS
Sub analog/digita linterface	Y/B-Y/R-Y	Y/B-Y/R-Y	Y,C	Y,C
Demodulator/Modulator	Analog/Analog	Digital/Digital	Analog/Analog	Digital/Digital
Vertical filter	None	None	Provided	Provided
PIP display	1/9th x 1	1/9th x 1	1/9th x 1~4, 1/16th x 1~7	1/9th x 1, 1/16th x 1

Fig. 1 Evolution of Mitsubishi PIP products.

Shigehiro Tamaki and Kenji Murakami are with the Microcomputer & ASIC Division.

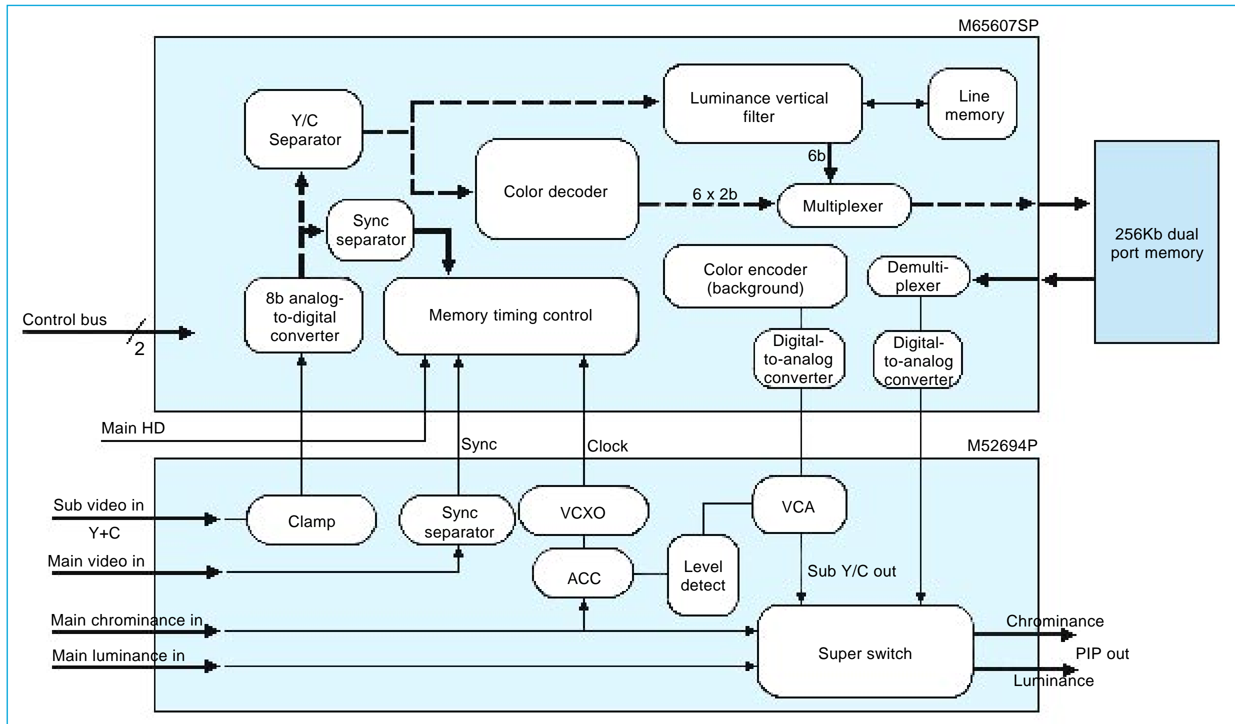


Fig. 2 A block diagram of the current mass production PIP system.

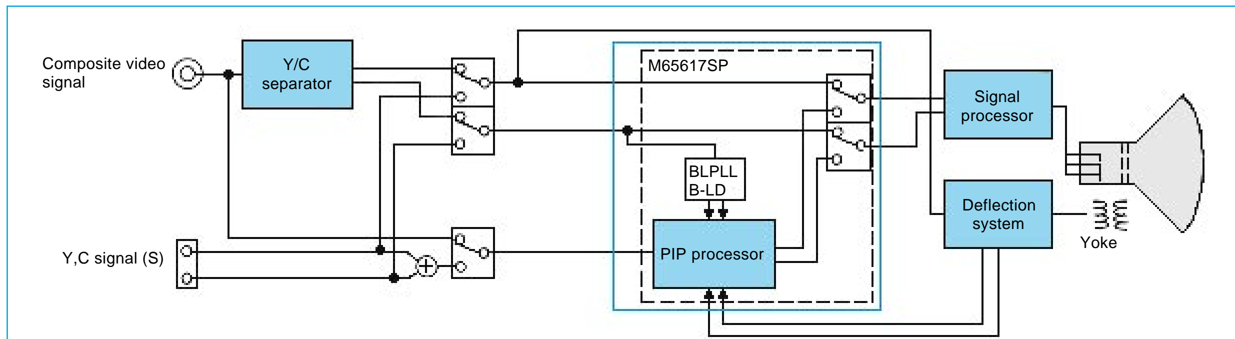


Fig. 3 PIP system configuration.

Table 1 One-Chip PIP LSI Specifications

Process	0.5µm CMOS
Supply voltage	3.3V
Current dissipation	140mA
Built-in field memory	96Kb
Package	52-pin shrink DIP
Signal sub-picture	1/9th or 1/16th screen size
I/O interface Main picture Sub-picture	 Luminance/chrominance Composite
Sub-picture processing Luminance signal Chrominance signal	 171 pixels/line, 70 lines/field 28.5 pixels/line, 70 lines/field
Adjustable PIP position	280ns/step horizontal, 1 field line/step vertical
Picture freeze	Available to freeze one field picture
3-pin serial bus interface	Connects to IIC bus with simple external circuit

nance and chrominance components. To prepare for later 1/4 rate resampling for horizontal compression, the luminance signal passband is set for approximately 1.7MHz. Vertical interpolation filter processing is performed on the pedestal-clamped luminance signal. The chrominance signal passes through an automatic chrominance-level control (ACC) circuit, and is demodulated to recover the two 8b color difference signals, R–Y and B–Y. This color demodulation processing provides the same functionality as analog signal technology.

The on-chip field buffer memory is 96Kb single-port RAM configured as 6,144 16b words. We developed the memory allocation scheme shown in Fig. 6 to help improve the resolution of the image data. Data is organized in blocks of nine samples of eight bits each. Nine luminance signal samples are stored along with two samples of each of the

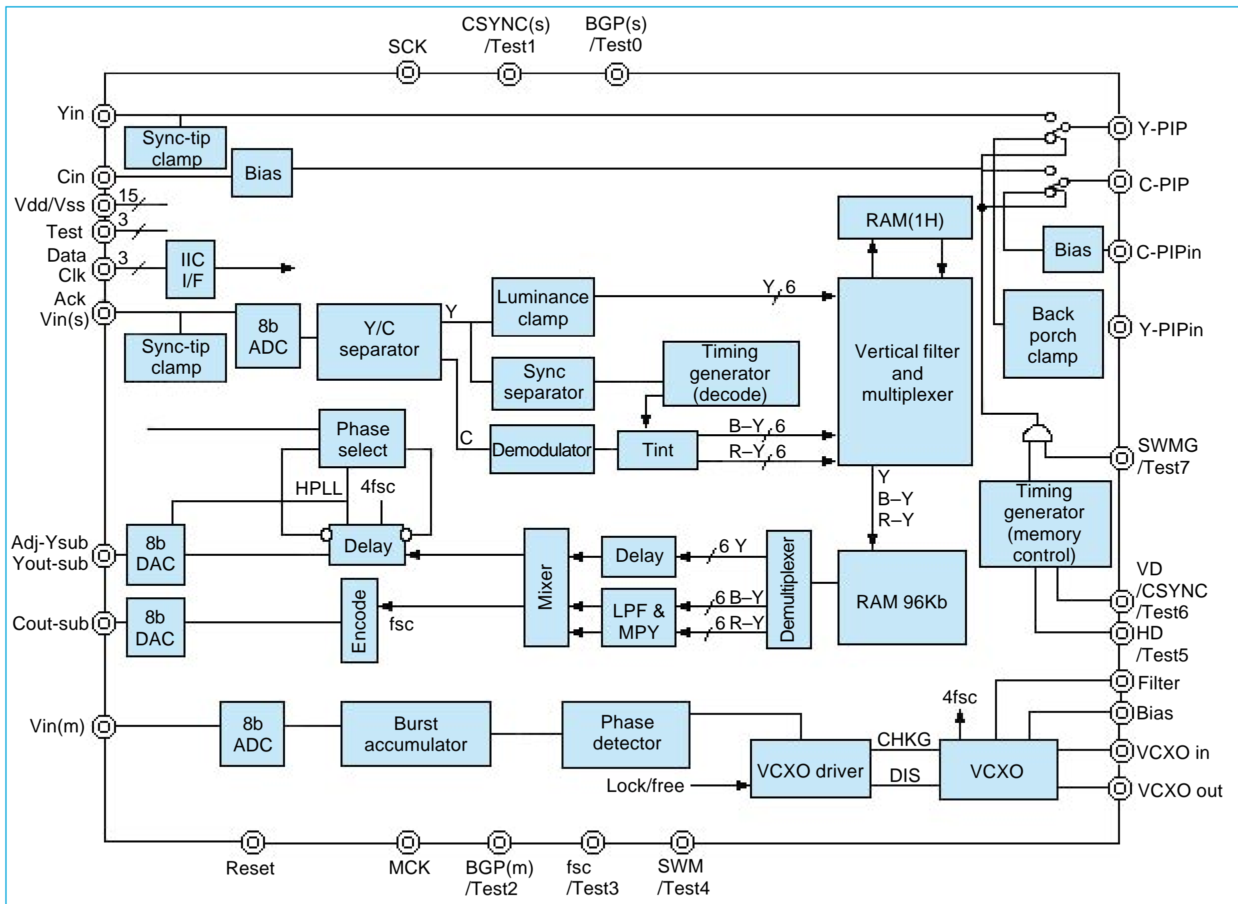


Fig. 4 Block diagram of M65617SP PIP LSI.

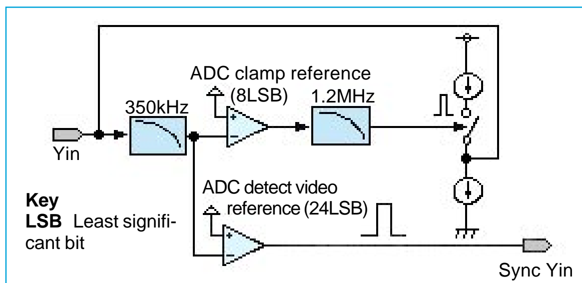
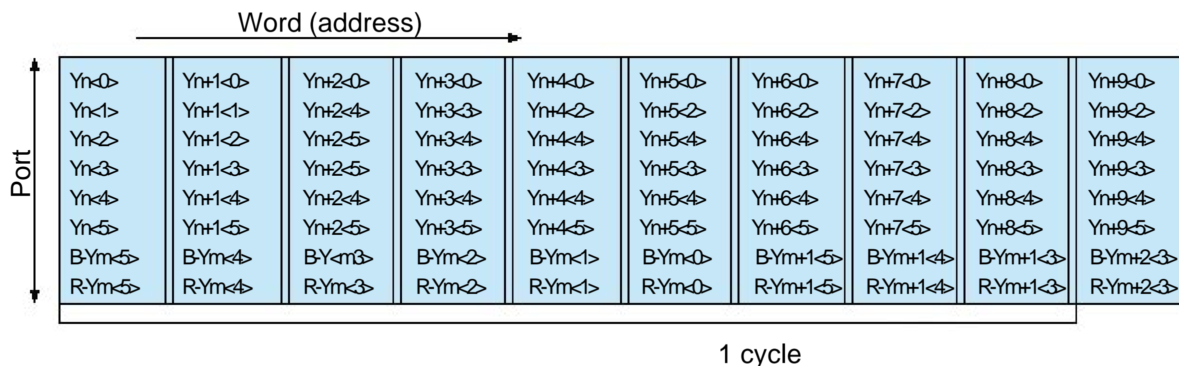


Fig. 5 Sync-tip-level slice circuit.

R–Y and B–Y signals. The color difference information between samples is written with half of the depth information, and interpolated on readout to reduce the required memory.

The horizontal compression ratio is fixed at 1/4 during the memory write. For pictures with 1/3 horizontal compression, the memory readout is conducted at a rate of three samples per four periods. The luminance data is expanded by interpolation and the color difference signal data is updated every six periods (Fig. 7).

The relatively low fsc input data rate allows the data transfer between the main and sub-picture systems to be realized rather simply. The write input data and write permission signal are passed using a field buffer memory that functions as a first-in-first-out (FIFO) buffer.



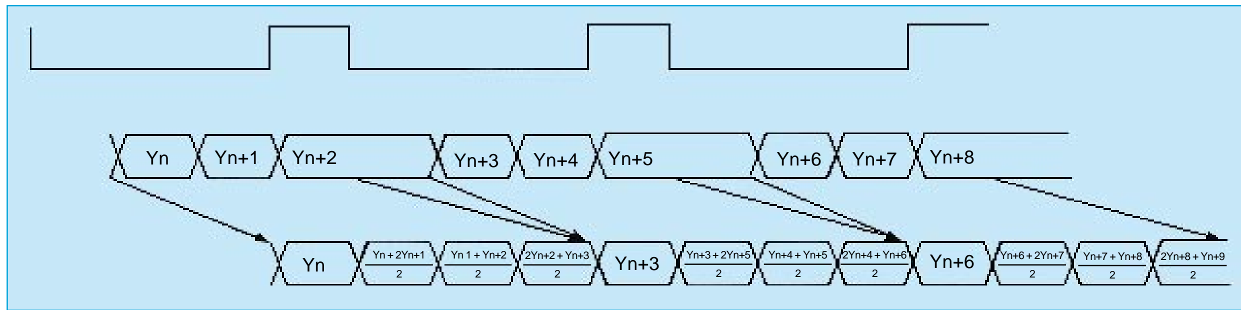


Fig. 7 Horizontal data 4/3 expansion.

We developed a special FIFO macrofunction for the PIP system using single-port RAM as a unit cell that works as follows: The head address at the storage destination is initialized when the valid vertical signal begins. Then, during each valid horizontal trace period (for each valid line), the specified number of samples are stored in successive address locations during each period that valid data is generated. Memory is utilized efficiently because values are stored only when a valid signal is present. By fixing the number of samples to be written during one valid horizontal scanning period and storing the values in succession, the RAM addresses for each valid horizontal period can be fixed and aligned in the vertical direction. Also, after the valid portion of a line starts, the addresses of a fixed number of samples are updated. This means that the noise associated with loss of input is not frozen in place.

The readout address for the main picture is initialized at the beginning of the valid vertical signal. Data is then read out of successive addresses during the readout period. Then, when each valid horizontal period begins, the starting address for the next line is also computed in preparation for a jump to that address when the next valid line begins. This ensures that the correct line information will be read out of each horizontal period, even when the main picture signal exhibits irregular synchronization.

MAIN PICTURE SIGNAL PROCESSING. The TV provides the luminance signal and color signals for the main picture source. The luminance signal is sync-tip clamped and an analog switch is provided to toggle between main and sub pictures. The LSI can use the horizontal and vertical retrace signals for the TV set deflector system as sync signals for the main picture. It can also obtain horizontal and vertical sync signals by sync-tip-level slicing the composite sync signal in the same manner employed for the sub-picture.

The sub-picture data can be read out of RAM for any arbitrary position and display area using the main picture sync signals as a trigger. The luminance data is mixed with the optional regenerated compound sync signal, the blanking period pedestal level and background level (also used as frame level) and output to an 8b digital-to-analog converter (DAC) to generate the luminance signal output.

The sub-picture color difference data is mixed with the regenerated color burst signal, the no-signal level for the blanking and frame periods and the background level, and output to an 8b DAC. (The regenerated color burst signal has a variable color difference signal level setting, and is present when the regenerated compound sync signal is present.)

Future PIP products will require multiple-screen and multiple television signal standard capabilities, including design for wide-screen format. High-density DRAM processes will be used to increase memory capacity and reduce die size, and a core cell implementation of PIP functions will be adopted to increase design efficiency. ❑

A Programmable Realtime MPEG2 Video Encoder Chipset

by Tetsuya Matsumura, Shin'ichi Nakagawa and Kazuya Ishihara

Mitsubishi Electric has developed a new chipset architecture for a programmable video encoder based on the MPEG2 main profile at main level (MP@ML) specifications. The chipset consists of a controller LSI, a macroblock-level pixel processor LSI and a motion estimation LSI. The chipset, combined with synchronous DRAMs, supports all processing layers including rate control, and provides realtime encoding capability for ITU-R-601 resolution video (720 x 480 pixels at 30 frames/s) with glueless logic. The exhaustive motion estimation capability is scalable up to ±63.5 in the horizontal direction and ±15.5 in the vertical direction. The chipset can realize a low-cost MPEG2 video encoder system with excellent video quality on a small PC add-on card. This article reports on the new architecture, LSI design and development, and on an MPEG2 encoder evaluation system.

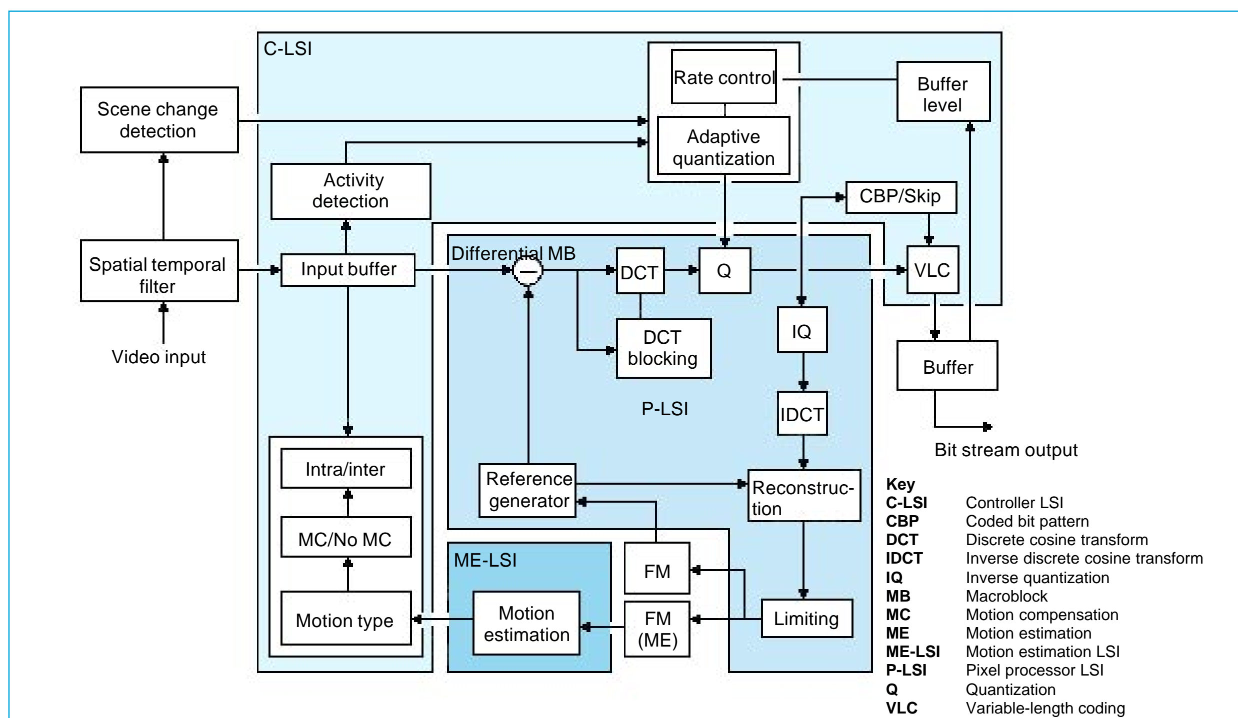
Background

The market for digital CATV, digital satellite broadcasts, video servers and multimedia computer systems is actively expanding now that CCITT Moving Picture Experts Group Phase 2 has completed the specifications for the MPEG2 video compression standard. There is strong demand for competitively priced high-picture-quality realtime video encoder/decoder hardware suitable for MPEG2 MP@ML compression.

Implementations of the MPEG2 MP@ML video compression algorithm need more than ten times the processing capability of MPEG1 because they must deal with interlaced video signals, handle four times the number of pixels, and support field-scale calculations for motion prediction and discrete cosine transform (DCT) processing.

One of the first implementation tasks is to efficiently partition the functions and memory among several devices, since current technologies are not capable of implementing an MPEG2 encoder as a single device.

We developed a three-LSI chipset based on a



**Tetsuya Matsumura, Shin'ichi Nakagawa and Kazuya Ishihara are with the System LSI Laboratory.*

new architecture that makes it possible to realize a low-cost MPEG2 MP@ML video encoder with high picture quality.

Chipset Architecture

FUNCTIONAL PARTITIONING. Fig. 1 shows the functional partitioning of the MPEG2 encoding flow over all layers. The basic functional partitioning is governed by the following principles:

1. The signal processing in sequence, GOP, picture and slice layers, which consists primarily of adaptive processing, should be performed by a device that incorporates a programmable processor.
2. Macroblock level processing functions, such as filtering, discrete cosine transform/inverse discrete cosine transform (DCT/IDCT) and quantization/inverse quantization (Q/IQ) conversions, and run-length encoding, should be assigned to a monolithic pixel processing device with performance of at least 5GOPs.
3. A fully dedicated hardware device with a performance of more than 100GOPS should be assigned to the task of motion estimation, which is implemented using an exhaustive search scheme. To satisfy picture-quality objectives, the search window data is fed from a reconstructed image rather than an original image. The search range is expanded by increasing the chip count.

ENCODER SYSTEM CONFIGURATION. Fig. 2 shows the block diagram of an MPEG2 video encoder system consisting of a controller LSI (C-LSI), pixel processor LSI (P-LSI) and motion estimation LSI (ME-LSI) designed on the above principles. The system configuration includes a solution to eliminate bus traffic problems. MPEG2 encoding requires that data be transferred between memory and video compression devices at rates exceeding 140Msample/s. Two 32b data buses, the main data bus and the ME data bus, have been introduced to eliminate bus traffic problems associated with these transfer demands. The main data bus is used to transfer the original image, predictive image and reconstructed image, which are stored in the main frame memory. The ME data bus is available to transfer the reconstructed image stored in the ME frame memory. The pixel data is packed vertically in groups of four pixels, which improves transfer efficiency by reducing the RAS access frequency of the synchronous DRAM (SDRAM) memory.

The processing pipeline is flushed for processing of each picture, allowing adaptive search range expansion in each picture based on picture type and source image, which results in video quality improvement. During motion estimation for P-type pictures, the entire motion estimation LSI is allocated to forward estimation. During motion estimation for B-type pictures, the motion estimation LSI's capabilities are partitioned into two parts for forward and reverse estimation, and the motion estimation engine and search window memory are controlled accordingly. This allows the same hardware encoding system to handle double the horizontal scanning range for P-type pictures.

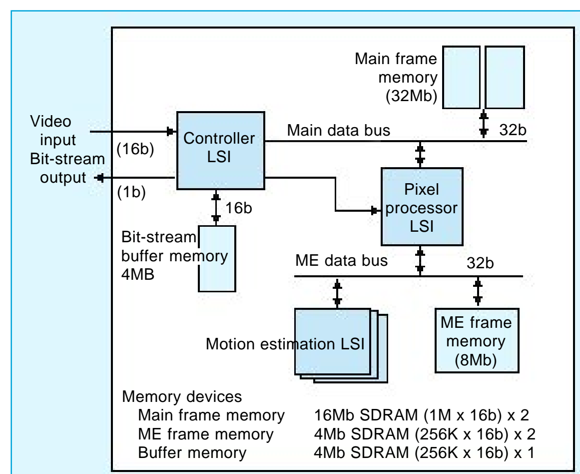


Fig. 2 Block diagram of MPEG2 video encoder.

LSI Description

CONTROLLER LSI. The C-LSI controls the P-LSI, ME-LSI and all of the SDRAMs. It interfaces to the video input port and the serial output port and manages the total encoding sequence through all layers. It consists of seven functional units, a frame memory controller (FMC), a pixel processor controller (PPC), a motion estimation controller (MEC), an MB parameter detection unit (MPD), a global control unit (GCU), a RISC processor unit (RPU) and a variable-length coding unit (VLC).

By having independent main and host processor buses, the host processor can freely access internal hardware while coding is underway. The GCU generates the synchronization signal for the picture, slice and macroblock layers, and controls the picture sequence.

The VLC generates run-length limited code from the headers for each layer and the pixel processor output, supporting a 20Mbps bit stream at the serial interface.

The RPU is a 16b RISC processor in which each of about 200 registers in each block can be

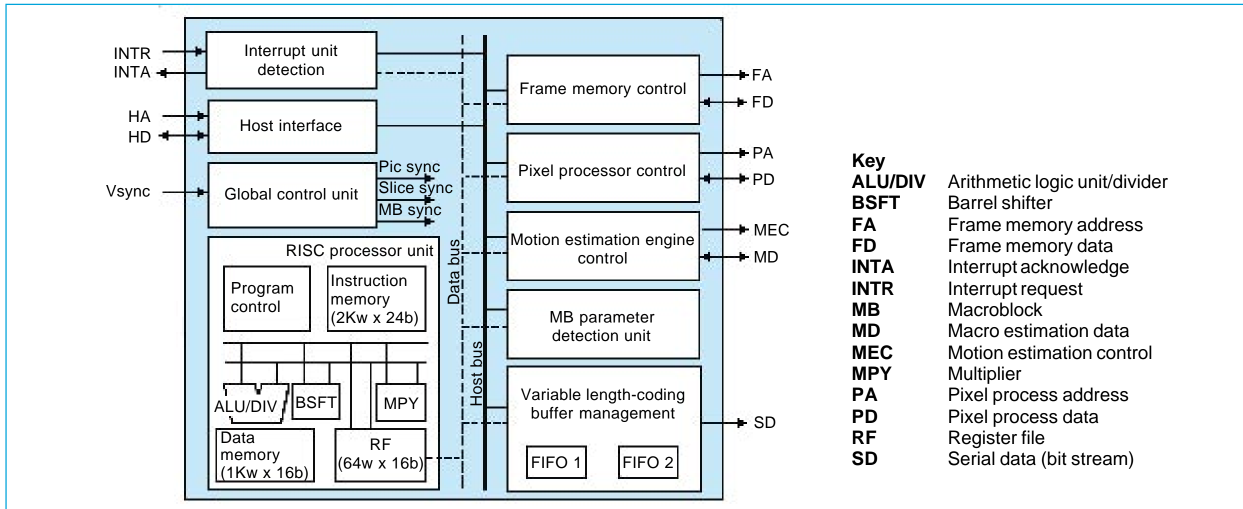


Fig. 3 Block diagram of controller LSI.

accessed within one clock cycle. This not only allows continuous monitoring of the encoding status, but supports adaptive processing in which the values of the encoding parameter registers are changed in response to the encoding status.

PIXEL PROCESSOR LSI. Fig. 4 show a block diagram and micrograph of this device. It consists of two predictive image generators with half-pel filtering functions, DCT processor, quantization processor, run-length encoder, zig-zag/alternate-scan converter and RISC processor. It has two 32b data ports and can rewrite the two frame memories simultaneously over the two 32b data buses. The internal operating frequency is 81MHz.

MOTION ESTIMATION LSI. Fig. 5 show a block diagram and micrograph of this device. The ME-LSI supports all MPEG2 prediction modes, providing three vectors with half-pel precision concurrently in the exhaustive search path. The architecture allows multiple devices to be used together to expand the search range, without an increase in the size of the search window data transfer. A single ME-LSI handles a search range of ±7.5 in the horizontal and ±15.5 in the vertical direction. Table 1 summarizes the characteristics of the three LSIs.

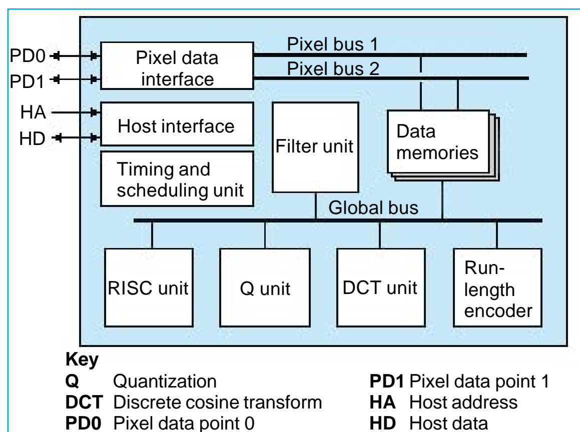


Fig. 4 A block diagram of the pixel-processor LSI.

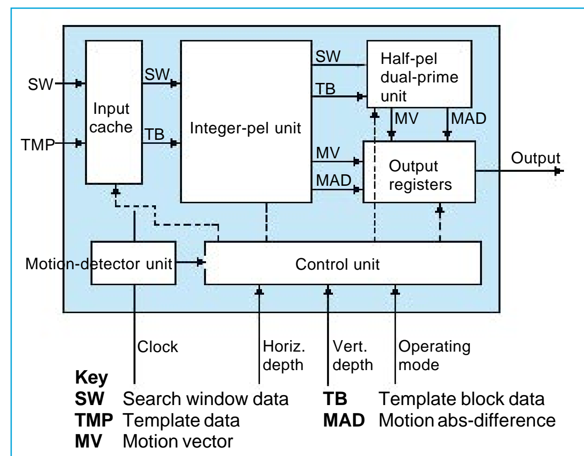


Fig. 5 A block diagram of the motion-estimation LSI.

MPEG2 Encoder Evaluation System

PERSONAL COMPUTER ADD-ON BOARD. Table 2 lists the functional characteristics of an encoder system based on the new chipset. The system supports both frame and field pictures. It receives digital video sources in 4:2:2 or 4:2:0 formats, and transmits an output bit stream at up to 20Mbps. The chip set handles the entire rate control process.

We developed an MPEG2 MP@ML encoder system as an add-on board for personal comput-

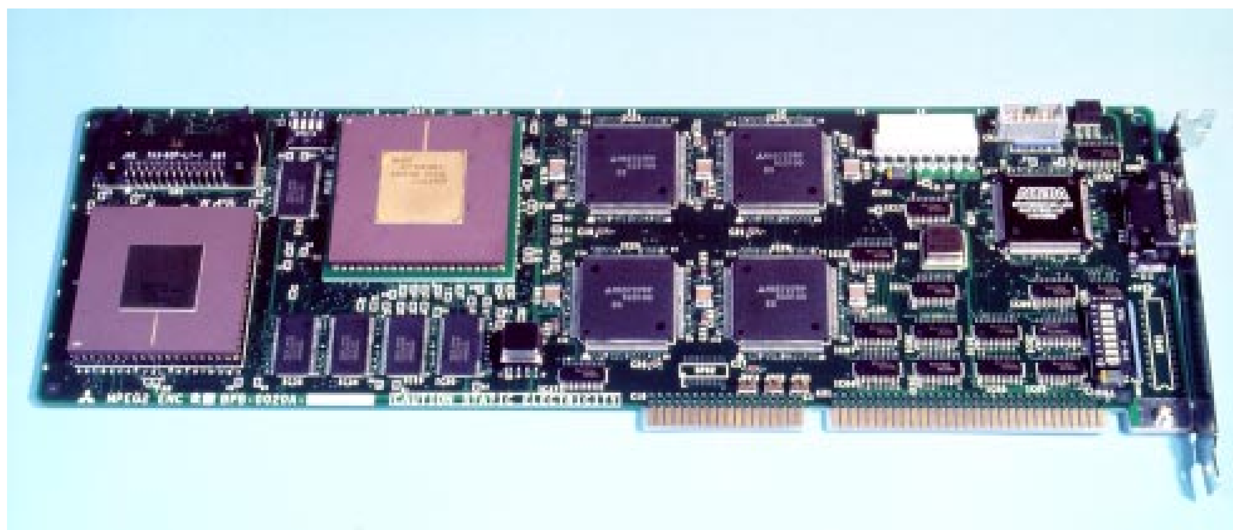


Fig.6 An MPEG2 encoder add-on board for personal computer use.

Table 1 Basic Chipset Specifications

LSI Devices	Controller	Pixel Processor	Motion Estimation
Die size (mm)	14.98 x 14.84	14.54 x 14.89	13.85 x 13.55
Transistor count	1,140K	920K	850K
Operation frequency	40.5MHz	81MHz (40.5MHz)	40.5MHz
Technology	0.5µm 2Al-CMOS		
Power consumption	3.0W	3.5W	1.9W
Supply voltage	3.3V		
Package	393-pin PGA	257-pin PGA	152-pin plastic QFP

Table 2 Functional Characteristics of the Encoder System

Algorithm	MPEG2 (MP@ML), MPEG1
Resolution	720 x 480 pixels (ITU-R-601)
Frame rate	Up to 30 frames/s (40,500MB/s)
Bit rate	Up to 20Mbps
Picture structure	Frame or field structure
Picture type	I/P/B picture (M = 1~4, N = 5~15)
Motion estimation type	Full exhaustive search
Max. search range P picture B picture	 ±63.5 horizontal, ±15.5 vertical ±31.5 horizontal, ±15.5 vertical
Accuracy	Integer/half-pel
Motion type Frame Field	 Frame/field Field/16 x 8MV
DCT	Frame/field adaptive blocking
Coding mode	Intra/inter, motion compensation/no motion compensation
Rate control	User defined control
Quantization	Adaptive

ers (Fig. 6). The board operates with a 40.5MHz system clock. It employs six LSIs: the C-LSI, P-LSI and four ME-LSIs. Four additional ME-LSI's can be mounted on the rear surface of the board for a ten-chip implementation that offers a search range of ±63.5 in the horizontal direction and ±15.5 in the vertical direction.

EVALUTATION SYSTEM. We developed an MPEG2 encoder evaluation system based on the MPEG2 encoder board. The input port can receive digital or analog sources, and the digital signal is transferred to the encoder board in blocks. The encoder board performs encoding and transfers the bit stream to an MPEG2 decoder board via a local port, allowing realtime encoding and decoding with side-by-side monitoring of the original and recovered signals. To support storage applications, we provide a high-capacity memory board that stores the bit stream to allow later uploading via the bus. The system includes application software for operation under Microsoft Windows.

With the development of the advanced architecture MPEG2 LSI chipset presented here, equipment manufacturers can use these three devices in conjunction with external memory to implement competitively priced MPEG2 MP@ML realtime encoding systems offering high picture quality. ❑

Q-Band Low-Noise Variable-Gain Amplifier MMIC Modules Using Dual-Gate HEMTs

*by Takuo Kashiwa, Takayuki Kato and Makio Komaru**

Mitsubishi Electric has developed two monolithic millimeter-wave amplifier modules for the Q band (41~ 46GHz) that offer gain of 20 ~ 50dB with a noise figure of 1.8 ~ 2.5dB. The devices promise to improve the performance and versatility of future millimeter communications equipment.

Module Configuration

Variable-gain GaAs millimeter-wave amplifiers have numerous applications for monolithic microwave ICs (MMICs), and for temperature-compensated amplification. Fig. 1 shows the basic configuration of the modules we developed. The system consists of a low-noise amplifier incorporating a single-gate high-electron-mobility transistor (HEMT) and a dual-gate variable-gain HEMT amplifier.

Device Modeling

The required S parameters for the MMIC were determined by on-wafer measurements from DC to 110GHz. However, commercial test equipment for determining optimum source impedance and other noise-related parameters can perform accurate measurements only up to about 26GHz, so we determined millimeter-wave parameters by mathematical modeling based on microwave-band parameters.

The active element in the low-noise amplifier is a single-gate AlGaAs/InGaAs pseudomorphic HEMT with a 0.15μm gate length and an 80μm gate width. Fig. 2 shows a cross section of the device. We used a gate electrode with a low-resistance T-shaped cross section, since reductions in parasitic resistance lead to large improvements in gain and noise characteristics. The electrode was formed by a combination of electron-beam and optical photolithography.

To determine the parasitic resistance and other parameters that influence the noise characteristics, we derived equivalent small-signal circuit parameters as follows:

1. The FET S parameter measured in the cold bias state (drain-source voltage = 0V) was used to calculate the bias-independent parasitic parameters.
2. The FET S parameter was measured at the operating point and combined with the results of (1) to eliminate the effect of external parasitic circuit elements.
3. The correlated noise matrix was measured at a practical frequency (12GHz) and used to determine the transistor noise parameters independent of the effects of external parasitic circuit elements.

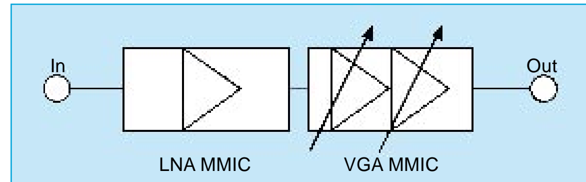


Fig. 1 A block diagram of the Q-band variable-gain amplifier module.

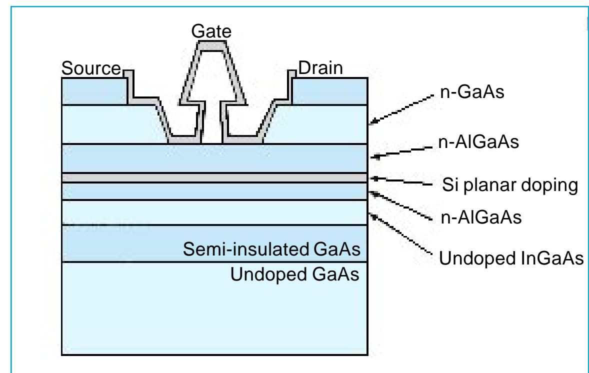


Fig. 2 A cross section of the single-gate HEMT. (AlGasAs/InGaAs Pseudomorphic HEMT)

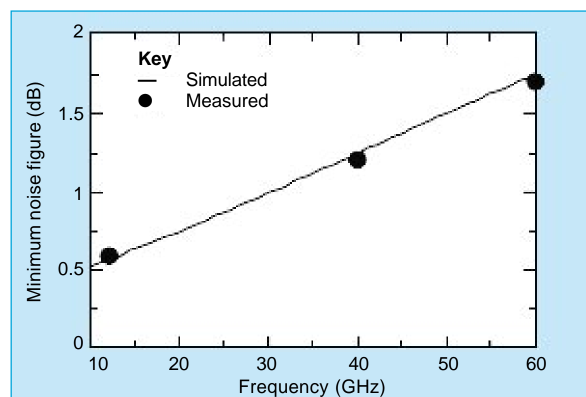


Fig. 3 Minimum noise figure.

**Takuo Kashiwa, Takayuki Kato and Makio Komaru are with the Optoelectronics & Microwave Devices Laboratory.*

We verified these values by measuring the minimum noise figures of the HEMT. The noise figure is a scalar quantity that can be accurately measured by tuning at millimeter-wave frequencies of 30GHz and higher. Fig. 3 compares the results determined by modeling with actual measurements, showing excellent correspondence through 60GHz.

Low-Noise Amplifier MMIC Design

The first stage of the low-noise amplifier is single-ended. A matching circuit was designed based on parameters determined by our mathematical model. The matching circuit was configured with an open stub, and matching conditions were selected as the best trade-off between noise figure and input voltage standing-wave ratio (VSWR). The bias circuit is configured as a quarter-wave high-impedance line and a radial stub that provides low loss at 40 ~ 50GHz with little effect on the amplifier matching. A resistor and capacitor provide stability at low frequencies. The circuit ground is implemented by a small via hole formed by unisotropic etching near the HEMT, where it contributes to lower inductance.

Dual-Gate HEMT Construction

Dual-gate and cascade transistors are often used as gain-control elements. Fig. 4 shows the cross section of a dual-gate HEMT. The first gate serves as source, the second gate as drain. The epitaxial construction is the same as for a single-gate HEMT, and can be formed simultaneously by the same processes. The maximum available gain (MAG), maximum stable gain (MSG) and k factor for the dual-gate HEMT are given by the following equations:

$$MAG = MSG[1 - (k_{dual}^2 - 1)^{1/2}] \quad \text{(Eq. 1)}$$

$$k_{dual} \fallingdotseq k_{single} + 2(\omega Cgs2/gm2) \quad \text{(Eq. 2)}$$

where k_{dual} and k_{single} are the k factors for dual-gate and single-gate HEMTs, Cgs2 is the gate-source capacitance and gm2 the transconductance of the HEMT's common-gate FET.

The dual-gate HEMT has good isolation characteristics and high gain in the MSG region, but the k factor is larger than in single-gate HEMTs, causing a changeover to MAG at relatively low frequencies.

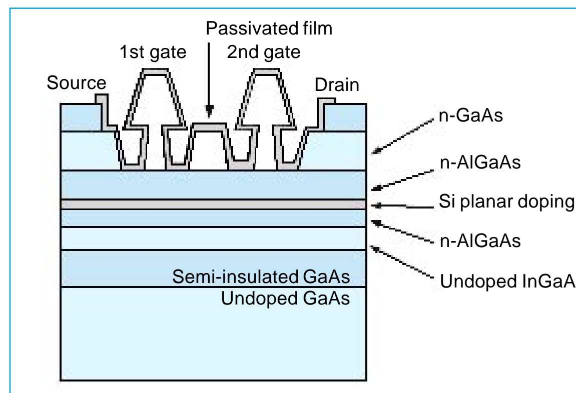


Fig. 4 A cross section of the dual-gate HEMT.

Fig. 5 compares the MAG/MSG performance of dual- and single-gate HEMTs. MAG performance of the dual-gate HEMT decreases approximately 9dB/octave as compared to 6dB/octave of the single-gate HEMT. However, the dual-gate HEMT has a sufficiently higher MSG in the conditionally stable region and a MAG of 8~10dB in the 40~50GHz band (unconditionally stable region). The transistor has satisfactory characteristics for use as a variable-gain amplifier in this band. The amplifier is a two-stage single-ended type, and the dual-gate HEMTs for both

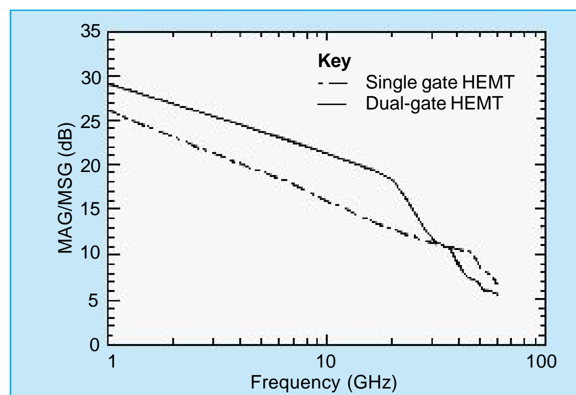
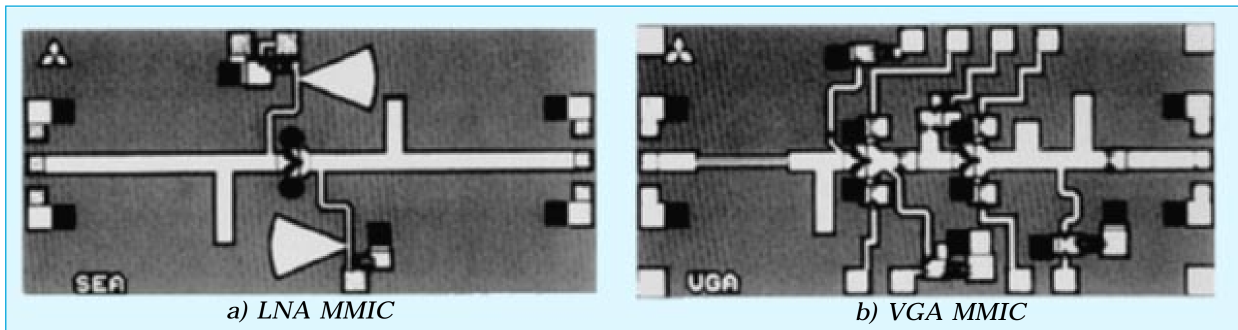


Fig. 5 MAG/MSG performance of single- and dual-gate HEMTs under conditions of V_D = 2V, I_D = 10mA, 2nd gate = 0V and Wg = 80μm.



a) LNA MMIC *b) VGA MMIC*

Fig. 6 Micrographs of the MMICs.

stages have an 80μm gate width. The second gate has an RF ground through a metal-insulator-metal (MIM) capacitive coupling.

The two stages are joined by a conjugate matching circuit to reduce die size. The bias circuit uses a quarter-wave high-impedance line except for the bias circuits between the two stages. The capacitive open stub gives the amplifier the characteristics of a low-pass filter.

The dual-gate HEMT has an undesirable gain in low frequencies because of the higher MSG performances in low frequencies. A quarter-wave coupled line is used as DC blocking for suppression of this undesirable gain.

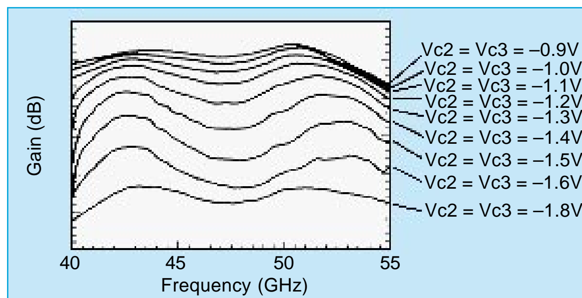


Fig. 7 Measured gain-control performance of the combined modules under conditions of $V_D1 = V_D2 = V_D3 = 2V$, $VG1 = +0.2V$, $VG2 = VG3 = +0.3V$.

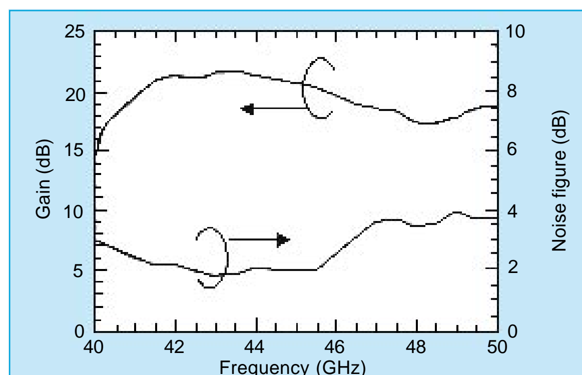


Fig. 8. Measured noise performance of the combined modules under conditions of $V_D1 = V_D2 = V_D3 = 2V$, $V_G1 = 0V$, $V_G2 = V_G3 = +0.3V$, $Vc2 = Vc3 = -1.1V$.

Test Results

The low-noise amplifier module was connected in series to the variable-gain module and mounted on a carrier for testing. Fig. 6 shows a photograph of the devices, both of which measure 2.6 x 1.3mm. Fig. 7 shows the gain vs. frequency characteristics with the voltage at the second gate (the gain-control line) as a parameter. The base gain is better than 20dB over the 41 ~ 52GHz band, reaching a maximum of 24.5dB at 50GHz. The second-gate voltage (V_c) can boost this gain by up to 30dB. Fig. 8 shows the frequency dependence of gain and noise under minimum-noise bias conditions. Gain is better than 20dB over the 41~ 46GHz range with a noise figure under 2.5dB. Noise reaches a minimum of 1.8dB at 43GHz with a gain of 22dB, approximately equivalent to the performance of previously reported low-noise InP HEMT amplifiers.

Careful engineering of these millimeter-wave modules has made it possible to achieve excellent low-noise performance while achieving the variable gain needed for sophisticated applications. ❑

The World's Largest-Capacity 8kV/3.6kA Light-Triggered Thyristor

*by Katsumi Sato**

Mitsubishi Electric has developed an 8kV/3.6kA light-triggered thyristor (LTT) based on a six-inch wafer for power-converter applications in high-voltage DC transmission and back-to-back systems. New design features give the device double the power-control capacity of previous LTTs based on four-inch wafers while mitigating the problems that occur with large-capacity devices.

Development Objectives

There is a market for high-capacity LTTs with a high blocking voltage, since they will enable equipment manufacturers to build power-control systems that are simpler, more compact and more reliable. However, increasing thyristor blocking voltage and capacity generally involves sacrificing on-state voltage (V_{TM}), reverse recovered charge (Q_{rr}), critical rate-of-rise of on-state current (*di/dt*), leakage current and other operating characteristics. In developing the new LTT, we needed to improve these characteristics, reduce the minimum light triggering power (P_{LT}) (which helps extends the lifetime of the light source), reduce the loss in the snubber circuit, and for reasons of equipment size, improve critical rate-of-rise of off-state voltage (*dv/dt*) capability.

Description

Fig. 1 shows the 8kV/3.6kA LTT and its semiconductor element. The element consists of small light-sensitive pilot thyristors at the center that are triggered by an optical signal, and the main thyristor, which turns on in response to a gate current supplied by the pilot thyristors. The package is designed to ensure uniform mounting pressure, and is constructed to prevent alloying between the element and the heat-absorber disc. The ceramic seal has a clear window to admit light.

The photocurrent induced in the pilot thyristor and the displacement current generated by *dv/dt* turn on the pilot thyristor, forcing a trade-off between P_{LT} and *dv/dt* capacity. We reduced P_{LT} without sacrificing *dv/dt* capability by use of a channeled cross section for the junction between the p-base and n-base layers, thus mak-

Fig. 1 The package and semiconductor element of the 8kV/3.6kA LTT.

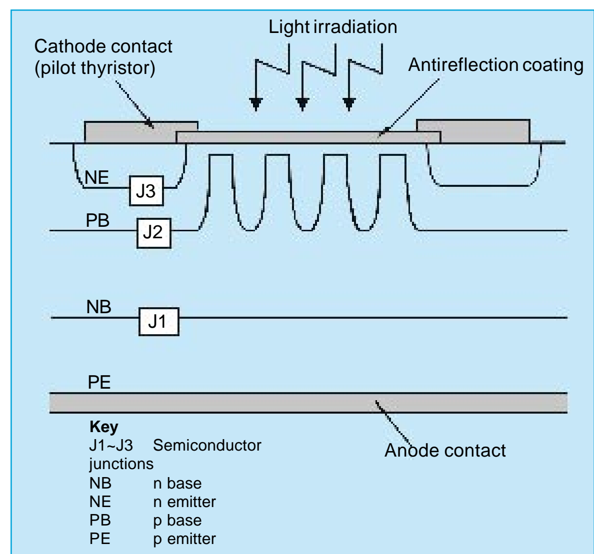


Fig. 2 A cross section of the light-sensitive area.

ing better use of the large photocurrent near the wafer surface (Fig. 2). To improve the *dv/dt* capacity, we surrounded the main thyristor with pilot thyristors, and developed a gate-emitter structure that prevents *dv/dt* mistriggering. These structural enhancements, combined with design optimizations, yield a dramatic improvement in the trade-off relationship between P_{LT} and *dv/dt* capability (Fig. 3).

Large-capacity thyristors typically employ a dynamic gate structure, with the pilot thyristors (which supply the trigger current) arranged in concentric circles. However, in order to turn

**Katsumi Sato is with the Power Device Division.*

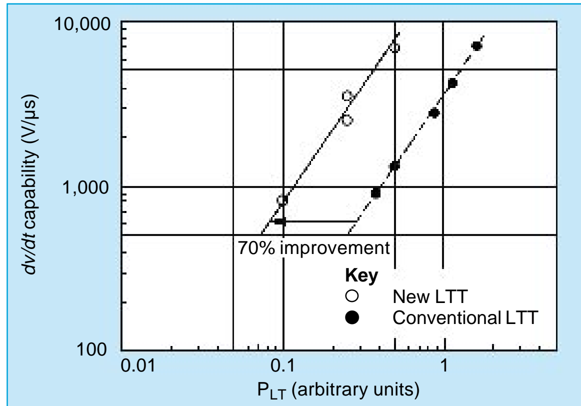


Fig. 3 The tradeoff between P_{LT} and dv/dt capability.

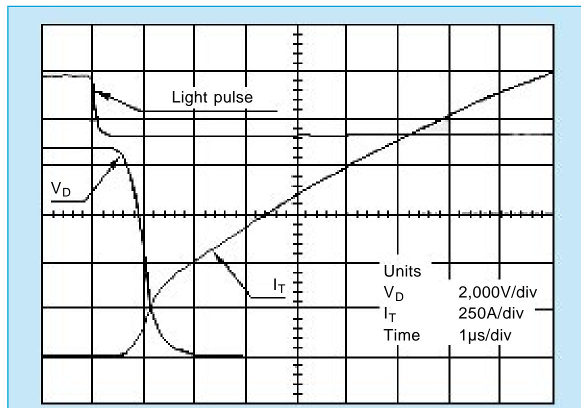


Fig. 4 The turn-on waveforms at 8.8kV.

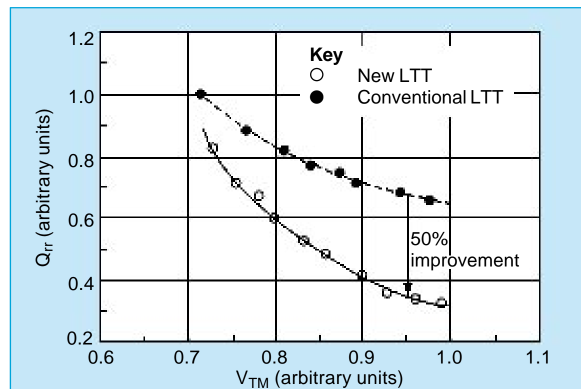


Fig. 5 The trade-off between V_{TM} and Qrr.

on the main thyristor more quickly, we developed a new dynamic gate structure in which the main thyristor area is dotted with pilot thyristors. This arrangement has dramatically improved the turn-on characteristics: With an applied voltage of 8.8kV, a *di/dt* of 200A/µs is achieved. Fig. 4 shows a typical turn-on waveform at 8.8kV.

Lifetime control technology helps optimize the trade-off between V_{TM} and Qrr, but conventional techniques such as heavy metal diffusion and electron-beam irradiation affect the entire wafer. We chose instead to use proton irradiation, which allowed us to control the lifetime profile in the thickness direction. This localized lifetime control prevents a rise in V_{TM} while reducing Q_{rr} and the subsequent continuous leakage currents. (There is no reduction of carrier lifetime of the n-base.) Fig. 5 shows the trade-off relationship between V_{TM} and Q_{rr} of a conventional LTT compared with that of this device, indicating a 50% improvement. Table 1 lists the major specifications of the new device.

Table 1 Major Ratings and Characteristics

Item	Symbol	Value
Repetitive peak off-state voltage	V_{DRM}	8,000V
Repetitive peak reverse voltage	V_{RRM}	8,000V
Average current	$I_{T(AV)}$	3,600A
Critical rate-of-rise of on-state current	*di/dt*	200A/µs
On-state voltage	V_{TM}	2.8V
Critical rate-of-rise of off-state voltage	*dv/dt*	2,300V/µs
Minimum light triggering power	P_{LT}	8.0mW
Turn-off time	t_q	400µs
Thermal resistance	$R_{th(j-f)}$	0.004°C/W

The unprecedented voltage and current ratings of this light-triggered thyristor will make it possible to manufacture high-capacity power-control and power-conversion equipment that is compact and reliable. ❑

A Gigabit-Scale DRAM Cell Fabricated Using X-ray Lithography

by Kyozo Kanamoto, Yasutaka Nishioka and Dr. Yasunori Tokuda*

One gigabit DRAMs are now in the early stages of development.[1] Several problems must be addressed to achieve memory capacities of 1Gb and larger: the limitations of optical lithography, ensuring sufficient storage capacitance and the development of pattern-size-independent processes. In this article, we report on the fabrication of a gigabit-scale experimental memory cell structure using advanced technologies that address these issues: synchrotron-radiation (SR) X-ray lithography, a simple stacked capacitor employing a $(Ba,Sr)TiO_3$ (BST) high-dielectric-constant film and etching by improved plasmas.

Memory Cell Arrays

The memory cell arrays fabricated for 1Gb devices have a unit cell of 0.38 x 0.76μm (0.29μm^2) with a simple Ru/BST/Ru stacked capacitor. The cell layout, shown in Fig. 1, is designed for an 8F^2 folded bit-line arrangement with 0.14μm process technology. Fig. 2 shows a cross-sectional secondary electron micrograph (SEM). Critical layers were patterned by X-ray lithography, and the patterning for the contact holes for the bit lines and storage nodes was performed by electron-beam lithography. Each cell is isolated by 0.14μm-wide, 0.3μm-deep trenches filled with SiO_2. The 0.14μm-wide transfer gates and bit lines were made of tungsten silicide (WSi_2) and n$^+$-doped polysilicon. Storage node contact holes approximately 0.1μm in diameter were obtained with an aspect ratio of approximately 5 and a contact resistance of 3kΩ at the Ru-polysilicon interface.

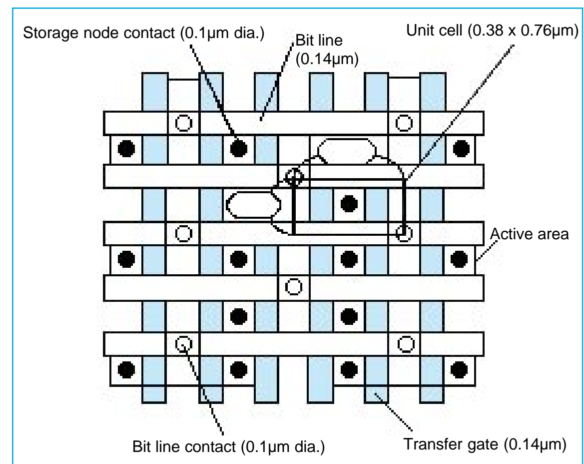


Fig. 1 Memory cell layout designed using 0.14μm rule.

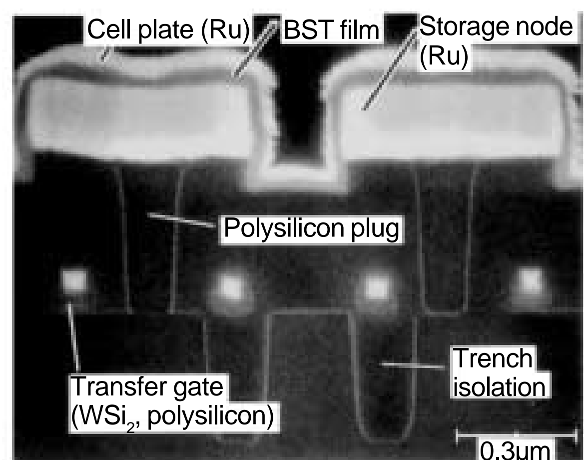


Fig. 2 Cross-sectional SEM photograph of the fabricated memory cell.

X-Ray Lithography

We developed a proximity SR X-ray lithography system that solves several optical lithography problems at a stroke and has the potential to be the leading technology for volume replication of the next generation of ultrafine patterns.

The SR exposure system consists of a Mitsubishi Electric SR facility and a Canon XFPA stepper.[2] The X-ray source has a peak emission wavelength of 0.69nm. The maximum image area of the stepper is 30 x 30mm. To minimize overlay errors, the X-ray masks are made of stress-free W-Ti absorber and rigid SiC membrane. We utilized a 30μm proximity gap between the pattern mask and the wafer.

Fig. 3 shows 0.14μm transfer-gate patterns replicated with a 500nm-thick single-layer negative tone resist without any antireflection coating. The patterns are sharp and successfully overlaid on isolation patterns. The resist line widths deviate from the 0.14μm design value by 0.014μm (3σ). Overlay errors in the device pattern in x and y directions were 0.072 and 0.078μm (3σ), respectively. The proximity

*Kyozo Kanamoto, Yasutaka Nishioka and Yasunori Tokuda are with the Advanced Technology R&D Center.

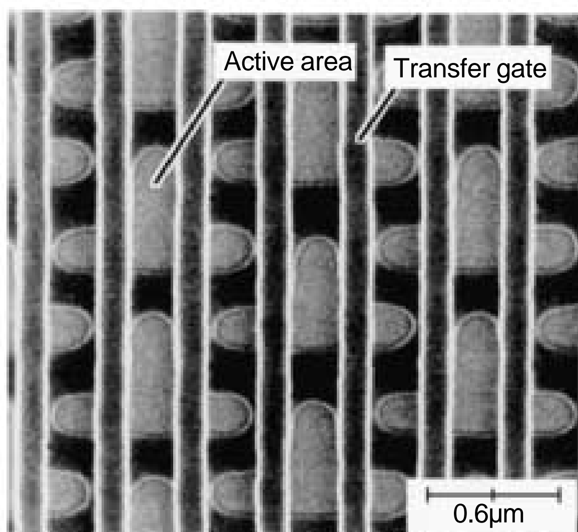


Fig. 3 Transfer gate patterns on isolation patterns.

gap offset margin, which corresponds to the focus margin of optical lithography, was as wide as 25μm. The excellent fine-pattern formation as well as the large gap offset margin illustrates the dramatic advantages of this technique over optical lithography.

Ru/BST/Ru Stacked Capacitor

DRAM capacitor structures must be complicated to achieve sufficient storage capacities when conventional dielectric materials are used in high-density devices.[1] We present a simple stacked capacitor suitable for mass production that employs BST high-dielectric-constant film and Ru metal electrodes. Thick (0.2μm) Ru-metal film for the storage electrodes was deposited by RF sputtering, then defined by magnetically enhanced reactive ion etching using 50nm SiO_2 film as a mask. A high Ru etching to SiO_2 mask selectivity of 20:1 was achieved by using an O_2-based halogen gas mixture. Fig. 4 shows Ru storage node arrays having smooth and almost vertical side walls and a projection area of 0.24 x 0.60μm.

BST films were grown at 420°C by a two-step metal organic chemical vapor deposition method on the Ru storage electrodes. The relatively low-temperature growth is effective for achieving conformal coverage. The films were annealed after each deposition at 700°C in N_2 to improve their crystallinity. A significantly low leakage current density (J_L) of 7 x 10^{-9}A/cm^2 was obtained at V = 1.1V for a 25nm-thick BST film with an SiO_2 equivalent thickness of as low as 0.56nm. Assuming this J_L, the loss of the stored charge for a 1Gb DRAM during a 10s refresh interval is estimated to be less than 10% of the initial charge.

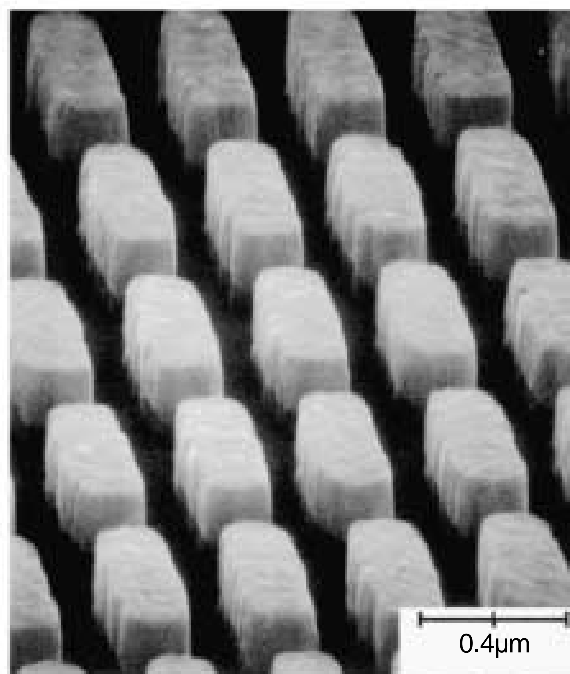


Fig. 4 SEM photograph of an Ru-metal storage node array with a projection area of 0.24 x 0.60μm and a height of 0.2μm.

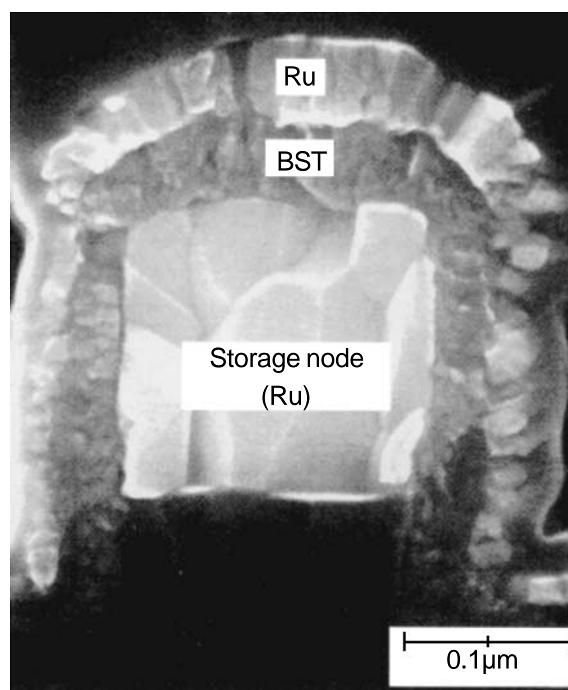


Fig. 5 Cross-sectional SEM photograph of an Ru/BST/Ru capacitor cell.

Fig. 5 shows a cross-sectional SEM of the Ru/BST/Ru stacked capacitor. The step coverage of the BST film was approximately 75%. No degradation of the Ru electrode was observed during the BST film formation.

Fig. 6 shows the relation between the storage capacitance and the electrode height deter-

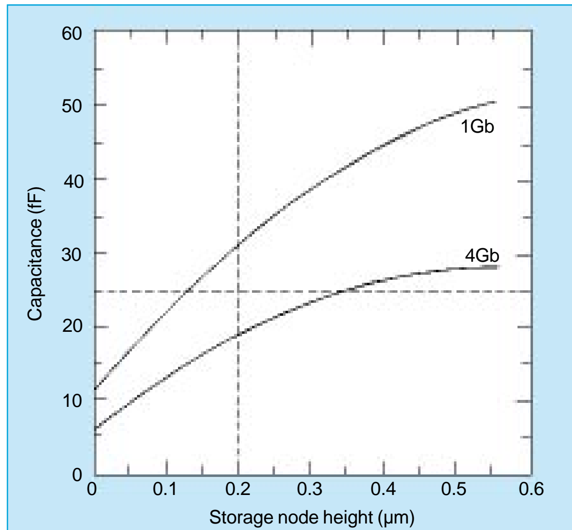


Fig. 6 Relation between storage capacitance and storage node height. The projection area is 0.24 x 0.6µm for a 1Gb device and 0.16 x 0.42µm for a 4Gb device, with teq = 0.56nm.

mined from experimental data. According to this data, the present configuration yields a storage node capacitance of more than 25fF/cell, which is sufficient for 1Gb DRAM devices. The requirement for 4Gb DRAM devices can be satisfied with a storage node higher than 0.35µm.

Fine Pattern Etching

The 0.14µm-wide transfer gate and the 0.14µm-wide trenches were etched by improved electron-cyclotron-resonance-discharge plasmas. The etch selectivity of polysilicon over the gate oxide was more than 50. We also developed a size-independent etching technique with less microloading effects employing beam plasmas generated by a gas-puff plasma source.[3]

The processes developed for fabricating the prototype memory cell structures reported here offer not only unprecedented sharpness and accuracy, but also are excellent candidates for future mass production processes. ❑

References

1. Kaga, T., et al. "A 0.29µm² MIM-Crown Cell and Process Technologies for 1-Gigabit DRAMs." IEDM Technical Digest, p. 927, 1994.
2. Sumitani, H., et al. "Replicating Characteristics by SR Lithography," SPIE International Symposium on Microlithography, p. 2,437, 1995.
3. Oomori, T., Taki, M, Nishikawa, K. and Ootera, H. "Etching for 0.15µm Level Patterns with Low Microloading Effect Using Beam Plasmas Generated by Gas Puff Plasma Sources." Proceedings of 8th International Microprocess Conference, p. 152, 1995.

High-Pin-Count Packaging Technologies for LSI Devices

*by Yoshihiro Tomita and Naoto Ueda**

This report surveys the construction and performance of high-pin-count packages including quad flat packages (QFPs) and ball grid arrays (BGAs) as well as chip-scale packages (CSPs), which represent the next generation of packages.

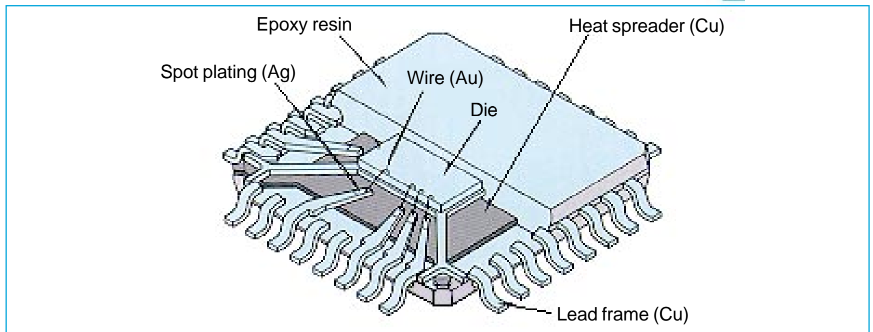


Fig. 1 A copper-lead QFP with a drop-in heat spreader.

Quad Flat Packages

Mitsubishi Electric has developed two high-pin-count QFPs: a 2W-class package employing a copper lead frame and a 3W-class package that adds a drop-in copper heat spreader (Fig. 1). The packages use a 0.5mm lead pitch. The 208-pin version has a 28 x 28mm outline, the 240-pin version a 32 x 32mm outline. By reducing the lead pitch to 0.4mm, this technology will support up to 296 leads. Thinner and smaller QFPs, namely low-profile QFPs (LQFPs), are required as the next generation in this family of packages.

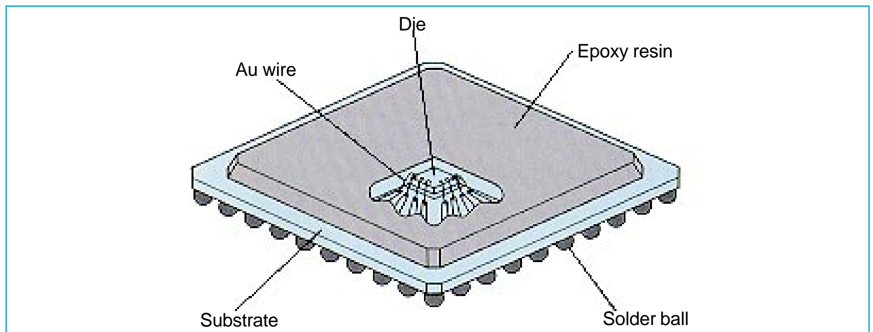


Fig. 2 A molded-plastic BGA package.

Ball Grid Arrays

Fig. 2 shows the construction of a molded-plastic BGA package. The 225-pin package has a 27 x 27mm outline and a pin spacing of 1.5mm. In general, BGAs offer a wider lead pitch, easy soldering and higher density mounting than QFPs. Moreover, as several ICs can be mounted on an internal board during the packaging process, molded-plastic BGAs promote excellent productivity and cost effectiveness.

Molded-plastic BGA packages still face several improvement issues regarding high-pin-count area, such as reducing package warpage, higher moisture-induced crack resistivity and better thermal and electrical characteristics.

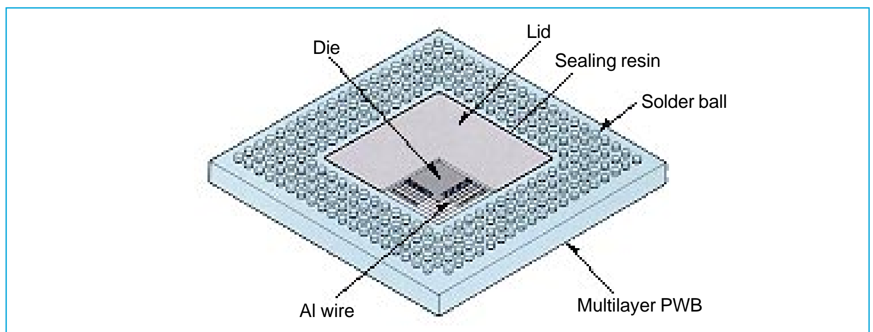


Fig. 3 A cavity BGA package.

Fig. 3 shows the typical package construction of cavity BGAs. The company has developed a 256-pin cavity BGA with a 27 x 27mm outline, and a 520-pin version with a 40 x 40mm outline. The multilayer printed-wiring board (PWB) forms a cavity and provides signal and ground planes. This allows use of a microstrip signal-line structure with the shortest power-supply and ground lines, giving devices low inductance and other desirable electrical characteristics. The thermal via located under the die provides an excellent thermal pathway to an external heat sink, allowing the package to dissipate power levels as high as 7 ~ 8W. Use of aluminum wire with wedge-bonding technol-

*Yoshihiro Tomita and Naoto Ueda are with the Product Engineering Division of the Semiconductor Group.

ogy allows use of closely spaced bonding pads, which contributes to smaller devices. Use of a lid over an open cavity instead of resin encapsulation gives this package greater reliability. We are currently developing versions with approximately 700 pins. Reducing the cost of the multilayer PWB will be a production issue.

Performance Comparison

Table 1 compares the thermal and electrical characteristics of all these packages as calcuted by simulation. The allowable power dissipation figures are based on air cooling at 1.0m/s. The heat-spreader QFP and cavity BGA offer similar dissipation, with the molded BGA somewhat less capable. Cavity BGA packages with attached heat sinks offer the best thermal performance. In terms of electrical characteristics, low inductance means better signal integrity, which allows higher operating frequencies, and maximum and minimum inductance values reflect wiring layout variations.

The cavity BGA offers the lowest inductance, followed by the molded BGA and copper-frame QFP packages. All the new packages offer better thermal and electrical characteristics than conventional plastic packages with ferroally lead frames.

Table 1 Performance of High-Pin-Count Packages

Type	Package	Body size (mm)	Lead pitch (mm)	Power dissipation (1m/s cooling)	Inductance (nH, 1MHz)
PQFP (Fe lead frame)	160-pin	28	0.5	< 1W	12.1~16.1
PQFP (Cu lead frame)	208-pin	28	0.5	2W	10.6~13.4
	208-pin with drop-in heat spreader	28	0.5	3W	9.7~12.3
	240-pin	32	0.5	2.5W	12.1~15.1
	240-pin with drop-in heat spreader	32	0.5	3.5W	9.4~11.4
BGA	225-pin molded	27	1.5	2W	7.5~14.4
	256-pin cavity with heat sink	27	1.27	3W	3.4~8.3
	520-pin cavity with heat sink	41	1.27	7W	4.4~9.7

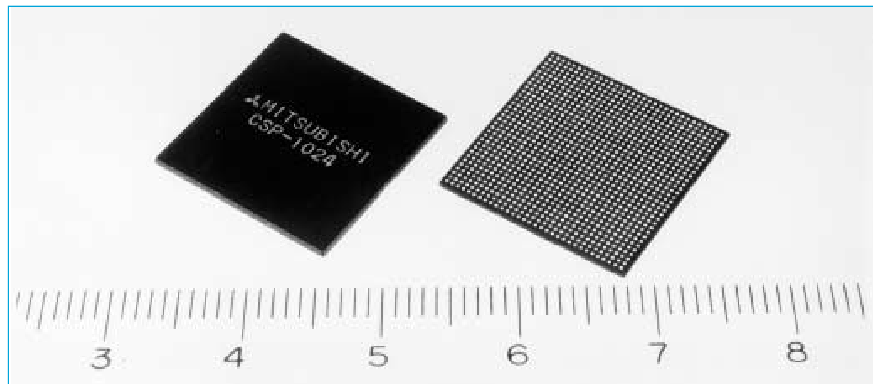


Fig. 4 A 1,024-pin CSP.

Chip-Scale Packages

This new, compact package technology is under development at Mitsubishi Electric with the aim of providing an alternative way for burned-in and tested "known-good devices" (KGDs) close to the size of bare dice. Fig. 4 shows a photo of a manufactured CSP test-package. The solder bumps are spaced at 0.5mm, allowing a pin count of 1,024 in a 16.6 x 16.6mm package that accomodates a 16 x 16mm die. We provide transfer molding technology with this package to enhance its reliability. The CSPs can be mounted using existing technologies, and new methods based on flip-chip bonding and narrow-pitch printed solder bumps are under development. Use of printed solder bumps offers the advantage of constant cost, regardless of pin count. Flip-chip mounting results in short wiring lengths, giving a lower inductance than other mounting methods.

CSP will be well suited to fabrication of multichip modules, since it provides KGDs; however, making connections to the solder-bump array requires use of sophisticated multilayer PWBs with extremely fine conductors. Mounting design and technology infrastructure for this package need to be established before it can enter wide use. ❑

A Figure-Fracturing Algorithm for Generating High-Quality Electron-Beam Exposure Data

*by Hiroomi Nakao and Koichi Moriizumi**

Mitsubishi Electric has developed a figure-fracturing algorithm for generating exposure data in variable-shaped electron-beam mask production. The new algorithm dramatically improves LSI mask pattern accuracy and reduces the time required for mask pattern generation. It is being applied to the fabrication of 256Mb DRAM and other high-density semiconductor devices.

Background

Variable-shaped electron-beam exposure systems are widely utilized for LSI mask fabrication because of their high-speed exposure capability. For the input data of the system, which is called electron-beam (EB) exposure data, only trapezoids are allowed as exposure figures, while the original data of the layout design is comprised of complicated polygons. Each polygon in the layout must therefore be partitioned into trapezoids. This process, which we call figure-fracturing, is one of the most important steps in the generation of EB exposure data (Fig. 1) because the dimension accuracy of the fabricated mask pattern depends greatly on the results of this step.

The loss of accuracy due to a poor figure-fracturing algorithm becomes especially significant in fine-pattern devices such as 256Mb DRAMs. Our algorithm was developed to ensure near optimal choices for polygon partitioning.

Features

The algorithm we developed has three key functions, making it much more advanced and effective than previous methods.

First, the generation of narrow figures that degrade pattern accuracy is avoided (Fig. 2). The advantages of this optimization are well known, but only the simplest implementations have been reported.

Second, is an original function developed by the authors. Polygons are partitioned so that gate electrodes and others mask features that demand especially tight width tolerances are not partitioned (Fig. 3). We call these mask features "critical parts." This optimization improves the dimension accuracy of critical parts because each part can be exposed with a single electron-beam shot.

Third, the number of trapezoids is minimized, which reduces the

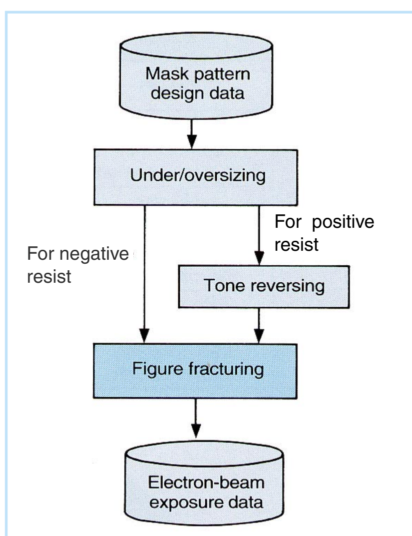


Fig.1 The process of generating electron-beam exposure data.

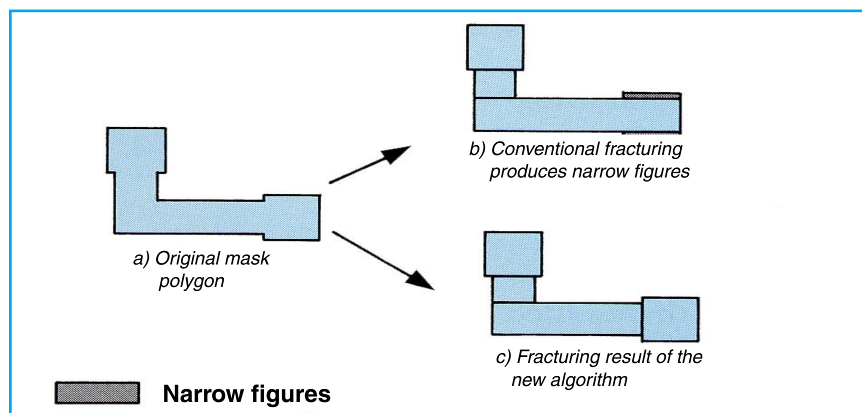


Fig. 2. Avoiding narrow figure generation.

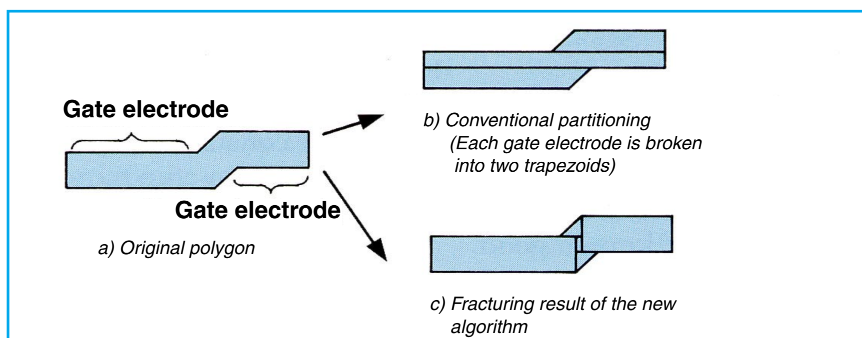


Fig. 3 Partitioning of gate electrodes.

**Hiroomi Nakao is with the System LSI Laboratory and Koichi Moriizumi with the Product Engineering Division of the Semiconductor Group.*

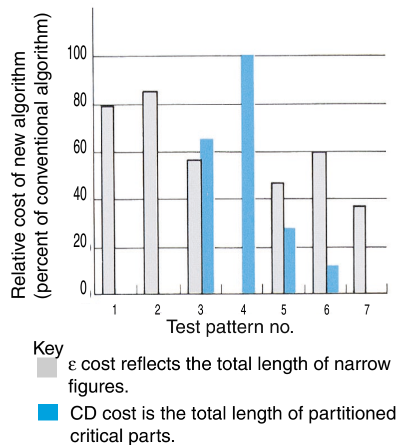


Fig. 4 Comparison of ε and CD costs of conventional and new algorithms. Zeros indicate where the cost of the new algoririthm is zero.

time the electron-beam system requires to generate the pattern.

The algorithm performs these optimizations by constructing a bipartite graph that represents "touch" and "cross" relations between all possible vertical and horizontal partitioning lines. This graph ensures near-optimal solutions since nearly all partitioning possibilities can be taken into a account.

Application Results

We used the algorithm to generate mask exposure data for a 64Mb DRAM device. As shown in Fig. 4, the algorithm reduces the ε cost and the CD cost to less than half of the conventional method, where ε cost is the penalty associated with narrow figure generation, and CD cost is the penalty associated with breaking up critical parts. Fig. 5 shows an example of partitioning by our algorithm.

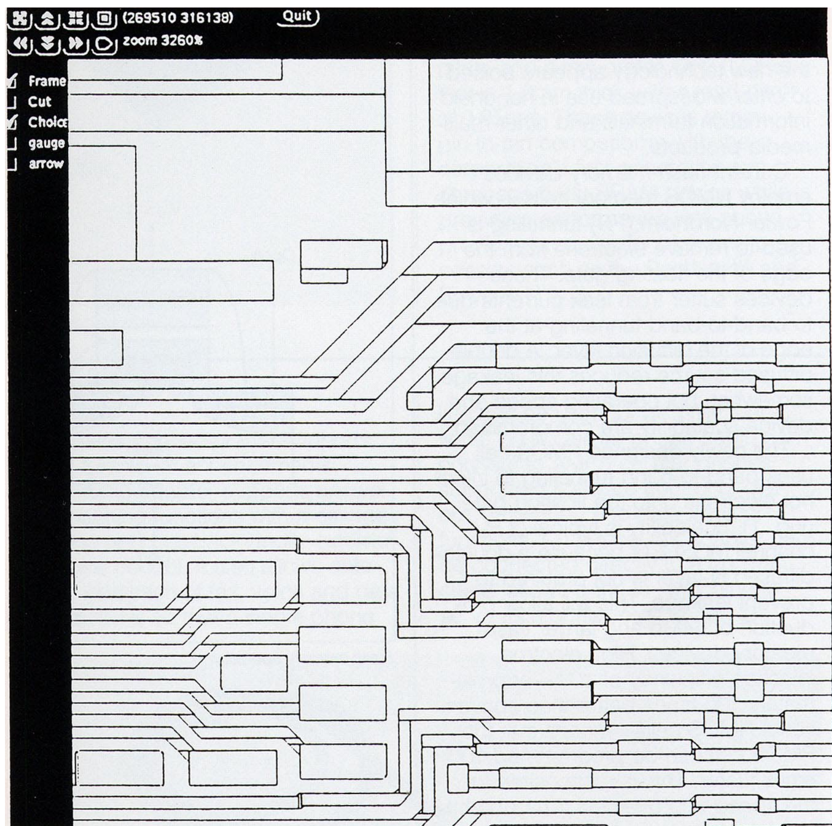


Fig. 5 Typical fracturing result.

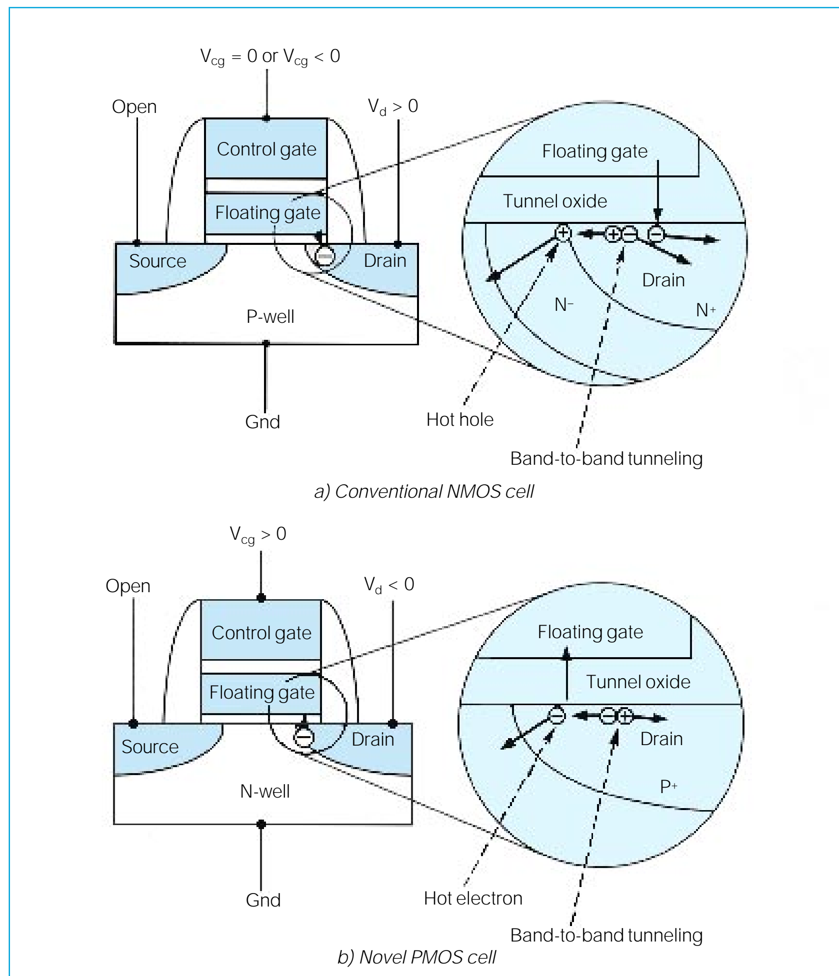
Increasingly small microelectronic devices demand LSI masks of ever greater accuracy. The algorithm presented here helps satisfy this requirement, and is being applied to the fabrication of state-of-the-art devices. ❑

A Novel PMOS Memory Cell for Flash Memory of 64Mb and Larger

Mitsubishi Electric has developed an efficient, high-speed PMOS-based memory cell suitable for fabricating high-density flash-memory devices of 64Mb and larger. The cell features a divided bit-line NOR flash-memory structure that permits programming at speeds 100 times faster than current flash-memory devices. Prototype devices based on the new technology demonstrated high-speed programming at 60ns/byte with a low power consumption of less than 1mA. With all of these advantages, the new technology appears poised to enter widespread use in handheld information terminals and other multimedia products.

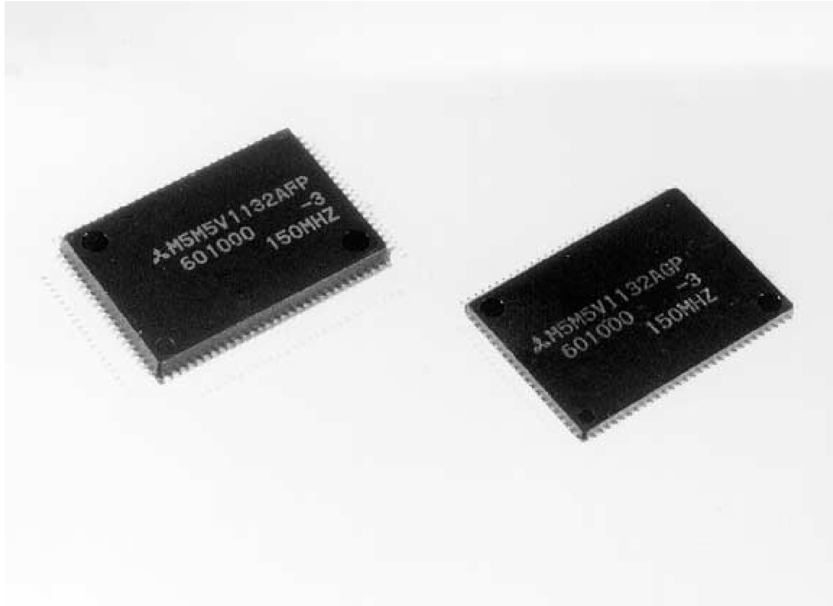
Current flash-memory devices employ NMOS memory cells in which Fowler-Nordheim (FN) tunneling is used to remove electrons from the edge of the floating gate. These devices suffer from leak currents due to band-to-band tunneling at the edge of the diffusion layer. A double-diffused source reduces this leakage somewhat, but operating speed and device scalability are compromised.

The newly designed PMOS cell uses band-to-band tunneling to inject hot electrons onto the floating gate (Fig. 1). Scalability is typical of P-channel MOSFETs because a double-diffused N-layer is not required to prevent leakage. This will allow production of 64Mb and larger flash-memory devices. High electron injection efficiency of 10^{-2}—approximately 100 times better than conventional NMOS cells—means that the PMOS cell can be programmed 100 times faster. This is responsible for the speed improvement. The durability of the tunnel oxide layer is also much improved, since hot-hole injection is suppressed, and since the lower supply voltage reduces stress on the oxide layer. ❑



Flash memory operation.

Second-Generation 32Kword x 32b 150MHz Synchronous-Burst SRAM Devices

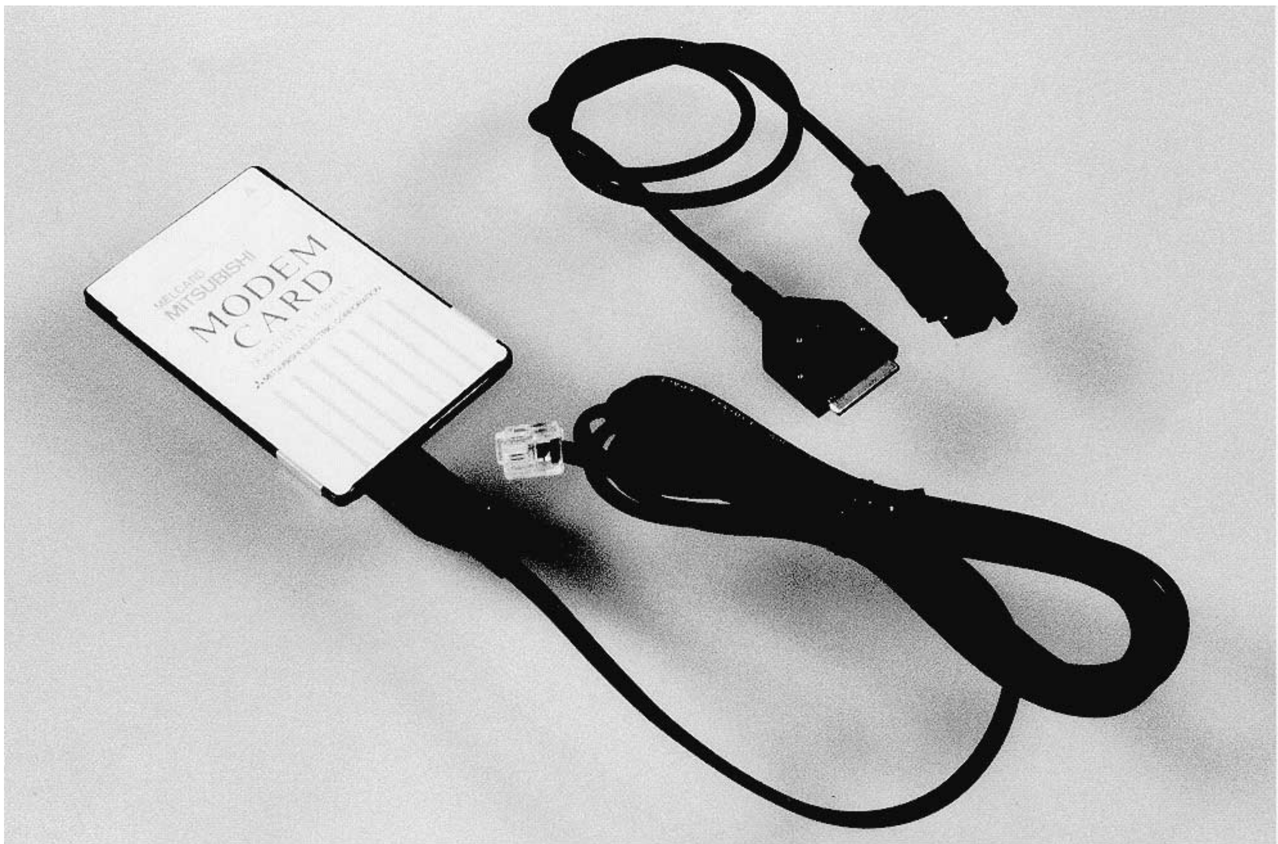


Second-genration 32Kw x 32b, 150MHz synchronous-burst SRAM devices.

Mitsubishi Electric has developed 32Kw x 32b synchronous-burst SRAM devices with maximum access times of 3.0ns and maximum clock frequencies of 150MHz. The devices are based on a 0.4µm CMOS process with three polysilicon layers and two metalization layers. To meet the secondary cache requirements of high-performance microprocessors, the new memory devices are designed for 3.3V operation, low maximum current drain of 290mA, and 2.5V or 3.3V I/O. Packages include a 14.0 x 20.0mm 100-pin quad flat package (QFP) with a 0.65mm lead pitch, and a low-profile QFP (LQFP) that is 1.6mm thick with a lead pitch of 0.65mm. These devices retain pin-to-pin compatibility with the corporation's first-generation synchronous-burst SRAM device while providing performance well above previous products for high-end processors such as the Pentium(TM) and PowerPC(TM). ❑

A V.34 PCMCIA Voice/Fax/Modem Card

Mitsubishi Electric has developed a PCMCIA/JEIDA add-on card for notebook computers that combines 28.8Kbps V.34 modem, Group III fax, and voice-mail functions. A built-in telephone line interface makes the card easier to use and more portable than predecessors. It also has an expansion connector that supports three functional enhancements:
(1) A voice adapter supports answering machine functions with message storage and playback under external software control. It also allows automatic detection of fax, voice and data connections so that a single phone line can be used for all three functions. (2) A cellular phone cable can connect to AMPS cellular phones, supporting software control of dial-out, answering and data transfer functions. (3) A local fax adaptor can be connected directly to a fax machine, allowing the fax machine to serve as a printer or scanner. ❑



The V.34 PCMCIA modem card and adapters.

MITSUBISHI ELECTRIC OVERSEAS NETWORK (Abridged)

Country	Address		Telephone
U.S.A.	Mitsubishi Electric America, Inc.	5665 Plaza Drive, P.O. Box 6007, Cypress, California 90630-0007	714-220-2500
	Mitsubishi Electronics America, Inc.	5665 Plaza Drive, P.O. Box 6007, Cypress, California 90630-0007	714-220-2500
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	Astronet Corporation	37 Skyline Drive, Suite 4100, Lake Mary, Florida 32746-6214	407-333-4900
	Powerex, Inc.	Hills Street, Youngwood, Pennsylvania 15697	412-925-7272
	Mitsubishi Electric Research Laboratories, Inc.	201 Broadway, Cambridge, Massachusetts 02139	617-621-7500
Canada	Mitsubishi Electric Sales Canada Inc.	4299 14th Avenue, Markham, Ontario L3R 0J2	905-475-7728
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Mexico	Melco de Mexico S.A. de C.V.	Mariano Escobedo No. 69, Tlalnepantla, Edo. de Mexico	5-565-6269
Brazil	MELCO do Brazil, Com. e Rep. Ltda.	Av. Rio Branco, 123, a 1507, 20040, Rio de Janeiro	21-221-8343
	MELCO-TEC Rep. Com. e Assessoria Tecnica Ltda.	Av. Rio Branco, 123, a 1507, 20040, Rio de Janeiro	21-221-8343
Argentina	MELCO Argentina S.R.L.	Florida 890-20º-Piso, C.P. 1005, Buenos Aires	1-312-6982
Colombia	MELCO de Colombia Ltda.	Calle 35 No. 7-25, Oficinas No. 1201/02, Edificio, Caxdac, Apartado Aereo 29653, Bogotá	1-287-9277
U.K.	Mitsubishi Electric U.K. Ltd.	Travellers Lane, Hatfield, Herts. AL10 8XB, England	707-276100
	Apricot Computers Ltd.	3500 Parkside, Birmingham Business Park, Birmingham, B37 7YS, England	21-717-7171
	Mitsubishi Electric Europe Coordination Center	Centre Point (18th Floor), 103 New Oxford Street, London, WC1A 1EB	71-379-7160
France	Mitsubishi Electric France S.A.	55, Avenue de Colmar, 92563, Rueil Malmaison Cedex	1-47-08-78-00
Netherlands	Mitsubishi Electric Netherlands B.V.	3rd Floor, Parnassustoren, Locatellikade 1, 1076 AZ, Amsterdam	20-6790094
Germany	Mitsubishi Electric Europe GmbH	Gothaer Strasse 8, 40880 Ratingen	2102-4860
	Mitsubishi Semiconductor Europe GmbH	Konrad Zuse Strasse 1, 52477 Alsdorf	2404-990
Spain	MELCO Iberica S.A. Barcelona Office	Polígono Industrial "Can Magi", Calle Joan Buscallà 2-4, Apartado de Correos 420, 08190 Sant Cugat del Vallés, Barcelona	3-589-3900
Italy	Mitsubishi Electric Europe GmbH, Milano Office	Centro Direzionale Colleoni, Palazzo Persero-Ingresso 2, Via Paracelso 12, 20041 Agrate Brianza, Milano	39-60531
China	Shanghai Mitsubishi Elevator Co., Ltd.	811 Jiang Chuan Rd., Minhang, Shanghai	21-4303030
Hong Kong	Mitsubishi Electric (H.K.) Ltd.	41st Floor, Manulife Tower, 169 Electric Road, North Point	510-0555
	Ryoden Holdings Ltd.	10th Floor, Manulife Tower, 169 Electric Road, North Point	887-8870
	Ryoden Merchandising Co., Ltd.	32nd Floor, Manulife Tower, 169 Electric Road, North Point	510-0777
Korea	KEFICO Corporation	410, Dangjung-Dong, Kunpo, Kyunggi-Do	343-51-1403
Taiwan	MELCO Taiwan Co., Ltd.	2nd Floor, Chung-Ling Bldg., No. 363, Sec. 2, Fu-Hsing S. Road, Taipei	2-733-2383
	Shihlin Electric & Engineering Corp.	No. 75, Sec. 6, Chung Shan N. Rd., Taipei	2-834-2662
	China Ryoden Co., Ltd.	Chung-Ling Bldg., No. 363, Sec. 2, Fu-Hsing S. Road, Taipei	2-733-3424
Singapore	Mitsubishi Electric Singapore Pte. Ltd.	152 Beach Road #11-06/08, Gateway East, Singapore 189721	295-5055
	Mitsubishi Electric Sales Singapore Pte. Ltd.	307 Alexandra Road #05-01/02, Mitsubishi Electric Building, Singapore 159943	473-2308
	Mitsubishi Electronics Manufacturing Singapore Pte. Ltd.	3000, Marsiling Road, Singapore 739108	269-9711
	Mitsubishi Electric Asia Coordination Center	307 Alexandra Road #02-02, Mitsubishi Electric Building, Singapore 159943	479-9100
Malaysia	Mitsubishi Electric (Malaysia) Sdn. Bhd.	Plo 32, Kawasan Perindustrian Senai, 81400 Senai, Johor	7-5996060
	Antah MELCO Sales & Services Sdn. Bhd.	3 Jalan 13/1, 46860 Petaling Jaya, Selangor, P.O. Box 1036	3-756-8322
	Ryoden (Malaysia) Sdn. Bhd.	2nd Fl., Wisma Yan, Nos. 17 & 19, Jalan Selangor, 46050 Petaling Jaya	3-755-3277
Thailand	Kang Yong Watana Co., Ltd.	15th Floor, Vanit Bldg., 1126/1, New Petchburi Road, Phayathai, Bangkok 10400	2-255-8550
	Kang Yong Electric Co., Ltd.	67 Moo 11, Bangna-Trad Highway, Km. 20 Bang Plee, Samutprakarn 10540	2-312-8151
	MELCO Manufacturing (Thailand) Co., Ltd.	86 Moo 4, Km. 23 Bangna-Trad, Bangplee, Semudparkarn 10540	2-312-8350~3
	Mitsubishi Elevator Asia Co., Ltd.	Bangpakong Industrial Estate, 700/86~92, Moo 6 Tambon Don Hua Roh, Muang District Chonburi 20000	38-213-170
	Mitsubishi Electric Asia Coordination Center (Thailand)	17th Floor, Bangna Tower, 2/3 Moo 14, Bangna-Trad Highway 6.5 Km, Bangkawe, Bang Plee, Samutprakarn 10540	2-312-0155~7
Philippines	International Elevator & Equipment, Inc.	Km. 23 West Service Road, South Superhighway, Cupang, Muntinlupa, Metro Manila	2-842-3161~5
Australia	Mitsubishi Electric Australia Pty. Ltd.	348 Victoria Road, Postal Bag No. 2, Rydalmere, N.S.W. 2116	2-684-7200
New Zealand	MELCO Sales (N.Z.) Ltd.	1 Parliament St., Lower Hutt, P.O. Box 30-772 Wellington	4-569-7350
Representatives			
China	Mitsubishi Electric Corp. Beijing Office	SCITE Tower, Rm. 1609, Jianguo Menwai, Dajie 22, Beijing	1-512-3222
	Mitsubishi Electric Corp. Shanghai Office	Room No. 1506-8, Shanghai Union Building 100, Yanan-East Street, Shanghai	21-320-2010
Korea	Mitsubishi Electric Corp. Seoul Office	Daehan Kyoyuk Insurance Bldg., Room No. 1204 #1, Chongno 1-ka, Chongno-ku, Seoul	2-732-1531~2
Viet Nam	Mitsubishi Electric Corp. Ho Chi Minh City Office	8 B2, Han Nam Officetel 65, Nguyen Du St., 1st District, Ho Chi Minh City	8-243-984

MITSUBISHI ELECTRIC CORPORATION
HEAD OFFICE: MITSUBISHI DENKI BLDG., MARUNOUCHI, TOKYO 100-8310, FAX 03-3218-3455