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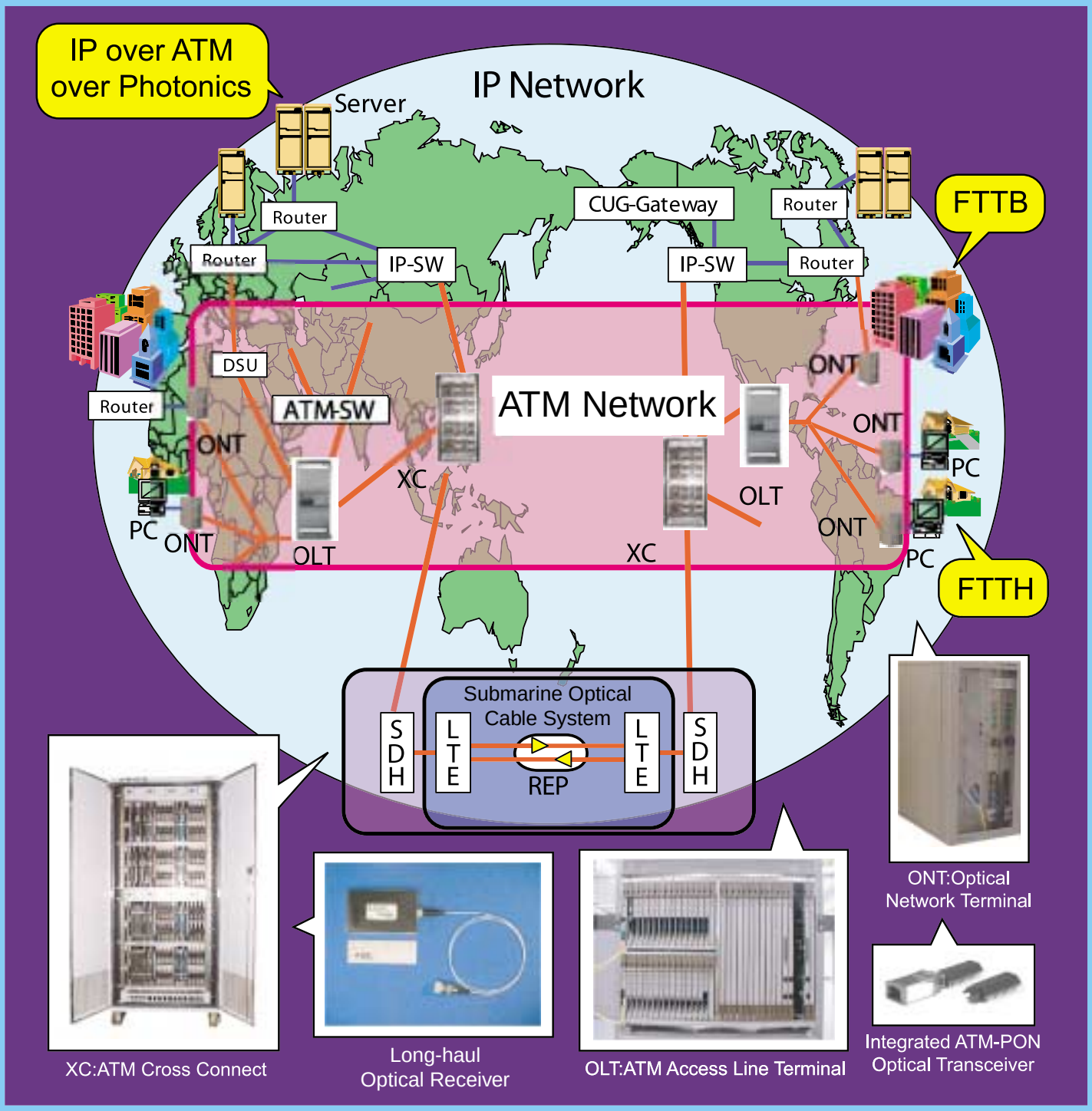
ATM Edition



MITSUBISHI ELECTRIC

A Quarterly Survey of New Products, Systems, and Technology
●Vol. 93/March 2001 Mitsubishi Electric **ADVANCE**

ATM Edition

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Cover Story
Our cover illustrates how Mitsubishi Electric has taken the concept of IP over ATM over photonics as the basis for the backbone of next-generation Internet communications, and is developing the related ATM network systems and the necessary IP communication equipment and optical devices.

Editorial Inquiries

Keizo Hama
Corporate Total Productivity Management & Environmental Programs
Mitsubishi Electric Corporation
2-2-3 Marunouchi
Chiyoda-ku, Tokyo 100-8310, Japan
Fax 03-3218-2465

Product Inquiries

Yasuhiko Kase
Global Strategic Planning Dept.
Corporate Marketing Group
Mitsubishi Electric Corporation
2-2-3 Marunouchi
Chiyoda-ku, Tokyo 100-8310, Japan
Fax 03-3218-3455

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Scope of ATM Network System

*by Katsuaki Kikuchi**

This article describes the system architecture and features of the ATM backbone network that will provide the multimedia communications underpinning the next-generation Internet. It also describes the new service network that is built into the ATM backbone network.

Issues Facing the Next-Generation Telecommunications Network

The Internet has experienced explosive growth since it began commercial services in North America in the 1980s and now handles not only data traffic but also traffic for applications such as telephone, video, and entertainment software that require responses in near real time. In the future, we can anticipate application of the Internet to electronic commerce, and remote education and medical treatment, requiring further advances in the Internet as the foundation for service industries requiring even higher levels of real-time responsiveness and reliability. This new Internet will have major repercussions on existing communications networks, and qualitative and quantitative changes in traffic, increases in access speed, redesign of communications billing systems and the like include elements that will dramatically change the structure of conventional telecommunications networks. One of the critical issues facing network operators is that of providing cost effective network capability sufficient for the explosive growth in demand for data traffic while still providing the quality of service that will set them apart from other firms. If they are to succeed in these ends, the network operators will have to make a critical decision about the type of architecture to use in the next-generation network. The choice of whether to create a new network infrastructure centering on IP services, or whether to evolve from the existing networks focusing on multiple services including existing services, is also critical.

In order to respond to the rapid growth of high-speed/wide-band communications accompanying increasing use of multimedia applications, the major network operators (including NTT) are pushing to move to integrated/backbone networks using ATM communications technology. ATM communications technology has the benefits of (1) uniformly handling multimedia data of all different speeds, (2) high-speed non-hierarchical multiplexing/switching, (3) superior control of the quality of service, etc, making it possible to structure an ATM backbone network that will integrate the handling of the multimedia communications services of the future. In networks that handle data traffic, network integration using ATM communications technologies will be particularly useful because the requirements for communications quality differ depending on the type of data handled.

Mitsubishi Electric has been championing technology development from a global perspective taking the latest market trends into account, and even in the coming age of IP-centric communications, the corporation wants to be sure that it continues to provide the optimal value-adding solution.

With the basic concept behind the next-generation network structure being "IP over ATM over photonics and wireless," the development of the backbone network and of the next-generation Internet will provide the foundation for the creation and development of new communications markets.

Next-Generation Communications Network Architecture

Research is underway worldwide on a variety of issues related to network architecture, issues such as reliability, safety, and quality - in addition to higher access speeds - allowing the network of today to become the foundation for social and economic activities in the future. One critical area of research is the form that the IP telecommunications infrastructure should take. The critical debates around this issue focus on the following (see Fig. 1):

- IP over asynchronous transfer mode (ATM)
- IP over synchronous digital hierarchy (SDH)
- IP over wavelength division multiplexing (WDM)

In terms of the general characteristics, from the perspective of the communications network

**Katsuaki Kikuchi is with Communication Systems R&D Center.*

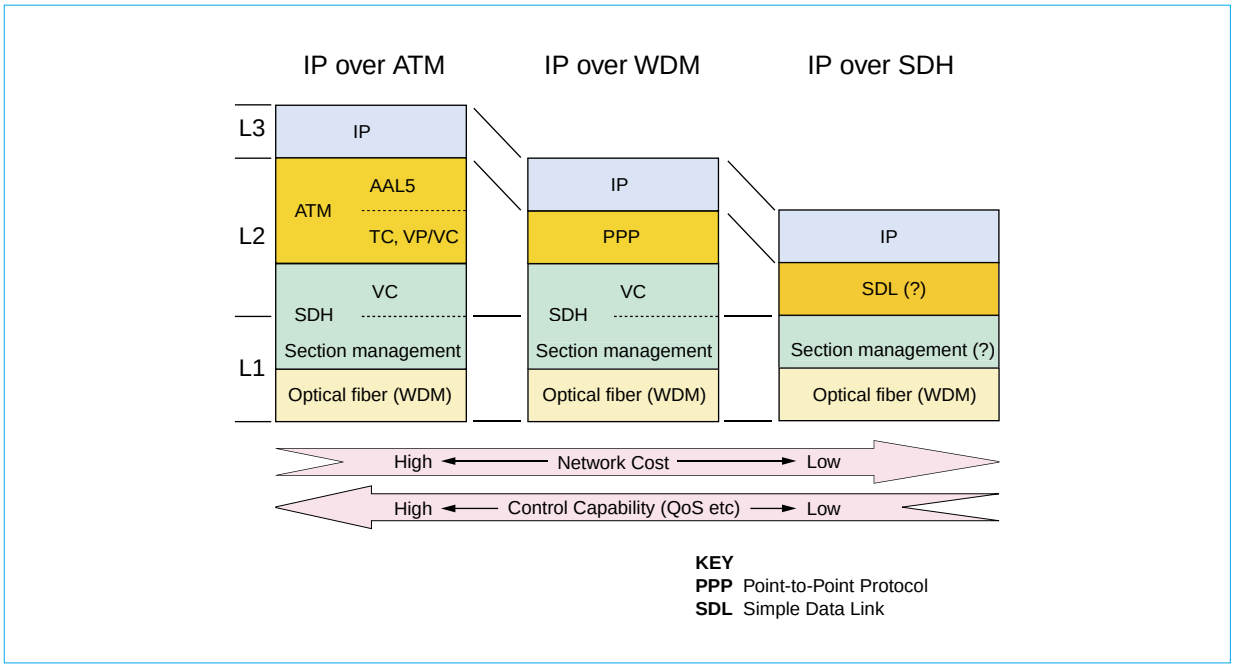


Fig. 1 Issues to be resolved in the backbone network.

structure, IP over WDM, which has the simplest protocol stack, has the potential for the greatest network cost reductions, while the IP over ATM approach would be useful in providing sophisticated network services such as virtual private networking (VPN) because of its excellent control capabilities.

Communications network cost reductions will be critically important in the future, and the simplification of network structures is essential. A key to these simplified structures will be to jettison the current multiplexing structures that are based on SDH. The essence of the ATM technology is non-hierarchical multiplexing, which does not require SDH multiplexing structures. Note that this approach is not in conflict with the approach of creating ATM network structures. If we reexamine the protocol stack from this perspective, the protocols can be summarized as shown in Fig. 2. The future of IP over WDM is a focus of current research, where the options at this point are:

- IP/ATM/STM Frame/WDM
- IP/PPP/STM Frame/WDM

These are compared in Fig. 3. IP over WDM has benefits in terms of transmission efficiency, while IP over ATM has benefits in terms of the control of quality of service and in terms of network services. However, it is essential to increase the speed of access for the Internet of the future, and because the application of ATM technology is anticipated to be important in the future of access systems, IP over ATM is a superior solution from the perspective of access system compatibility.

ATM Backbone Networks

ATM system services such as “megalink services” (which are ATM leased-line services), “shared link services” and “cell relay services” (which are forms of ATM switching services) are expanding steadily. In Japan, NTT is promoting the construction of an ATM backbone network as the shared foundation for these services, where, as shown in Fig. 4, this ATM backbone network will comprise an ATM switching system (which has virtual path/virtual channel (VP/VC)) handling functions, an ATM cross-connect system (which has VP handling functions),

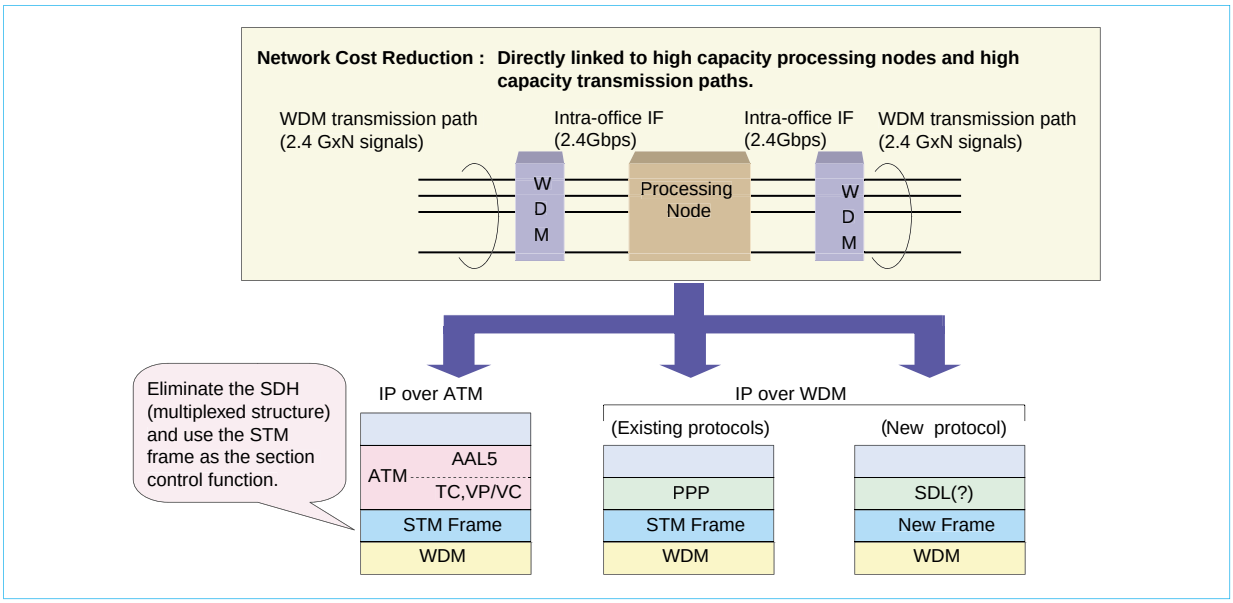


Fig. 2 Protocol structure for backbone network simplification.

and an ATM access system (which provides integrated access functions for the various services) in a structure with the three-part network element (NE), NE-OpS, and network-OpS (NW)-OpS structure.

THE ATM CROSS-CONNECT SYSTEM. The basic function of the ATM cross-connect system is efficient VP setup, and in the network it has the role of providing the structure of VP bundled with VC on the network and providing the structure that supplies direct-connect VP between end users. This equipment has a system configuration that is easily scalable, is able to provide a high-speed ATM interface, and makes it possible to structure an ATM backbone network economically.

	IP over ATM	IP over WDM	
Transmission efficiency	△	○	No particular difference.
Quality of service	○	×	At present, it is better to use the ATM layer.
Network services (VPN, etc.)	○	×	
Compatibility with access networks	○	×	Access systems in the future will use primarily ATM.
Ultra high speed processing nodes	△	△	No particular differences in feasibility or cost.

KEY
○ - Advantageous △ - Comparable × - Disadvantageous

Fig. 3 IP over ATM vs. IP over WDM.

ATM ACCESS SYSTEMS. These can transmit all speeds of signals efficiently while providing indispensable cost reductions, and there are calls for it to become the integrated access platform for all types of services.

The ATM-passive optical network (PON) technology, which is becoming the international standard in, for example, full service access networks (FSANs), is used to reduce the cost of access systems. This technology is equipped with sophisticated traffic control functions for supporting a variety of quality-of-service classes.

Next-Generation IP Networks

Fig. 5 shows the structure of the next-generation IP network conceived by Mitsubishi Electric. Faster access speeds will be important in the next-generation Internet, and there is the

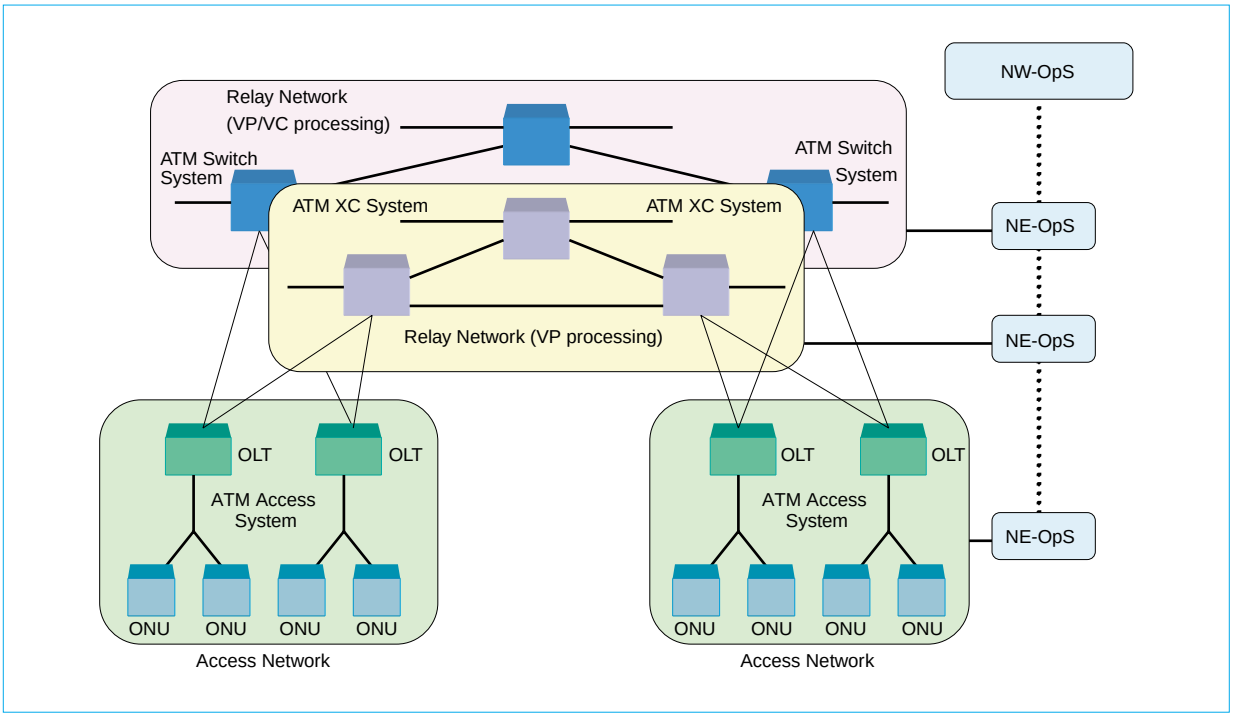


Fig. 4 ATM backbone network structure.

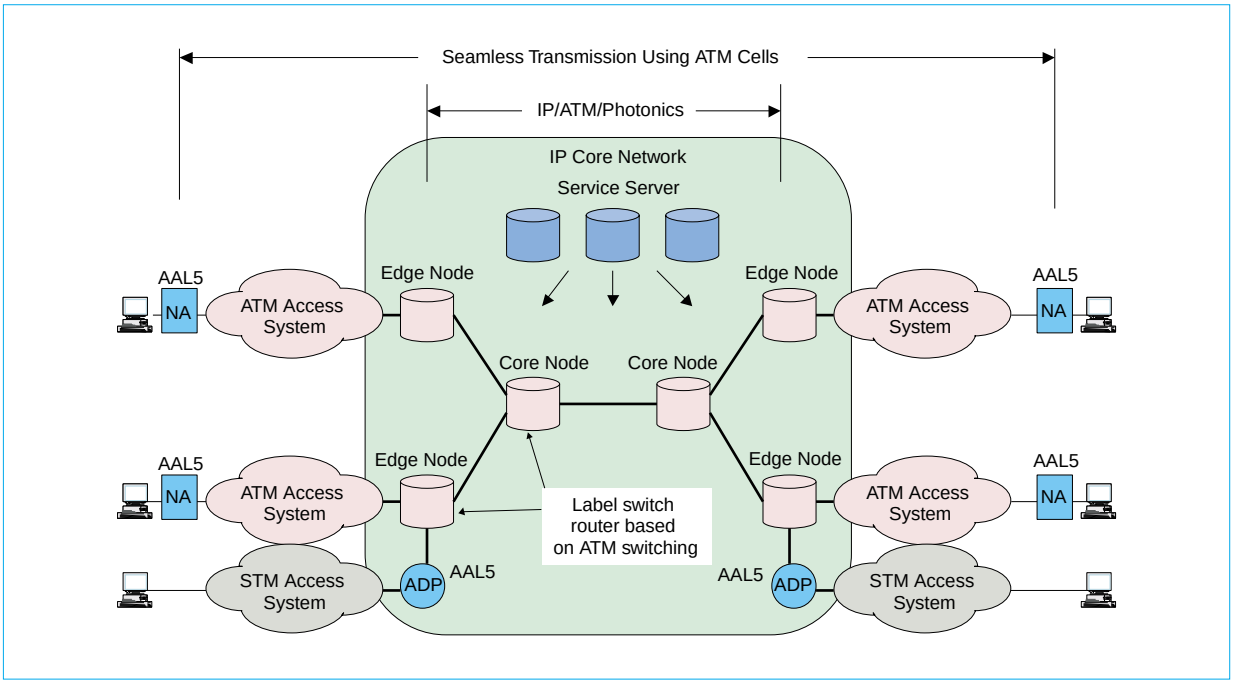


Fig. 5 Next-generation IP network concept.

potential for a variety of different access methods, such as fiberoptic access, metallic access, and wireless access to provide the faster access. However, ATM technology is central, and integrated access to IP services and ATM-system services (which will be at the heart of the high-speed/wide-band services of the future) is now a reality. The IP core network will be structured on the ATM backbone network, and will be equipped with core nodes and edge nodes structured from label switch routers (LSRs) that have IP packet routing functions. Furthermore, it is likely that a variety of service servers, such as gateway servers and policy servers, will be necessary as a result of the development of a variety of services in the future.

Not only will the IP core network need to provide minimal delay times and high throughputs through high-speed cut-through transmission, but will also have to provide a variety of quality-of-service levels. This architecture can provide seamless transmission using end-to-end ATM cells, and can provide for variety in QoS.

Even though the GMN-CL, proposed by NTT, uses as its core protocol a base of IPv6 in the IP core network, the use of MPLS in the future looks promising.

Whatever choices are made, the next-generation communications network centering on IP will need to make steady progress, where Mitsubishi Electric feels that it will be critical to continue to provide products with high levels of added value, and to continue to respond to the requests of its customers.❑

ATM Cross Connect System

*by Hiroyoshi Inoue**

Mitsubishi Electric Corporation has developed a large-capacity ATM cross-connect system (ATM-XC) supporting ATM backbone networks. Its role is to distribute multiplexed virtual paths (VPs) by destination.

The ATM-XC, which connects to ATM switching systems (ATM-SW) and ATM access systems (ATM-OLT), achieves a maximum throughput of 20Gbps. With intra-office and inter-office interfaces of 150Mbps, 600Mbps and 2.4Gbps, it has functions for multiplexing, demultiplexing and routing across interfaces in VP units.

Features

Major features of the new ATM cross-connect system include its high throughput, scalability and reliability. It incorporates large-capacity ATM switch circuits to realize throughput of up to 20Gbps. It expands readily from the basic configuration of two upper units (sub-racks), with each cabinet housing up to four units. The transmission capacity can be enhanced in 2.4Gbps steps by adding one MUX block which multiplexes and demultiplexes signals from/to 16 × 150Mbps interfaces.

Examples of the interfaces accommodated per unit are given below:

- 150Mbps interfaces: 128 single (all-simplex), 64 sets (all-duplex)
- 600Mbps interfaces: 32 single (all-simplex), 32 sets (all-duplex)
- 2.4Gbps interfaces: 8 single (all-simplex), 8 sets (all-duplex)

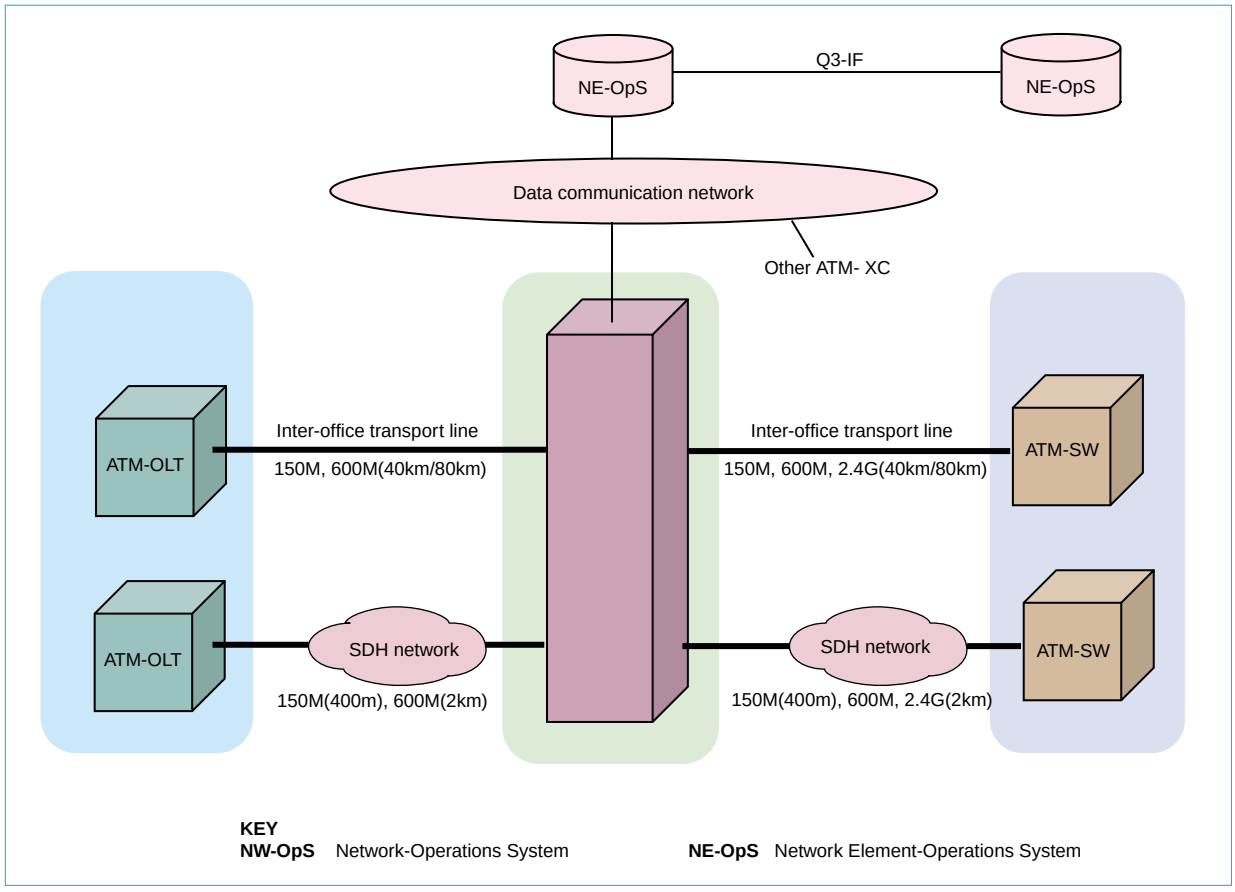


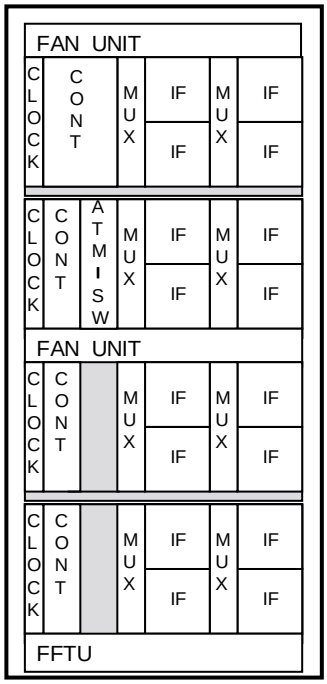
Fig. 1 A typical ATM backbone network.

**Hiroyoshi Inoue is with Communication Systems Business Division.*

A redundant configuration is adopted for high reliability, featuring 1+1 MS protection and VP protection.

VP-OAM functions are provided for alarm transfer, performance monitor, loopback test and continuity characteristics measurement. Remote operation, administration and maintenance is possible from an NE-OpS. By storing operations data in backup memory, the system can restart itself automatically after a power off or when a package is replaced.

In addition, the latest semiconductor-device technology is applied to achieve high integration and low power dissipation.



KEY

CLOCK	Clock block
CONT	Control and supervisory block
ATM-SW	ATM switch block
MUX	Multiplexing and demultiplexing block
IF	Interface block
FFTU	Fuse/Filter/Terminal Unit

Fig. 2 ATM-XC device configuration.

Fig. 3 Appearance of the ATM-XC.

The corporation is committed to developing an ongoing series of subsystems that will support the smooth upgrade of ATM services, which are sure to power many of the burgeoning needs of the information oriented society.❑

ATM Access System Using APON Technology

*by Hiroyuki Ueda**

Mitsubishi Electric Corporation has developed an ATM access system for the North American market, applying ATM passive optical network (APON) technology based on international standards given in the International Telecommunication Union (ITU-T) recommendations.

By running optical fiber lines to corporate offices fiber to the business (FTTB) or to ordinary households fiber to the home (FTTH) and applying APON technology with this system, it is possible to replace the existing synchronous transfer mode (STM) channels serving large numbers of subscribers and provide fast, high-quality Internet services economically.

Features of the units making up the access system are outlined below:

1. ATM-OLT (product name: ADS2000)
- Interfaces: DS-3 (45Mbps), OC-3c 155Mbps, APON 155Mbps
- Slot-free card configuration: Cards can be mounted in any slot.
- Front access optical interfaces
- Economical: One APON-155M-IF connects to as many as 32 ATM-ONT units at the same time, with the total 150Mbps bandwidth allocated freely to each ONT.
- Highly reliable: A duplex configuration is adopted for the ATM switch, clock and controller modules.

Fig. 2 Cabinet appearance

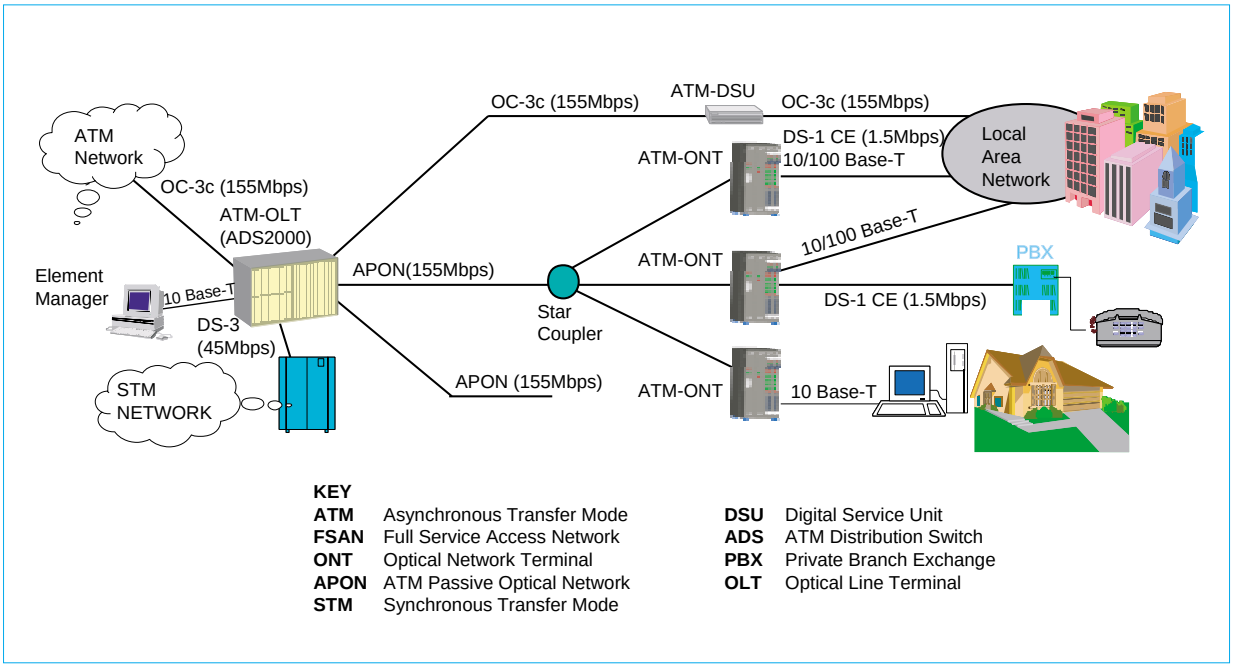


Fig. 1 ATM Access System configuration

**Hiroyuki Ueda is with Communication Systems Business Division.*

- Mounts in the North American specification 23-inch-wide cabinet.
- One system/one unit (sub-rack) configuration.

Fig. 3 ADS2000 appearance

2. ATM-ONT (product name: AONT-B200)
- Access line interface: APON 155Mbps
- User-network interface: One or any two of the following interfaces;
  10/100 Base-T, DS1-CE (1.5Mbps circuit emulation), or ATM155Mbps (to be developed)

Fig. 4 AONT-B200 appearance

3. Element Manager (product name: ISEM)
- Capable of remote system operation, administration and maintenance.
- Equipped with a Java-based user-friendly graphical user interface (GUI) for easy, intuitive operation.❑

New Products Support IP-over-ATM Network System

*by Keiichi Edahiro**

Mitsubishi Electric Corporation has developed three new products for internet protocol (IP) networks based on ATM technology, meeting the accelerating trend toward the use of IP networking for data communications traffic. As illustrated in Fig. 1, the next-generation IP network system, employing IP over ATM, has an ATM backbone network as the lower layer, with the upper layer consisting of IP transport network edge nodes connecting to ATM routers in the access network, and a network gateway providing IP gateway services.

The newly developed systems and their features are introduced here.

EDGE NODE. The role of the IF-2000 edge node is to connect the access network with the core network (see Fig.2).

- The IF2000 was developed to realize high transport capability, incorporating a hardware-based high-speed address search engine. Able to complete address searches within one cell duration time, it features high throughput not only for long-packet streams but also for short-packet streams.
- High security is achieved without a cryptographic system by mapping each subscriber's virtual channel (VC) to the closed user group (CUG) to which it belongs.
- As traffic control technology, not only best-effort service is supported but also three classes of IP-level priority control, enabling various service quality classes to be offered.

MITSUBISHI NETWORK GATEWAY. The MX-8000 network gateway was developed for connections between different CUGs or between CUGs and the Internet.

- One unit can handle as many as 256 CUGs.
- As address conversion methods it supports Bi-directional NAT, Basic NAT and NAPT. Any combination of these methods can be applied to each CUG.
- Large-scale IP flow handling is provided, with as many as 130,000 address conversion table entries for application to large-lot customers.

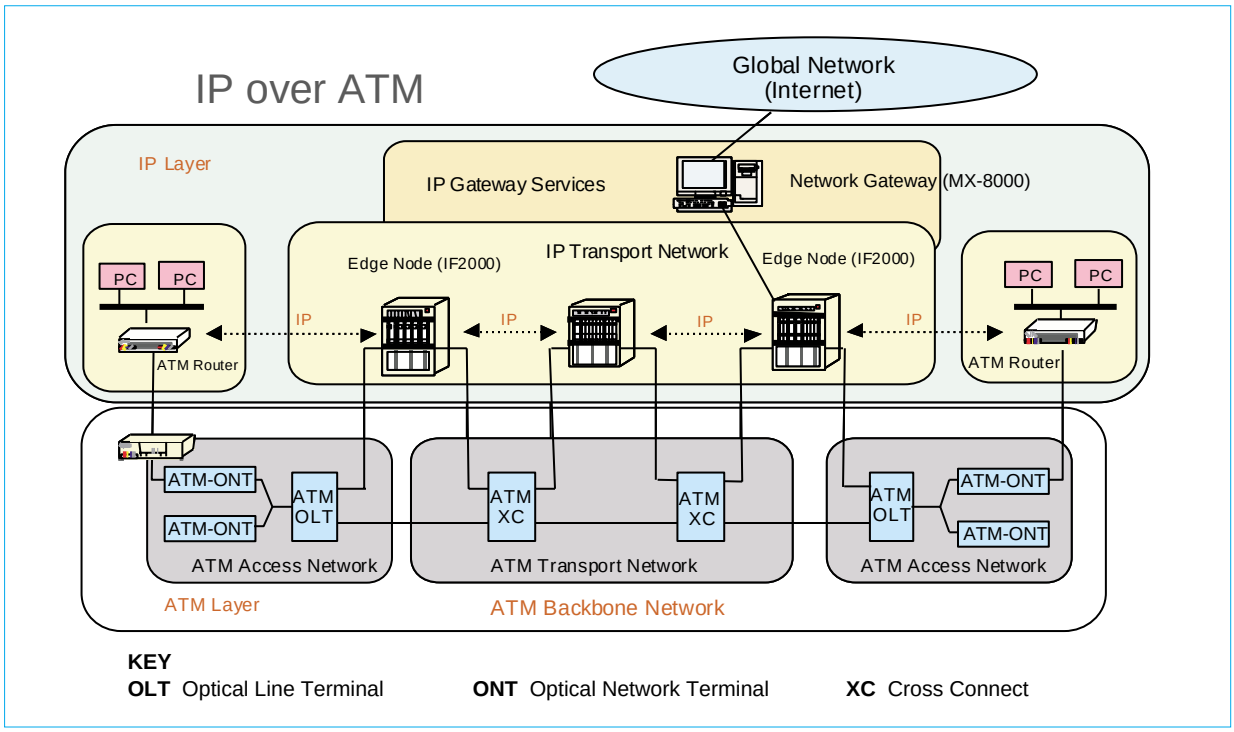


Fig. 1 Configuration of the IP Network System

**Keiichi Edahiro is with Communication Systems Business Division.*

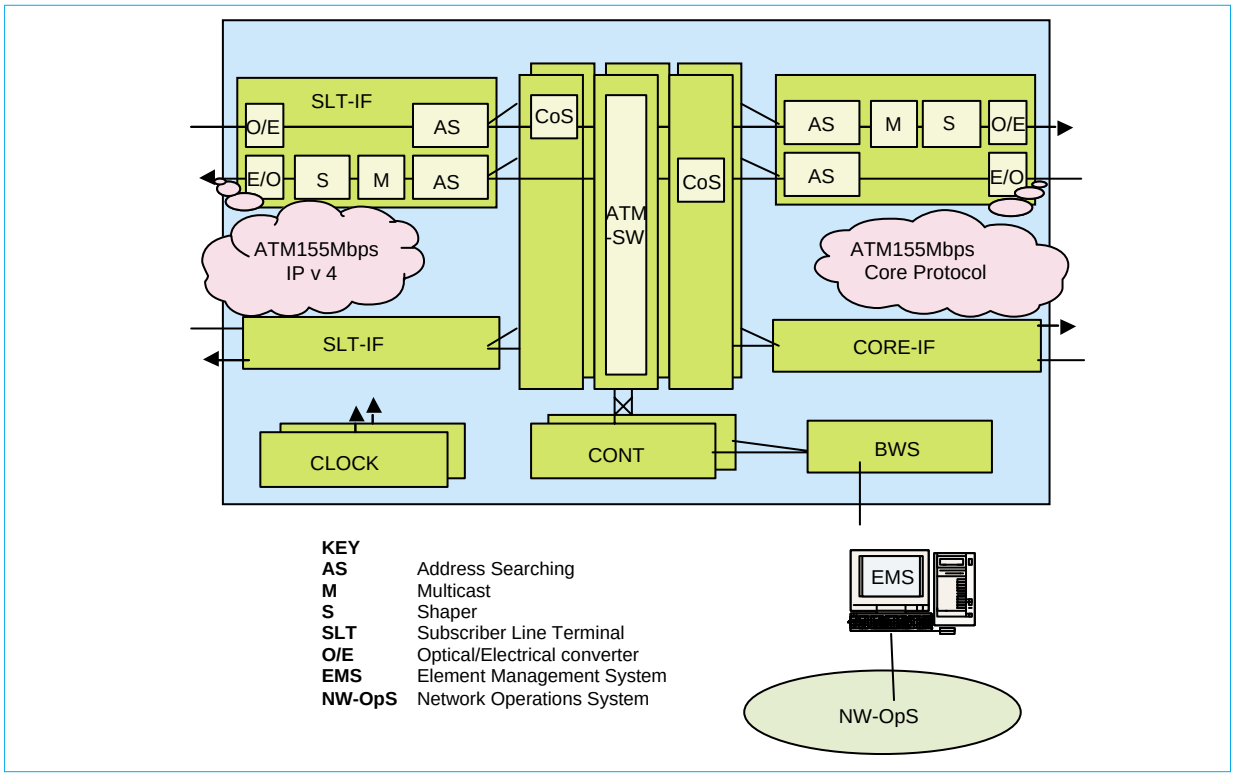


Fig. 2 IF2000 configuration

- Different packet filtering conditions can be set for each CUG, namely, by IP address, by port number, or by connection destination.
- Maximum packet transfer capability of 120Mbps is achieved by means of cut-through processing involving both software and hardware.
- The small size of this unit means it can be implemented on a platform with a PC server, and can also be operated as an all-in-one system including the operation, administration and management functions.

ATM ROUTER. The MR25 ATM router, see Fig. 3, connects a user's LAN (10Base-T) to an ATM leased line service (ATM 25Mbps).

- Packet transfer control is achieved by identifying each IP flow and mapping to a VC or channel in packet units.
- Fine control of QoS (quality of service) on ATM is supported, including functions for minimum guaranteed bandwidth per VC, and bandwidth-designated CLP 0/1 cell tagging.
- Bandwidth control of multiple virtual channels defined between multiple VCs or within a VC, priority control, and congestion changeover functions are also provided.
- Shaping is supported per VC, VP, or VC group.

Fig. 3 ATM Router (MR25)

IP networks based on ATM technology promise to play an increasingly important role in data communications traffic. These three new products demonstrate the corporation's ability to anticipate next-generation network needs. ❑

ATM Traffic Control for Guaranteed QoS

*by Tetsuya Yokotani**

Traffic control technology for guaranteeing each of the offered quality of service (QoS) classes is an important part of ATM networking technologies. This article presents the QoS-related requirements in an ATM network and discusses traffic control for guaranteeing QoS. It then describes technology for implementing this control in an ATM access system.

QoS requirements in an ATM network

QoS in an ATM network is defined in ITU-T recommendation I.356 and in the ATM Forum "Traffic Management Specification" Ver. 4.0/4.1. [1] Today there is broad support for both of these specifications. Features of the main QoS classes stipulated by the ATM Forum are shown in Table 1.

Table 1 QoS classes

CBR (Constant Bit Rate)	Delay, cell discard rate, and delay variation guaranteed
rt-VBR (Real Time Variable Bit Rate)	Delay, cell discard rate, and delay variation guaranteed
nrt-VBR (Non Real Time Variable Bit Rate	Cell discard rate guaranteed
GFR (Guaranteed Frame Rate)	Minimum bit-rate guaranteed, and packet-level discard control
ABR (Available Bit Rate)	Minimum bit-rate guaranteed, and cell-level flow control
UBR (Unspecified Bit Rate)	No quality specified

Functions for guaranteeing QoS

The functions for QoS guarantee are shown in Fig. 1.

CONNECTION CONTROL IN ADVANCE. Before setting up a new connection, the ATM network first determines whether it has the resources to meet the customer's requirements, using connection admission control (CAC) functions. If the necessary resources are available, it sets up the connection. The algorithm used to judge connection admission is not specified in the standards but is system-specific, with much research going into techniques for optimizing this to the system characteristics[2]. The two main approaches in designing these algorithms are called non-parametric and parametric. In the former approach, actual traffic is monitored to estimate whether sufficient resources are available to establish a new connection. The parametric approach creates a queue model such as M/D/1, based on the user-requested resources, analyzes its features mathematically and bases the connection admission decision on this result.

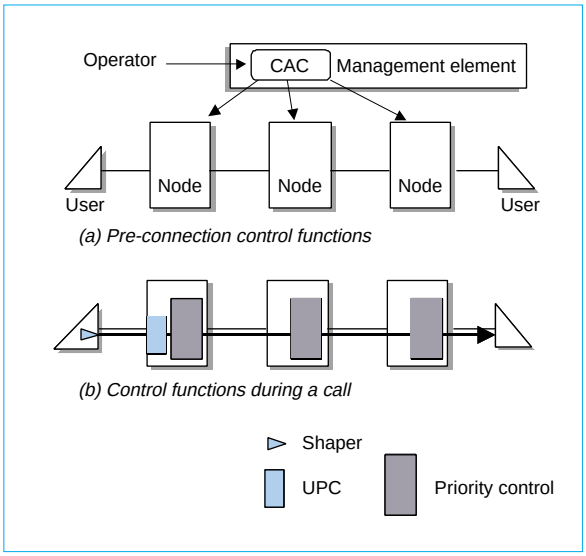


Fig. 1 Deployment of functions for QoS guarantee

CONTROL FUNCTIONS DURING A CALL. The control functions used during a call include user shaping, usage parameter control (UPC) at the network entrance, and cell priority control in nodes.

1. Shaping function and UPC
   The shaping function is used to control the traffic sent by the user so that it matches the parameters requested by the user prior to the call. UPC monitors the incoming traffic to see whether it conforms to the user-requested parameters.
   The algorithm used here is called generic cell-rate algorithm (GCRA), and it is specified in both the ATM Forum and ITU-T recommendations.

2. Priority control function
   Priority control, like CAC, is not specified in

**Tetsuya Yokotani is with the Information Technology R&D Center.*

the standards; but it has long been researched as a function required by the system in order to guarantee a diverse range of quality levels.

Generally, the function is implemented as shown in Fig. 2, using separate queues per connection or per QoS class at each output interface, and controlling the priority of each queue. Among the possible control techniques, head of the line (HOL) and weighted round robin (WRR) make it relatively easy to implement high-speed processing in hardware.

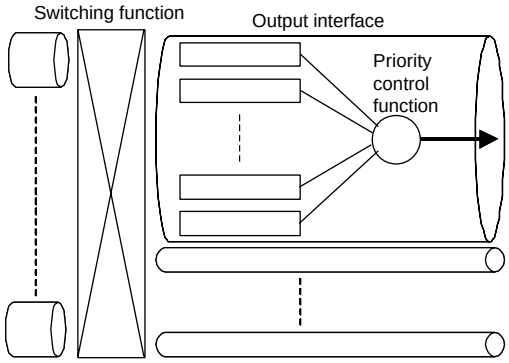


Fig. 2 Role of the priority control function

HOL defines various priority levels based on delay time. A cell can be sent only if there are no other cells with higher priority at the time. WRR, on the other hand, allows a minimum guaranteed bandwidth to be defined for individual queues, allocating a portion of available bandwidth to each queue in proportion to its minimum guarantee setting.

Implementation of traffic control in an ATM access system

The traffic control function has been implemented as follows in an ATM access system. The access system, as shown in Fig. 3, uses passive optical network (PON) technology to accommodate a large number of subscribers at low cost. The description here of the traffic control techniques focuses mainly on the optical line termination (OLT) part.

APPROACH TO QOS GUARANTEE. The OLT basically adopts a priority control method based on QoS class, in order to achieve effective bandwidth use while providing a diversity of QoS classes at low cost. With this method, QoS guarantee for each connection is based on the traffic

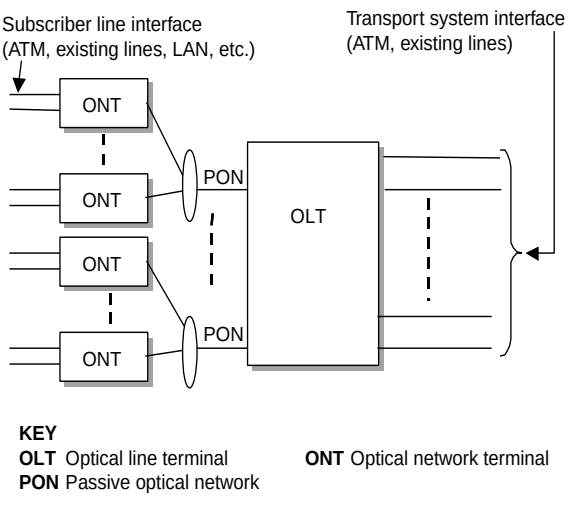


Fig. 3 ATM access system configuration

behavior during the connection setup time (long-term guarantee).

PRIORITY CONTROL METHOD. The priority control method applied to this access system is shown in Fig. 4. The access system is divided into a core switch for ATM switching and sub-switches, with the latter separated into priority

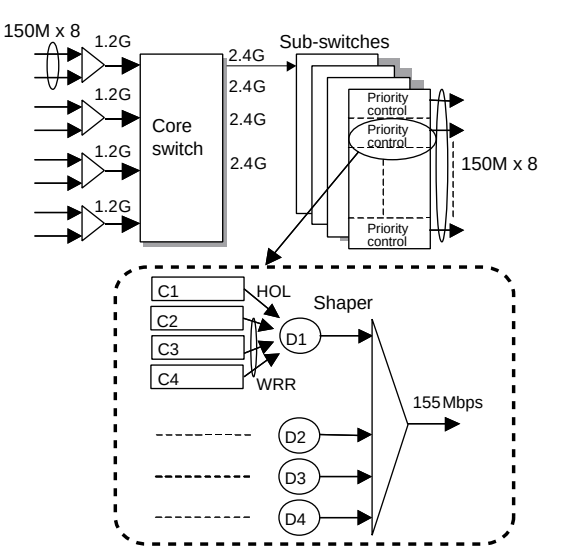


Fig. 4 Priority control method

control and low-speed interface functions. The core switch is able to obtain a very low cell loss rate thanks to the high-speed (1.2Gbps) multiplexing effect on input lines and the 50 percent load reduction (2.4Gbps) on output lines.

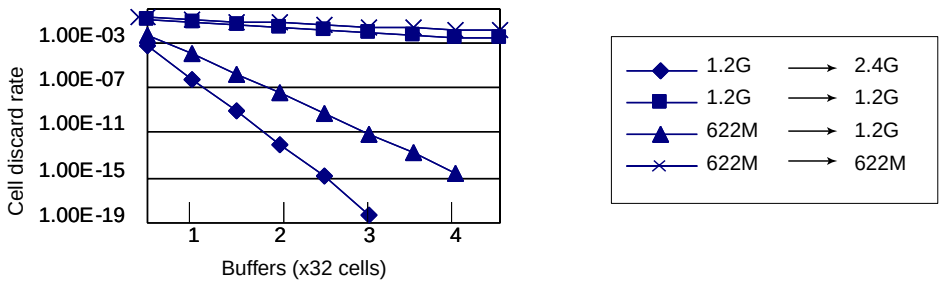


Fig. 5 Cell discard rate in core switch

Fig. 5 shows examples of actual values for these and also indicates, for the sake of comparison, the values achieved in the case of other multiplexing rates and output speeds. These results show that with the method adopted for this system (1.2Gbps input: 2.4Gbps output), an extremely low cell discard rate is achieved by buffering only a few dozen cells. This enables the quality control points to be concentrated at the sub-switches.

Priority control in the sub-switches, as shown in Fig. 4, makes use of a shaper at each output interface for controlling the bandwidth division and output traffic in each interface. Each shaper has a separate queue for each QoS class, with a division made between classes with stringent delay requirements (for the time being only the CBR class) and other classes.

HOL scheduling is used for control between these two types of classes. Between classes with no delay requirement (for the time being only nrt-VBR and UBR classes), WRR is used to guarantee a minimum bandwidth for each class. In this way a long-term minimum bandwidth is guaranteed also for each connection.

SUB-SWITCH DEVELOPMENT. The priority control described above was implemented using LSI chips (advanced switching LSI chips). Each chip accommodates eight 155Mbps interfaces. As many as four shapers can be operated per interface. For each shaper there are six queues. For future needs, faster speed can be achieved by bundling four interfaces into one 622Mbps interface. For each queue in Fig. 4 a buffer size of up to 64k cells (for a total of 512k cells) can be provided. The appearance of the access system board is shown in Fig. 6.

RESOURCE ALLOCATION BY CAC. Next we discuss the use of the CAC function in connection setup. This system adopts a parametric approach needing no special hardware. The decision on connection admission takes into account the following factors:

1. Number of established connections: A decision is made as to whether the supported number of connections are used up.
2. Availability of requested bandwidth: A decision is made as to whether the bandwidth requested by the user can be obtained from the amount allocated in advance in the management element. Specifically, the decision is made as follows:
   $\Sigma PCR <$ allocated bandwidth (for CBR)
   $\Sigma SCR <$ allocated bandwidth (for VBR) etc.
3. Buffer availability: Even when the required bandwidth is available, as above, there will generally be delay variation in the input traffic. A decision must therefore be made as to whether there is enough buffer capacity to absorb this variation.

   With this system, the decision is based on a queue model defined for each queue. For

Fig. 6 ATM access system

the CBR class, which is processed with the highest priority in this system, an M/D/1 model is used; for other classes, a GI/G/1 model is applied. In so doing, an ON/OFF model is applied to the cell arrival process to account for burstiness.

Further, by applying a virtual server technique to the service process, the priority control function described above is accounted for. The techniques described by Yokotani, Ichihashi and Yabe[3] are applied to the analysis methods.

EXTENDED FUNCTIONS. Besides the traffic control functions described above, a strict QoS guarantee is implemented for each connection using per-connection queuing and shaping. In addition, early packet discard/partial packet discard (EPD/PPD) are applied, which are demonstrably effective in packet-based communication. These extended functions are connected to the core switch as in Fig. 7 so they can be shared by each

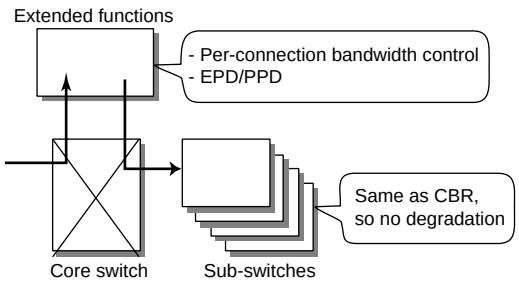


Fig. 7 Implementation of extended functions

output interface. To prevent quality degradation in the existing sub-switches, control is carried out equivalent to that for CBR traffic. ❑

References

[1] The ATM Forum: "Traffic Management Specification," Version 4.0, February 1996.

[2] R. Onvural, "Asynchronous Transfer Mode Networks: Performance Issues," 2nd Edition, Artech House, 1995.

[3] T. Yokotani, T. Ichihashi, M. Yabe, "An Ultra Light Weight CAC Mechanism (ULCAC) for Soft Guarantee in ATM Networks," IEEE 22nd LCN, pp. 432-440, 1997.

New LSI Chips Provide ATM Termination, OAM Processing and Traffic Control for Broadband Communications

*by Kazuumi Koguchi & Seiji Kozaki**

ATM transport systems are used for backbone networks because of their high speed and large data-handling capacity. In addition to raw bandwidth, however, they require sophisticated operation, administration and maintenance (OAM) functions for quick response to failures, along with advanced traffic control functions. Applying the latest device technology, we have developed LSI chips that realize high speed and the required advanced functionality while reducing equipment size and power needs.

Specifications of the newly developed LSI chips are given in Table 1. Here we give an overview of each chip and describe their main functions. Applied to an ATM cross-connect system and an ATM access system, the chips contribute to the compact system size and low power consumption.

2.4Gbps/622Mbps ATM termination chip

We developed LSI chips that implement ATM interface functions, featuring throughput of 2.4Gbps and compliant with the relevant ITU-T recommendations and ATM Forum standards. ATM cell-handling functionality is implemented in high-density CMOS LSI chips employing 32-bit parallel processing. By switching modes, a single chip can function as a 622Mbps throughput ATM interface chip.

The ATM termination LSI chips provide the following functions:

1. Section overhead (SOH) generation and termination
2. Pointer generation and termination
3. Path overhead (POH) generation and termination
4. ATM cell transmission and reception
5. Virtual container (VC) path testing
6. Alarm handling
7. Performance monitoring

The format of transmission frames is based on a synchronous digital hierarchy (SDH). SOH, pointer and POH generation and termination are carried out as stipulated in the ITU-T recommendations, as are the mapping and demapping between ATM cells and their frames.

The function for VC path testing can be used to confirm continuity of VC-carried information on the SDH layer. The alarm-handling function collects alarm data on the lower (physical) layer, transfers alarms to connected equipment, and handles such processing as the notification of alarms to the upper (management) layer. The performance-monitoring function monitors transmission quality at the SDH and ATM level, ATM cell count, pointer justification count, and other parameters. In addition there are communication ports for order wire, data communication channels, etc., assigned on the SOH, and ports for transmitting and receiving automatic protection switching (APS) information.

Table 1 Main chip specifications

LSI chip functions	2.4G/622Mbps ATM termination	622/156Mbps OAM processing	2.4Gbps OAM processing	UPC and shaping	Advanced switching
Process	0.35µ CMOS	0.25µ CMOS	0.25µ CMOS	0.35µ CMOS	0.25µ CMOS
Package	520-pin BGA	304-pin QFP	304-pin QFP	208-pin QFP	576-pin BGA
Operation	155.52/77.76/19.44MHz	77.76/19.44MHz	77.76MHz	19.44MHz	77.76MHz
Number of gates	523k	770k	750k	120k	1000k
On-chip RAM	31Kbits	1150Kbits	360Kbits	500Kbits	-
Supply voltage	3.3V	3.3V, 2.5V	3.3V, 2.5V	3.3V	3.3V, 2.5V
I/O level	LVPECL/LVCMOS	LVCMOS	LVCMOS	LVCMOS	LVCMOS
Power dissipation	4.98W(Rx)/3.99W(Tx)	4.2W	3.3W	0.9W	2.55W

**Kazuumi Koguchi is with Communication Systems Development Center and Seiji Kozaki is with Information Technology R&D Center.*

The specifications of each function are given in Table 2.

Table 2 ATM termination LSI functions and standards

Function	Standard
SOH generation/termination Pointer generation/termination POH generation/termination ATM cell transmission/receipt	ITU-T rec. G.707 to 709 ITU-T rec. I.432 ATM Forum af-phy-0133.000, af-phy-0046.000
VC path testing	ITU-T rec. 0.181
Alarm handling	ITU-T rec. G.783, G.784 ITU-T rec. I.432
Performance monitoring	ITU-T rec. G.826 ITU-T rec. I.732

LSI CHIP CONFIGURATION. The LSI chips implementing ATM termination functions are configured as shown in Fig. 1.

In this figure, the flow from upper left to right is the reception processing of signals on the transmission line, and that from lower right to left is the transmission processing of transmission line signals. The I/O interface on the transmission-line side is for 16-bit parallel 156Mbps signals in 2.4G mode, and 8-bit parallel 78Mbps signals in 622M mode; these signals undergo further parallel processing and 32-bit parallel internal processing.

For the path-testing function, either ATM cells or continuity test signals dropped/inserted inside the LSI chip can be selected as the signals contained in the VC area; normally ATM cell data from the equipment side is transmitted. The I/O interface on the equipment side is for 32-bit parallel 78Mbps signals in 2.4G mode, and 8-bit parallel 78Mbps signals in 622M mode.

In transmit mode, the clock supply in the receive circuits is disabled, and in receive mode the clock supply in the transmission circuits is disabled, as a power-saving measure. Parity information is sent with every eight bits of user information to check the normalcy of each processing block, in order to detect failure on the internal processing path. The chip supports a variety of clock-system designs so as to allow switching of clock sources in the pointer termination and cell receive processing blocks on the receiving side, and in the cell transmit processing and parallel-to-serial conversion blocks on the transmitting side.

FEATURES. The main features of the ATM termination LSI chip are summarized below.

1. Compact size, low power consumption and low cost

ATM termination functions are implemented in high-density CMOS LSI chips using 32-bit parallel processing.

2. Switched operating modes

A 2.4Gbps interface uses two chips (switching between transmit and receive modes); a 622 Mbps interface uses a single chip.

3. Incorporates peripheral functions

The alarm-handling functions, performance monitoring, path-continuity testing and other management-control functions are consolidated on chip rather than as the external circuits of conventional chips.

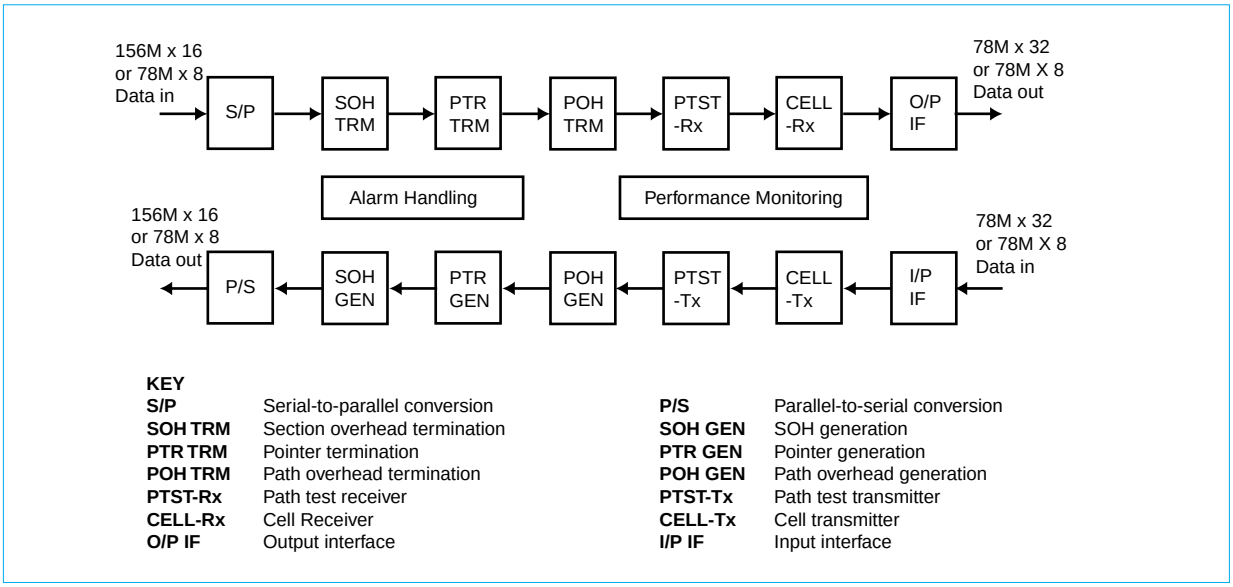


Fig. 1 Configuration of the ATM termination LSI chip

4. Compliant with standards
Each of the functions conforms to ITU-T recommendations and ATM Forum standards (see Table 2). Where clear-cut standards are lacking, parameters can be set via the CPU interface for flexible support.

OAM processing LSI chip

Rapid action in response to transmission-line or equipment failures is vital to minimize their impact. We developed OAM processing LSI chips for 622/156Mbps and 2.4Gbps interfaces, implementing operation, administration and maintenance (OAM) functions[1] for this purpose.

FUNCTIONAL SPECIFICATIONS. The OAM processing LSI chip implements the following OAM functions:

1. Fault management
2. Performance monitoring
3. Loopback testing
4. Continuity characteristics measurement
5. Virtual-path switching
6. Continuity check (supported only for the 622/156Mbps interface)

The fault management function generates the OAM cells (VP/VC-AIS and VP-RDI) that are used to send alarms when transmission-line or system trouble occurs. Equipment in the network detects these cells to determine the failure status.

The performance-monitoring function measures the service quality of a designated VP/VC by sending OAM cells containing maintenance information back and forth between equipment.

The loopback testing function is used to locate a faulty section by sending test OAM cells from one point on the network and looping them back at various other points to confirm VP/VC continuity.

The continuity characteristics measurement function measures bit-error rate, cell loss and other factors by exchanging OAM cells containing test signals with equipment and confirming the designated VP/VC continuity. VP switching is used in duplex sections; OAM cells for VP switching are generated when a failure occurs or for normal maintenance, and failure information or switchover information is notified.

Continuity checking is performed by periodically sending OAM cells for this purpose between equipment to monitor the designated VP/VC continuity and detect broken connections.

The OAM processing LSI chip supports both the user network interface (UNI) and network node interface (NNI), and is capable of handling as many as 4,096 VP/VC connections.

LSI CHIP CONFIGURATION. The configuration of the 622/156Mbps OAM-processing LSI chip is shown in Fig. 2. OAM-processing functions for the transmitting and receiving sides of the transmission line are implemented on a single chip. Cell I/O and internal processing are handled as 8-bit parallel processing.

Operation is at 77.76MHz for the 622Mbps interface and 19.44 MHz for the 156Mbps interface modes. Each of the OAM functions consists of an independent block, and it is possible to operate only the blocks for the functions being used, stopping the clock supply to blocks not in use. In this way, power use can be minimized in equipment that makes only partial use of the functions provided.

The order of OAM cell sending and of drop/monitor operations can be set, using the CPU interface, for flexible adaptation to the functional needs of various equipment. Two cell I/O interfaces are provided at both the sending and receiving sides, supporting external circuits where additional functionality is required.

The 2.4Gbps OAM-processing LSI chip operates at 77.76MHz and uses 32-bit parallel processing of cell I/O and for internal processing. The basic configuration is similar to that of the 622/156Mbps chip, with the same power-saving options and adaptability to the functional needs of the equipment in which it is used. Cell I/O interfaces are limited to one each in order to reduce pin count and power consumption.

FEATURES. The main features of the OAM processing LSI chips are as follows:

1. A 0.25µ CMOS process is adopted for high density and low power use.
2. 2.4Gbps OAM processing for the transmitting and receiving sides is implemented on a single chip.
3. The power needs and functions can be adapted flexibly to the applied system.

Traffic control LSI chips

UPC AND SHAPER LSI CHIP. The usage parameter control (UPC) functions for monitoring and restricting cell bandwidth incoming from subscribers and the shaping function for reducing cell-delay variation (CDV) have been implemented on a single LSI chip.

The GCRA algorithm[2][3] specified by the ITU-T and ATM Forum is adopted as the UPC algo-

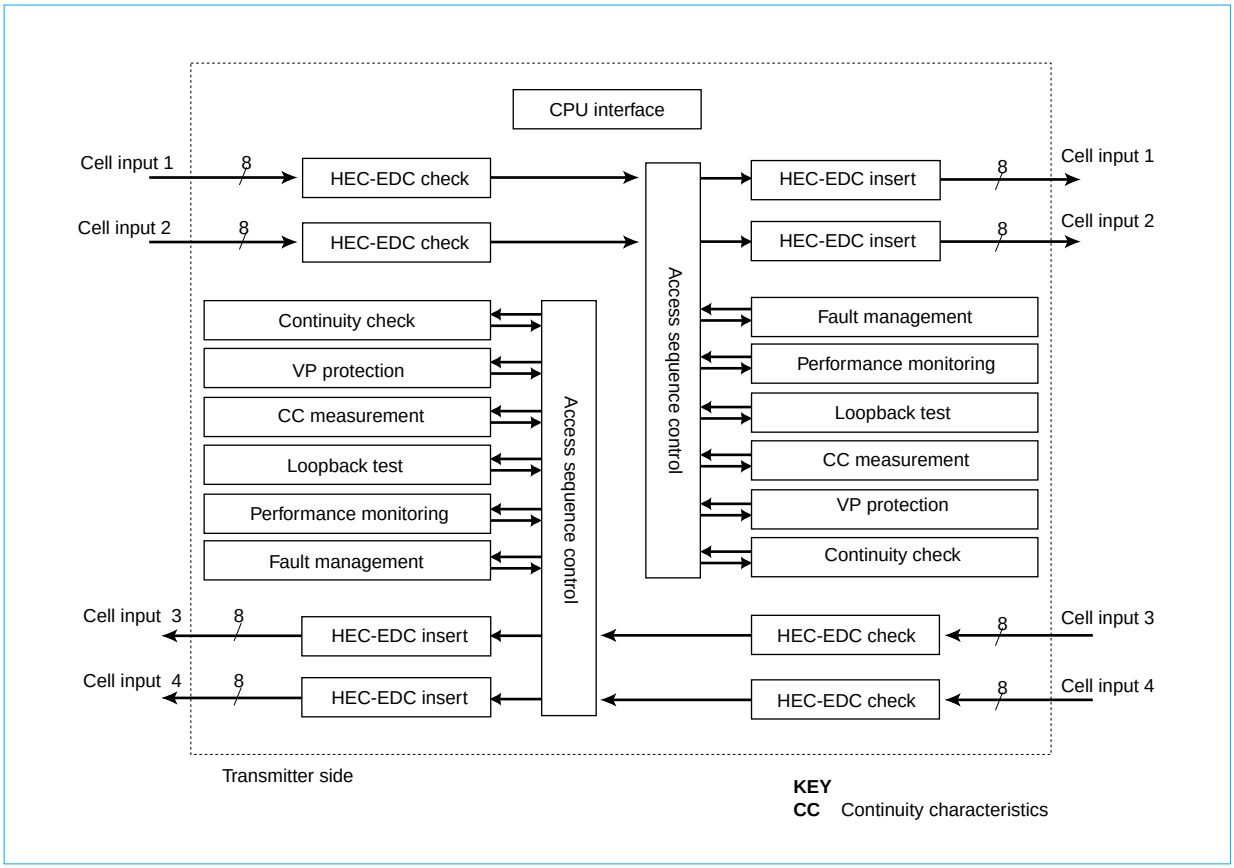


Fig. 2 Configuration of the 622/156 Mbps OAM processing LSI chip

rithm. In order to support guaranteed frame rate (GFR), an F-GCRA algorithm is also implemented for monitoring and control at the individual frame level.

This chip is able to handle up to 1,024 VP/VC connections.

ADVANCED SWITCHING LSI CHIP. We developed an ATM switching LSI chip with advanced traffic-control functions. The single chip implements an output buffer-type switch, realizing 2.4Gbps throughput. External SDRAM is used as the buffer memory, providing a buffer capacity of 512,000 cells. The main features are as follows:

1. Large-capacity cell buffer
2. Supports multiple service classes
3. Minimum bandwidth guaranteed by WRR.
4. Shaping functions
5. Parallel synchronous operation (instantaneous protection switching)

The devices described point the way to smaller and highly efficient systems for the reliable operation of broadband communications, and have extremely wide potential applications. ❑

References

1. ITU-T rec. I.610: B-ISDN Operation and Maintenance Principles and Functions (1999).
2. ITU-T rec. I.371: Traffic Control and Congestion Control in B-ISDN (1996).
3. ATM Forum: Traffic Management Specification Ver. 4.1 (1999).

Devices for ATM Fiber Optics Communication

*by Shin-ichi Kaneko**

New devices developed for ATM optical communications are described here. They are an optical transceiver and a hybrid integrated optical transceiver module with improved compactness, power consumption and economy. ATM-PON termination LSI chips were also developed for use on the office side (OLT) and subscriber side (ONT), conforming to ITU-T international recommendation G.983.1.

Transceiver for optical access network and optical trunk network

An optical transmitter IC that can be used for both continuous and burst modes, a continuous-mode optical receiver IC, and a burst-mode optical receiver IC were developed to realize the compact size, low-power use and low cost required in an optical access network. These devices are applicable to the 52Mbps and 622Mbps optical interfaces of the optical system, with the transmitter and receiver functions implemented on a single chip. Adopting a PECL I/O electrical interface, the chips operate on a single 3.3V power source (the burst-mode receiver IC operates at +5.0V) and consume less than one watt total for transmitting and receiving.

Specialized ICs were also developed for a 2.5Gbps optical interface, consisting of a one-chip transmitter and a two-chip receiver. Both power consumption and size are less than half that of previous chips. Fig. 1 shows the ITU-T G.957 L-16.3 optical receiver and Table 1 lists the developed optical interfaces.

Optical transceiver module for ATM-PON ONT

The optical modules used in an optical access network must be compact and low cost. Active research has therefore been directed at developing an optical transceiver module with hybrid integration of a laser diode, a receiver photodiode, and wavelength division multiplexing (WDM) components on a silicon substrate.

One design issue was how to suppress cross-talk between the transmitter and the receiver because the receiver should detect very weak signals whereas the transmitter should output powerful signals in the same package. Another was to meet the need for low cost. A description of the structure and features of the developed module follows.

Fig. 1 ITU-T rec. G.957 L-16.3 optical transceiver

STRUCTURE OF THE OPTICAL TRANSCEIVER MODULE. The appearance of the developed optical transceiver module is shown in Fig. 2 and its structure in Fig. 3. On a silicon substrate, this module integrates a 1.3µm-band laser diode, a receiver photodiode, a polymer-waveguide chip, single-mode fiber (SMF) and multi-mode fiber (MMF), using passive alignment technology to build a hybrid integrated optical transceiver module. A transfer-mold package, which is suitable for reflow mounting, offers good mass productivity and low-cost packaging. At the same time, an MU-type optical adapter was developed for a standard optical interface, reducing cost by eliminating the fiber for connector adaptation.

The polymer-waveguide chip was implemented for ease of mass production and low cost.

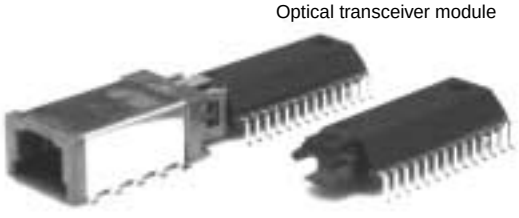


Fig. 2 Module and adapter

**Shin-ichi Kaneko is with the Information Technology R&D Center.*

Table 1 Optical interface specifications

Line	Bit rate	Interface specifications	Distance	Wavelength (μm)	Optical devices		Power consumption (max)
					Transmit (Tx)	Receive (Rx)	
Transport	51.840Mbps (SDH)	JT-G957 I-0	2km (intra-office)	1.3	LD with waveguide lens	PD	Tx:0. 5W, Rx:0.5 W
	155.52Mbps (SDH)	ITU-T G. 957 I-1	2km (intra-office)	1.3	LD with waveguide lens	PD	Tx:0. 5W, Rx:0.5 W
		ITU-T G. 957 L-1. 1	40km (inter-office)	1.3	LD with waveguide lens	PD	Tx:0. 5W, Rx:0.5 W
		ITU-T G. 957 L-1. 3	40km (inter-office)	1.55	FP-LD	PD	Tx:0. 5W, Rx:0.5 W
	622.08Mbps (SDH)	ITU-T G. 957 I-4	2km (intra-office)	1.3	LD with waveguide lens	PD	Tx:0. 5W, Rx:0.5 W
		ITU-T G. 957 L-4. 1	40km (intra-office)	1.3	DFB-LD*	PD	Tx:0. 6W, Rx:0.8 W
		ITU-T G. 957 L-4. 3	80km (inter-office)	1.55	DFB-LD*	PD	Tx:0. 6W, Rx:0.8 W
		ITU-T G. 691 V-4. 1	80km (inter-office)	1.3	DFB-LD*	APD	Tx:0. 6W, Rx:0.9 W
		ITU-T G. 691 V-4. 3	120km (inter-office)	1.55	DFB-LD*	APD	Tx:0. 6W, Rx:0.9 W
		ITU-T G. 691 U-4. 3	160km (inter-office)	1.55	DFB-LD*	APD Booster: Er doped Optical fiber amp.	Tx:0. 6W, Rx:0.9 W 0pt. Amp. :5. 5W
	2488. 32Mbps (SDH)	ITU-T G. 957 L-16. 1	40km (inter-office)	1.3	DFB-LD**	APD	Tx:5. 9W, Rx:3.0 W
		ITU-T G. 957 L-16. 3	80km (inter-office)	1.55	DFB-LD**	APD	Tx:5. 9W, Rx:3.0 W
Access	155. 52Mbps (PDS)	ITU-T G. 983. 1	-	WDM (Tx:1. 55, Rx:1. 3)	DFB-LD*	PD WDM fiber coupler	Tx:0. 5W, Rx:0. 5 W
			-	WDM (Tx:1. 3, Rx:1. 55)	LD with waveguide lens	PD WDM fiber coupler	Tx:0. 5W, Rx:0. 5 W
	155. 52Mbps (SS)	ITU-T G. 957 L-1. 1	40km	SDM 1. 3	LD with waveguide lens	PD	Tx:0. 5W, Rx:0. 5 W

***** : With isolator, without temperature control device. ****** : With isolator and temperature control device.

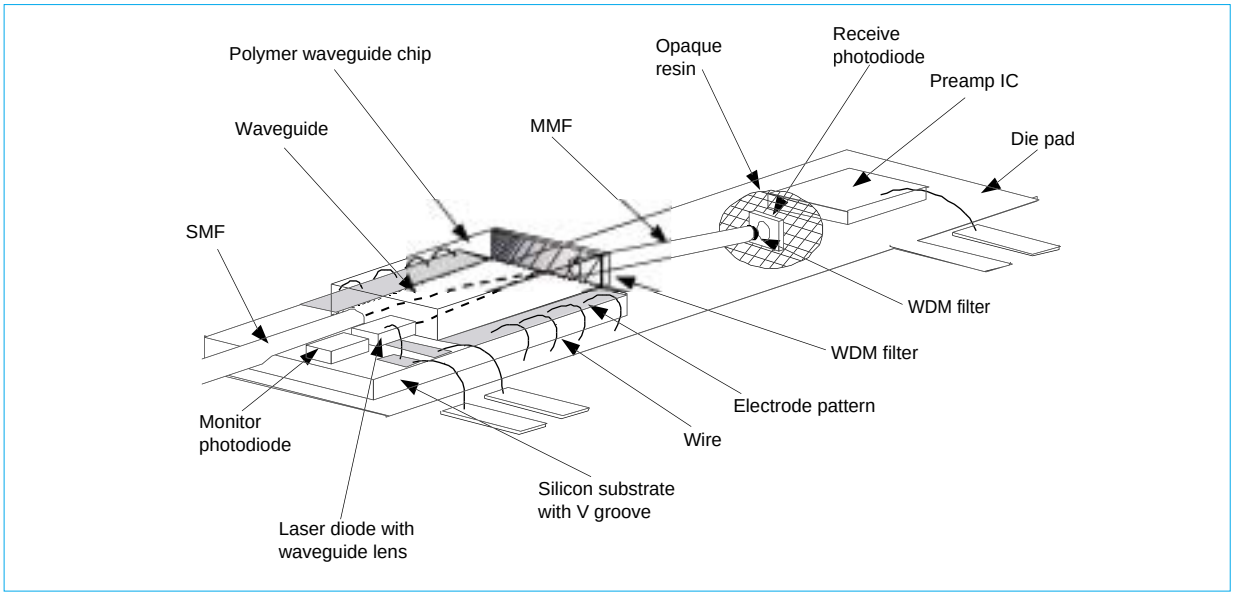


Fig. 3 Module structure

The chip has the WDM filter which reflects 1.3μm light and transmits 1.5μm light.

FEATURES OF THE OPTICAL TRANSCEIVER MODULE. As noted above, a key feature of the optical transceiver module is the reduction of cross-talk between the transmitter and the receiver. Cross-talk is caused by optical and electrical coupling between the transmitter and receiver of the module.

The following measures were taken to prevent optical coupling between the laser diode and photodiode:

- A high-isolation WDM filter is applied to the edge of the polymer waveguide chip.
- Multi-mode fiber is inserted between the polymer waveguide chip and photodiode.
- The photodiode is surrounded by opaque resin.
- A WDM filter is formed on the end of the MMF.

These measures succeeded in reducing optical cross-talk to an extremely low level of -61.9dB. The following measures were taken to reduce electrical coupling between the transmitter and the receiver of the module:

- The laser diode is electrically isolated from the die pad with ground potential.
- An electrode pattern is formed on the silicon substrate between the transmitter and the receiver and is connected to ground.
- The receiver is kept apart from the transmitter by inserting multi-mode fiber between the polymer waveguide chip and the photo diode.

The effect of these measures was to reduce electrical cross-talk to the extremely low level of -83.5dB.

By reducing optical and electrical cross-talk as described above, we were able to achieve excellent receive characteristics. Fig. 4 compares the bit-error-rate performance when only the receiver is operated (simplex) and when both transmitter and receiver are operated together (duplex). The minimum sensitivity (error rate 10^{-10}) under the duplex operation is -35.5dBm, and a power penalty caused by the cross-talk is

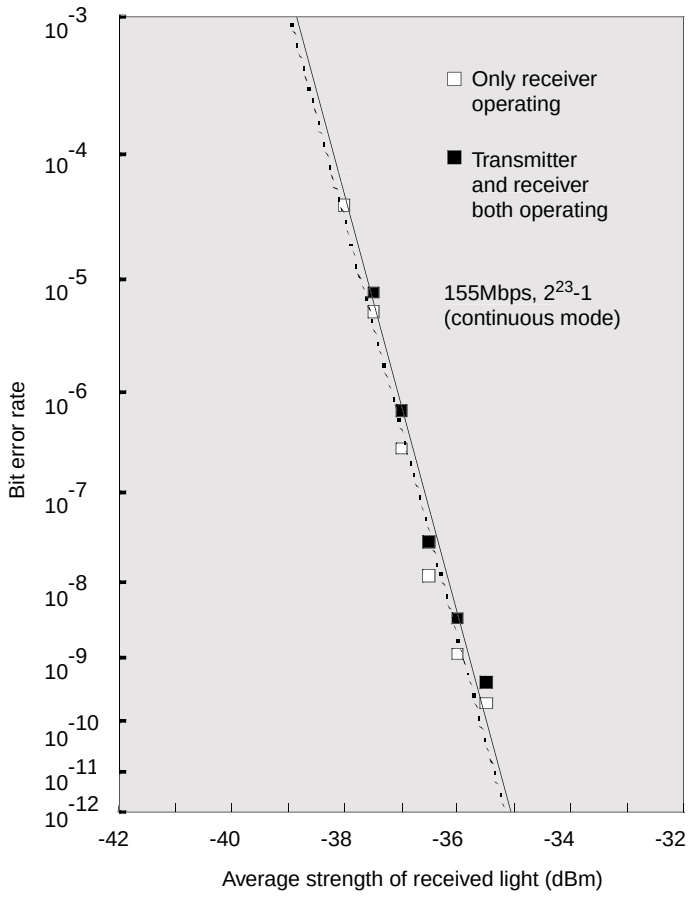


Fig. 4 Sensitivity

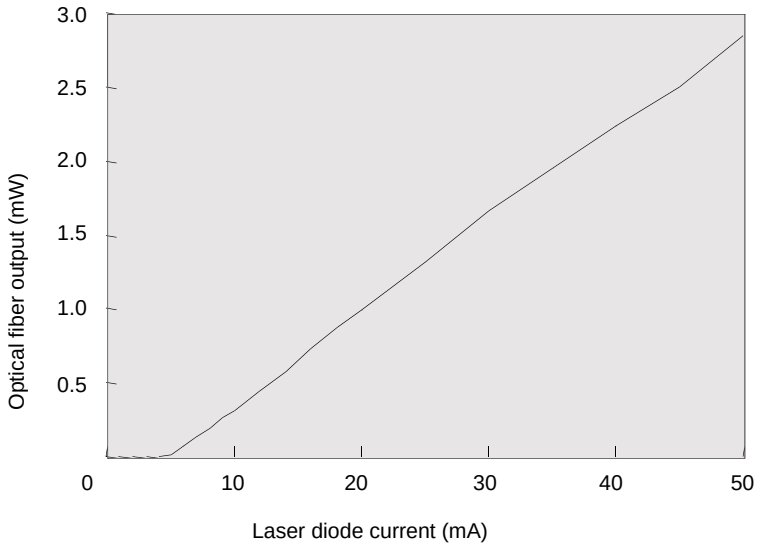


Fig. 5 I-L curve

0.1dB. This small penalty indicates that cross-talk is adequately suppressed. Fig. 5 shows the I-L curve of the module. Output optical power of 2mW is achieved at a laser-diode current of 35mA.

The receiver characteristics and optical output characteristics of this module both satisfy the specifications for an ONT optical transceiver module in an ATM-PON system given in ITU-T rec. G.983.1.

ATM-PON termination LSI chips

Finally, two ATM-PON termination LSI chips were developed in compliance with ITU-T rec. G.983.1, the international standard for optical network systems. These chips, applicable to the optical-line terminal (OLT) and optical-network terminal (ONT), were developed, applying CMOS gate array LSI with a 0.25μm process.

ATM-PON TERMINATION LSI CHIP FOR OLT. This is mounted on a 156Mbps ATM-PON interface board in the OLT. Transmission speed is 155.52Mbps both upstream and downstream. The chip incorporates circuitry for serial-to-parallel and parallel-to-serial conversion supporting this transmission speed and a burst-mode bit synchronization circuit. It can interface directly with the 155.52Mbps LV-PECL-level signals of the optical-transceiver module (see Fig. 6). The

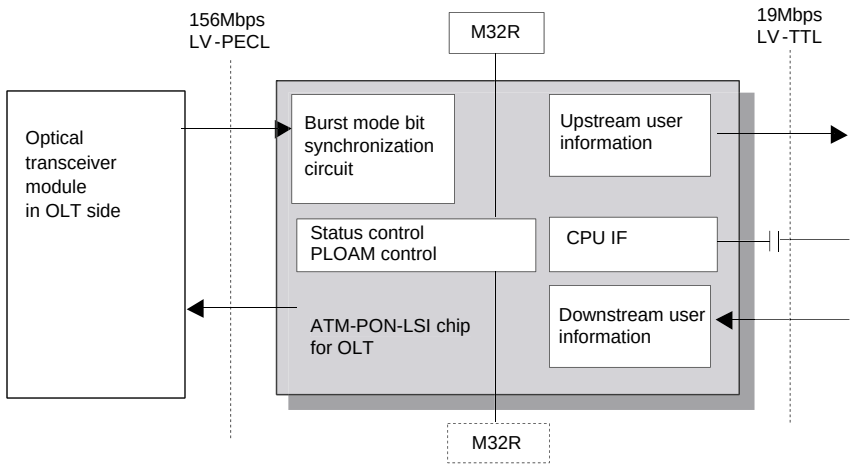


Fig. 6 Configuration of ATM-PON chip for OLT

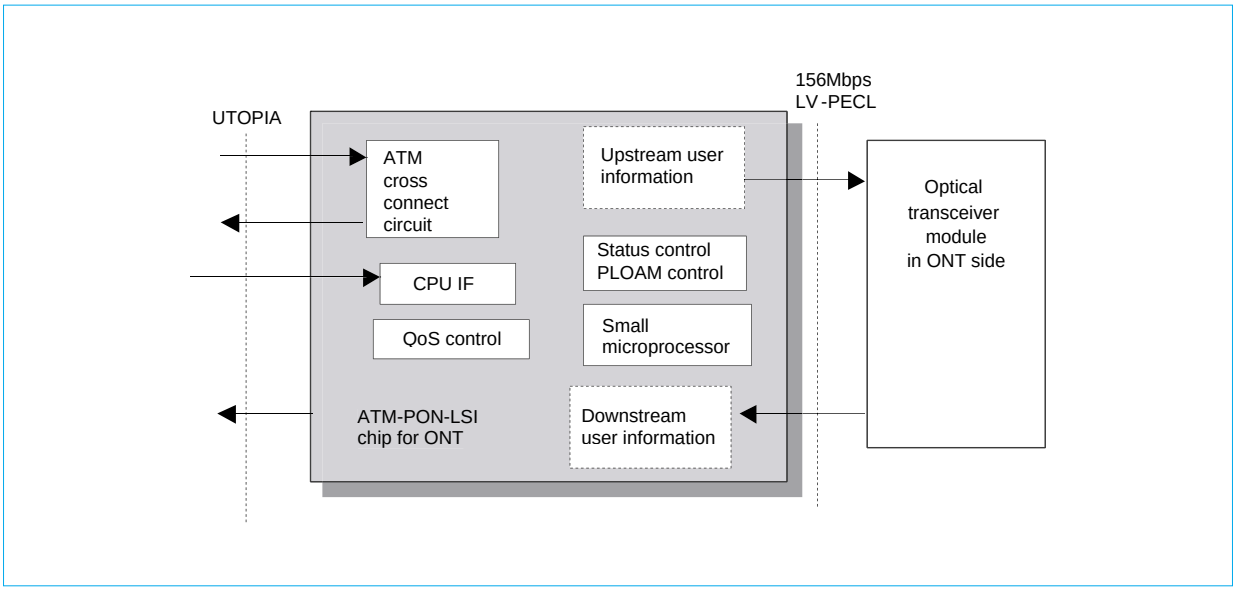


Fig. 7 Configuration of ATM-PON chip for ONT

ITU-T rec. G.983.1-specified functions for start/stop control, alarm-handling control and control of message handling with the ONT are realized by firmware control, using one Mitsubishi Electric M32R microprocessor each for the transmitter control and the receiver control. This configuration makes it easy to change functions as specifications change.

ATM-PON TERMINATION LSI CHIP FOR ONT. The ONT installed in subscriber premises must be compact and low cost. An LSI chip was therefore developed implementing ATM-PON functions, OAM functions and QoS control functions for each of the line cards accommodated by different UNI types.

Speed of the transmission system is 155.52Mbps in both upstream and downstream directions, and direct interfacing is possible with the 155.52Mbps LV-PECL-level signals of the optical-transceiver module. This LSI chip features the adoption of firmware processing for state control and for some of the alarm processing, using a simple on-chip control processor. Additional features include OAM cell-processing functions such as VP-AIS generation and loopback cell termination and generation; the provision of ATM-Forum standard Utopia Level 1 interfaces to one or two line cards of 155.52 Mbps each (19.88MHz, 8-bits parallel); and the ability to realize optimum QoS for different line-card UNI by variable settings of the QoS buffer parameters as shown in Fig. 7. ❑