Trench SiC-MOSFET Structure for Controlling Short-Circuit Capability

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Abstract

With the growing environmental awareness in recent years, there is an increased demand for energy-saving power electronics equipment, so power devices using Silicon Carbide (SiC) as a material are being developed and marketed. Of these, anticipation is high for the trench-type SiC-Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) that features lower loss, but due to the high conductivity of trench-type SiC-MOSFETs, it is extremely difficult to ensure short-circuit capability if a short-circuit occurs in the device. To support a wide range of applications as a switching device, acquiring a means of controlling short-circuit capability in the device structure design is crucial. Mitsubishi Electric has improved the device structure of the trench SiC-MOSFET that has been under development as a way of achieving a trench SiC-MOSFET capable of trade-off control between lower resistance and higher short-circuit capability.

1. Introduction

With the growing environmental awareness in recent years, advances are being made toward energy conservation in power electronics equipment, and SiC has been drawing attention as a next-generation power semiconductor material. SiC exhibits much better properties as power devices, including a larger band gap and higher critical electric field than Si used conventionally. Mitsubishi Electric has been developing and mass-producing SiC-MOSFETs and SiC-Schottky Barrier Diode (SBD) s using SiC, and in the past has marketed products across a broad range of withstand voltage classes, from 600V for home appliances to 3.3kV for electric railways.

Lowering loss of power devices used in equipment is crucial for energy conservation in power electronics equipment, and efforts are advancing for the development and marketing of trench-type SiC-MOSFETs that allow even lower losses. Embedding the gate electrode in the trench allows trench-type MOSFETs to achieve a higher cell integration by reducing the cell pitch, so can achieve a lower resistance in devices. Meanwhile, the electric field is prone to concentrating at the bottom of the trench, so this electric field needs to be alleviated in order to achieve sufficient device reliability.

Mitsubishi Electric has developed trench SiC-MOSFETs with a unique structure that enables lower resistance, higher reliability and lower switching losses[(1)(2)(3)]. The schematic of the trench SiC-MOSFET developed by Mitsubishi Electric is shown in Fig. 1. The characteristics of Mitsubishi Electric's trench SiC-MOSFET structure feature three injection layers: (1) P-type protective layer (BPW: Bottom P-Well) for relaxing the electric field applied to the bottom of the trench, (2) Sidewall P-type pillar (SP: Sidewall Pillar) for grounding the BPW, and (3) N-type Junction Field Effect Transistor (JFET) doping layer (JD: JFET Doping) for preventing narrowing of the current path. The advantage of this structure that utilizes tilted ion implantation into the trench is that it makes it easier to achieve lower loss through high integration and can be fabricated using simple processes.

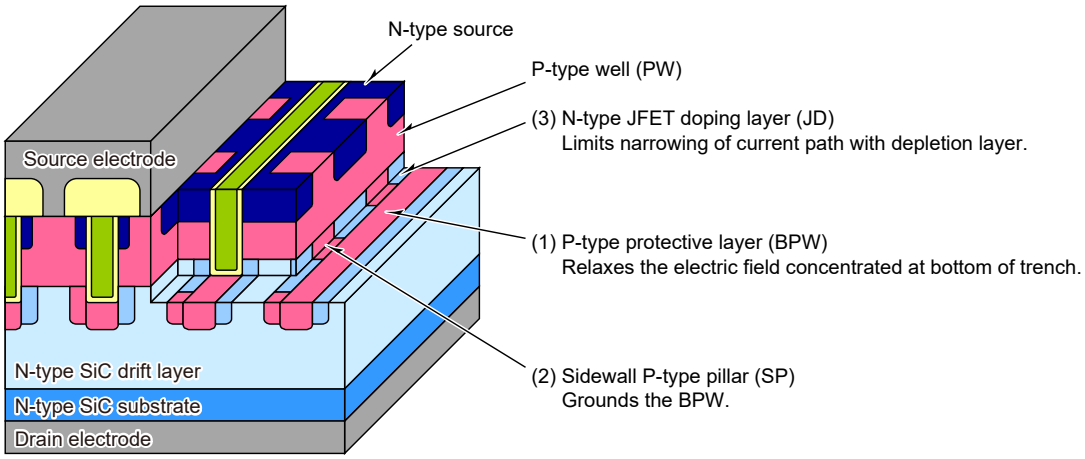


Fig. 1 Schematic of developed trench SiC-MOSFET

Yet while trench SiC-MOSFETs are capable of lower losses, their high conductivity means it is extremely difficult to ensure short-circuit capability if a short-circuit occurs in the device. To support a wide range of applications as a switching device, add methtods for controlling short-circuit capability in the device structure design is essential. Thus the device structure of the conventional trench SiC-MOSFET has been improved as a way of developing a trench SiC-MOSFET capable of trade-off control between lower resistance and higher short-circuit capability.

2. Short-circuit Capability Control Trench-type SiC-MOSFET

2.1 Device structural concept and process flow

The schematic of the fabricated trench SiC-MOSFET that has been developed is shown in Fig. 2. As a way of controlling the trade-off between lower resistance and higher short-circuit capability, a method of adjusting the area density ratio of the SP area that makes up the trench sidewall (sidewall P-type pillar ratio: r_{sp}) has been developed. The SP areas are therefore spaced periodically apart each other on trench sidewall and feature grounding for the BPW and achieving stable switching as described in Chapter 1. As a function of the SP area, this development focused on restricting the Metal Oxide Semiconductor (MOS) channel current and current path of the Junction FET (JFET)-region when the device is conducting (ON). To achieve trade-off control between lower resistance and higher short-circuit capability, devices with different r_{sp} values compared to the conventional structure of r_{sp} = 1 were created, and tests were conducted to assess the effects that r_{sp} has on the electrical characteristics and short-circuit capability of the MOSFETs.

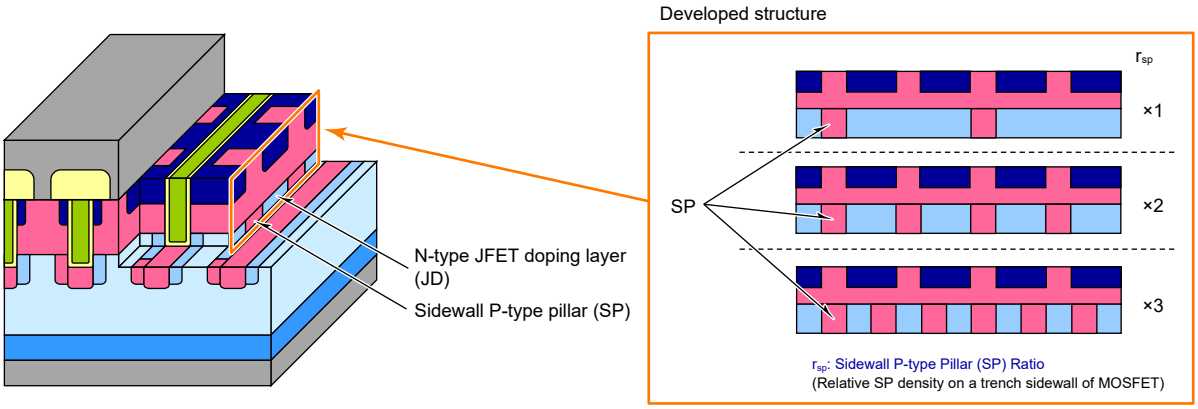


Fig. 2 Schematic of fabricated trench SiC-MOSFET and controlled its Sidewall P-type Pillar (SP) Ratio r_{sp}

The cross-sectional schematic diagram of the process flow of the developed trench SiC-MOSFET separated into (a) Area with SP and (b) Area without SP are shown in Fig. 3. The first step involves implanting Al and N ions into the N-type drift layer before trench etching, to form a P-type well (PW) and N-type source. Next, an SiO_2 film was deposited and photolithography performed to form a trench on

the SiC with dry etching. BPW is formed at the bottom of the trench with self-align Al ion implantation by utilizing the SiO_2 film remaining after trench etching (Fig. 3(i)). After the SiO_2 film is removed, the JD is formed with tilted N ion implantation on the trench sidewalls on both sides (Fig. 3(ii)). Next, SP is formed after photolithography using tilted Al ion implantation only for one side of the trench sidewall (Fig. 3(iii)). The r_{sp} can be adjusted with the photolithography mask pattern. Next, P-type contact is formed and after implantation ion activation annealing, the gate formation is performed (Fig. 3(iv)). This is then followed by contact formation, metallization and other processes to complete the device.

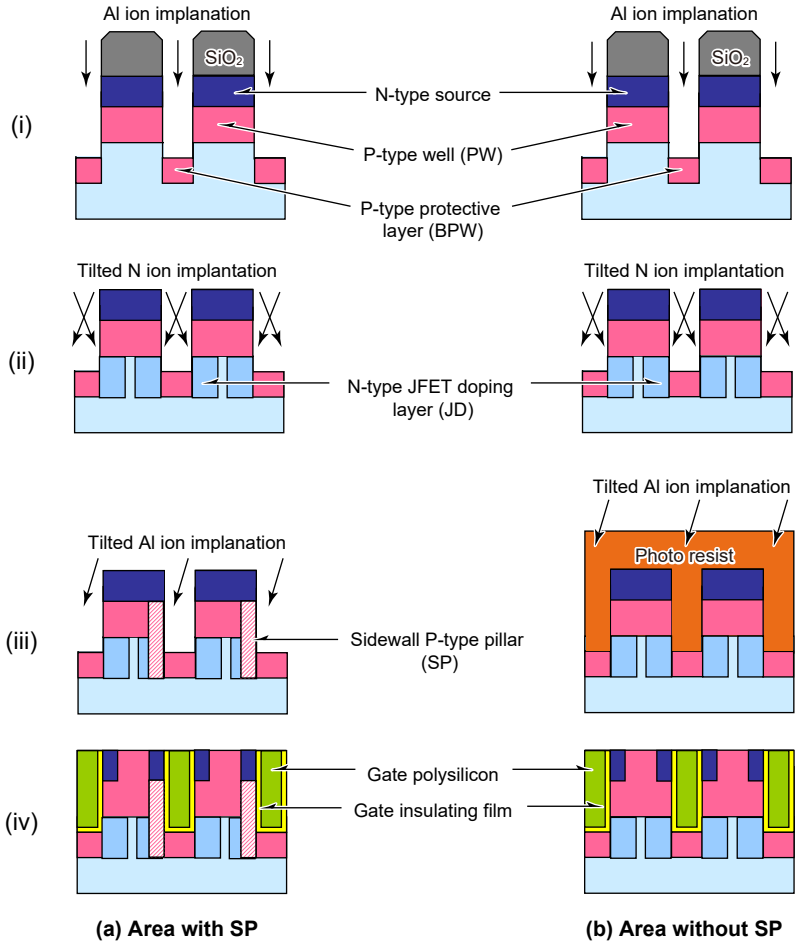
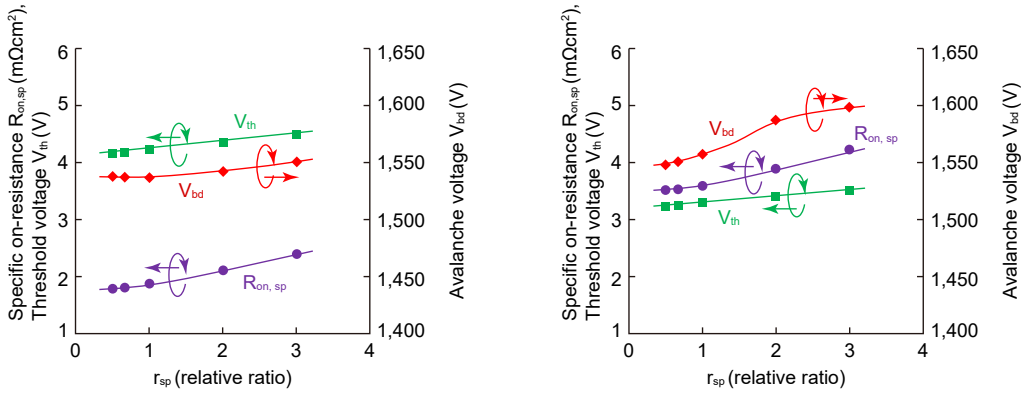


Fig. 3 Fabrication process flow of the trench-gate SiC-MOSFET

2.2 Dependence of static characteristics on sidewall P-type pillar ratio

To assess the effect of the r_{sp} structure design on static characteristics, the electrical characteristics of the prototype trench SiC-MOSFET was tested. The r_{sp} dependences of the specific on-resistance $R_{on,sp}$, threshold voltage V_{th} and avalanche voltage V_{bd} are shown with the measurement results in Fig. 4(a) at room temperature and in Fig. 4(b) at 150°C respectively. With increases in r_{sp}, that is the SP area densely formed on the trench sidewalls, both $R_{on,sp}$ and V_{th} increase gradually at either temperature due to the reduction in MOS channel density and current path of the JFET-region. Furthermore, V_{bd} increases as r_{sp} increases due to the densely formed SP area resulting in relaxation of electric field effect. As a result, with device voltage V_{bd} to 1550V being satisfied, an on-resistance of $R_{on,sp}$ = 2.2mΩcm^2 was achieved at room temperature for the r_{sp} = 2 structure and $R_{on,sp}$ = 2.4mΩcm^2 for the r_{sp} = 3 structure.



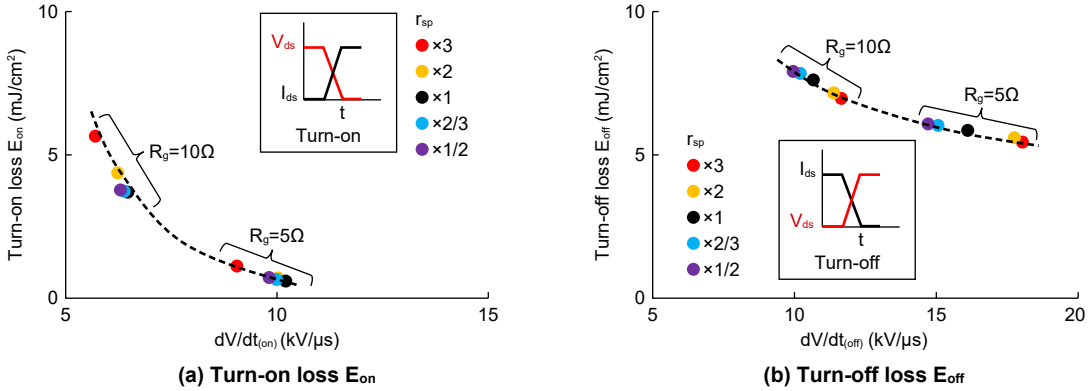
(a) Measurement results at room temperature **(b) Measurement results at 150°C**

*1 Definitions are $R_{on,sp}$ is gate voltage, V_g = 20V, Value of drain current density J_{ds} = 450A/cm², V_{th} is voltage between drain-source electrodes, V_{ds} = 10V, Value of drain current density J_{ds} = 100mA/cm², Avalanche voltage V_{bd} is V_g = 0V, I_{ds} = 100μA value.

Fig. 4 The r_{sp} dependences of $R_{on,sp}$, V_{th} and V_{bd}*1

2.3 Dependence of dynamic characteristics on sidewall P-type pillar ratio

The dynamic characteristics, where the effect of the r_{sp} structure design on the trade-off relationship between switching speed dV/dt and switching loss, was assessed. Switching measurements were conducted with double-pulse tests, and dV/dt was adjusted by changing the external gate resistance (R_g). The results of dV/dt dependence when changing r_{sp} are shown for turn-on loss E_{on} in Fig. 5(a), and turn-off loss E_{off} in Fig. 5(b). For both E_{on} and E_{off}, the relationship between switching loss and dV/dt for changes in r_{sp} was found to follow the same trade-off line. This suggests that switching losses can be controlled by the external gate resistance (R_g) independently of r_{sp}.



(a) Turn-on loss E_{on} **(b) Turn-off loss E_{off}**

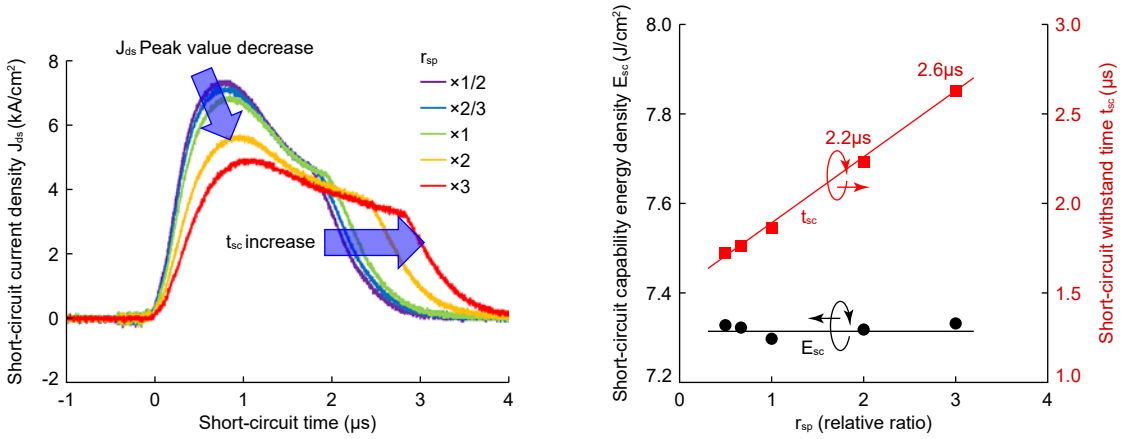
*2 V_{DD}= 600V, Value of drain current density J_{ds}=260A/cm²

Fig. 5 The dV/dt dependence of turn-on loss E_{on} and turn-off loss E_{off} at various r_{sp}

2.4 Dependence of short-circuit capability on sidewall P-type pillar ratio

The results of the dependence of r_{sp} on short-circuit capability are shown in Fig. 6. Figure 6(a) shows the r_{sp} dependence of the short-circuit current density J_{ds} waveform immediately prior to the device breakdown during arm short-circuit (V_{DD} = 650V, V_{gs} = 20V, at 150°C). As an increase in r_{sp} causes a decrease in the MOS channel density and the current path in the JFET-region, the short-circuit withstand time t_{sc} increases due to significant suppression of the J_{ds} peak value. This revealed that r_{sp} = 2 structure can ensure up to t_{sc} = 2.2μs, while the r_{sp} = 3 structure can ensure up to t_{sc} = 2.6μs.

Figure 6(b) shows the r_{sp} dependence of short-circuit energy E_{sc} and short-circuit withstand time t_{sc}. The structural design with increased r_{sp} leads to an increase in t_{sc}, but E_{sc} was found to be independent of r_{sp}. This indicates that the short-circuit breakdown is a thermal breakdown mode due to the short-circuit current, and as such E_{sc} is limited to a constant (r_{sp} has no effect on the design of thermal conductivity of the MOSFET). As a result, the short-circuit withstand time t_{sc} can be controlled by controlling the sidewall P-type pillar ratio, which is a device structure parameter.



(a) The J_{ds} waveforms of short circuit event with various r_{sp}

(b) The r_{sp} dependence of short-circuit withstand time t_{sc} and short-circuit energy E_{sc}

*3 Either values are V_{DD}=650V, V_{gs}= 20V, 150°C

Fig. 6 The waveforms of short circuit event with various r_{sp} and the r_{sp} dependence of short-circuit withstand time t_{sc} and short-circuit energy E_{sc}*3

2.5 Trade-off control of DC loss/AC loss ratio and short-circuit capability

Based on the results of sections 2.2, 2.3 and 2.4, the dependence of DC loss, AC loss and short-circuit withstand time t_{sc} on the sidewall P-type pillar ratio were calculated. The DC loss was calculated from the $R_{on,sp}$ value, and the AC loss was calculated by referring to the switching loss value at R_g = 5Ω, based on the assumption that the device is driven at 20kHz.

The results are shown in Fig. 7. t_{sc} can be increased with the use of a structure with high r_{sp}, wherein the DC loss increases slowly but the AC loss remains almost constant. The r_{sp} is a key parameter for designing the DC loss and short-circuit withstand time t_{sc}, and this revealed that Mitsubishi Electric's trench SiC-MOSFETs can be adapted to suit various applications required of SiC-MOSFETs by adjusting the r_{sp} design.

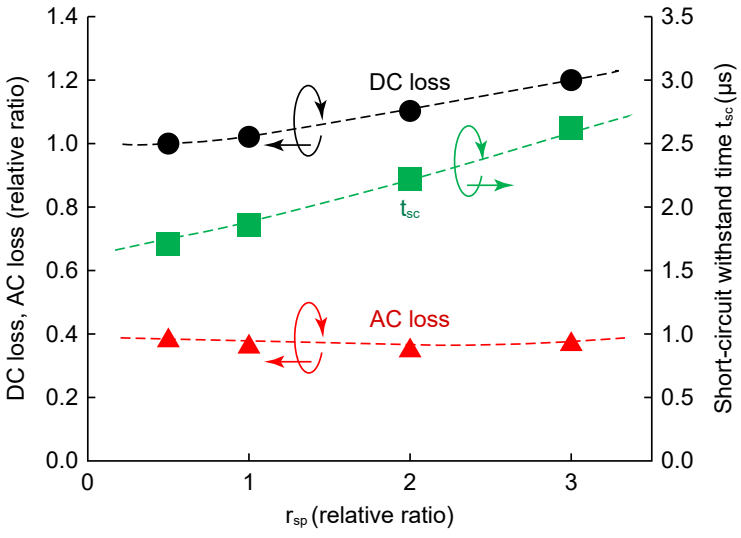


Fig. 7 The relationships between total DC/AC losses, t_{sc} and r_{sp}

3. Conclusion

While trench SiC-MOSFETs are capable of lower losses, their high conductivity means it is difficult to ensure short-circuit capability if a short-circuit occurs in the device. To meet the requirements of a diverse range of applications, a method is needed for controlling the short-circuit capability through the device structure design. Mitsubishi Electric has achieved trade-off control between lower resistance and higher short-circuit withstand time by controlling the short-circuit current resulting from adjustment of the sidewall P-type pillar ratio (r_{sp}) for the device structure of Mitsubishi Electric's proprietary trench-type SiC-MOSFETs. Mitsubishi Electric will continue to move ahead with mass-production of its trench SiC-MOSFETs that are capable of meeting the requirements of a diverse range of applications.

References

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