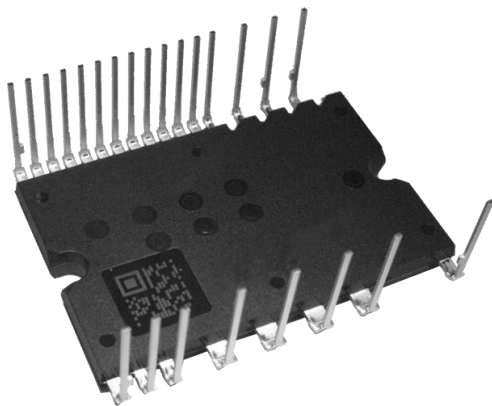


< DIPM >

PSF15S92F6-A6

TRANSFER MOLDING TYPE
INSULATED TYPE

OUTLINE



MAIN FUNCTION AND RATINGS

- 3 phase DC/AC inverter
- 600V / 15A (MOSFET)
- N-side MOSFET open source
- Built-in bootstrap diodes with current limiting resistor

APPLICATION

- AC 100~240Vrms(DC voltage:400V or below) class low power motor control

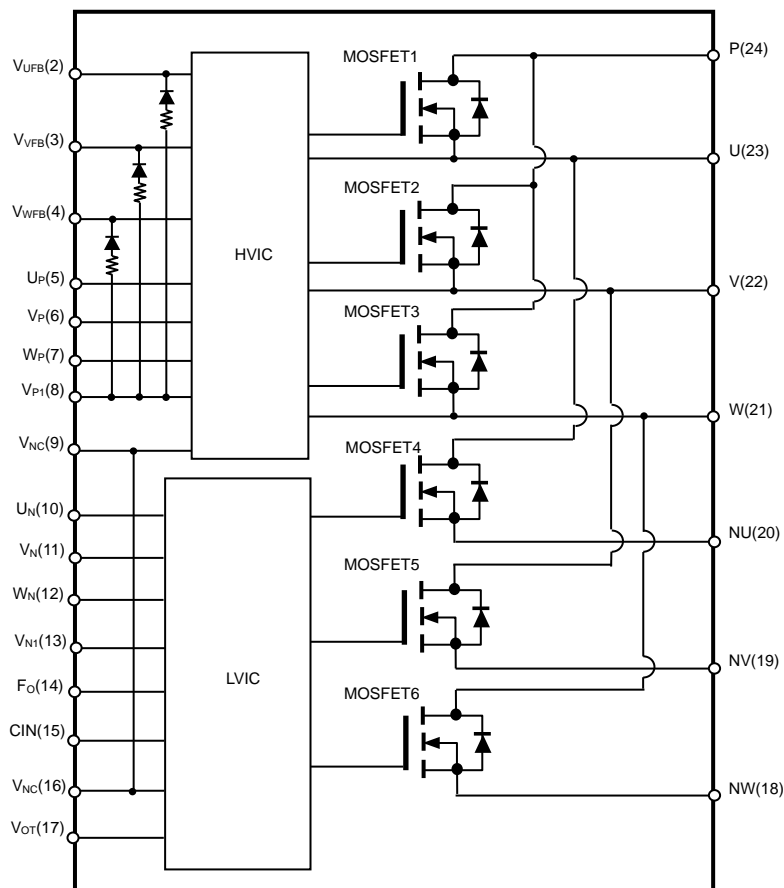
TYPE NAME

PSF15S92F6-A6	With temperature output function
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INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For P-side : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection
- For N-side : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC)
- Fault signaling : Corresponding to SC fault (N-side IGBT), UV fault (N-side supply)
- Temperature output : Outputting LVIC temperature by analog signal
- Input interface : 3, 5V line, Schmitt trigger receiver circuit (High Active)
- UL Recognized : UL1557 File E323585

INTERNAL CIRCUIT



MAXIMUM RATINGS ($T_{ch} = 25^{\circ}\text{C}$, unless otherwise noted)**INVERTER PART**

Symbol	Parameter	Condition	Ratings	Unit
V_{DD}	Supply voltage	Applied between P-NU,NV,NW	450	V
$V_{DD(surge)}$	Supply voltage (surge)	Applied between P-NU,NV,NW	500	V
V_{DS}	Drain-source voltage		600	V
$\pm I_D$	Each MOSFET drain current	$T_{ch} = 25^{\circ}\text{C}$ (Note 1)	15	A
$\pm I_{DP}$	Each MOSFET drain current (peak)	$T_{ch} = 25^{\circ}\text{C}$, less than 1ms	30	A
T_{ch}	Channel temperature	(Note 2)	-30~+150	$^{\circ}\text{C}$

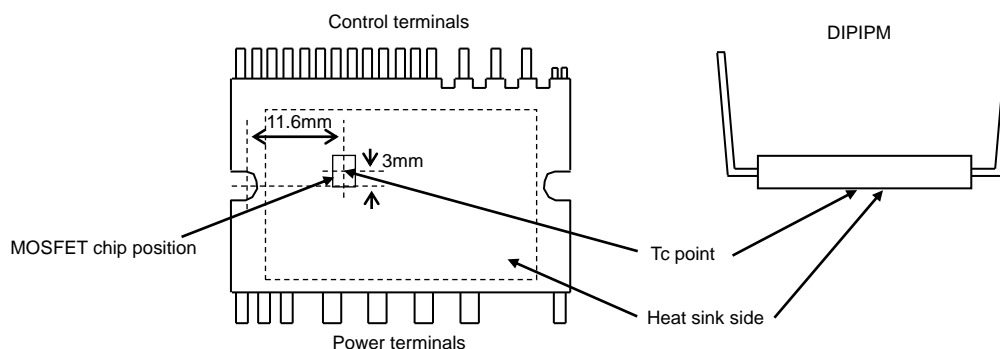
Note1: Pulse width and period are limited due to channel temperature.

Note2: The maximum channel temperature rating of built-in power chips is 150°C (@ $T_c \leq 100^{\circ}\text{C}$). However, to ensure safe operation of DIIPM, the average channel temperature should be limited to $T_{ch(Ave)} \leq 125^{\circ}\text{C}$ (@ $T_c \leq 100^{\circ}\text{C}$).**CONTROL (PROTECTION) PART**

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between $V_{P1}-V_{NC}$, $V_{N1}-V_{NC}$	24	V
V_{DB}	Control supply voltage	Applied between $V_{UFB}-U$, $V_{VFB}-V$, $V_{WFB}-W$	24	V
V_{IN}	Input voltage	Applied between U_P , V_P , W_P , U_N , V_N , W_N-V_{NC}	-0.5~ $V_D+0.5$	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	-0.5~ $V_D+0.5$	V
I_{FO}	Fault output current	Sink current at F_O terminal	1	mA
V_{SC}	Current sensing input voltage	Applied between $CIN-V_{NC}$	-0.5~ $V_D+0.5$	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(prot)}$	Self protection supply voltage limit (Short circuit protection capability)	$V_D = 17\sim 19\text{V}$, Inverter Part $T_{ch} = 125^{\circ}\text{C}$, non-repetitive, less than 2 μs	400	V
T_C	Module case operation temperature	Measurement point of T_C is provided in Fig.1	-30~+100	$^{\circ}\text{C}$
T_{stg}	Storage temperature		-40~+125	$^{\circ}\text{C}$
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	1500	V_{rms}

Fig. 1: T_C MEASUREMENT POINT**THERMAL RESISTANCE**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(ch-c)Q}$	Channel to case thermal resistance	Inverter MOSFET part (per 1/6 module)	-	-	3.7	K/W

Note 3: Grease with good thermal conductivity and long-term endurance should be applied evenly with about $+100\mu\text{m}\sim+200\mu\text{m}$ on the contacting surface of DIIPM and heat sink. The contacting thermal resistance between DIIPM case and heat sink $R_{th(c-f)}$ is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ is about 0.3K/W (per 1/6 module, grease thickness: 20 μm , thermal conductivity: 1.0W/m \cdot K).

ELECTRICAL CHARACTERISTICS ($T_{ch} = 25^{\circ}\text{C}$, unless otherwise noted)**INVERTER PART**

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{DS(on)}$	Drain-source on-state voltage	$V_D=V_{DB} = 18V, V_{IN}= 5V$	$I_D = 15A, T_{ch} = 25^{\circ}C$	-	1.10	1.80	V
			$I_D = 15A, T_{ch} = 125^{\circ}C$	-	1.10	1.80	
			$I_D \approx 1.5A, T_{ch} = 25^{\circ}C$	-	0.10	0.25	
$V_{SD(off)}$	Source- drain voltage	$V_D=V_{DB} = 18V, V_{IN}= 0V, -I_D= 15A$		-	4.00	5.00	V
t_{on}	Switching times	$V_{DD}= 300V, V_D= V_{DB}= 18V$ $I_D= 15A, T_{ch}= 125^{\circ}C, V_{IN}= 0 \leftrightarrow 5V$ Inductive Load (upper-lower arm)		0.70	1.30	1.85	μs
$t_{c(on)}$				-	0.10	0.36	μs
t_{off}				-	1.50	2.10	μs
$t_{c(off)}$				-	0.10	0.18	μs
t_{rr}				-	0.10	-	μs
I_{DSS}	Drain-Source cut-off current	$V_{DS}=V_{DSS}$	$T_{ch} = 25^{\circ}C$	-	-	1	mA
			$T_{ch}=125^{\circ}C$	-	-	10	

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
I _D	Circuit current	Total of V _{P1} -V _{NC} , V _{N1} -V _{NC}	V _D =18V, V _{IN} =0V	-	-	3.50	mA
I _{DB}			V _D =18V, V _{IN} =5V	-	-	3.50	
		Each part of V _{UFB} -U, V _{VFB} -V, V _{WFB} -W	V _D =V _{DB} =18V, V _{IN} =0V	-	-	0.38	
			V _D =V _{DB} =18V, V _{IN} =5V	-	-	0.38	
V _{SC(ref)}	Short circuit trip level	V _D = 18V (Note 4)		0.455	0.480	0.505	V
UV _{DBt}	P-side Control supply under-voltage protection(UV)	T _{ch} ≤125°C	Trip level	10.0	-	12.0	V
UV _{DBr}			Reset level	10.5	-	12.5	V
UV _{Dt}	N-side Control supply under-voltage protection(UV)		Trip level	10.3	-	12.5	V
UV _{Dr}			Reset level	10.8	-	13.0	V
V _{OT}	Temperature Output	Pull down R=5.1kΩ (Note 5)	LVIC Temperature=90°C	2.63	2.77	2.91	V
			LVIC Temperature=25°C	0.88	1.13	1.39	V
V _{FOH}	Fault output voltage	V _{SC} = 0V, F _O terminal pulled up to 5V by 10kΩ		4.9	-	-	V
V _{FOL}		V _{SC} = 1V, I _{FO} = 1mA		-	-	0.95	V
t _{FO}	Fault output pulse width	(Note 6)		20	-	-	μs
I _{IN}	Input current	V _{IN} = 5V		0.70	1.00	1.50	mA
V _{th(on)}	ON threshold voltage	Applied between U _P , V _P , W _P , U _N , V _N , W _N -V _{NC}		-	2.10	2.60	V
V _{th(off)}	OFF threshold voltage			0.80	1.50	-	
V _{th(hys)}	ON/OFF threshold hysteresis voltage			0.35	0.65	-	
V _F	Bootstrap Di forward voltage	I _F =10mA including voltage drop by limiting resistor (Note 7)		0.9	1.3	1.7	V
R	Built-in limiting resistance	Included in bootstrap Di		48	60	72	Ω

Note 4 : SC protection works only for N-side MOSFETs. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.

5 : DIIPM don't shutdown MOSFETs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIIPM. Temperature of LVIC vs. V_{OT} output characteristics is described in Fig. 3.

6 : Fault signal F_O outputs when SC or UV protection works. F_O pulse width is different for each protection modes. At SC failure, F_O pulse width is a fixed width (=minimum 20 μs), but at UV failure, F_O outputs continuously until recovering from UV state. (But minimum F_O pulse width is 20 μs .)

7 : The characteristics of bootstrap Di is described in Fig.2.

Fig. 2 Characteristics of bootstrap Di V_F - I_F curve (@ $T_a=25^{\circ}\text{C}$) including voltage drop by limiting resistor (Right chart is enlarged chart.)

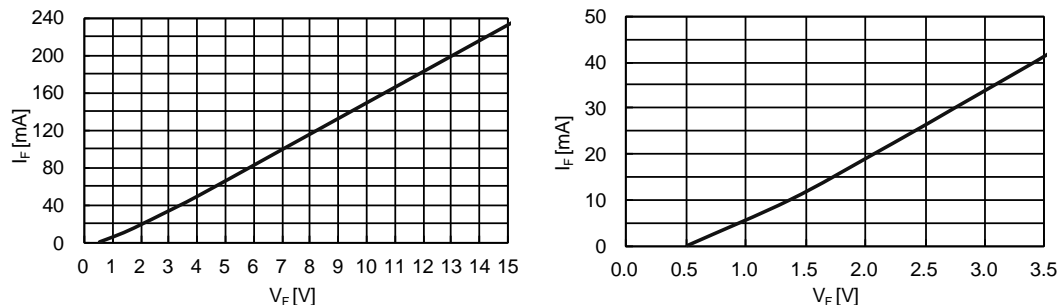
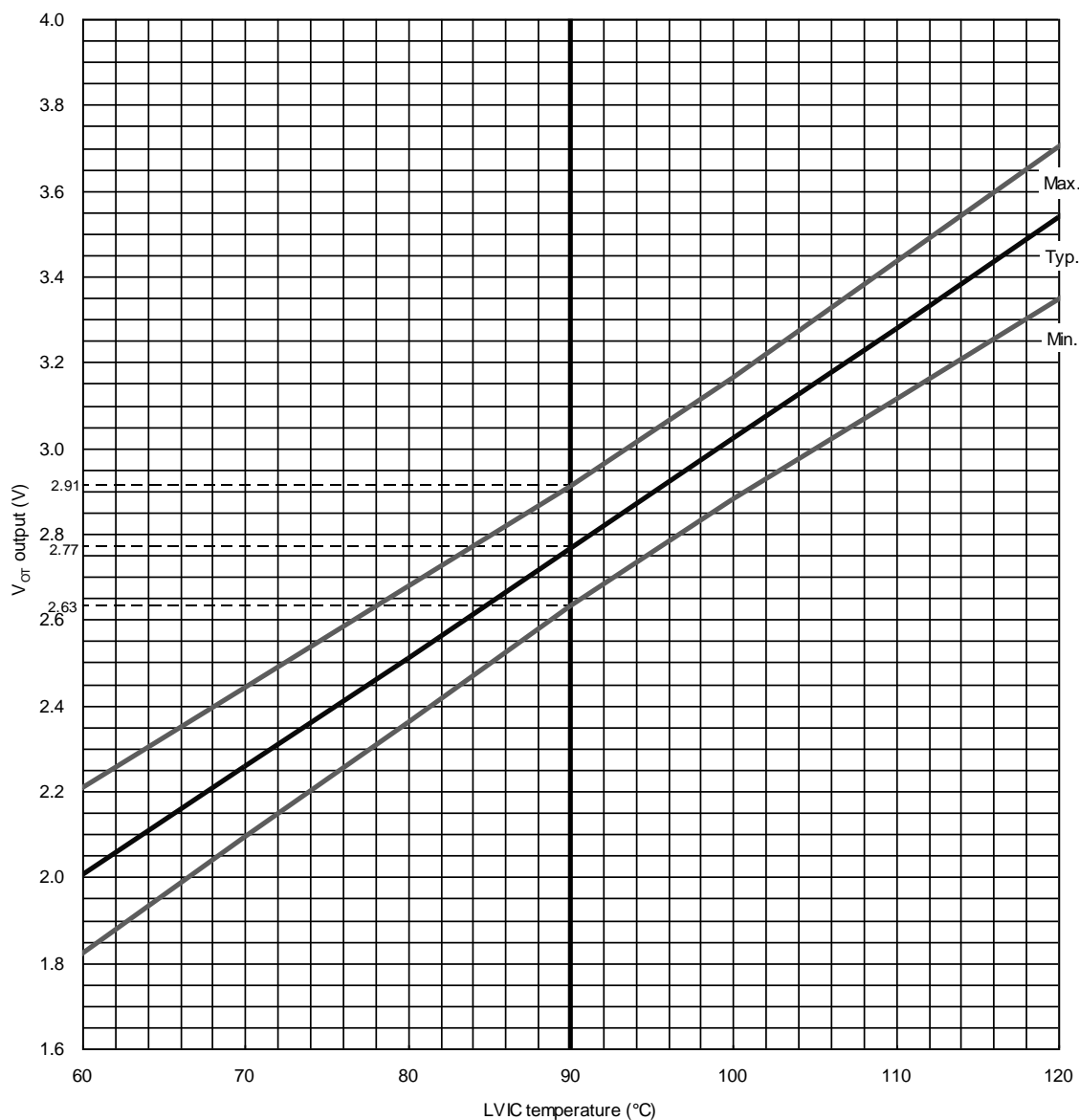
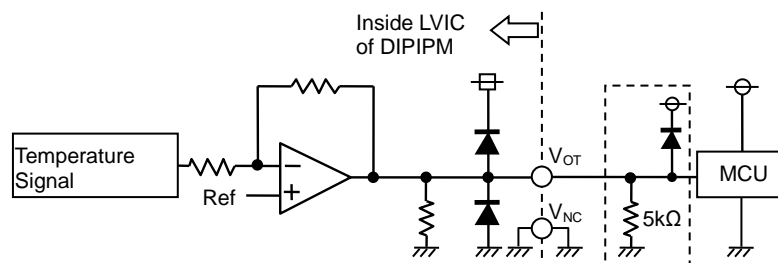


Fig. 3 Temperature of LVIC vs. V_{OT} output characteristicsFig. 4 V_{OT} output circuit

- (1) It is recommended to insert 5kΩ (5.1kΩ is recommended) pull down resistor for getting linear output characteristics at low temperature below room temperature. When the pull down resistor is inserted between V_{OT} and V_{NC} (control GND), the extra circuit current, which is calculated approximately by V_{OT} output voltage divided by pull down resistance, flows as LVIC circuit current continuously. In the case of using V_{OT} for detecting high temperature over room temperature only, it is unnecessary to insert the pull down resistor.
- (2) In the case of using V_{OT} with low voltage controller like 3.3V MCU, V_{OT} output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and V_{OT} output for preventing over voltage destruction.
- (3) In the case of not using V_{OT} , leave V_{OT} output NC (No Connection).

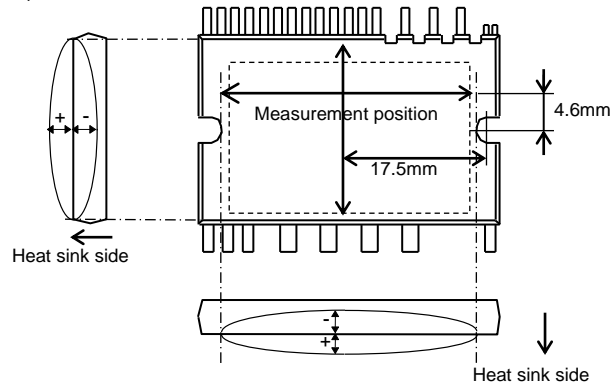
Refer the application note for Super Mini DIIPM Ver.6 series about the usage of V_{OT} .

PSF15S92F6-A6**TRANSFER MOLDING TYPE
INSULATED TYPE****MECHANICAL CHARACTERISTICS AND RATINGS**

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3 (Note 8)	Recommended 0.69N·m	0.59	0.69	0.78	N·m
Terminal pulling strength	Control terminal: Load 4.9N Power terminal: Load 9.8N	JEITA-ED-4701	10	-	-	s
Terminal bending strength	Control terminal: Load 2.45N Power terminal: Load 4.9N 90deg. bend	JEITA-ED-4701	2	-	-	times
Weight			-	8.5	-	g
Heat radiation part flatness	(Note 9)		-50	-	100	μm

Note 8: Plain washers (ISO 7089~7094) are recommended.

Note 9: Measurement point of heat radiation part flatness

**RECOMMENDED OPERATION CONDITIONS**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	Applied between P-NU, NV, NW	0	300	400	V
V_D	Control supply voltage	Applied between V_{P1} - V_{NC} , V_{N1} - V_{NC}	17.0	18.0	19.0	V
V_{DB}	Control supply voltage	Applied between V_{UFB} -U, V_{VFB} -V, V_{WFB} -W	15.0	18.0	22.0	V
ΔV_D , ΔV_{DB}	Control supply variation		-1	-	+1	V/μs
t_{dead}	Arm shoot-through blocking time	For each input signal	1.5	-	-	μs
f_{PWM}	PWM input frequency	$T_C \leq 100^\circ\text{C}$, $T_{ch} \leq 125^\circ\text{C}$	-	5	20	kHz
I_O	Allowable r.m.s. current	$V_{DD} = 300\text{V}$, $V_D = V_{DB} = 18\text{V}$, P.F = 0.8, Sinusoidal PWM $T_C \leq 100^\circ\text{C}$, $T_{ch} \leq 125^\circ\text{C}$ (Note10)	-	-	10	Arms
PWIN(on)		(Note 11)	0.7	-	-	
PWIN(off)	Minimum input pulse width	$200\text{V} \leq V_{DD} \leq 350\text{V}$, $17\text{V} \leq V_D \leq 19\text{V}$, $15\text{V} \leq V_{DB} \leq 22\text{V}$, $-30^\circ\text{C} \leq T_C \leq 100^\circ\text{C}$, N-line wiring inductance less than 10nH (Note 12) Between rated current and 1.7 times of rated current	1.5	-	-	μs
V_{NC}	V_{NC} variation	Between V_{NC} -NU, NV, NW (including surge)	-5.0	-	+5.0	V
T_{ch}	Channel temperature		-30	-	+125	°C

Note 10: In the case of turning on the MOSFET into which free-wheeling current is flowing. Allowable r.m.s. current depends on the actual application conditions.

11: DIIPM might not make response if the input signal pulse width is less than PWIN(on).

12: IPM might make delayed response or no response for the input signal with off pulse width less than PWIN(off). Please refer below about delayed response.

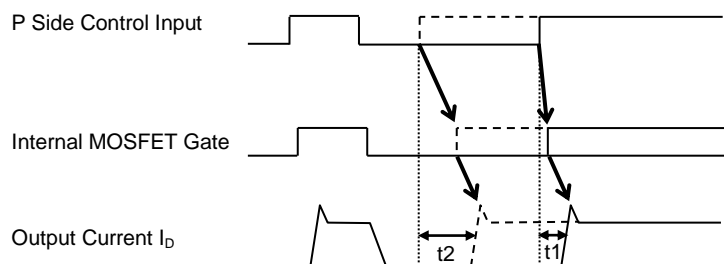
Delayed Response against Shorter Input Off Signal than PWIN(off) (P-side only)Real line: off pulse width > PWIN(off); turn on time t1
Broken line: off pulse width < PWIN(off); turn on time t2
(t1: Normal switching time)

Fig. 5 Timing Charts of The DIIPM Protective Functions

[A] Short-Circuit Protection (N-side only with the external shunt resistor and RC filter)

a1. Normal operation: MOSFET ON and outputs current.

a2. Short circuit current detection (SC trigger)

(It is recommended to set RC time constant 1.5~2.0 μ s so that MOSFET shut down within 2.0 μ s when SC.)

a3. All N-side MOSFET's gates are hard interrupted.

a4. All N-side MOSFETs turn OFF.

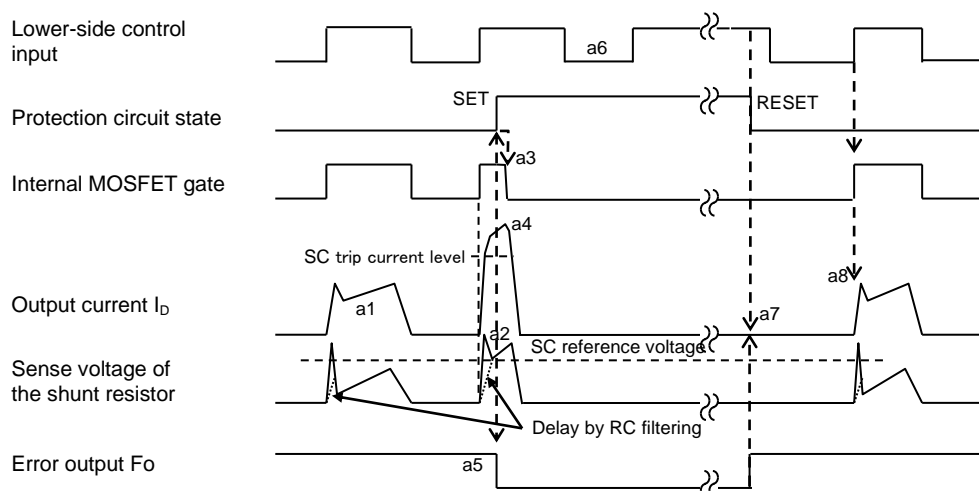
a5. F_O outputs for t_{Fo} =minimum 20 μ s.

a6. Input = "L": MOSFET OFF

a7. F_O finishes output, but MOSFETs don't turn on until inputting next ON signal (L \rightarrow H).

(MOSFET of each phase can return to normal state by inputting ON signal to each phase.)

a8. Normal operation: MOSFET ON and outputs current.

**[B] Under-Voltage Protection (N-side, UV_D)**b1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but MOSFET turns ON by next ON signal (L \rightarrow H).

(MOSFET of each phase can return to normal state by inputting ON signal to each phase.)

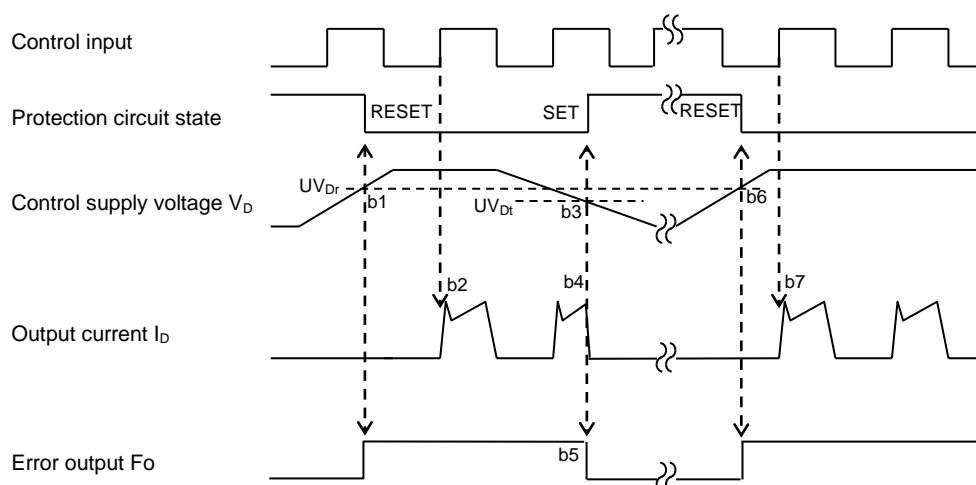
b2. Normal operation: MOSFET ON and outputs current.

b3. V_D level drops to under voltage trip level. (UV_{Dt}).

b4. All N-side MOSFETs turn OFF in spite of control input condition.

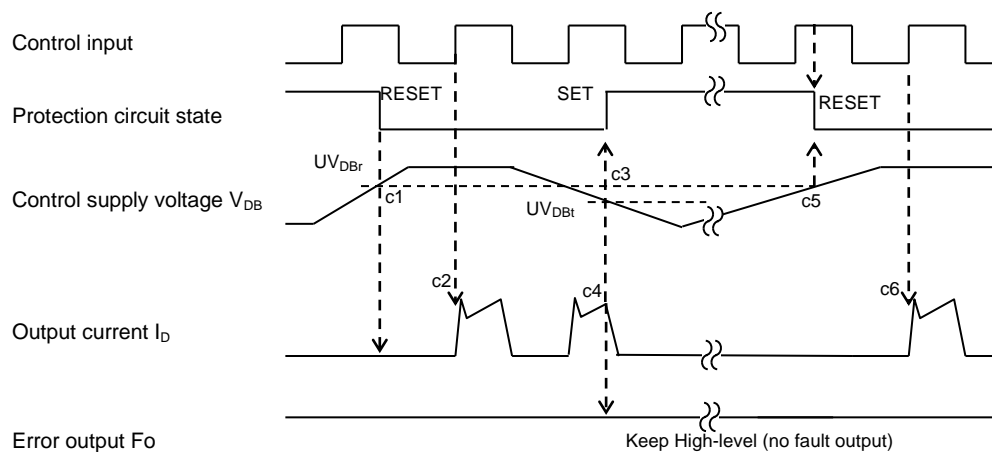
b5. F_O outputs for t_{Fo} =minimum 20 μ s, but output is extended during V_D keeps below UV_{Dr} .b6. V_D level reaches UV_{Dr} .

b7. Normal operation: MOSFET ON and outputs current.



[C] Under-Voltage Protection (P-side, UV_{DB})

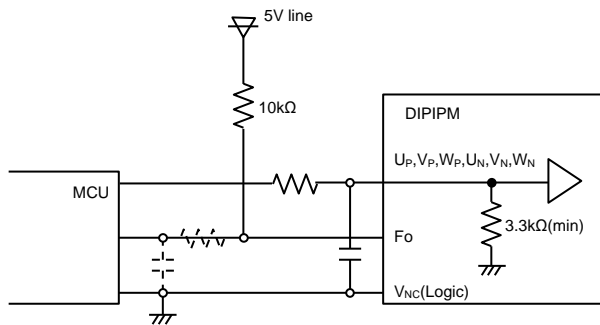
- c1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr} , MOSFET turns on by next ON signal (L→H).
- c2. Normal operation: MOSFET ON and outputs current.
- c3. V_{DB} level drops to under voltage trip level (UV_{DBt}).
- c4. MOSFET of the corresponding phase only turns OFF in spite of control input signal level, but there is no F_O signal output.
- c5. V_{DB} level reaches UV_{DBr} .
- c6. Normal operation: MOSFET ON and outputs current.



[illegible]

- 8

Fig. 7 MCU I/O Interface Circuit

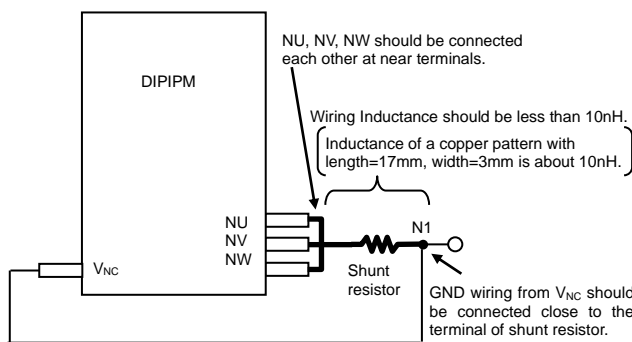


Note)

Design for input RC filter depends on PWM control scheme used in the application and wiring impedance of the printed circuit board. DIIPM input signal interface integrates a minimum 3.3kΩ pull-down resistor. Therefore, when inserting RC filter, it is necessary to satisfy turn-on threshold voltage requirement.

F_O output is open drain type. It should be pulled up to control power supply (e.g. 5V, 18V) with a resistor that makes F_O sink current I_{F_O} 1mA or less. In the case of pulled up to 5V supply, 10kΩ (5kΩ or more) is recommended.

Fig. 8 Pattern Wiring Around the Shunt Resistor



Low inductance shunt resistor like surface mounted (SMD) type is recommended.

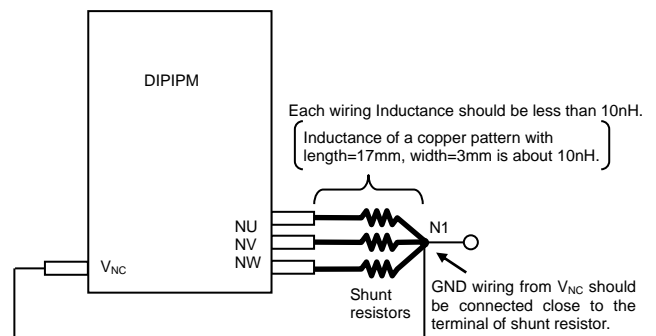
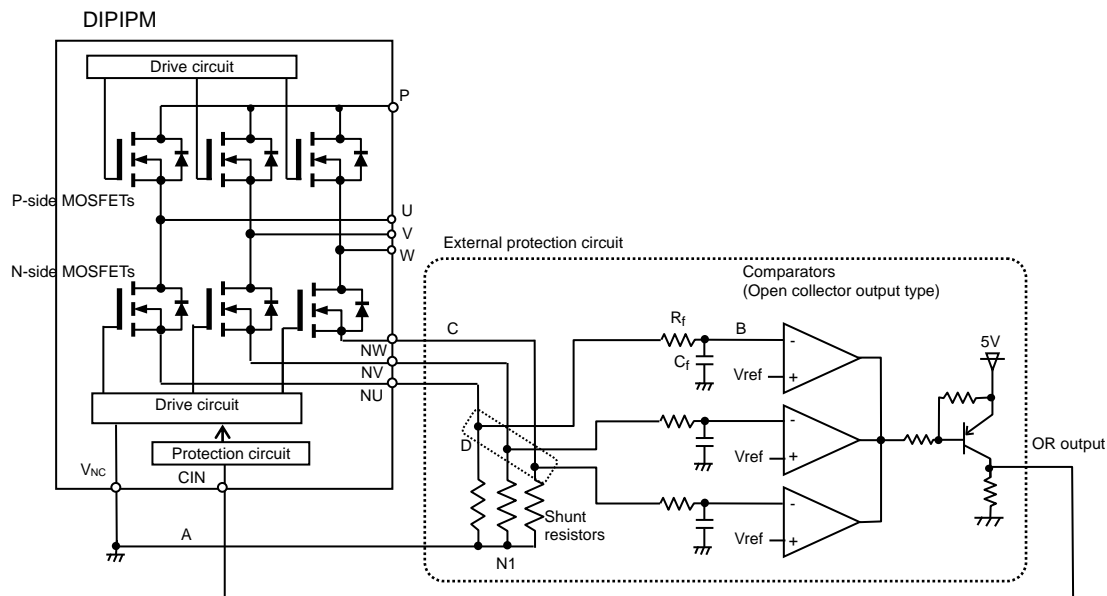


Fig. 9 Pattern Wiring Around the Shunt Resistor (for the case of open emitter)

When DIIPM is operated with three shunt resistors, voltage of each shunt resistor cannot be input to CIN terminal directly. In that case, it is necessary to use the external protection circuit as below.

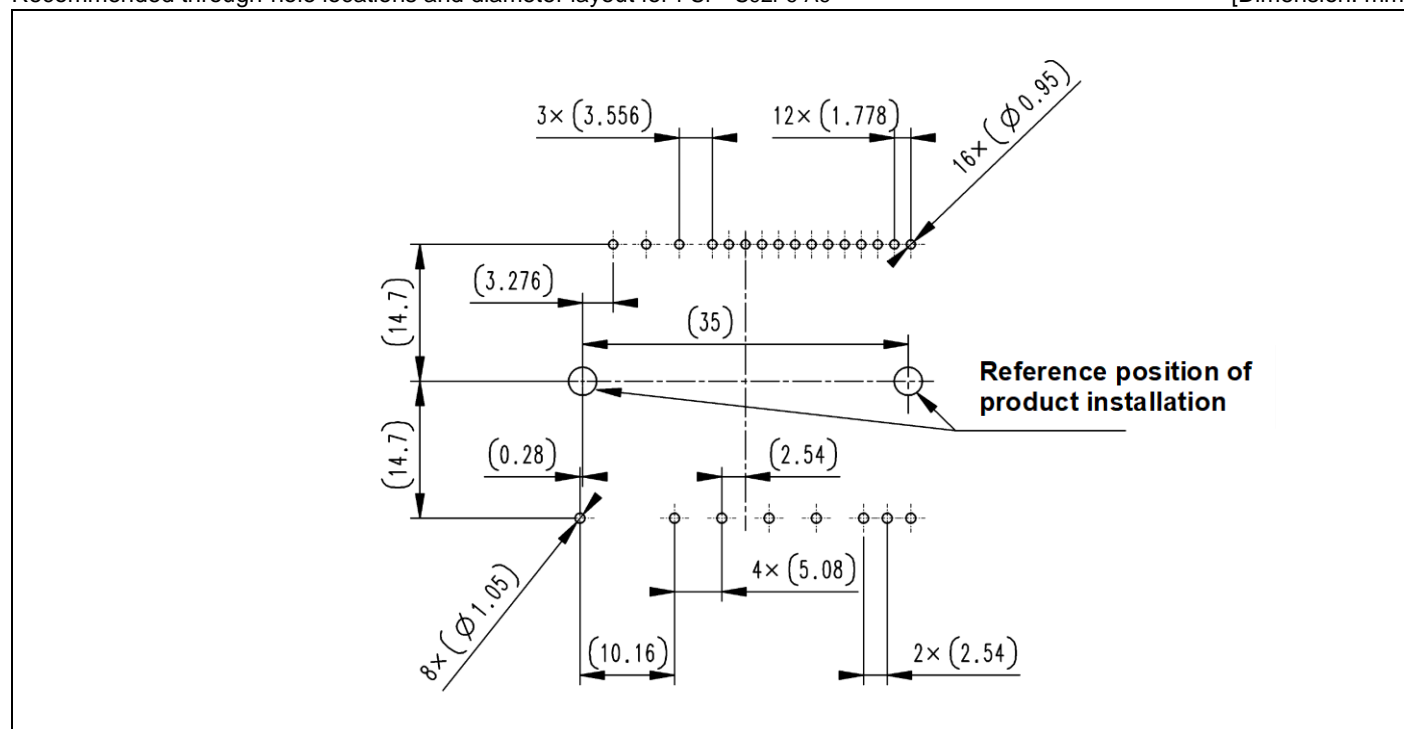


- (1) It is necessary to set the time constant $R_f C_f$ of external comparator input so that IGBT stops within 2μs when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on.
- (2) It is recommended for the threshold voltage V_{ref} to set to the same rating of short circuit trip level ($V_{sc(ref)}$: typ. 0.48V).
- (3) Select the external shunt resistance so that SC trip-level is less than specified value (≈ 1.7 times of rating current).
- (4) To avoid malfunction, the wiring A, B, C should be as short as possible.
- (5) The point D at which the wiring to comparator is divided should be close to the terminal of shunt resistor.
- (6) OR output high level when protection works should be over 0.505V (\approx maximum $V_{sc(ref)}$ rating).

Fig. 10 (Reference Figure) PCB Through-hole Pattern

Recommended through-hole locations and diameter layout for PSF**S92F6-A6

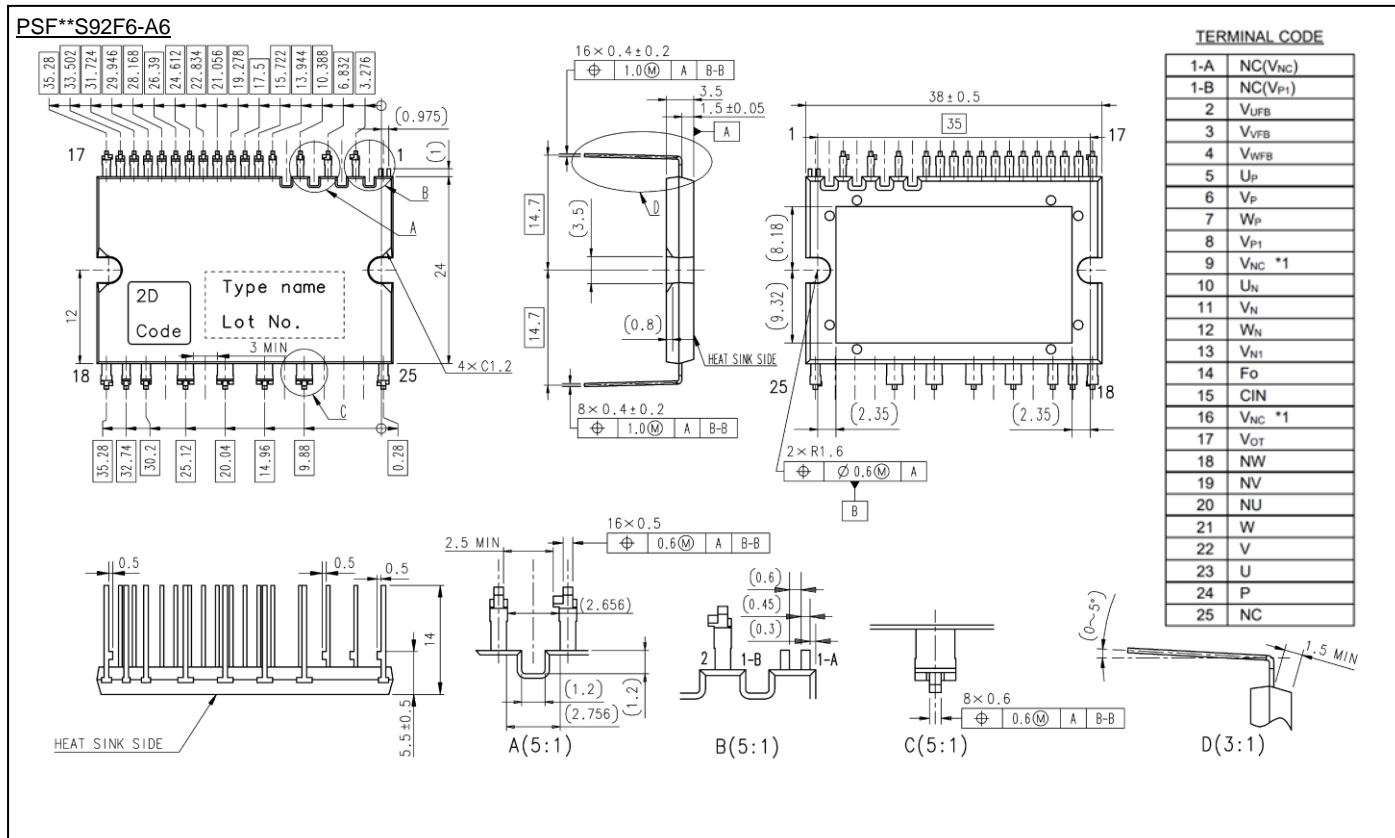
[Dimension: mm]



PSF15S92F6-A6**TRANSFER MOLDING TYPE
INSULATED TYPE**

Fig. 11 Package Outlines

[Dimension: mm]



1) 9 & 16 pins (V_{NC}) are connected inside DIIPM, please connect either one to the control power supply GND outside and leave another one open.

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