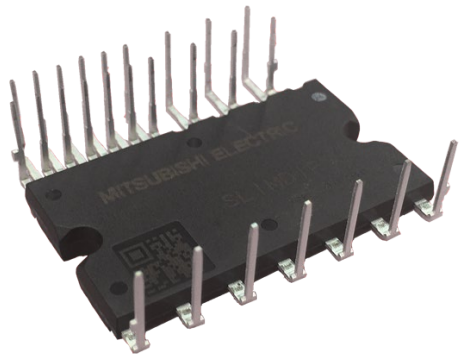
MITSUBISHI ELECTRIC

< DIPIPM >

PSF15SG1G6

TRANSFER MOLDING TYPE
INSULATED TYPE

OUTLINE



Normal terminal

MAIN FUNCTION AND RATINGS

- 3 phase DC/AC inverter
- 600V / 15A (SiC MOSFET)
- N-side MOSFET open source
- Built-in bootstrap diodes with current limiting resistor

APPLICATION

- AC 100~240Vrms(DC voltage:400V or below) class low power motor control

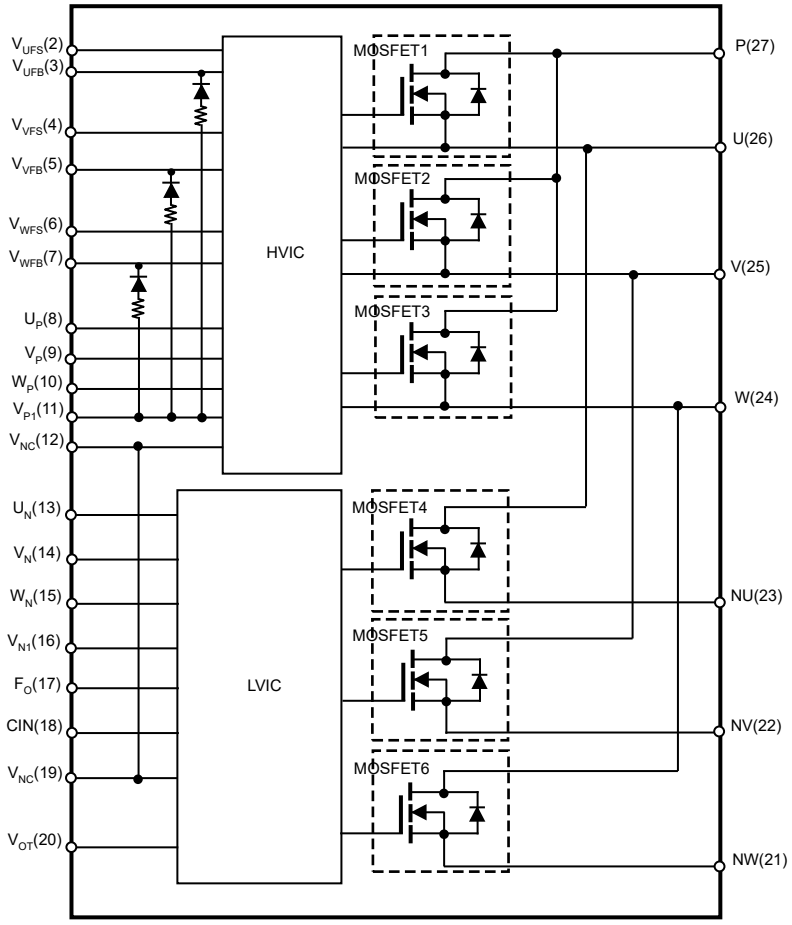
TERMINAL LINE UP

Normal terminal	PSF15SG1G6
Short terminal	PSF15SG1G6-S

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For P-side : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage protection (UV)
- For N-side : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC), Over temperature protection (OT)
- Fault signaling : Corresponding to SC fault (N-side MOSFET), UV fault (N-side supply) and OT fault
- Temperature output : Outputting LVIC temperature by analog signal
- Input interface : 3, 5V line, Schmitt trigger receiver circuit (High Active)
- UL Recognized : UL1557 File E323585

INTERNAL CIRCUIT



MAXIMUM RATINGS (T_{ch} = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{DD}	Supply voltage	Applied between P-NU, NV, NW (Voltage at smoothing capacitor)	450	V
$V_{DD(surge)}$	Supply voltage (surge)	Applied between P-NU,NV,NW	500	V
V_{DSS}	Drain-source voltage		600	V
$\pm I_D$	Each MOSFET drain current	T_C= 25°C (Note 1)	15	A
$\pm I_{DP}$	Each MOSFET drain current (peak)	T_C= 25°C, less than 1ms	30	A
T_{ch}	Channel temperature	(Note 2)	-30~+150	°C

Note1: Pulse width and period are limited due to channel temperature.
Note2: The maximum channel temperature rating of the power chips integrated within the DIPIPM is 150°C(@Tc≤115°C) however, to insure safe operation of the DIPIPM, the average channel temperature should be limited to Tch ≤125°C (@Tc≤115°C).

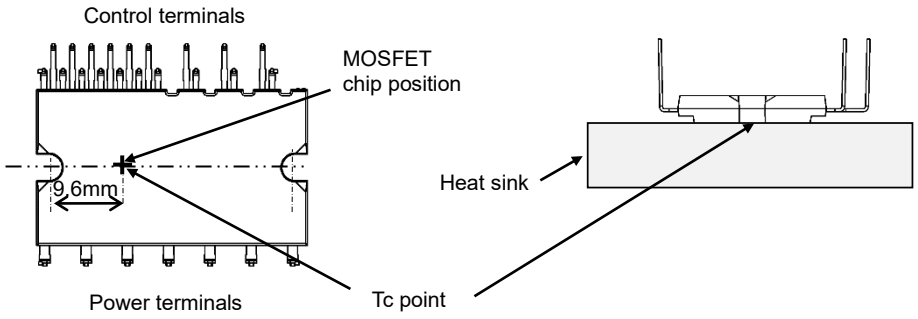
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	20	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	20	V
V_{IN}	Input voltage	Applied between U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}	-0.5~V_D+0.5	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	-0.5~V_D+0.5	V
I_{FO}	Fault output current	Sink current at F_O terminal	1	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	-0.5~V_D+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{DD(PROT)}$	Self protection supply voltage limit (Short circuit protection capability)	V_D = 13.5~16.5V, Inverter Part T_{ch}= 125°C, non-repetitive, less than 2μs	400	V
T_C	Module case operation temperature	Measurement point of Tc is provided in Fig.1	-30~+115	°C
T_{stg}	Storage temperature		-40~+125	°C
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	2000	V_{rms}

Fig. 1: T_C MEASUREMENT POINT



THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(ch-c)Q}$	Channel to case thermal resistance (Note 3)	Inverter MOSFET part (per 1/6 module)	-	-	4.0	K/W

Note 3: Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100μm~+200μm on the contacting surface of DIPIPM and heat sink. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.4K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m•K).

ELECTRICAL CHARACTERISTICS (T_{ch} = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$V_{DS(ON)}$	Drain-source on-state voltage	V_D=V_{DB}=15V, V_{IN}= 5V, I_D=15A	-	1.30	2.15	V
$V_{SD(OFF)}$	Source-drain off-state voltage	V_D=V_{DB}=15V, V_{IN}=0V, -I_D=15A	-	4.00	5.00	V
t_{on}	Switching times	V_{DD}= 300V, V_D= V_{DB}= 15V I_D= 15A, V_{IN}= 0↔5V Inductive Load (upper-lower arm)	0.45	0.75	1.10	μs
$t_{c(on)}$			-	0.15	0.30	μs
t_{off}			-	0.70	1.05	μs
$t_{c(off)}$			-	0.05	0.15	μs
t_{rr}			-	0.15	-	μs
I_{DDS}	Drain-Source cut-off current	V_{DS}=V_{DSS}	-	-	1	mA

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit current	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	V_D=15V, V_{IN}=0V	-	-	3.10	mA
			V_D=15V, V_{IN}=5V	-	-	4.20	
I_{DB}		Each part of V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	V_D=V_{DB}=15V, V_{IN}=0V	-	-	0.10	
			V_D=V_{DB}=15V, V_{IN}=5V	-	-	0.10	
V_{FOH}	Fault output voltage	V_{SC} = 0V, F_O terminal pulled up to 5V by 10kΩ		4.9	-	-	V
V_{FOL}		V_{SC} = 1V, I_{FO} = 1mA		-	-	0.95	V
I_{IN}	Input current	V_{IN} = 5V		0.70	1.00	1.50	mA
$V_{SC(ref)}$	Short circuit trip level	V_D = 15V (Note 4)		0.455	0.480	0.505	V
V_{OT}	Temperature Output	LVIC Temperature=95°C, Pull down R=5.1kΩ (Note 5)		2.76	2.89	3.03	V
OT_t	Over temperature Protection (Note8)	V_D=15V, At temperature of LVIC	Trip level	115	130	145	°C
OT_{rh}			Trip/reset hysteresis	-	10	-	
UV_{DBt}	P-side Control supply under-voltage protection	Trip level		9.0	10.0	12.0	V
UV_{DBr}		Reset level		9.0	10.0	12.0	V
UV_{Dt}	N-side Control supply under-voltage protection	Trip level		10.3	-	12.5	V
UV_{Dr}		Reset level		10.8	-	13.0	V
t_{FO}	Fault output pulse width	(Note 6)		20	-	-	μs
$V_{th(on)}$	ON threshold voltage	Applied between U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}		-	1.70	2.35	V
$V_{th(off)}$	OFF threshold voltage			0.70	1.30	-	
$V_{th(hys)}$	ON/OFF threshold hysteresis voltage			0.25	0.40	-	
V_F	Bootstrap Di forward voltage	I_F=10mA including voltage drop by limiting resistor (Note 7)		0.9	1.3	1.7	V
R	Built-in limiting resistance	Included in bootstrap Di		48	60	72	Ω

Note 4 : SC protection works only for N-side MOSFETs. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.

5 : For temperature output type, DIPIPM don't shutdown MOSFETs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIPIPM. Temperature of LVIC vs. VOT output characteristics is described in Fig. 3.

6 : Fault signal Fo outputs when SC or UV protection works. Fo pulse width is different for each protection modes. At SC failure, Fo pulse width is a fixed width (=minimum 20μs), but at UV failure, Fo outputs continuously until recovering from UV state. (But minimum Fo pulse width is 20μs.)

7 : The characteristics of bootstrap Di is described in Fig.2.

Fig. 2 Characteristics of bootstrap Di V_F-I_F curve (@Ta=25°C) including voltage drop by limiting resistor (Right chart is enlarged chart.)

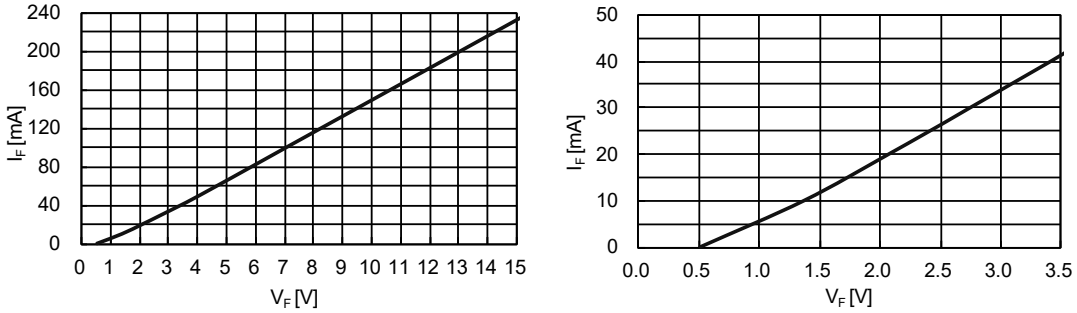


Fig. 3 Temperature of LVIC vs. V_{OT} output characteristics

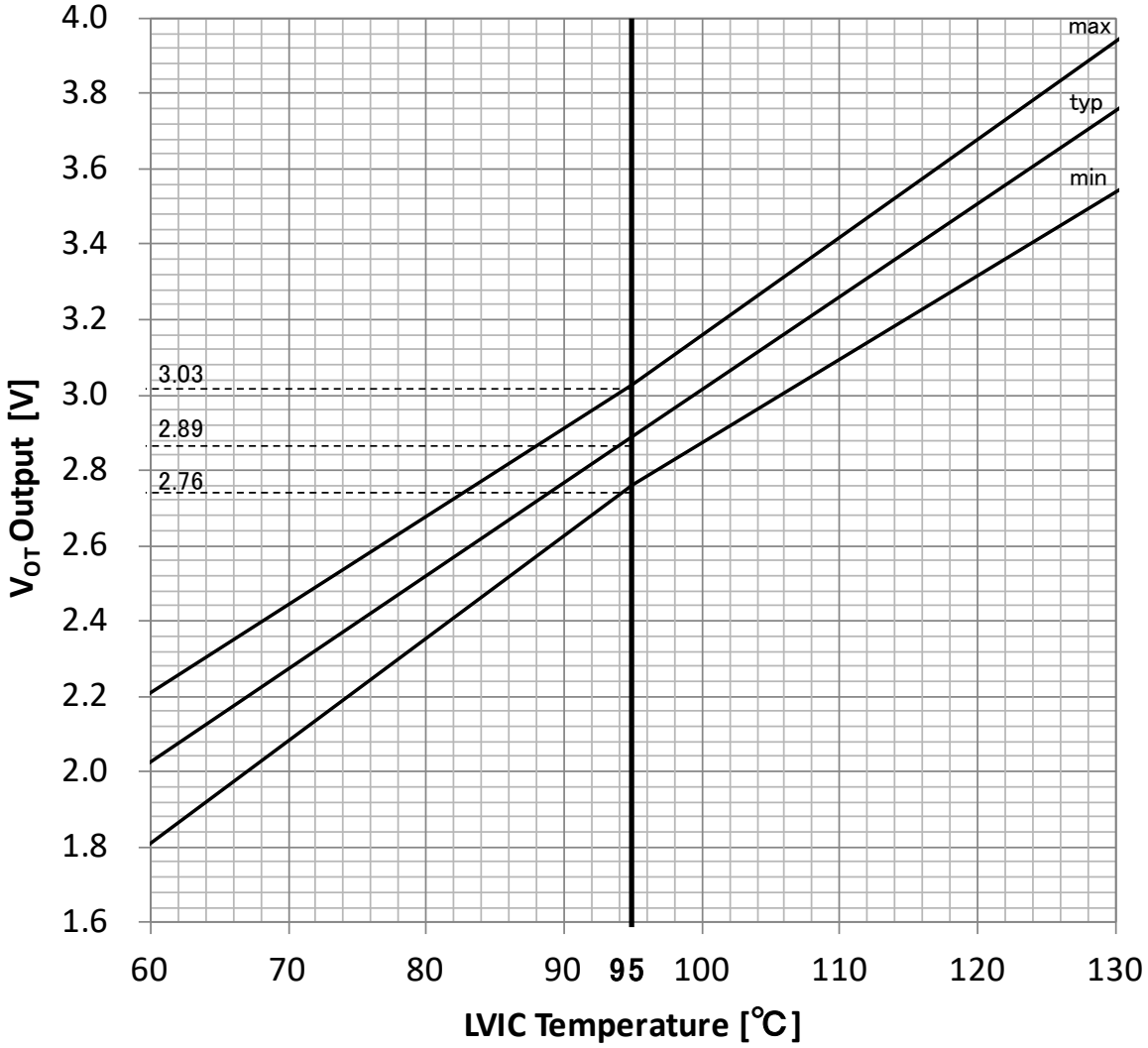
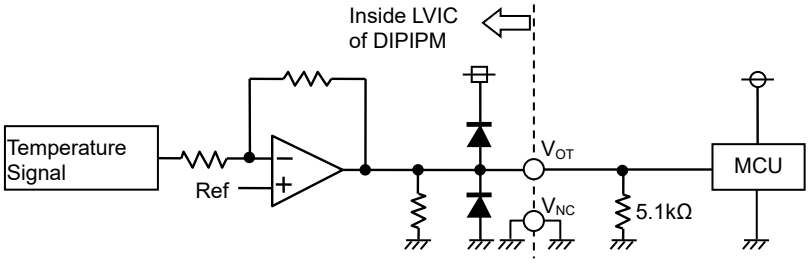


Fig. 4 V_{OT} output circuit



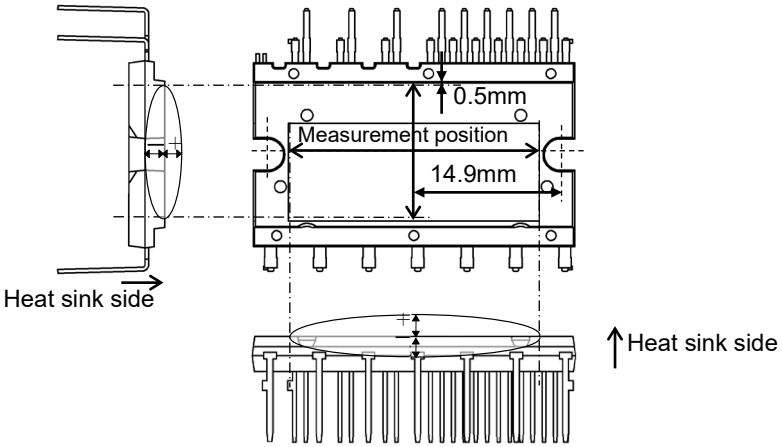
(1) It is recommended to insert 5kΩ (5.1kΩ is recommended) pull down resistor for getting linear output characteristics at low temperature below room temperature. When the pull down resistor is inserted between V_{OT} and V_{NC}(control GND), the extra circuit current, which is calculated approximately by V_{OT} output voltage divided by pull down resistance, flows as LVIC circuit current continuously. In the case of using V_{OT} for detecting high temperature over room temperature only, it is unnecessary to insert the pull down resistor.
(2) In the case of using V_{OT} with low voltage controller like 3.3V MCU, V_{OT} output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and V_{OT} output for preventing over voltage destruction.
(3) In the case of not using V_{OT}, leave V_{OT} output NC (No Connection).
Refer the application note about the usage of V_{OT}.

Note.8 The Over Temperature (OT) protection function outputs a fault signal (Fo) and shutdown all three low-side MOSFETs when the LVIC chip temperature reaches the OT trip level. The input control signals will be blocked and the MOSFETs will be kept shutdown during OT trip period. The Fo output will be reset when the LVIC chip temperature drops down below the OT reset level, however, the MOSFET will be kept to shutdown till the next input signal. For those cases that OT protection is activated due to the over temperature caused by loosening of the installation or the DIPIPM coming off the fin, it is strongly recommended to exchange the DIPIPM for new one.
(Please do not use the that DIPIPM continuously, because the channel temperature of the internal power chips might exceed the allowable maximum temperature 150°C.)

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition	Reference	Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3 (Note 9)	JEITA-ED-4701 402 method Ⅱ	0.59	0.69	0.78	N·m
Terminal pulling strength	Control terminal: Load 5N Power terminal: Load 10N	JEITA-ED-4701 401 method Ⅰ	10	-	-	s
Terminal bending strength	Control terminal: Load 2.5N Power terminal: Load 5N 90deg. Bend	JEITA-ED-4701 401 method Ⅲ	2	-	-	times
Weight			-	5.5	-	g
Heat radiation part flatness	(Note 10)		-30	-	+80	μm

Note 9: Plain washers (ISO 7089~7094) are recommended.
Note 10: Measurement point of heat radiation part flatness



RECOMMENDED OPERATION CONDITIONS

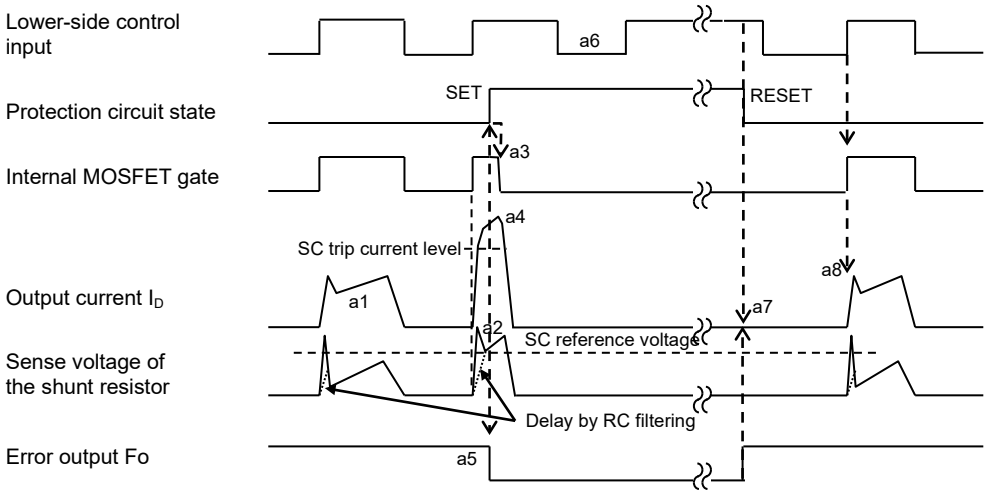
Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	Applied between P-NU, NV, NW	0	300	400	V
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	13.0	15.0	18.5	V
ΔV_D, ΔV_{DB}	Control supply variation		-1	-	+1	V/μs
t_{dead}	Arm shoot-through blocking time	For each input signal	1.0	-	-	μs
f_{PWM}	PWM input frequency	$T_C \leq 115°C$, $T_{ch} \leq 125°C$	-	-	20	kHz
V_{NC}	V_{NC} variation	Between V_{NC}-NU, NV, NW (including surge)	-5	-	+5	V
PWIN(on)	Minimum input pulse width	(Note 11)	0.7	-	-	μs
PWIN(off)			0.7	-	-	
T_{ch}	Channel temperature		-20	-	+125	°C

Note 11: DIPIPM might not make response if the input signal pulse width is less than PWIN(on), PWIN(off).

Fig. 5 Timing Charts of The DIPIPM Protective Functions

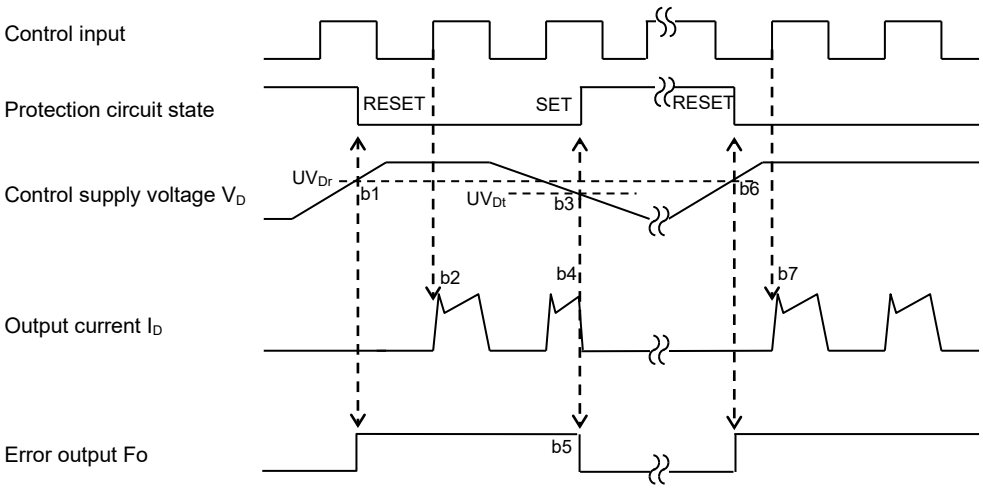
[A] Short-Circuit Protection (N-side only with the external shunt resistor and RC filter)

a1. Normal operation: MOSFET ON and outputs current.
a2. Short circuit current detection (SC trigger)
(It is recommended to set RC time constant 1.5~2.0μs so that MOSFET shut down within 2.0μs when SC.)
a3. All N-side MOSFETs gates are hard interrupted.
a4. All N-side MOSFETs turn OFF.
a5. F_O outputs for t_{Fo}=minimum 20μs.
a6. Input = "L": MOSFET OFF
a7. Fo finishes output, but MOSFETs don't turn on until inputting next ON signal (L→H).
(MOSFETs of each phase can return to normal state by inputting ON signal to each phase.)
a8. Normal operation: MOSFET ON and outputs current.



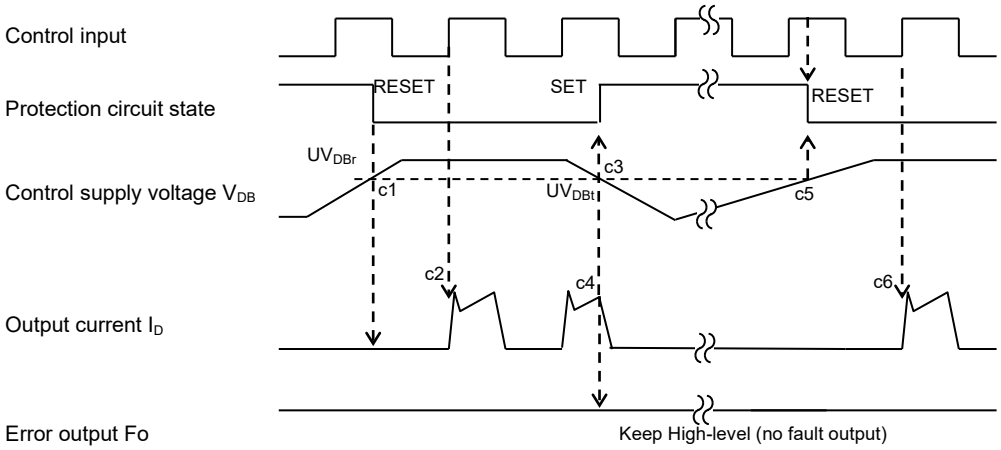
[B] Under-Voltage Protection (N-side, UV_D)

b1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but MOSFET turns ON by next ON signal (L→H).
(MOSFET of each phase can return to normal state by inputting ON signal to each phase.)
b2. Normal operation: MOSFET ON and outputs current.
b3. V_D level drops to under voltage trip level. (UV_{Dt}).
b4. All N-side MOSFETs turn OFF in spite of control input condition.
b5. Fo outputs for t_{Fo}=minimum 20μs, but output is extended during V_D keeps below UV_{Dr}.
b6. V_D level reaches UV_{Dr}.
b7. Normal operation: MOSFET ON and outputs current.



[C] Under-Voltage Protection (P-side, UV_{DB})

c1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr}, MOSFET turns on by next ON signal (L→H).
c2. Normal operation: MOSFET ON and outputs current.
c3. V_{DB} level drops to under voltage trip level (UV_{DBt}).
c4. MOSFET of the corresponding phase only turns OFF in spite of control input signal level, but there is no F_O signal output.
c5. V_{DB} level reaches UV_{DBr}.
c6. Normal operation: MOSFET ON and outputs current.



[D] Over Temperature Protection (N-side, Detecting LVIC temperature)

d1. Normal operation: MOSFET ON and outputs current.
d2. LVIC temperature exceeds over temperature trip level(OT_t).
d3. All N-side MOSFETs turn OFF in spite of control input condition.
d4. Fo outputs for t_{Fo}=minimum 20μs, but output is extended during LVIC temperature keeps over OT_t.
d5. LVIC temperature drops to over temperature reset level.
d6. Normal operation: MOSFET turns on by next ON signal (L→H).
(MOSFET of each phase can return to normal state by inputting ON signal to each phase.)

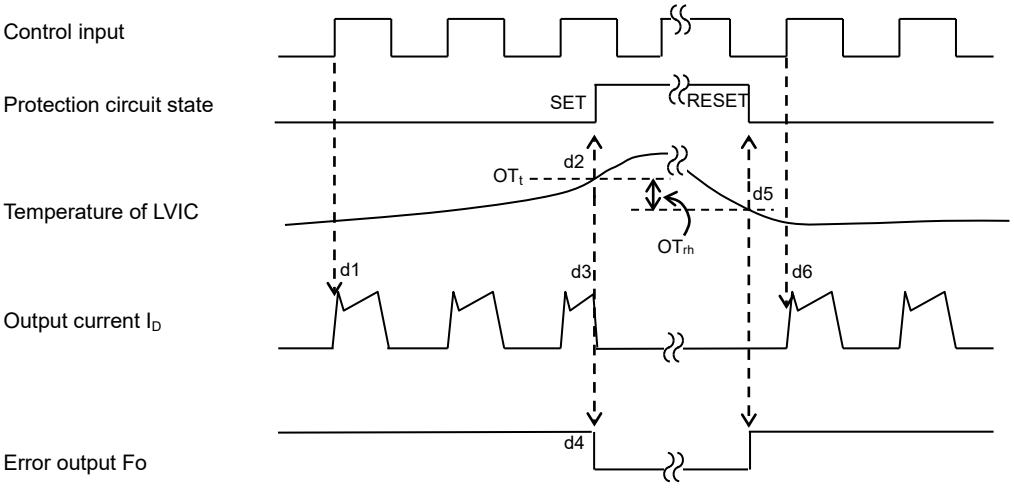
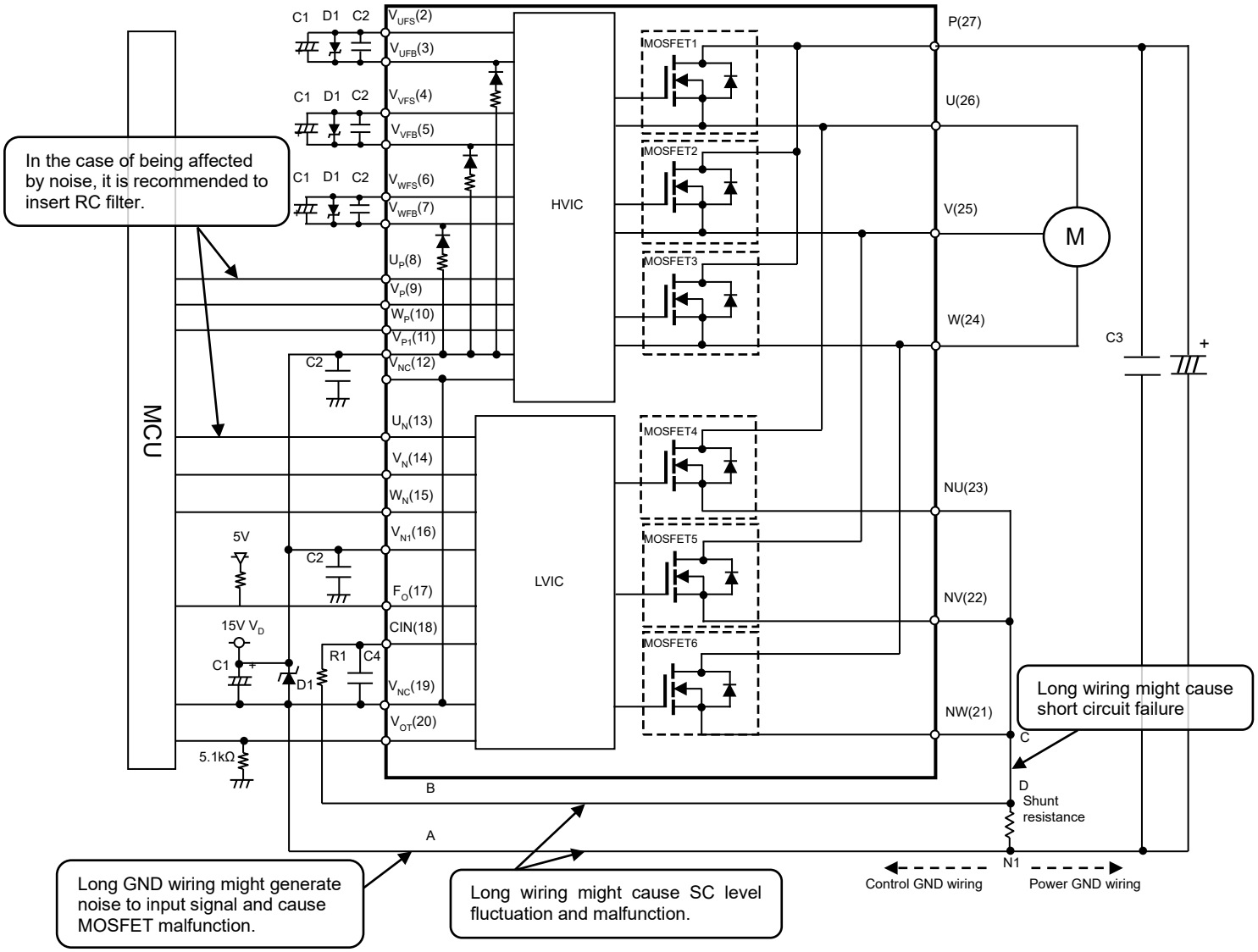
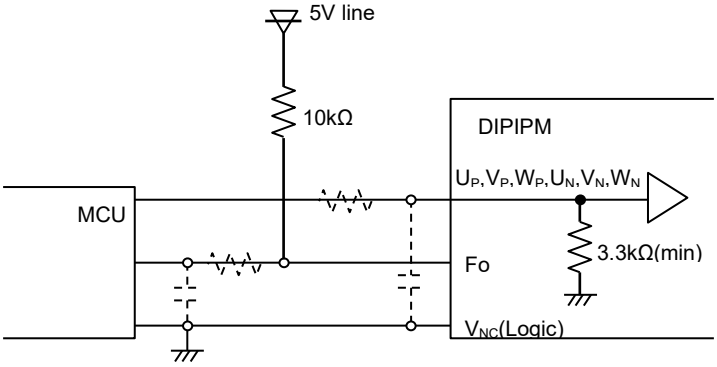


Fig. 6 Example of Application Circuit



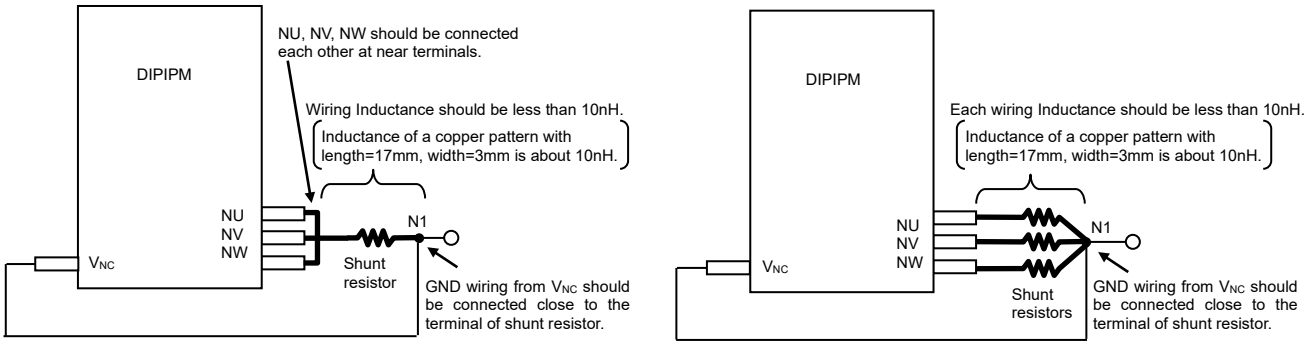
(1) If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point N1 (near the terminal of shunt resistor).
(2) It is recommended to insert a Zener diode D1(24V/1W) between each pair of control supply terminals to prevent surge destruction.
(3) To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a snubber capacitor C3 (more than 0.1μF) between the P-N1 terminals is recommended. C3 capacitor value should be selected by enough system evaluation.
(4) R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2μs. (1.5μs~2μs is general value.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is necessary.
(5) To prevent malfunction, the wiring of A, B, C should be as short as possible.
(6) The point D at which the wiring to CIN filter is divided should be near the terminal of shunt resistor. NU, NV, NW terminals should be connected at near NU, NV, NW terminals.
(7) All capacitors should be mounted as close to the terminals as possible. (C1: good temperature, frequency characteristic electrolytic type and C2:0.01μ-2μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.)
(8) Input drive is High-active type. There is a minimum 3.3kΩ pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.
(9) Thanks to built-in HVIC, direct coupling to MCU without any optocoupler or transformer isolation is possible.
(10) Fo output is open drain type. It should be pulled up to MCU or control power supply (e.g. 5V,15V) by a resistor that makes I_{Fo} up to 1mA. (I_{FO} is estimated roughly by the formula of control power supply voltage divided by pull-up resistance. In the case of pulled up to 5V, 10kΩ (5kΩ or more) is recommended.)
(11) Two V_{NC} terminals are connected inside DIPIPM, please connect either one to the 15V power supply GND outside and leave another one open.
(12) If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet dV/dt ≤+/-1V/μs, Vripple≤2Vp-p.
(13) For DIPIPM, it isn't recommended to drive same load by parallel connection with other phase MOSFET or other DIPIPM.

Fig. 7 MCU I/O Interface Circuit



Note: The RC coupling (parts shown in the dotted line) at each input depends on user's PWM control strategy and the wiring impedance of the printed circuit board. The DIPIPM signal input section integrates a 3.3kΩ(min) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

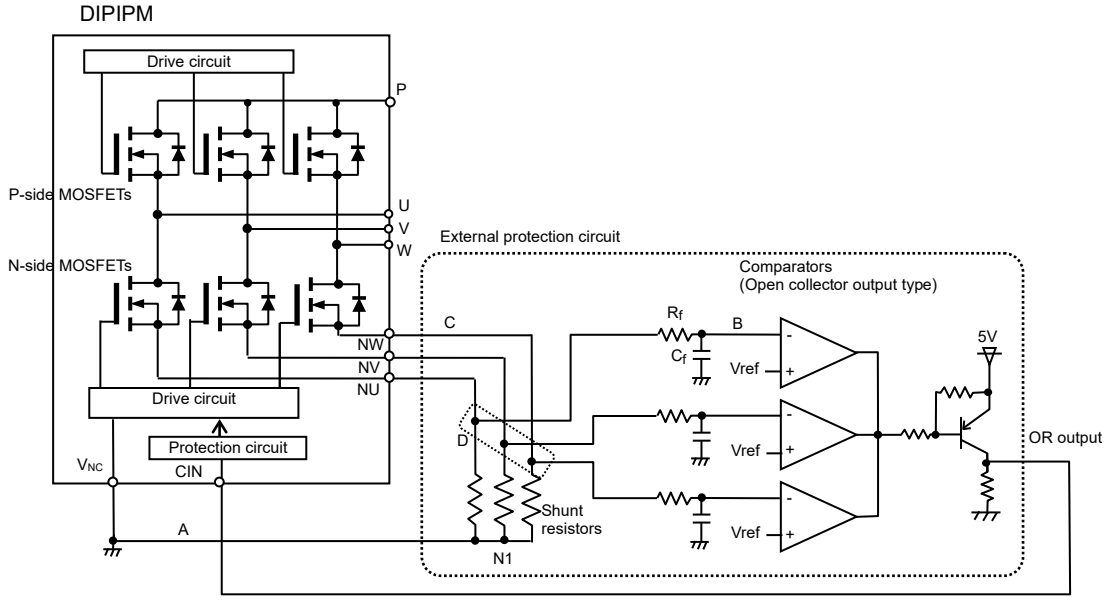
Fig. 8 Pattern Wiring Around the Shunt Resistor



Low inductance shunt resistor like surface mounted (SMD) type is recommended.

Fig. 9 External SC Protection Circuit with Using Three Shunt Resistors

When DIPIPM is operated with three shunt resistors, voltage of each shunt resistor cannot be input to CIN terminal directly. In that case, it is necessary to use the external protection circuit as below.



(1) It is necessary to set the time constant R_fC_f of external comparator input so that MOSFET stop within 2μs when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on.
(2) The threshold voltage Vref should be set up the same rating of short circuit trip level (Vsc(ref) typ. 0.48V).
(3) Select the external shunt resistance so that SC trip-level is less than specified maximum value.
(4) To avoid malfunction, the wiring A, B, C should be as short as possible.
(5) The point D at which the wiring to comparator is divided should be near the terminal of shunt resistor.
(6) OR output high level should be over 0.505V (=maximum Vsc(ref)).
(7) GND of Comparator, Vref circuit and Cf should be not connected to noisy power GND but to control GND wiring.

Fig. 10 (Reference Figure) PCB Through-hole Pattern
Recommended through-hole locations and diameter layout for SLIMDIP [Dimension: mm]

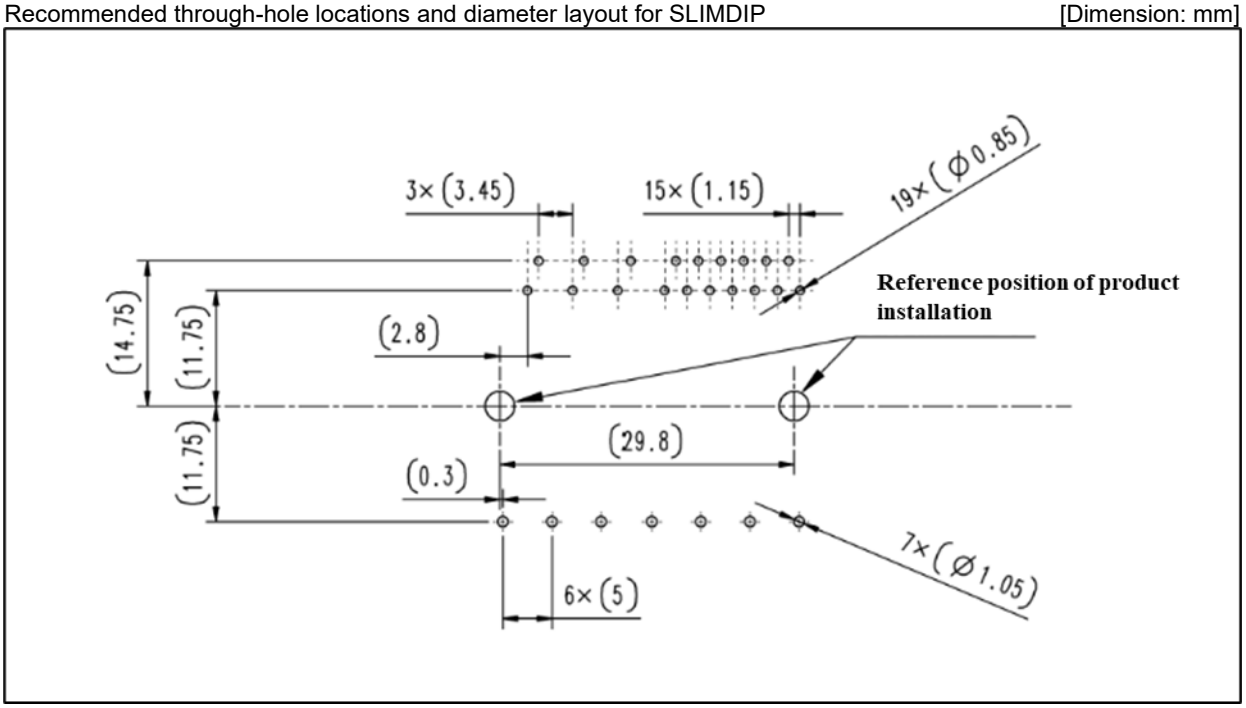
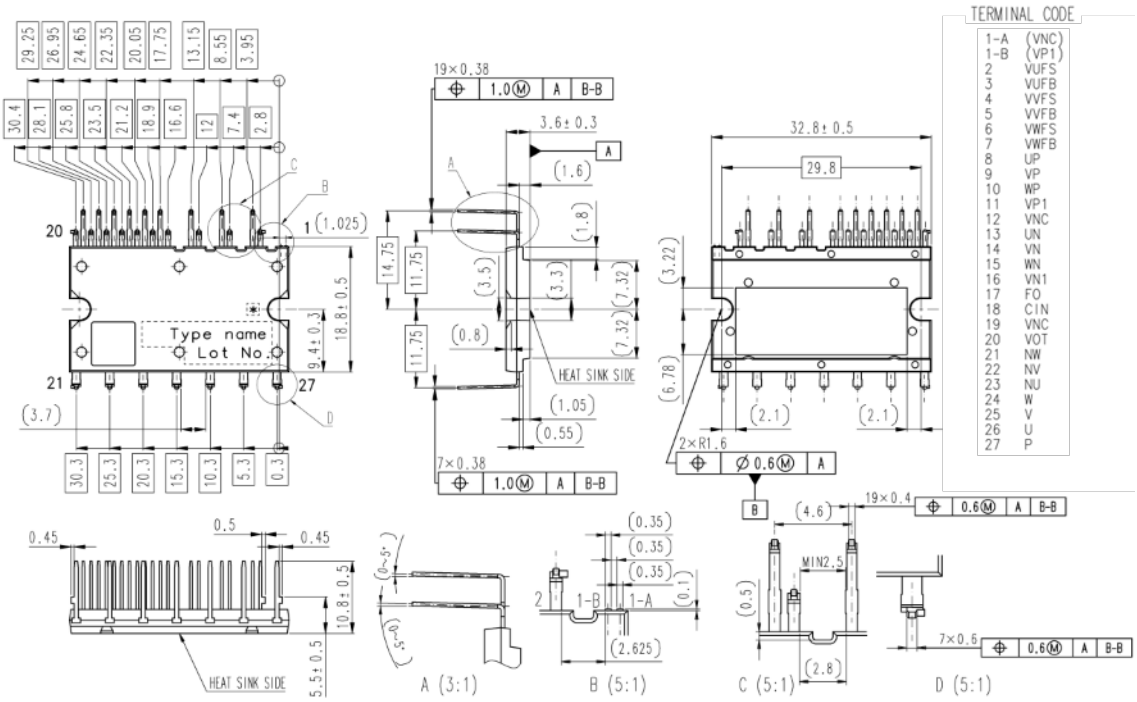
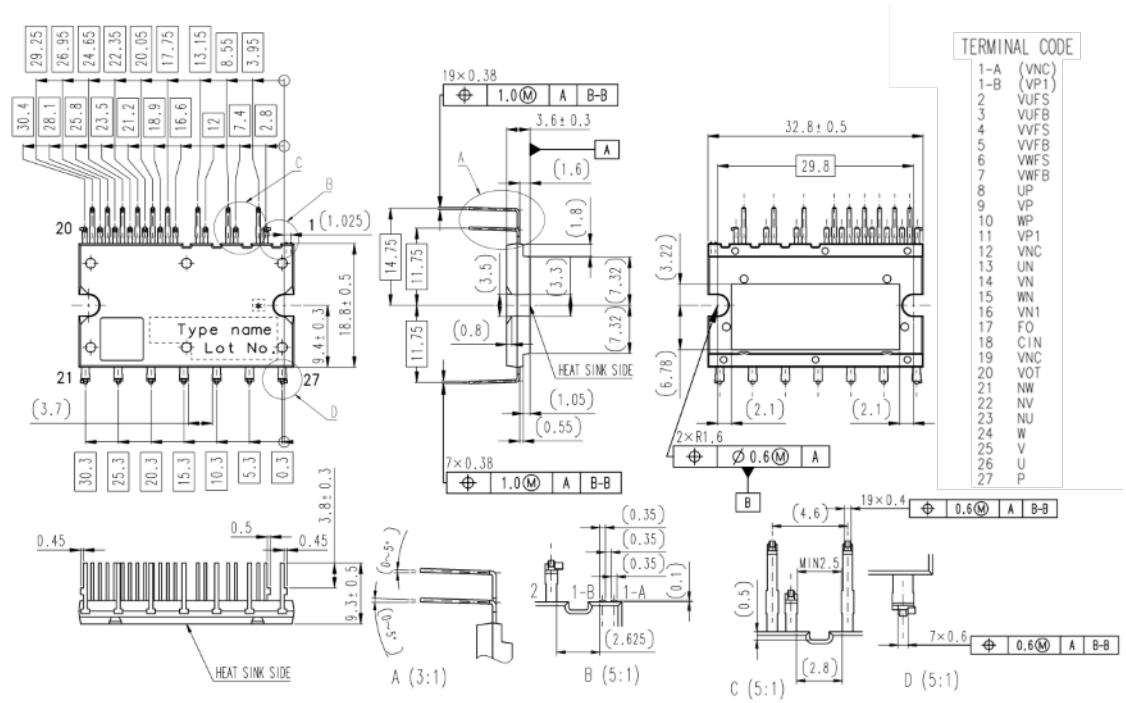


Fig. 11 Package Outlines [Dimensions in mm]

PSF15SG1G6 : Normal Terminal Type



PSF15SG1G6-S : Short Terminal Type



Note: Connect only one V_{NC} terminal (No.12 or 19) to the system GND and leave another one open.

Important Notice

The information contained in this datasheet shall in no event be regarded as a guarantee of conditions or characteristics. This product has to be used within its specified maximum ratings, and is subject to customer's compliance with any applicable legal requirement, norms and standards.

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