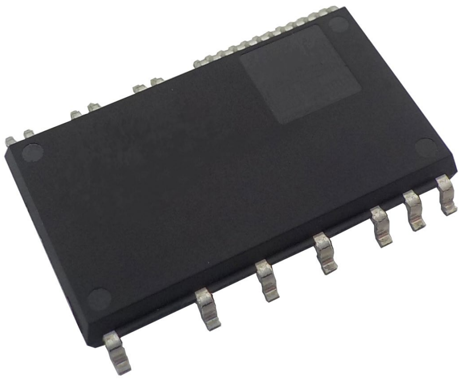
< SOPIPM >

SP2SK

TRANSFER MOLDING TYPE
INSULATED TYPE

OUTLINE



MAIN FUNCTION AND RATINGS

- 3 phase DC/AC inverter
- 600V / 2A (RC-IGBT)
- N-side IGBT open emitter
- Built-in bootstrap diodes with current limiting resistor

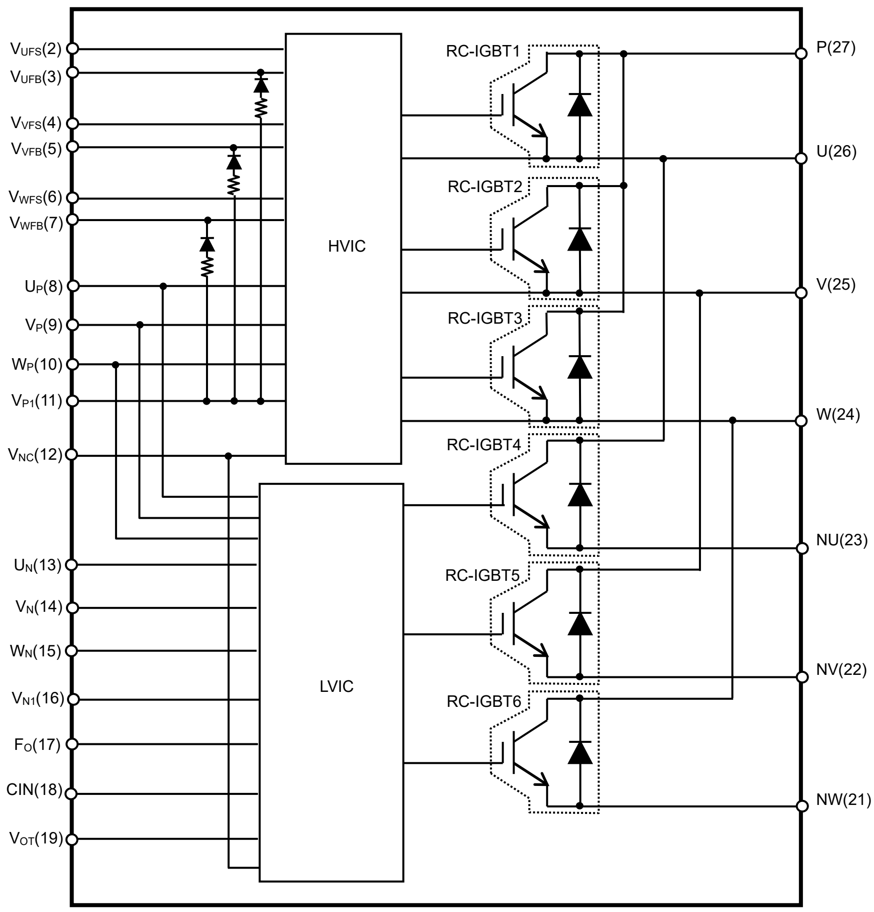
APPLICATION

- AC 100~240Vrms(DC voltage:400V or below) class low power motor control

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For P-side : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection
- For N-side : Drive circuit, Control supply under-voltage protection (UV), Over temperature protection (OT), Short circuit protection (SC) with outer shunt resistor
- Fault signaling : Corresponding to SC fault (N-side IGBT), UV fault (N-side supply) and OT fault
- Temperature output : Outputting LVIC temperature by analog signal
- Arm short circuit prevention : Interlock (IL)
- Input interface : 3, 5V line, Schmitt trigger receiver circuit (High Active)
- UL Recognized : UL1557 File E323585

INTERNAL CIRCUIT



Publication Date : August 2022

MITSUBISHI ELECTRIC CORPORATION

MAXIMUM RATINGS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage	Applied between P-NU,NV,NW	450	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-NU,NV,NW	500	V
V_{CES}	Collector-emitter voltage	-	600	V
$\pm I_C$	Each IGBT collector current	T_C= 25°C (Note 1)	1.5	A
I_{OP}	Output current (peak)	Sine-wave, T_C= 25°C, fo≥1Hz	2	A
$\pm I_{CP}$	Each IGBT collector current (peak)	T_C= 25°C, less than 1ms	3	A
T_j	Operation junction temperature	-	-30~+150	°C

Note 1: Pulse width and period are limited due to junction temperature.

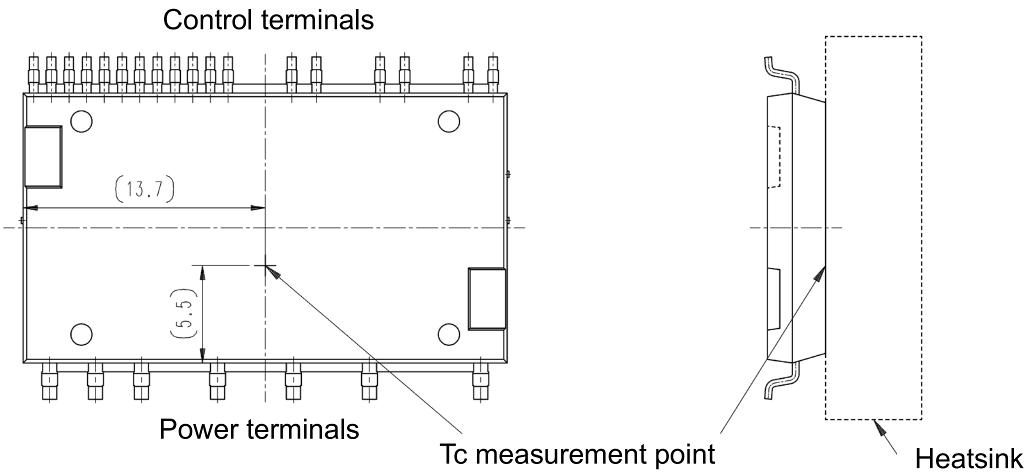
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	20	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS} ,V_{WFB}-V_{WFS}	20	V
V_{IN}	Input voltage	Applied between U_P, V_P, W_P-V_{PC}, U_N, V_N, W_N-V_{NC}	-0.5~V_D+0.5	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	-0.5~V_D+0.5	V
I_{FO}	Fault output current	Sink current at F_O terminal	1	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	-0.5~V_D+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(PROT)}$	Self protection supply voltage limit (Short circuit protection capability)	V_D = 13.5~16.5V, Inverter Part T_j = 125°C, non-repetitive, less than 2μs	400	V
T_C	Module case operation temperature	Measurement point of Tc is provided in Fig.1	-30~+115	°C
T_{stg}	Storage temperature	-	-40~+125	°C
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	1500	V_{rms}

Fig. 1: T_C MEASUREMENT POINT (unit: mm)



THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits Min.	Limits Typ.	Limits Max.	Unit
$R_{th(j-c)Q}$	Junction to case thermal Resistance (Note 2)	Inverter RC-IGBT part (per 1/6 module)	-	-	15	K/W
$R_{th(j-a)Q}$	Junction to ambient thermal resistance (Note 3)	Inverter RC-IGBT part (per 1 module)	-	-	31	K/W

Note 2: With heatsink
Note 3: The measurement condition complies with JEDEC51-2A. The junction to ambient thermal resistance depends on the environment condition of board patterns, board specifications, placement, etc.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition		Limits Min.	Limits Typ.	Limits Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_D=V_{DB} = 15V, V_{IN}= 5V	I_C= 2A, T_j= 25°C	-	2.30	3.10	V
			I_C= 2A, T_j= 125°C	-	2.60	3.55	
V_{EC}	FWD forward voltage	V_{IN}= 0V, -I_C= 2A		-	2.30	3.00	V
t_{on}	Switching times	V_{CC}= 300V, V_D= V_{DB}= 15V I_C= 2A, T_j= 125°C, V_{IN}= 0↔5V Inductive Load (upper-lower arm)		0.40	0.85	1.30	μs
$t_{C(on)}$				-	0.20	0.50	μs
t_{off}				-	0.90	1.60	μs
$t_{C(off)}$				-	0.10	0.35	μs
t_{rr}				-	0.25	-	μs
I_{CES}	Collector-emitter cut-off current	V_{CE}=V_{CES}	T_j= 25°C	-	-	1	mA
			T_j= 125°C	-	-	10	

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits Min.	Limits Typ.	Limits Max.	Unit
I_D	Circuit current	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	V_D=15V, V_{IN}=0V	-	-	4.20	mA
			V_D=15V, V_{IN}=5V	-	-	4.20	
I_{DB}		Each part of V_{UFB}- V_{UFS}, V_{VFB}- V_{VFS}, V_{WFB}- V_{WFS}	V_D=V_{DB}=15V, V_{IN}=0V	-	-	0.10	
			V_D=V_{DB}=15V, V_{IN}=5V	-	-	0.10	
$V_{SC(ref)}$	Short circuit trip level	V_D = 15V (Note 4)		0.455	0.480	0.505	V
UV_{DBt}	P-side Control supply under-voltage protection(UV)	T_j ≤125°C	Trip level	8.0	10.0	12.0	V
UV_{DBr}			Reset level	8.0	10.0	12.0	V
UV_{Dt}	N-side Control supply under-voltage protection(UV)		Trip level	10.3	-	12.5	V
UV_{Dr}			Reset level	10.8	-	13.0	V
V_{OT}	Temperature Output	LVIC Temperature=95°C, Pull down R=5.1kΩ (Note 5)		2.76	2.89	3.03	V
OT_t	Over Temperarure protection (OT)	V_D = 15V Detect LVIC temperature	Trip level	125	135	145	°C
OT_{rh}			Hysteresis of trip-reset	-	10	-	°C
V_{FOH}	Fault output voltage	V_{SC} = 0V, F_O terminal pulled up to 5V by 10kΩ		4.9	-	-	V
V_{FOL}		V_{SC} = 1V, I_{FO} = 1mA		-	-	0.95	V
t_{FO}	Fault output pulse width	(Note 7)		20	-	-	μs
I_{IN}	Input current	V_{IN} = 5V		0.70	1.00	1.50	mA
$V_{th(on)}$	ON threshold voltage	Applied between U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}		-	1.70	2.35	V
$V_{th(off)}$	OFF threshold voltage			0.70	1.20	-	
$V_{th(hys)}$	ON/OFF threshold hysteresis voltage			0.25	0.50	-	
V_F	Bootstrap Di forward voltage	I_F=10mA including voltage drop by limiting resistor (Note 8)		1.1	1.7	2.3	V
R	Built-in limiting resistance	Included in bootstrap Di		80	100	120	Ω

Note 4 : SC protection works only for N-side IGBT. Please select the external shunt resistance such that the SC trip-level is less than 2.5A.
5 : Temperature of LVIC vs. VOT output characteristics is described in Fig. 3. When temperature exceeds the protective level that user defined, controller (MCU) should stop the SOPIPM.
6 : When the LVIC temperature exceeds OT trip temperature level (OTt), OT protection works and Fo outputs. In that case if the cooling system is in an abnormal state (e.g. the air cooling fan failure) or if operating the SOPIPM without heatsink, don't reuse that SOPIPM. There is a possibility that junction temperature of power chips exceeded maximum Tj(150°C).
7 : Fault signal Fo outputs when SC, UV or OT protection works. Fo pulse width is different for each protection modes. At SC failure, Fo pulse width is a fixed width (=minimum 20μs), but at UV or OT failure, Fo outputs continuously until recovering from UV or OT state. (But minimum Fo pulse width is 20μs.)
8 : The characteristics of bootstrap Di is described in Fig.2.

Fig. 2 Characteristics of bootstrap Di V_F-I_F curve (@Ta=25°C) including voltage drop by limiting resistor (Right chart is enlarged chart.)

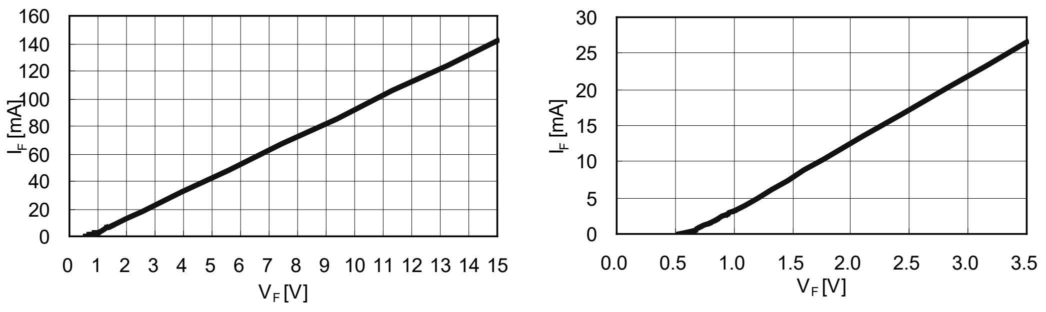


Fig. 3 Temperature of LVIC vs. V_{OT} output characteristics

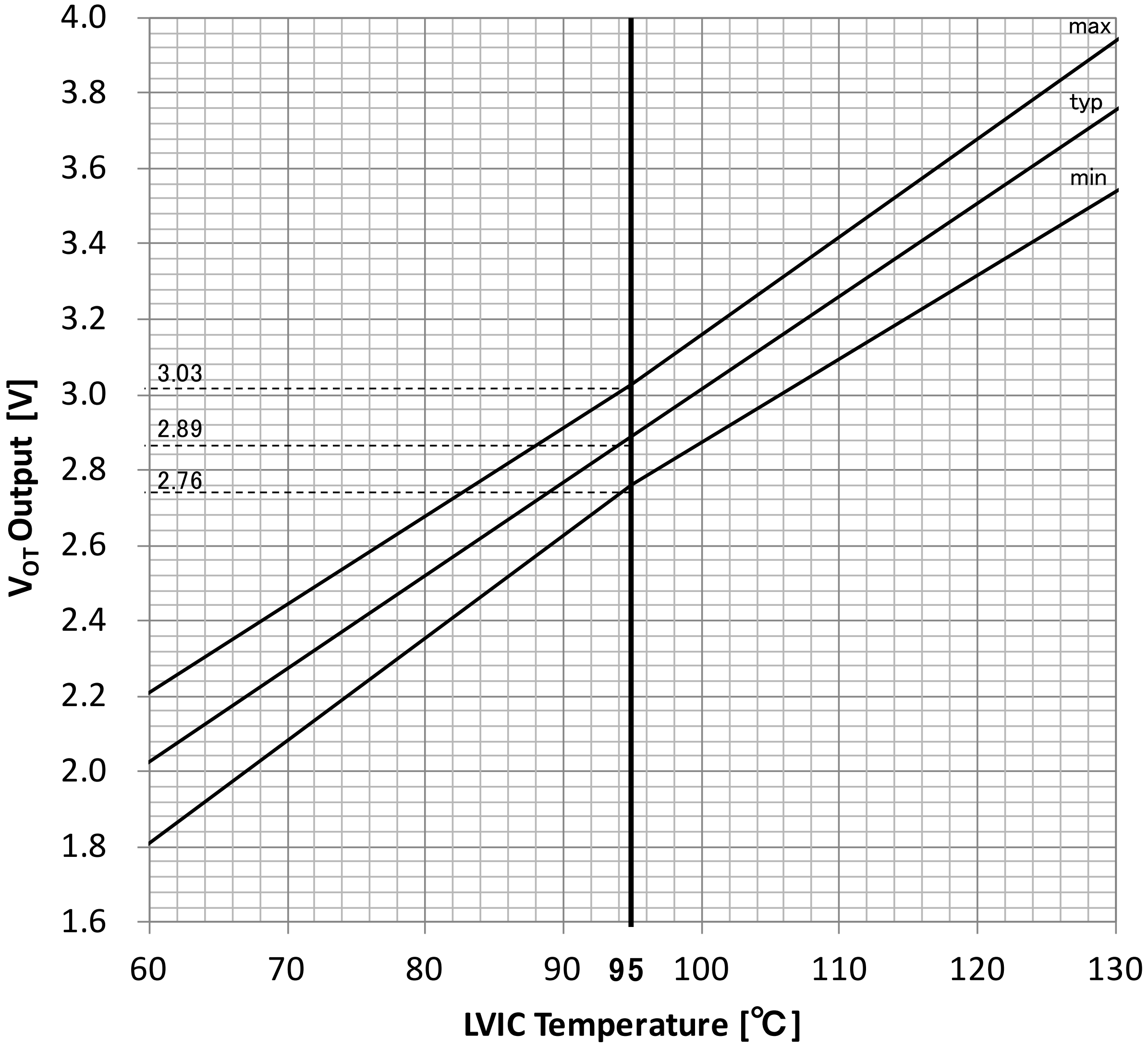
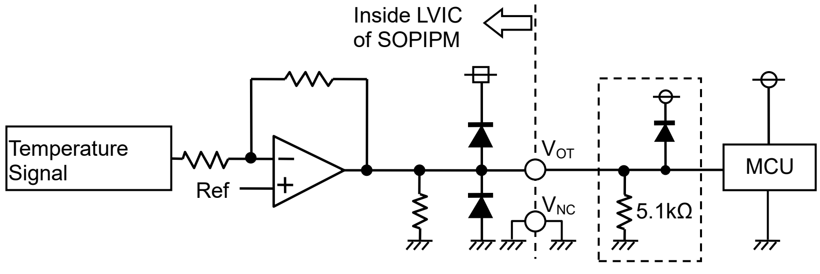


Fig. 4 V_{OT} output circuit



(1) It is recommended to insert 5.1kΩ pull down resistor for getting linear output characteristics at low temperature below room temperature. When the pull down resistor is inserted between V_{OT} and V_{NC}(control GND), the extra circuit current, which is calculated approximately by V_{OT} output voltage divided by pull down resistance, flows as LVIC circuit current continuously. In the case of using V_{OT} for detecting high temperature over room temperature only, it is unnecessary to insert the pull down resistor.
(2) In the case of using V_{OT} with low voltage controller like 3.3V MCU, V_{OT} output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and V_{OT} output for preventing over voltage destruction.
(3) In the case of not using V_{OT}, leave V_{OT} output NC (No Connection).

Refer the application note for this product about the usage of V_{OT}.

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition	Standard	Limits			Unit
			Min.	Typ.	Max.	
Weight	-	-	-	3.7	-	g
Terminal pulling strength	Weight ; 2.2N	JEITA ED-4701 401 method I	30	-	-	s

RECOMMENDED OPERATION CONDITIONS

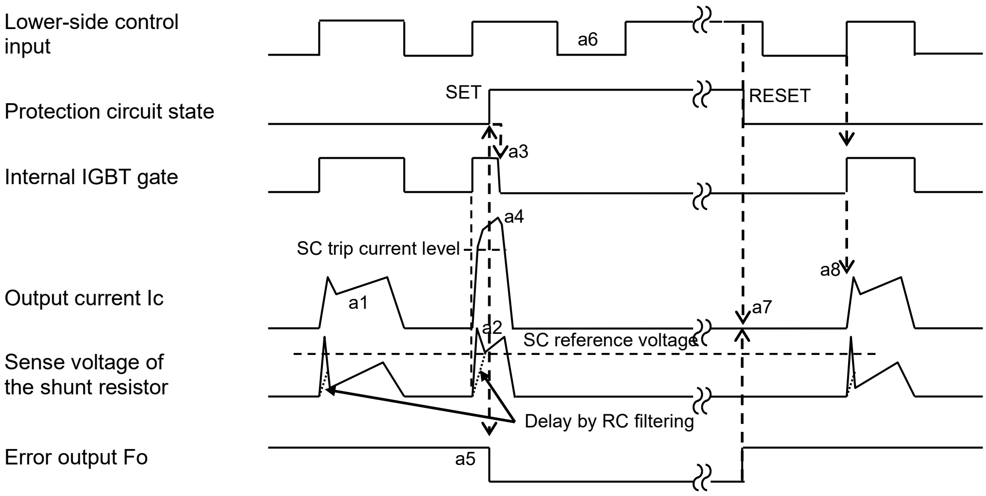
Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage	Applied between P-NU, NV, NW	0	300	400	V
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	13.0	15.0	18.5	V
ΔV_D, ΔV_{DB}	Control supply variation	-	-1	-	+1	V/μs
t_{dead}	Arm shoot-through blocking time	For each input signal	1.0	-	-	μs
f_{PWM}	PWM input frequency	$T_C \le 100°C$, $T_j \le 125°C$	-	-	20	kHz
PWIN(on)	Minimum input pulse width	(Note 9)	0.7	-	-	μs
PWIN(off)			0.7	-	-	
V_{NC}	V_{NC} variation	Between V_{NC}-NU, NV, NW (including surge)	-5	-	+5	V
Tj	Junction temperature	-	-20	-	125	°C

Note 9: SOPIPM might not make response if the input signal pulse width is less than PWIN(on) / PWIN(off).

Fig. 5 Timing Charts of The DIPIPM Protective Functions

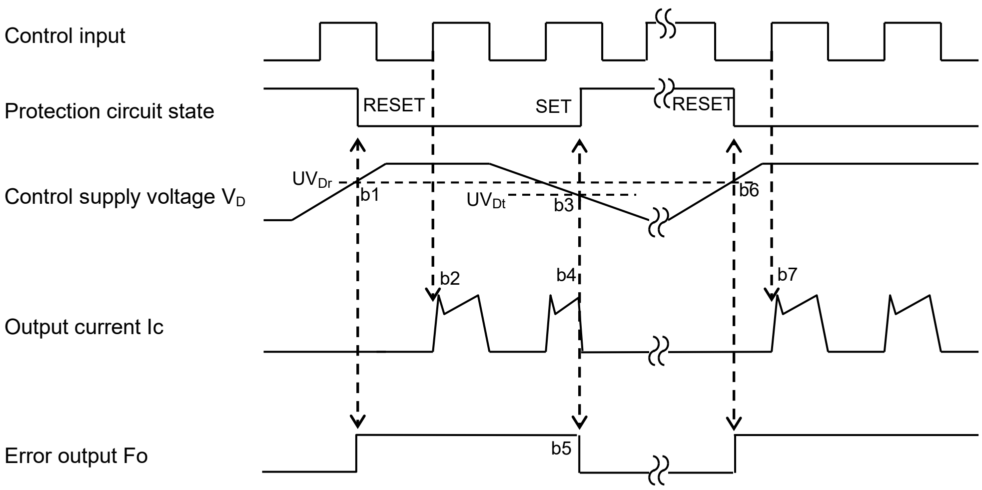
[A] Short-Circuit Protection (N-side only with the external shunt resistor and RC filter)

a1. Normal operation: IGBT ON and outputs current.
a2. Short circuit current detection (SC trigger)
(It is recommended to set RC time constant 1.5~2.0μs so that IGBT shut down within 2.0μs when SC.)
a3. All N-side IGBT's gates are hard interrupted.
a4. All N-side IGBTs turn OFF.
a5. F_O outputs for t_{Fo}=minimum 20μs.
a6. Input = "L": IGBT OFF
a7. Fo finishes output, but IGBTs don't turn on until inputting next ON signal (L→H).
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
a8. Normal operation: IGBT ON and outputs current.



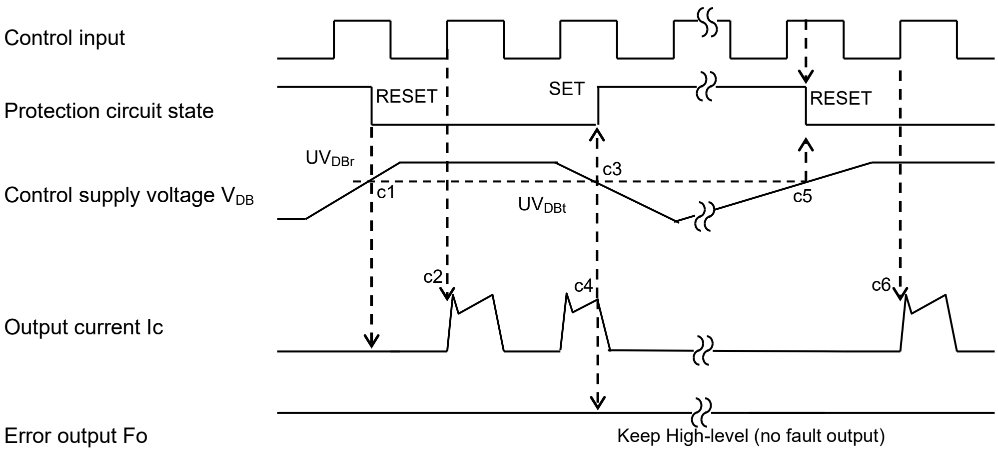
[B] Under-Voltage Protection (N-side, UV_D)

b1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but IGBT turns ON by next ON signal (L→H).
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
b2. Normal operation: IGBT ON and outputs current.
b3. V_D level drops to under voltage trip level. (UV_{Dt}).
b4. All N-side IGBTs turn OFF in spite of control input condition.
b5. Fo outputs for t_{Fo}=minimum 20μs, but output is extended during V_D keeps below UV_{Dr}.
b6. V_D level reaches UV_{Dr}.
b7. Normal operation: IGBT ON and outputs current.



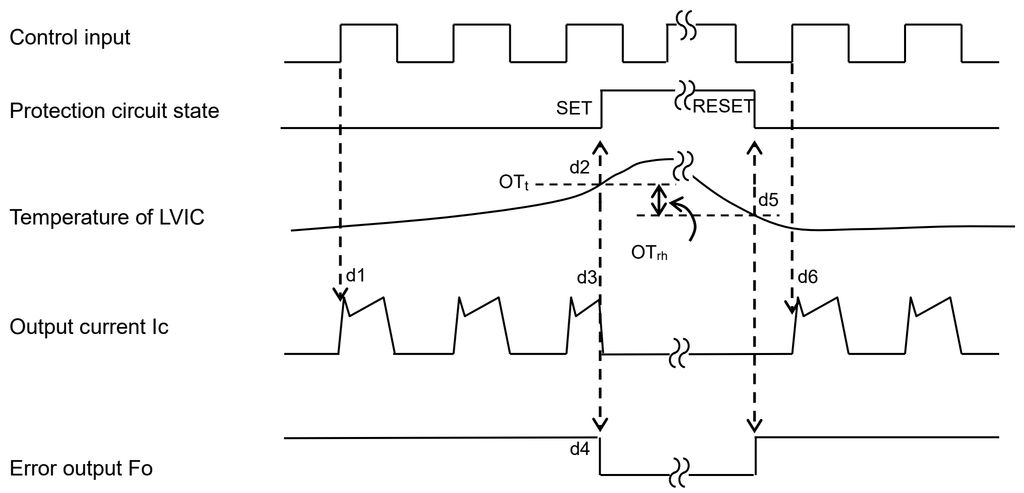
[C] Under-Voltage Protection (P-side, UV_{DB})

c1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr}, IGBT turns on by next ON signal (L→H).
c2. Normal operation: IGBT ON and outputs current.
c3. V_{DB} level drops to under voltage trip level (UV_{DBt}).
c4. IGBT of the corresponding phase only turns OFF in spite of control input signal level, but there is no F_O signal output.
c5. V_{DB} level reaches UV_{DBr}.
c6. Normal operation: IGBT ON and outputs current.



[D] Over Temperature Protection (N-side, Detecting LVIC temperature)

d1. Normal operation: IGBT ON and outputs current.
d2. LVIC temperature exceeds over temperature trip level (OT_t).
d3. All N-side IGBTs turn OFF in spite of control input condition.
d4. Fo outputs for t_{Fo}=minimum 20μs, but output is extended during LVIC temperature keeps over OT_t.
d5. LVIC temperature drops to over temperature reset level.
d6. Normal operation: IGBT turns on by next ON signal (L→H).
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)



[E] Interlock Sequence

e1. When N-side is ON state(H), P-side turn ON(L→H) ······ N-side shut off
e2. When P-side is ON state(H), N-side turn ON(L→H) ······ N-side shut off
e3. P-side turn OFF(H→L) and N-side is ON state(H) ······ N-side turn ON

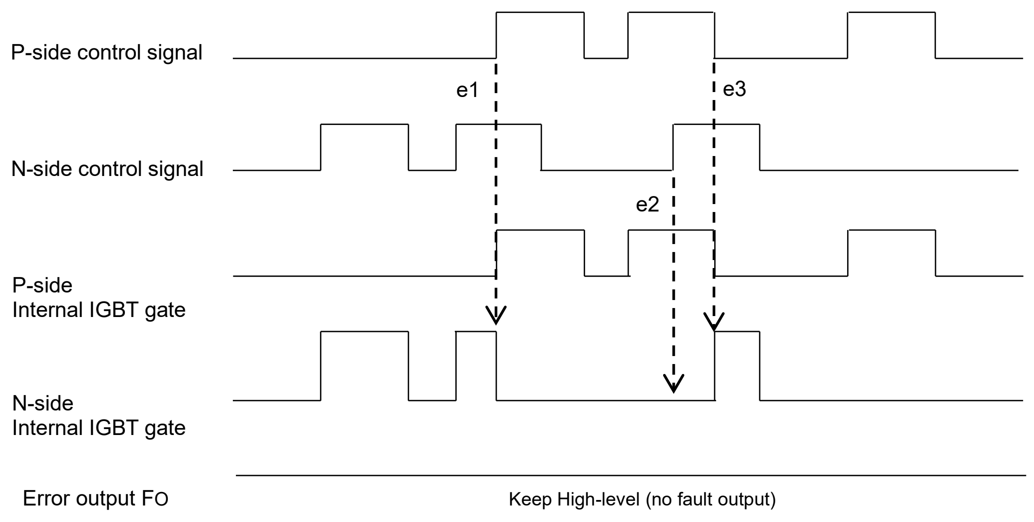
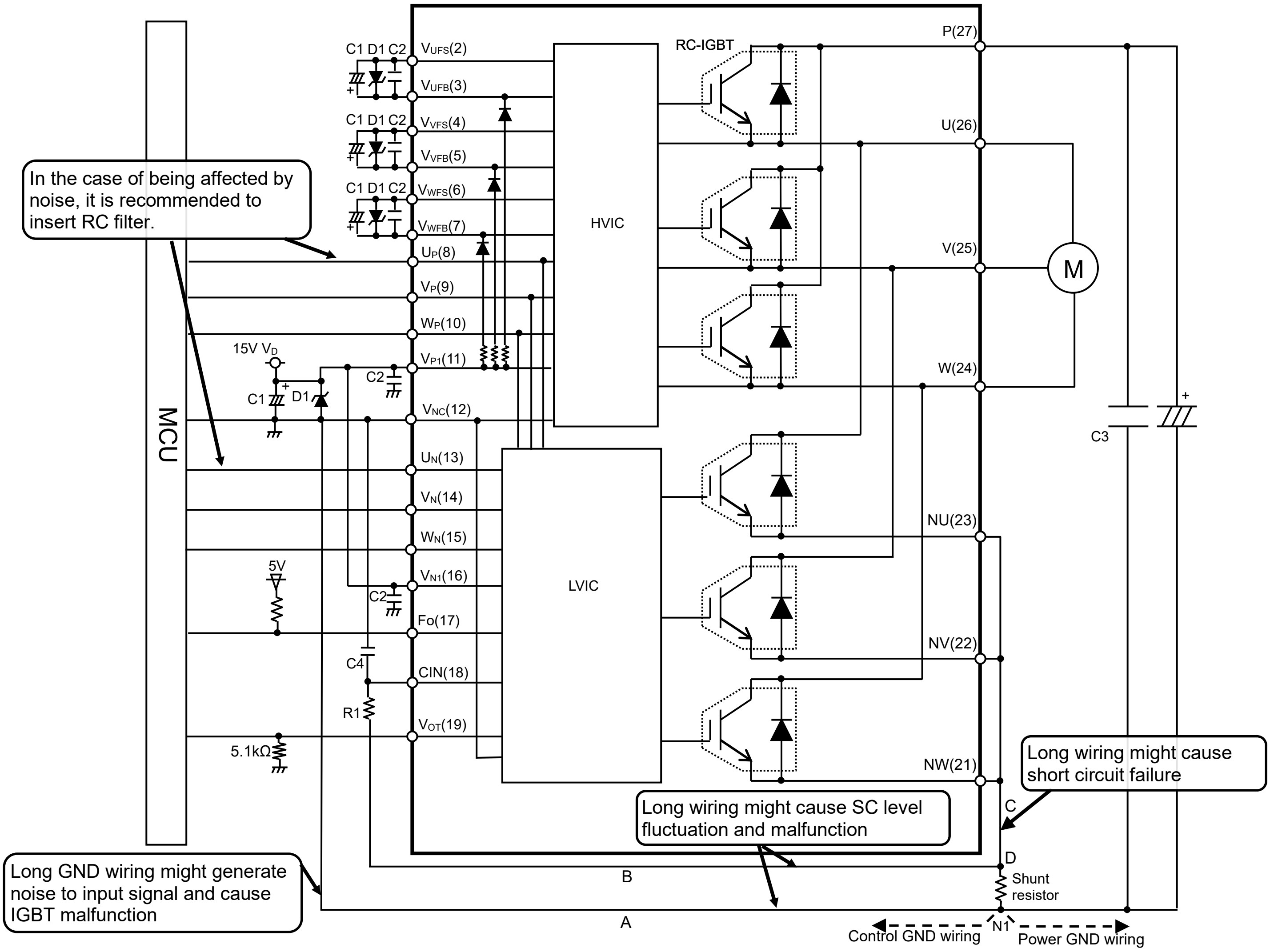
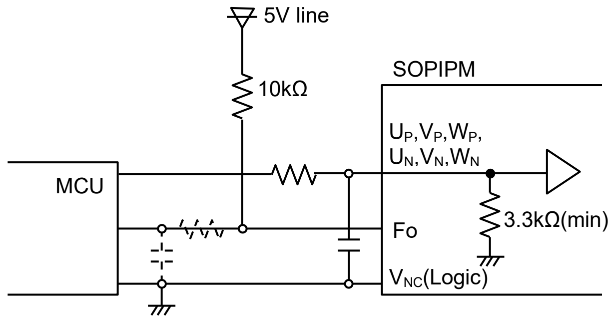


Fig. 6 Example of Application Circuit



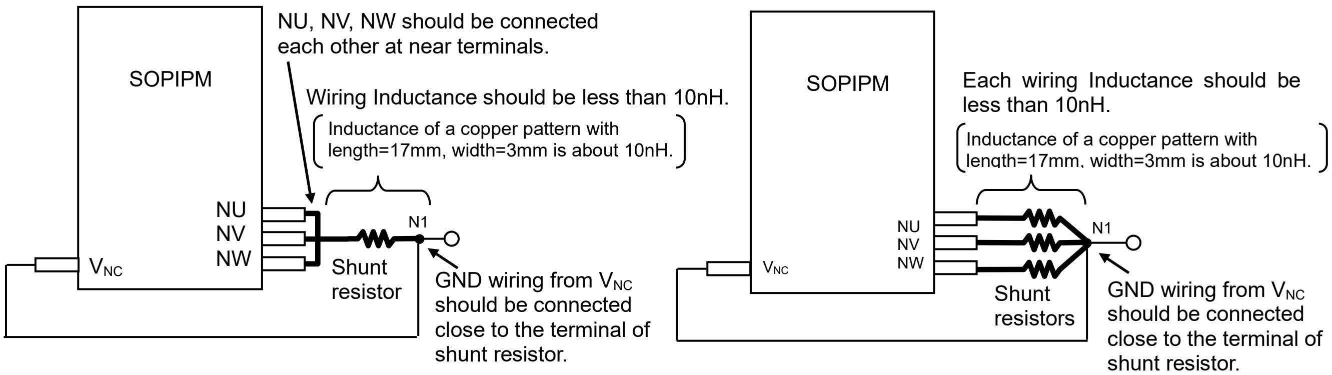
(1) If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point N1 (near the terminal of shunt resistor).
(2) To absove surge voltage for control power supply, it is recommended to insert a Zener diode D1 (24V/1W) between each pair of control supply terminals nearby.
(3) To prevent surge destruction, the wiring between the smoothing capacitor C3 and the P, N1 terminals should be as short as possible. Generally a 0.1-0.22μF snubber capacitor C3 between the P-N1 terminals is recommended.
(4) R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2μs. (1.5μs~2μs is recommended generally.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is necessary.
(5) To prevent malfunction, the wiring of A, B, C should be as short as possible.
(6) The point D at which the wiring to CIN filter is divided should be near the terminal of shunt resistor. NU, NV, NW terminals should be connected at near NU, NV, NW terminals when it is used by one shunt operation. Low inductance SMD type with tight tolerance, temp-compensated type is recommended for shunt resistor.
(7) All capacitors should be mounted as close to the terminals as possible. C1: good temperature, frequency characteristic electrolytic type and C2: 0.22μ-2μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.
(8) Input logic is High-active. There is a 3.3kΩ(min.) pull-down resistor in the input circuit of IC. To prevent malfunction, the input wiring should be as short as possible. When using RC coupling, make the input signal level meet the turn-on and turn-off threshold voltage. SOPIPM is able to connect with MCU directly because hiring HVIC. (It is not electrical isolation.)
(9) Fo output is open drain type. It should be pulled up to power supply of MCU (e.g. 5V,3.3V) by a resistor that makes I_{Fo} up to 1mA. I_{FO} is roughly estimated by the formula of control power supply voltage divided by pull-up resistance. In the case of pulled up to 5V, 10kΩ (5kΩ or more) is recommended.
(10) If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause SOPIPM erroneous operation. To avoid such problem, line ripple voltage should meet dV/dt ≤+/-1V/μs, Vripple≤2Vp-p.
(11) For SOPIPM, it isn't recommended to drive same load by parallel connection with other phase IGBT or other SOPIPM.

Fig. 7 MCU I/O Interface Circuit



Note)
Design for input RC filter depends on PWM control scheme used in the application and wiring impedance of the printed circuit board.
SOPIPM input signal interface integrates a minimum 3.3kΩ pull-down resistor. Therefore, when inserting RC filter, it is necessary to satisfy turn-on threshold voltage requirement.
Fo output is open drain type. It should be pulled up to control power supply (e.g. 5V, 15V) with a resistor that makes Fo sink current I_{Fo} 1mA or less. In the case of pulled up to 5V supply, 10kΩ (5kΩ or more) is recommended.

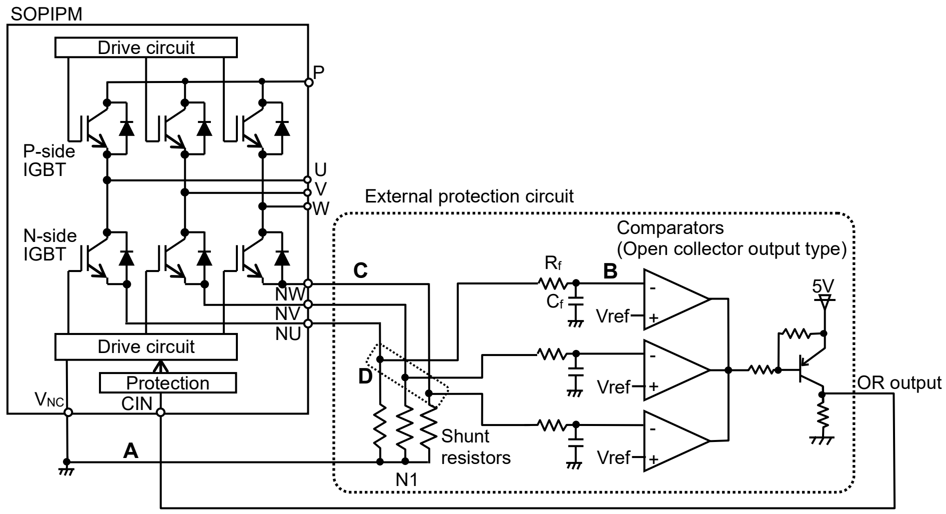
Fig. 8 Pattern Wiring Around the Shunt Resistor



Low inductance shunt resistor like surface mounted (SMD) type is recommended.

Fig. 9 Pattern Wiring Around the Shunt Resistor (for the case of open emitter)

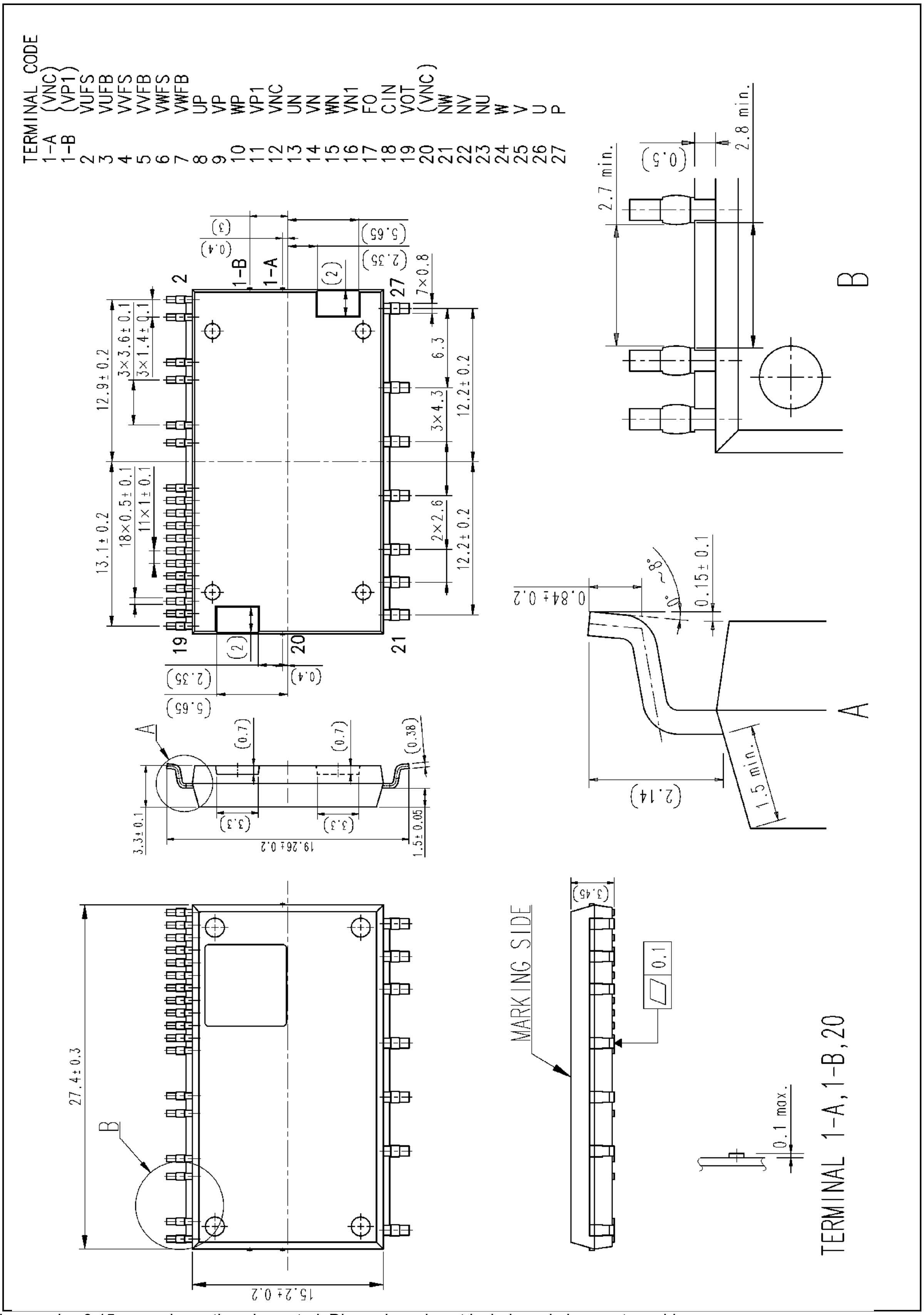
When SOPIPM is operated with three shunt resistors, voltage of each shunt resistor cannot be input to CIN terminal directly. In that case, it is necessary to use the external protection circuit as below.



(1) It is necessary to set the time constant R_fC_f of external comparator input so that IGBT stops within 2μs when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on.
(2) It is recommended for the threshold voltage Vsc(ref) to set to the same rating of short circuit trip level (Vsc(ref): typ. 0.48V).
(3) Select the external shunt resistance so that SC trip-level is less than specified value (=2.5A).
(4) To avoid malfunction, the wiring A, B, C should be as short as possible.
(5) The point D at which the wiring to comparator is divided should be close to the terminal of shunt resistor.
(6) OR output high level when protection works should be over 0.505V (=maximum Vsc(ref) rating).
(7) GND of Comparator, GND of Vref circuit and Cf should be not connected to power GND but to control GND wiring.

Fig. 10 Package Outlines

Dimensions in mm



* The tolerance is ±0.15mm, unless otherwise noted. Dimensions do not include resin burr, gate residue.
* No.1-A, 1-B and No.20 terminals are used internally and has some potential (15V or GND), so it is necessary to leave no connection.

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