

<IGBT Modules>

CM400DY-40T

HIGH POWER SWITCHING USE INSULATED TYPE



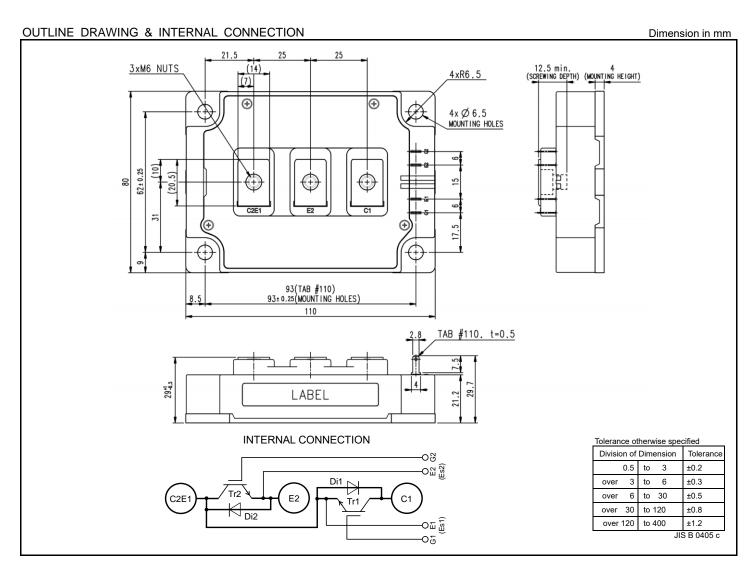
- •Dual switch (Half bridge)
- •Copper base plate (Nickel-plating)
- Tin-plating tab terminals
- •RoHS Directive compliant
- •UL Recognized under UL1557, File No.E323585

APPLICATON

Photo-voltaic , ESS , etc.

OPTION

V_{CEsat} selection for parallel connection



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MAXIMUM RATINGS (Tvj=25 °C, unless otherwise specified)

Symbol	Item	Conditions	Rating	Unit	
V _{CES}	Collector-emitter voltage	G-E short-circuited	2000	V	
V _{GES}	Gate-emitter voltage	C-E short-circuited	± 20	V	
Ic	Callantan aumant	DC, T _C =94°C (Note2, 4)	400		
I _{CRM}	Collector current	Pulse, Repetitive (Note3)	800	1 A	
P _{tot}	Total power dissipation	T _C =25 °C (Note2, 4)	2235	W	
I _E (Note1)	Fitte	DC (Note2)	400		
I _{ERM} (Note1)	Emitter current	Pulse, Repetitive (Note3)	800	A	
V _{isol}	Isolation voltage	Terminals to base plate, RMS, f=60 Hz, AC 1 min	4000	V	
T _{vjmax}	Maximum junction temperature	Instantaneous event (overload) (Note8)	175	°C	
T _{Cmax}	Maximum case temperature	(Note4, 8)	125	°C	
T _{vjop}	Operating junction temperature	Continuous operation (Note8)	-40 ~ +150	°C	
T _{stg}	Storage temperature	-	-40 ~ +125	°C	

Cumbal	Itom	Conditions		Limits			1.1
Symbol	Item			Min.	Тур.	Max.	Unit
I _{CES}	Collector-emitter cut-off current	V _{CE} =V _{CES} , G-E short-circuited		-	-	1	mA
I _{GES}	Gate-emitter leakage current	V _{GE} =V _{GES} , C-E short-circuited		-	-	0.5	μA
$V_{GE(th)}$	Gate-emitter threshold voltage	I _C =40 mA, V _{CE} =10 V		5.5	6.0	6.6	V
· · ·		I _C =400 A, V _{GE} =15 V,	T _{vj} =25 °C	-	2.20	2.55	
V _{CEsat}		Refer to the figure of test circuit	T _{vj} =125 °C	-	2.60	-	V
(Terminal)	Oallantan and the marking at large	(Note5)	T _{vj} =150 °C	-	2.70	-	
.,	Collector-emitter saturation voltage	I _C =400 A, V _{GE} =15 V,	T _{vj} =25 °C	-	2.10	2.35	
V _{CEsat}		(Note5)	T _{vj} =125 °C	-	2.50	-	V
(Chip)			T _{vj} =150 °C	-	2.60	-	
Cies	Input capacitance	1		-	-	110	
Coes	Output capacitance	V _{CE} =10 V, G-E short-circuited		-	-	1.9	nF
Cres	Reverse transfer capacitance			-	-	0.8	
Q _G	Gate charge	V _{CC} =1300 V, I _C =400 A, V _{GE} =15 V		-	3.2	-	μC
t _{d(on)}	Turn-on delay time	V _{CC} =1300 V, I _C =400 A, V _{GE} =±15 V,		-	-	800	ns
t _r	Rise time			-	-	200	
t _{d(off)}	Turn-off delay time			-	-	800	
t _f	Fall time	$R_G=0 \Omega$, Inductive load		-	-	900	1
V _{EC} (Note1)		I _E =400 A, G-E short-circuited,	T _{vj} =25 °C	-	3.45	4.30) V
		Refer to the figure of test circuit	T _{vj} =125 °C	-	3.80	-	
(Terminal)		(Note5)	T _{vj} =150 °C	-	3.70	-	
(Note1)	- Emitter-collector voltage	I _E =400 A, G-E short-circuited,	T _{vj} =25 °C	-	3.35	4.10	
V _{EC} (Note1)		(Note5)	T _{vj} =125 °C	-	3.70	-	V
(Chip)			T _{vj} =150 °C	-	3.60	-	
t _{rr} (Note1)	Reverse recovery time	V _{CC} =1300 V, I _E =400 A, V _{GE} =±15 V,		-	-	300	ns
Q _{rr} (Note1)	Reverse recovery charge	$R_G=0 \Omega$, Inductive load		-	45	-	μC
Eon	Turn-on switching energy per pulse	V _{CC} =1300 V, I _C =I _E =400 A,		-	100	-	
E _{off}	Turn-off switching energy per pulse	V _{GE} =±15 V, R _G =0 Ω, T _{vi} =150 °C,		-	175	-	mJ
Err (Note1)	Reverse recovery energy per pulse	Inductive load		-	78	-	
R _{CC'+EE'}	Internal lead resistance	Main terminals-chip, per switch, T _C =25 °C (Note4)		-	0.65	-	mΩ
r _g	Internal gate resistance	Per switch			1.9	1	Ω

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THERMAL RESISTANCE CHARACTERISTICS

Symbol	Itama	Conditions		Limits			Unit
	Item			Min.	Тур.	Max.	Offic
$R_{th(j-c)Q}$	Thermal resistance	Junction to case, per Inverter IGBT (Note4)		-	-	67	K/kW
$R_{th(j-c)D}$	Thermal resistance	Junction to case, per Inverter FWD (Note4)		1	-	125	N/KVV
R _{th(c-s)}	Contact thermal resistance	Case to heat sink, per 1 module.	Thermal grease applied (Note4, 6, 8)	-	9	-	K/kW

MECHANICAL CHARACTERISTICS

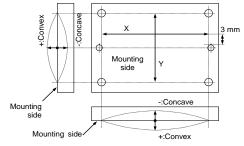
Symbol	Item	Conditions		Limits			l lmi4	
	item	Cond	IUOIIS	Min.	Тур.	Max.	N·m N·m	
Mt	Mounting torque	Main terminals	M 6 screw	3.5	4.0	4.5	N·m	
Ms		Mounting to heat sink	M 6 screw	3.5	4.0	4.5	N·m	
ds	Creepage distance	Terminal to terminal		16	-	-	mana	
		Terminal to base plate		16	-	-	mm	
da	Classes	Terminal to terminal		8	-	-	mana	
	Clearance	Terminal to base plate		8	-	-	mm	
ec	Flatness of base plate	On the centerline X, Y (Note7)	-50	-	+100	μm	
m	mass	_		-	530	-	g	

^{*} This product is compliant with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) directive 2011/65/EU and (EU)2015/863.

*Restriction of the use of certain Hazardous Substances in electrical and electronic equipment.

Note 1. Represent ratings and characteristics of the anti-parallel, emitter-collector free-wheeling diode (FWD).

- 2. Junction temperature (T_{vj}) should not increase beyond T_{vjmax} rating.
- 3. Pulse width and repetition rate should be such that the device junction temperature (Tvj) dose not exceed Tvjmax rating.
- 4. Case temperature (T_C) and heat sink temperature (T_S) are defined on the each surface (mounting side) of base plate and heat sink just under the chips. Refer to the figure of chip location.
- 5. Pulse width and repetition rate should be such as to cause negligible temperature rise. Refer to the figure of test circuit.
- 6. Reference value. Thermally conductive grease of thermal conductivity λ =0.9 W/(m·K) and thickness D_(C-S)=50 μ m.
- 7. The base plate (mounting side) flatness measurement points (X, Y) are shown in the following figure.



^{8.} Long term performance related to thermal conductive grease (including but not limited to aspects such as the increase of thermal resistance due to pumping out, etc.) should be verified under your specific application conditions. Each temperature condition (T_{vj max}, T_{vj op}, T_{C max}) must be maintained below the maximum rated temperature throughout consideration of the temperature rise even for long term usage.

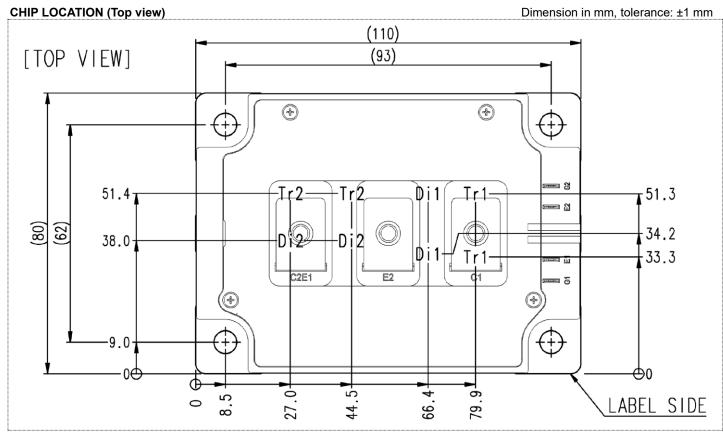
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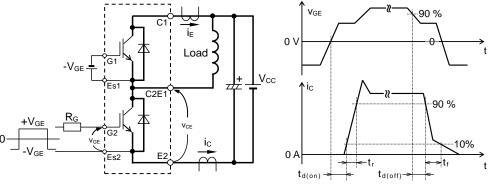
RECOMMENDED OPERATING CONDITIONS

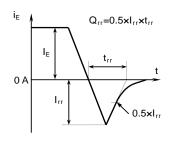
Symbol	Itam	Conditions	Limits			Unit
	Item	Conditions	Min.	Тур.	Max.	Unit
V _{cc}	(DC) Supply voltage	Applied across C1-E2 terminals	-	1300	1500	V
V_{GEon}	Gate-emitter drive voltage	Applied across G1-Es1/G2-Es2 terminals	13.5	15.0	16.5	V
R _G	External gate resistance	Per switch	0	-	10	Ω



Tr1/Tr2: IGBT, Di1/Di2: FWD

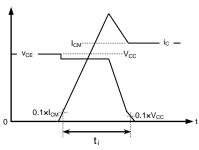
TEST CIRCUIT AND WAVEFORMS

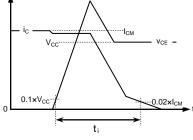


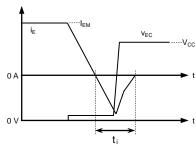


Switching characteristics test circuit and waveforms

t_{rr}, Q_{rr} characteristics test waveform





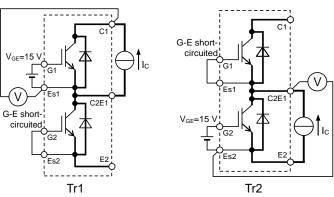


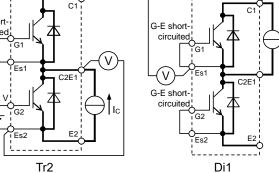
IGBT Turn-on switching energy

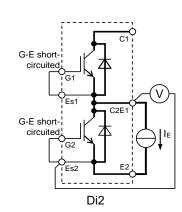
IGBT Turn-off switching energy

FWD Reverse recovery energy

Switching energy and Reverse recovery energy test waveforms (Integral time instruction drawing)







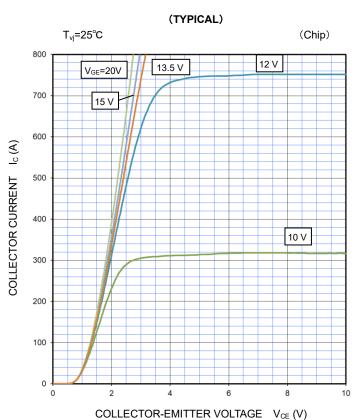
V_{CEsat} characteristics test circuit

V_{EC} characteristics test circuit

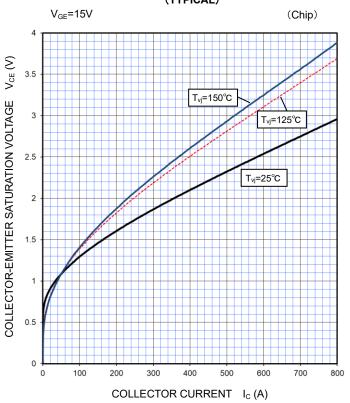
INSULATED TYPE



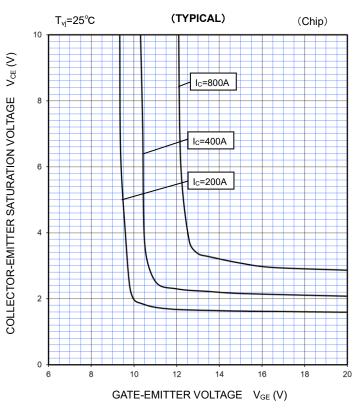
OUTPUT CHARACTERISTICS



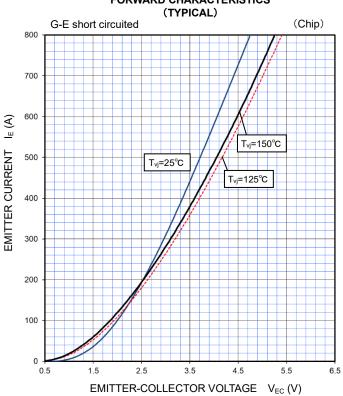
COLLECTOR-EMITTER SATURATION VOLTAGE CHARACTERISTICS (TYPICAL)



COLLECTOR-EMITTER VOLTAGE CHARACTERISTICS

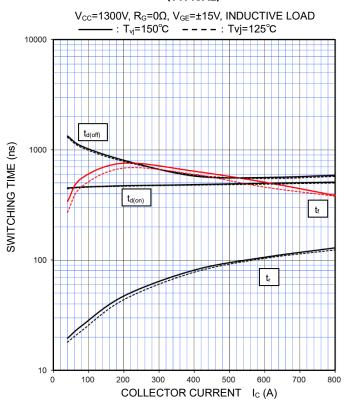


FREE WHEELING DIODE FORWARD CHARACTERISTICS

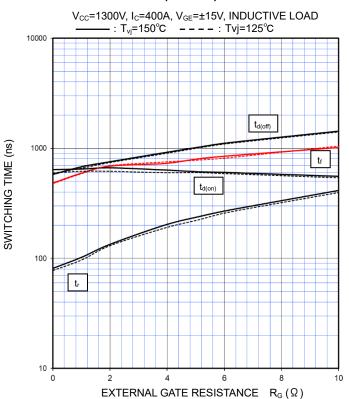


PERFORMANCE CURVES

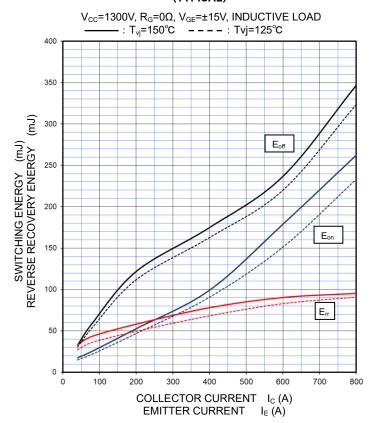
HALF-BRIDGE SWITCHING CHARACTERISTICS (TYPICAL)



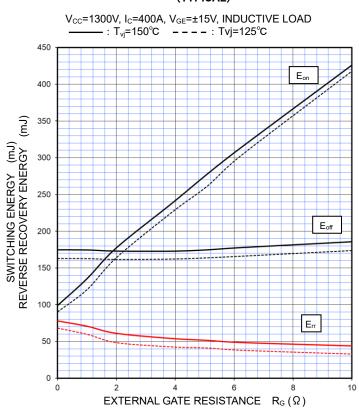
HALF-BRIDGE SWITCHING CHARACTERISTICS (TYPICAL)



HALF-BRIDGE SWITCHING CHARACTERISTICS (TYPICAL)



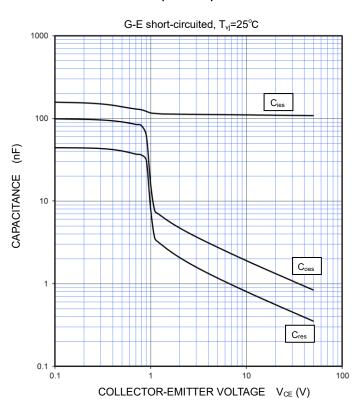
HALF-BRIDGE SWITCHING CHARACTERISTICS (TYPICAL)



PERFORMANCE CURVES

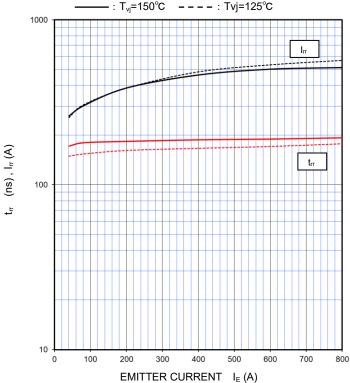
CAPACITANCE CHARACTERISTICS

(TYPICAL)

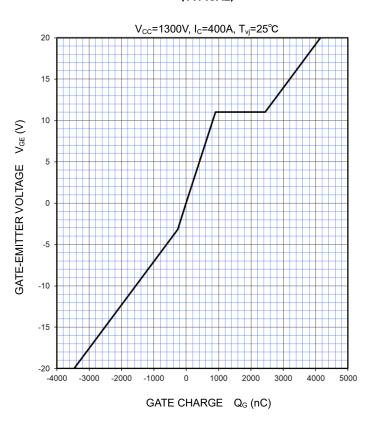


FREE WHEELING DIODE REVERSE RECOVERY CHARACTERISTICS (TYPICAL)

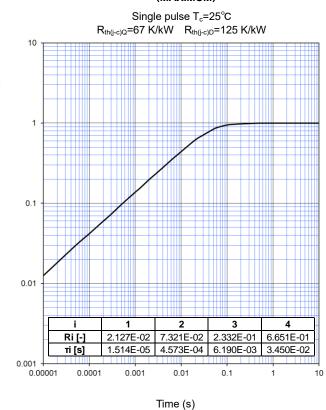
V_{CC}=1300V, R_G=0Ω, V_{GE}=±15V, INDUCTIVE LOAD



GATE CHARGE CHARACTERISTICS (TYPICAL)



TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS (MAXIMUM)



NORMALIZED TRANSIENT THERMAL RESISTANCE Z_{th(j-c)}

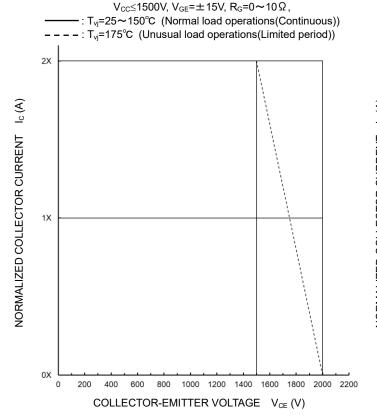
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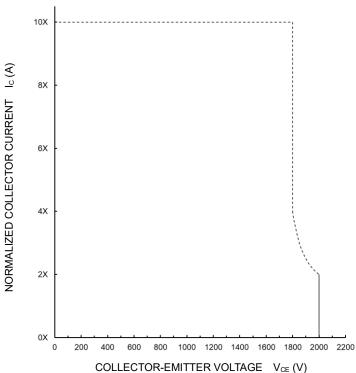
PERFORMANCE CURVES

TURN-OFF SWITCHING SAFE OPERATING AREA (REVERSE BIAS SAFE OPERATING AREA) (MAXIMUM)



SHORT-CIRCUIT SAFE OPERATING AREA (MAXIMUM)

 $V_{CC} \le 1500V$, $V_{GE} = \pm 15V$, $R_G = 0 \sim 10 \Omega$, $T_{vj} = 25 \sim 150^{\circ}C$, $tw \le 6\mu s$, Non-Repetitive



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