MITSUBISHI ELECTRIC

SiC Lecture Series

5. Crystal defects in SiC

Crystal defects in SiC

There are various possible defects found in SiC crystals that can affect the characteristics of devices fabricated therein. The main defects in SiC include large-scale defects such as micropipes, grain boundaries, polytype inclusions※1, and carbon inclusions, as well as Stacking Faults (SF), Threading Edge Dislocations (TED), Threading Screw Dislocations (TSD), Basal Plane Dislocations (BPD), and mixed dislocations which are complexes of these defects. The density of these defects in relatively high-quality, recent SiC crystals is approximately 1 to 10 micropipes per cm^2 and 10^3 to 10^4 dislocations per cm^2. It is still recognized that the defect density of SiC is significantly higher than that of Si.

Micropipes are considered to be very large TSDs with a cavity at their center. Carbon inclusions are formed when carbon dust particles become embedded during the bulk crystal growth process, and they serve as sources of high-density dislocations. These defects are critical and can be fatal for devices.

Figure 1 shows a microscopic image of the surface of an 8° off-axis (0001) 4H-SiC substrate etched with molten potassium hydroxide (molten KOH), forming pits at the crystal defect sites. Dislocation lines that extend perpendicularly to the surface reflect the symmetry of the crystal, and hexagonal pits appear due to etching. On the other hand, basal plane dislocations have dislocation lines that extend in various directions within the (0001) plane (parallel to the surface), resulting in elliptical pits. There are multiple types of threading screw dislocations with different magnitudes of crystal displacement. Large threading screw dislocations and mixed dislocations with significant crystal displacement can cause leakage currents in devices. Most small dislocations, however, do not significantly affect the characteristics of the devices.

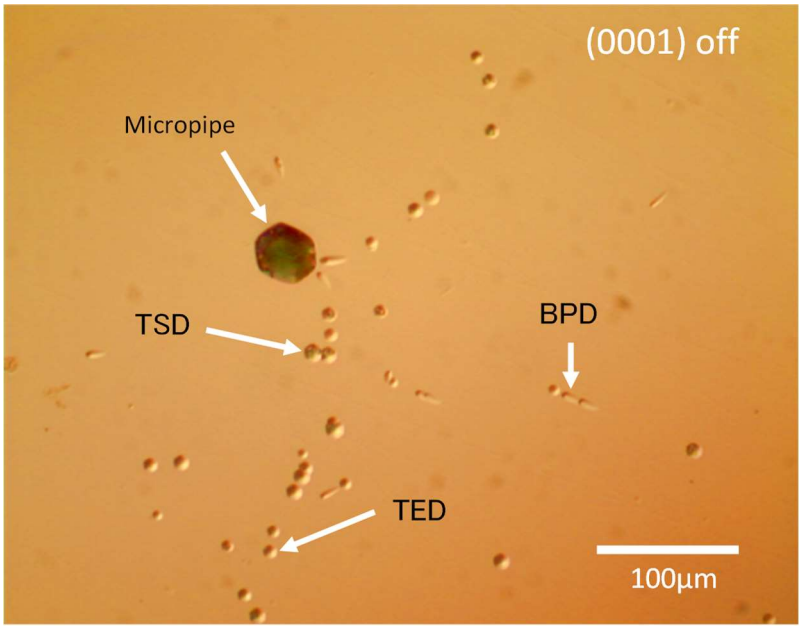

Figure 1 Etch pit※2 image of the SiC substrate surface etched with molten potassium hydroxide (molten KOH)

When examining the structure of basal plane dislocations in detail, they have a linear structure surrounded by two partial dislocations (Shockley partial dislocations※3). Regarding basal plane dislocations, when bipolar current flows through SiC devices, the region enclosed by the two partial dislocations can expand as a stacking fault, leading to an increase in resistance and causing degradation of the device characteristics.

Figure 2 explains the expansion of stacking faults when bipolar current flows.

(1) Basal plane dislocations present in the SiC substrate are carried over into the drift layer.

(2) When bipolar current flows, electrons and holes in the drift layer are captured by the basal plane dislocations.

(3) The captured electrons and holes recombine, releasing energy. This released energy causes the partial dislocations to move, and stacking faults are formed in the areas where the partial dislocations have moved. Since the stacking fault regions continue to capture more electrons and holes, the movement of partial dislocations (expansion of the stacking fault regions) continues. The regions where stacking faults are formed act as high-resistance regions.

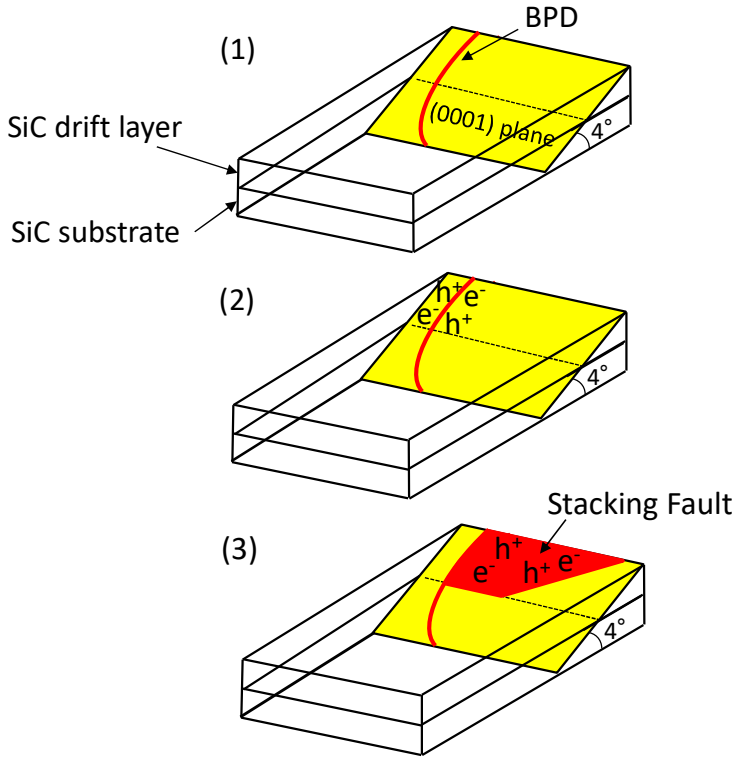

Figure 2 Formation of stacking faults from basal plane dislocations

In high-concentration n-type regions, the recombination lifetime of electrons and holes is short, resulting in low hole density in the buffer layer and substrate. Therefore, the expansion of stacking faults occurs within the drift layer. Additionally, stacking faults have some crystallographically stable (non-moving) boundaries. As a result, the expanded stacking fault regions often take on characteristic rectangular or triangular shapes.

Basal plane dislocations in the drift layer can be significantly reduced by appropriately setting the conditions for epitaxial growth. Today's SiC epitaxial wafers have greatly reduced the density of basal plane dislocations in the drift layer by forming an appropriate buffer layer.

Crystal defects are also generated when ion implantation is performed on SiC. Figure 3 shows a cross-sectional transmission electron microscopy (TEM) image after high-concentration Al ion implantation and annealing in SiC. As seen in Figure 3 (1), defects that appear dark due to strain are present at high density in the Al-implanted region. The crystal is not completely recovered even after high-temperature annealing. Figure 3 (2) shows a high-resolution TEM image (lattice image) of the defect area.

A structure with a period of four layers (period is 1 nm) is observed, indicating that it is 4H-type SiC. An extra layer is inserted at the location indicated by the arrow in the figure, forming a Frank-type stacking fault※4. It is known that elements such as Al introduced by implantation gather in layers and form stacking faults in this region.

Defects caused by ion implantation are known to act as carrier recombination centers, which, for example, reduce the stored charge and recovery current in SiC pn diodes. Recently, there have been attempts to use defects caused by ion implantation as a means to suppress conduction degradation in the body diode of SiC MOSFETs.

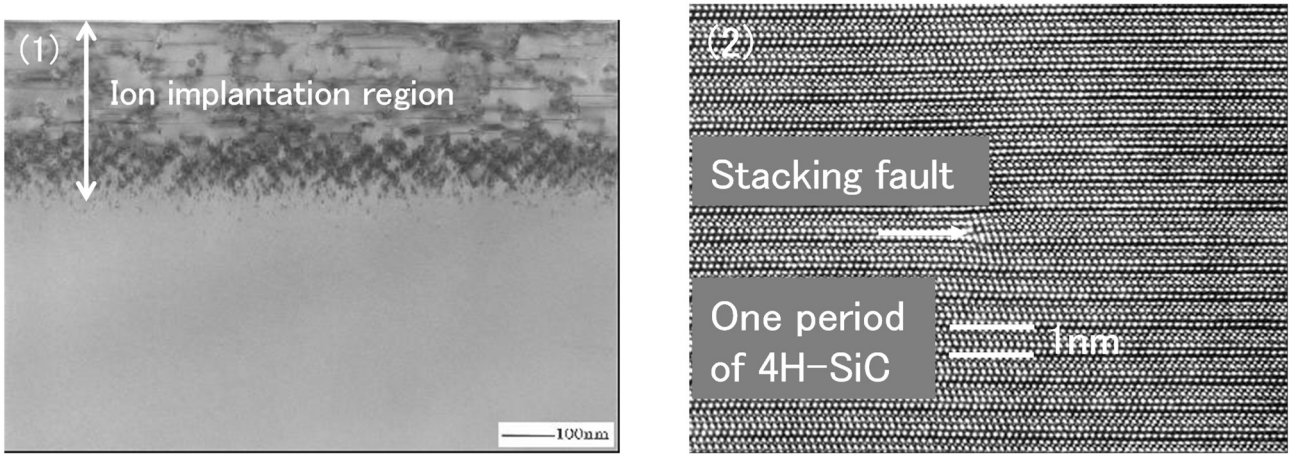

Figure 3 TEM image of crystal defects formed by ion implantation (left)
high-resolution image of the defect area (right)

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Power Device Works

[Glossary]

*1: Polytype Inclusion
Refers to defects formed by the partial inclusion of a crystal (different polytype) with a different form from the single crystal in the SiC single crystal.

*2: Etch Pit
Pits on the surface that appear in defect areas such as dislocations when the crystal surface is etched with chemicals.

*3: Shockley Partial Dislocation
A type of linear defect that appears around Shockley-type stacking faults, which are a kind of planar defect. The atomic displacement is smaller than that of a complete dislocation, making it more mobile within the crystal.

*4: Frank-Type Stacking Fault
A type of planar defect where the stacking sequence of atoms differs from the surrounding area due to the insertion or omission of atomic layers. Unlike Shockley-type stacking faults, they typically do not move.