Mitsubishi Electric Corporation has developed a low power baseband modem LSI for W-CDMA mobile phones. The LSI was installed in D900i, achieving approx. 170/90 minutes of continuous talk time for voice/video phones, and approx. 550/420 hours of continuous standby time in stationary/moving states respectively. The architecture of this LSI is similar to that of the baseband modem LSI chipset used for D2101V, which was optimized for lowering power consumption. To realize this LSI, 0.15 um low leak semiconductor process technology was applied to integrate an AFE (Analog Front End), a CPU, two DSPs and a hardware accelerator on a 10.6mm-square silicon chip. Then the chip was packed into a 15mm-square, 513-ball FBGA, and along with an external memory package (stacking 32M-bit Flash ROM and 32M-bit PSRAM), the LSI enables baseband modem processing for W-CDMA mobile phones.

To extend talk time, talk current was reduced by means of (1) minimizing the hardware (to fit into one chip) by optimizing the algorithm and the required memory size for each function; (2) shortening the circuit operation time by thoroughly applying a clock gating technique to each circuit; and (3) decreasing the internal power voltage of the LSI (from 1.8V to 1.5V) by applying optimized semiconductor process. As a result, the operating current for baseband modem processing, which previously accounted for 35%-40% (200mA) of total talk current was reduced by 85%. The standby time was also extended with reduced standby current by means of (4) shortening the processing time by modifying the software for standby processing in communication control, which decreased 90% of the operating current that previously accounted for over 60%(7mA) of the total standby time; (5) reducing the leak current (to half) by partly turning on/off the internal power of the LSI; etc.
1. Foreword

The third-generation W-CDMA mobile phone system has been providing commercial services since 2001, offering advanced features such as video phone and high speed packet communications that are more attractive than the services based on the second generation system. However, for this new system to become widely adopted, the continuous talk time and standby time had to be extended.

This article describes the low power baseband modem LSI developed as a solution to this need, starting with an overview of its basic structure and characteristics, followed by details of the low power technology.

2. Baseband Modem LSI

This baseband modem LSI applies 0.15um low leak semiconductor process technology to integrate an AFE, a CPU, two DSPs, and a hardware accelerator on a 10.6mm square silicon chip. Figure 1 shows its architecture. The internal power supply of this LSI consists of one part that is constantly set on (for the CPU, two DSPs, and AFE) and the other part that can be switched on/off for the hardware accelerator. The architecture of this hardware is similar to that of the baseband modem LSI chipset(1)(2) used for D2101V.

General functionality of the LSI is described below.

The AFE contains AD/DA converters, transmits/receives analog IQ signals, etc. to/from the RF block, and converts between analog and digital signals.

The CPU is a 32-bit RISC(M32R) that processes communication protocol every 10ms frame, and uses the external memory (32M-bit Flash ROM and 32M-bit PSRAM) as well.

Each of the two DSPs is a 16-bit DSP microcomputer (D10V) which controls the RF block, the hardware accelerator, and part of the digital signal processing for communications in cycles of 667 us.

The hardware accelerator is divided into the channel encoder, modulator, demodulator, and decoder as described in (1)-(4) below:

(1) Encoder

The encoder performs channel encoding and interleaving by executing convolutional/turbo encoding on the transmitted data, and outputs the results to the modulator as a transmitted bit sequence.

(2) Modulator

The modulator performs data mapping and spreading on the transmitted bit sequence to generate the chip sequence, and outputs the results to the AFE as transmitted digital IQ signal within a limited bandwidth of 5MHz.

(3) Demodulator

The searcher performs cell search and path timing detection for the received digital IQ signal input from the AFE. The finger performs RAKE receiving to execute despreading and pilot coherent detection on each of the detected delay paths, and outputs the obtained bit sequence to the decoder block.

(4) Decoder

The decoder performs channel decoding (error correction) through deinterleaving and Viterbi/Turbo decoding and obtains the received data.

![Diagram of Baseband Modem LSI](image-url)
A typical example is shown below to describe the characteristics of this LSI.

Figure 2 shows measurement results regarding the performance in the birth-death propagation condition at RMC12.2kbps (see 3GPP TS25.101 Annex B B.2.4). The required DPCCH_Ec/fo that satisfies BLER=1E-2 has secured a 3.4dB margin from 3GPP specification.

Generally speaking, securing such characteristics and lowering power consumption by reducing circuit volume are considered contradictory, but through efficient algorithm techniques and other factors, this LSI achieves a fair level of demodulator performance.

### 3. Low Power Technology

Table 1 shows the targets and achievements in extending talk time and standby time. Compared to the previous model (D2101V), the targets were set to two or three times longer for the talk time, and six to ten times longer for the standby time. The low power technologies applied to achieve these targets with reduced talk/standby current are described below.

#### 3.1 Talk Current Reduction

This LSI contributes to reduce talk current mainly in terms of operating current (charge/discharge current for the internal circuit), which is calculated using the following formula.

\[
\text{Operating current} = Q \times C \times V \times t
\]

The following (1)-(3) techniques were applied to reduce the operating current.

1. **Reduction of capacity (C)**
   - Optimized the algorithm and required memory size for each function, and reduced the hardware volume to fit into one chip.

2. **Shortening of time (t)**
   - Thoroughly applied clock gating technique to each circuit and reduced the circuit operation time.

3. **Reduction of voltage (V)**
   - Applied the optimized semiconductor process, and reduced the internal power voltage from 1.8V to 1.5V.
   - As results of these techniques, the operating current for baseband modem processing, which previously accounted for about 35%-40%(200mA) of total talk, current was reduced by 85%.

Figure 3 shows the clock gating technique applied here. For example, the processor turns the operating clock on/off at function level (Signal A), and the block control sequencer of each function turns the operating clock on/off (Signal B) at block level, and the circuit sequencer of each block turns the operating clock on/off at circuit level (Signal C). Unlike the type of processor that shares and repeatedly uses a small number of computing units or registers, this type of hardware accelerator has various computing units operating in parallel, which enables hierarchical clock gating to effectively reduce the operating current.

#### 3.2 Standby Current Reduction

Other than (1)-(3) in Section 3.1 Talk Current Reduction, the following (4)-(5) techniques were applied to reduce the standby current.

(4) **Shortening of standby processing time**
- Modified the software to reduce standby processing time in communication control.

<table>
<thead>
<tr>
<th>Item</th>
<th>Previously</th>
<th>Target</th>
<th>Results (D900i)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Talk time (voice)</td>
<td>60 min</td>
<td>x 2-3</td>
<td>170 min</td>
</tr>
<tr>
<td>Talk time (videophone)</td>
<td>50 min</td>
<td>(ditto)</td>
<td>90 min</td>
</tr>
<tr>
<td>Standby time</td>
<td>55 hrs</td>
<td>x 6-10</td>
<td>550 hrs (stationary)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>420 hrs (moving)</td>
</tr>
</tbody>
</table>

Fig. 3 Clock gating technique
Figure 4 shows an example of observing such current profile during standby time (receiving PICH + acquiring SFN). The upper three signals indicate operating status of DSP-2, DSP-1 and the CPU respectively. (The DSP operates at L level; the CPU at H level.) The lower signal reflects current waveform. Each processor was activated when necessary. By shortening the processing time in this way, the operating current of communication control, which previously accounted for over 60% (7mA) of total standby current, was reduced by 90%.

(5) Reduction of leak current
Partly turned off the internal power of the LSI, which reduced the leak current by half.

About half of the chip area of this LSI is used for the hardware accelerator, and the power for this part of the chip is turned off while operation is not required during standby.

4. Conclusion
Mitsubishi Electric Corporation has developed a low power baseband modem LSI for W-CDMA mobile phones.

To extend talk time, talk current was reduced by means of (1) minimizing hardware (to fit into one chip) by optimizing the algorithm and the required memory size for each function; (2) shortening the circuit operation time by thoroughly applying a clock gating technique to each circuit; and (3) decreasing the internal power voltage of the LSI (from 1.8V to 1.5V) through optimizing the semiconductor process. Moreover, the standby time was extended with reduced standby current by means of (4) shortening the processing time by modifying the software for standby processing in communications control; (5) reducing the leak current by partly turning on/off the internal power of the LSI; etc. By applying such techniques to lower power consumption, the operating current for baseband modem processing, which previously accounted for about 35-40% (200mA) of talk current, was reduced by 85%. Also, the operating current for the communication control, which previously accounted for over 60% (7mA), was reduced by 90%.

Thus, D900i equipped with this LSI has attained a performance level of approx. 170/90 minutes for continuous talk and approx. 550/420 hours for continuous standby in stationary/moving states respectively.

Fig. 4 Example of observed current profile

References