Technologies for Seventh Generation High Performance, High Ruggedness Power Chips

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For the evolution of power electronics, it is essential to enhance the performance of Insulate Gate Bipolar Transistors (IGBTs) and diodes, both mounted on the power modules. Since the late 1980s, Mitsubishi Electric has been developing low-loss structures for IGBTs such as by fine pattern processing and the CSTBT™ (1-2). Diode performance has also been improved by thin wafer processing and cathode profile optimization.

This paper presents the high performance and ruggedness (i.e., wide Safe Operating Area (SOA)) seventh generation IGBT and diode, which have been developed by employing an ultra-thin wafer process and newly optimized profiles in the backside doping layer.

1. Seventh generation IGBT

The first to third generation IGBTs were of the planar type structure, and their performance was improved by applying the conventional finer cell-pitch patterning technology. The fourth and later generations adopted a trench-type structure instead; and the fifth and later generations adopted Mitsubishi Electric's proprietary CSTBT™ structure, where a Carrier-Stored (CS) layer is formed beneath the Channel Dope layer. Since the CS layer can enhance the electron injection efficiency to hold high enough holes on the emitter side during on-state, i.e. carrier storing effect, it is possible to reduce the on-state forward voltage drop $V_{on}$. The sixth generation IGBT employed the narrower trench-gate pitch to enhance the carrier storing effect and the performance was further improved. In addition, the high energy ion implantation was used to form the CS layer, and the variance in the threshold voltage was successfully reduced.

The performance of the IGBT is described by the Figure Of Merit (FOM) defined by:

$$ FOM = \frac{J_C}{V_{CE(sat)}} \times E_{off} $$

(1)

where $J_C$ (A/cm²) is the collector current density, $V_{CE(sat)}$ (V) is the collector-emitter saturation voltage (on-state voltage $V_{on}$), and $E_{off}$ (mJ/cm²/A/pulse) is the normalized turn-off energy loss.

The sixth generation IGBT achieved far higher performance than the first generation: the FOM of the 1200V class IGBT was increased by more than 10-fold from the first generation. Additional improvements have also achieved the required product characteristics of high reliability such as high temperature operation and high ruggedness, and those are based upon the improved termination and backside structures as well as the metal oxide semiconductor (MOS) structure.

Figure 1 shows the cross-sectional schematics of the sixth and seventh generation IGBTs. The 600V class seventh generation IGBT employs the Light Punch-Through (LPT) structure by using the ultra-thin wafer process to improve the trade-off between $V_{on}$ and $E_{off}$. At the same time, the area ratio between the N⁺ emitter and P⁺ region of the gate structure as the MOS cell is also optimized to maintain the sufficiently low saturation current, thus ensuring the wide Short Circuit SOA (SCSOA)⁴.

Figure 2 shows the output $V_{CE}$-$J_C$ characteristics of the sixth and seventh generation 600V class IGBTs. In the seventh generation IGBT, the LPT structure reduced the concentration in the P⁺ collector and N⁺ buffer layers, which keeps the built-in potential (voltage) lower than that of the sixth generation IGBT, and
improved the more than 0.1V of $V_{on}$ at or around the rated current density of 500A/cm². In addition in the seventh generation IGBT, the trade-off between the $V_{on}$ and $E_{off}$ has been adjusted by the backside P collector concentration, so as to exhibit a lower cross point of the $V_{CE}$-$I_C$ curve suitable for parallel operation. The seventh generation IGBT requires no carrier lifetime control process such as electron beam irradiation. Therefore, it exhibits stable electrical characteristics for a long time, and is suitable for high temperature, large current operation.

Figure 3 shows the turn-off waveforms of the sixth and seventh generation IGBTs, both using 600V/10A rated power chips and measured under the following conditions: collector-emitter voltage $V_{CE} = 300V$, gate-emitter voltage $V_{GE} = 15V/0V$, collector current $I_C = 10A$, and temperature $T_j = 125\text{degC}$. The seventh generation IGBT has a lower tail current than that of the sixth generation and has reduced the turn-off loss by about 34%. Also, by optimizing the backside P-collector concentration, the seventh generation IGBT, just like the sixth, has successfully suppressed the oscillation in the turn-off waveform.

Figure 4 shows the waveforms of the seventh generation IGBT that demonstrate the characteristics of the SCSOA. As the described above, the optimized MOS structure maintained the saturation current sufficiently low to enhance the latch-up tolerance. As a result, a wide SCSOA that satisfies the product requirements is ensured up to a pulse width of 2.5μs under the conditions of $V_{CE} = 400V$, $V_{GE} = 15V/0V$, and $T_j = 125\text{degC}$.

So, the seventh generation IGBT has achieved the excellent performance with an FOM of 1.8 times of that of the sixth generation maintaining an even wider SCSOA.

2. Seventh generation diode

The free wheeling diode has reduced the forward voltage drop $V_F$ by employing the thin wafer process and optimizing the cathode profile\(^{(4)}\). While the thin wafer process is effective for reducing the $V_F$ for both the IGBT and diode, it in turn reduces the margin against a snap-off voltage endurance during the reverse recovery time period, and hence increases the risk of device breakdown. This time, the thin wafer process has been employed together with a new backside cathode doping profile to develop the seventh generation diode\(^{(5)}\).

Figure 5 shows the cross-sectional schematics of the conventional and seventh generation diodes. In the seventh generation diode, there are partial P type regions on the cathode side. This structure avoids carriers from an absence time period around the cathode even under the depletion severely hitting the cathode conditions during the reverse recovery mode operation. As a result, the electric field on the cathode side is relaxed and thus the oscillation phenomenon is prevented.

Figure 6 shows the output $V_{AK}$-$\text{J}_A$ characteristics of 1200V class conventional and seventh generation diodes. Maintaining the low $V_F$ characteristics, the seventh generation diode has reduced the cathode electron injection efficiency to keep a low current level of the cross point between the $V_{AK}$-$\text{J}_A$ curves at room
and high temperatures. This tends to reduce the unexpected current increase when the temperature rises at or around the rated current, and thus the seventh generation diode is suitable for the chip parallel operation of the high power module.

Figure 7 shows the reverse recovery waveforms of conventional and seventh generation diodes, both using 1200V/10A rated power chips and measured under the conditions of \( V_{\text{cc}} = 800 \text{V}, I_{A} = 0.6 \text{A}, \) and \( T_{J} = 25^\circ\text{C} \), in which condition the conventional diode tends to cause oscillation. The conventional diode generates a high voltage peak (snap-off) when the tail current is sharply shut off, as depicted by broken circles in Fig.7. In contrast, with the seventh generation diode, almost no voltage surge is observed and the snap-off is successfully prevented. This peak voltage, defined as the snap-off voltage \( V_{\text{snap-off}} \), was measured with increasing \( V_{\text{cc}} \) applied during the reverse recovery time period. The result revealing the ultimate characteristics is shown in Fig. 8. The \( V_{\text{snap-off}} \) of the conventional diode

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\text{is heavily dependent on the } V_{\text{cc}} \text{, and the } V_{\text{snap-off}} \text{ exceeds the rated breakdown voltage at } V_{\text{cc}} = 800 \text{V, and at } V_{\text{cc}} = 900 \text{V the chip was destroyed. On the other hand, the seventh generation diode effectively suppresses the } V_{\text{snap-off}}. \text{ This suppression effect is more conspicuous with increasing } V_{\text{cc}}, \text{ and allows the recovery operation even at } V_{\text{cc}} = 1000 \text{V without any breakdown.}
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Consequently, the seventh generation diode makes it possible to reduce the wafer thickness by about 21% from the sixth generation level without emerging oscillation phenomenon, resulting in the reduction of \( V_{R} \) and reverse recovery loss \( E_{\text{off}} \).

The FOM of the diode is also defined by Eq. (1), where the collector current density \( J_{C} \) (A/cm²) is replaced with the anode current density \( J_{A} \) (A/cm²), the collector-emitter saturation voltage \( V_{CE}\text{(sat)} \) (V) that determines the steady-state loss with the forward voltage drop at 125degC \( V_{R} \) (V), and the turn-off loss \( E_{\text{off}} \) (mJ/cm²/A/pulse) with the reverse recovery loss at

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\text{(a) Conventional diode} \quad \text{(b) Seventh generation diode}
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Fig. 5 Cross-sectional schematics of conventional and seventh generation diodes

Fig. 6 Output characteristics of conventional and seventh generation diodes

Fig. 7 Reverse recovery waveforms of conventional and seventh generation diodes under oscillation-prone conditions

Fig. 8 \( V_{\text{cc}} - V_{\text{snap-off}} \) relationship of conventional and seventh generation diodes under oscillation-prone conditions
125degC $E_{eff}$ (mJ/cm²/A/pulse). In terms of the FOM, the seventh generation diode has achieved a drastic improvement, 2.7 times higher than that of the conventional diode.

We are currently developing a 1200V class IGBT and diode that employ the new ultra-thin wafer process and the backside doping profile already applied to 600V class devices. In addition, we plan to apply the seventh generation technologies to all the diodes with a higher breakdown voltage including the 6500V class chips. We will continue to serve a series of high performance and high quality Si power chips to all the applications of the markets.

References