

TECHNICAL BULLETIN

[Issue No.] FA-A-0110-A

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[Title] Addition of the program cache memory auto recovery function

[Date of Issue] February 2011 (Ver.A: March 2012)

[Relevant Models] Universal model QCPU, LCPU

Thank you for your continued support of Mitsubishi programmable controllers, MELSEC-Q series.

To improve the availability of a Universal model QCPU and LCPU, the program cache memory auto recovery function has been added.

1. Program cache memory check function

In a Universal model QCPU and LCPU, program cache memory data is checked^{*1} to enhance the reliability of the memory during use.

If an error, such as data alteration due to excessive electrical noise, is detected in the program cache memory, RAM ERROR (error code: 1160)^{*2} will occur, and the CPU module will stop to prevent malfunction.

*1: A parity check is performed.

*2: If an error is detected when program cache memory data does not match with program memory data, RAM ERROR (error code: 1163) will occur.

2. New function (program cache memory auto recovery function)

With this function, the program cache memory automatically recovers from an error, detected by the memory check function described in 1. using program memory data in the flash ROM.

This function is activated when:

- A program is executed.
- "Verify with PLC" or "Read from PLC" is executed.

Even if program cache memory data is altered due to a cause such as noise, the CPU module can continue its operation.

2.1 Operating conditions

This function is activated when the following conditions are met.

[Condition 1] The CPU module is in RUN.

[Condition 2] Program cache memory data and program memory data match.

Even if these conditions are met, the function might not be activated. For details, refer to "2.2 Restrictions".

For how to meet Condition 2, refer to Page 3, Appendix.

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2.2 Restrictions

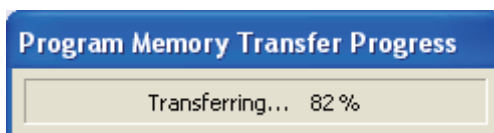
In the following cases, the function is not activated, and RAM ERROR (error code: 1160) will occur.

1) Program cache memory data is altered while any of the following operations are performed.

Operation item (Write operation)	Universal model QCPU with a serial No. (first 5 digits) of "12121" or earlier	Universal model QCPU with a serial No. (first 5 digits) of "12122" or later and LCPU with a serial No. (first 5 digits) of "13102" or later
Program writing while the CPU module is in RUN	×	△ ^{*3}
Password protection for the program file	×	○
Program memory batch-transfer	×	△ ^{*3}
Writing of program memory data to a ROM	×	○
Writing of device comments to the CPU module	×	△ ^{*3}

○: The auto recovery is performed and no error occurs. △: An error occurs under some conditions. ×: An error occurs.

*3: If an alteration of program cache memory data is detected while the data in the memory is being transferred to a program memory after write operation (while the following window is being displayed on a programming tool), the auto recovery is not performed, and an error occurs.



Window indicating data transfer to a program memory in progress

- 2) Alteration of the program cache memory data is detected using an SFC program.
- 3) Alteration of the program cache memory data is detected using a dedicated instruction (e.g. S(P)).
- 4) Alteration of the program cache memory data is detected using the rise/fall instruction.
- 5) Auto recovery failed due to failure of the memory.

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2.3 Compatible CPU module

The following table lists the versions of the CPU module supporting the function (first five digits of the serial number).

CPU model	Activation timing	
	A program is executed	<ul style="list-style-type: none"> • A program is executed • "Verify with PLC" or "Read from PLC" is executed • The write operations described in the section 2.2.1) are performed^{*4}
Q00UCPU, Q01UCPU, Q02UCPU, Q03UD(E)CPU, Q04UD(E)HCPU, Q06UD(E)HCPU, Q10UD(E)HCPU, Q13UD(E)HCPU, Q20UD(E)HCPU, Q26UD(E)HCPU	"11072" or later (Product released after June 2009)	"12122" or later (Product released after November 2010)
Q50UDEHCPU, Q100UDEHCPU	(Supported from the first-released product.)	
L02CPU, L26CPU-BT, L02CPU-P, L26CPU-PBT	"13102" or later (Product released after October 2011)	

*4: To perform the auto recovery while the write operations described in the section 2.2.1) are performed, use a programming tool with the version described in the table below.

CPU model	Programming tool version	
	GX Works2	GX Developer
Universal model QCPU	1.80J or later	8.102G or later
LCPU		Not supported

Because an LCPU does not support GX Developer, use GX Works2.

The serial number of the CPU module is shown on:

- The rating plate.
- The display on the front of the module (lower part).
- The label on the package.
- The "System Monitor" dialog box ("Product Information List" dialog box) of a programming tool.

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[Appendix] Making program cache memory data match with program memory data

To make them match, execute the following:

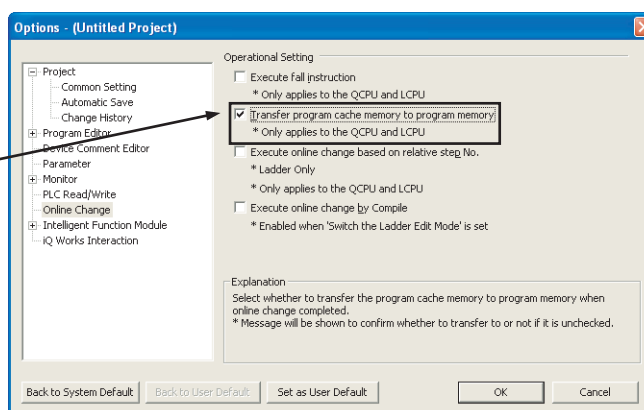
- 1) Setting auto data transfer that sends data to the program memory after data is written while the CPU module is in RUN or a T/C setting value is changed

To keep program cache memory data and program memory data matched even after data is written while the CPU module is in RUN or a T/C setting value is changed, set auto data transfer to the program memory.

By configuring the setting, data written to the program cache memory is immediately transferred to the program memory.

Configure the setting in the following dialog box, displayed by clicking [Tool] ([Tools] for GX Developer) → [Options] in a programming tool.*5

To avoid automatic transfer of program memory data, clear the checkbox.
(Selected by default.)



Dialog box of GX Works2

*5: The setting is configured for a programming tool by default.

- 2) Batch-transferring data to the program memory

When not setting 1), batch-transfer program cache memory data to the program memory.

To configure the setting, select [Online] → [Program Memory Batch Download] ([Program memory batch transfer] for GX Developer) in a programming tool.

For inquiries, contact your local Mitsubishi Electric System & Service Co., Ltd. or local Mitsubishi representative.

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REVISIONS

Version	Print Date	Revision
-	December 2007	First edition
A	March 2012	<ul style="list-style-type: none">• An LCPU was added to the relevant models.• The descriptions in "2.2 Restrictions" and "2.3 Compatible CPU module" were revised.