<DIPIPM>
600V LARGE DIPIPM Ver.6 Series APPLICATION NOTE
PSS**SA2F6

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CHAPTER 1 INTRODUCTION

1.1 Target Applications

Motor drives for industrial use, such as packaged air conditioners, general-purpose inverter, servo, except for automotive applications.

1.2 Product Line-up

<table>
<thead>
<tr>
<th>Type Name</th>
<th>IGBT Rating</th>
<th>Motor Rating (Note 1)</th>
<th>Isolation Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSS50SA2F6</td>
<td>50A/600V</td>
<td>3.7kW / 220VAC</td>
<td>$V_{iso} = 2500$Vrms</td>
</tr>
<tr>
<td>PSS75SA2F6</td>
<td>75A/600V</td>
<td>5.5kW / 220VAC</td>
<td>(Sine 60Hz, 1min)</td>
</tr>
</tbody>
</table>

Note 1: These motor ratings are general ratings, so those may be changed by conditions.

1.3 Functions and Features

600V Large DIPIPM Ver.6 is a compact intelligent power module with transfer molding package favorable for larger mass production. And it includes power chips, drive and protection circuits. This series apply same package, which has high thermal radiation performance by the insulated sheet structure, and pin compatibility with current Large DIPIPM Ver.4 series. In addition, this series newly integrate low loss 7th generation IGBT optimized for DIPIPM and 600V bootstrap diodes for generating P-side driver 15V supply. Large DIPIPM Ver.6 will contribute to improve system efficiency, cost and also design time.

Outline photograph and internal cross-section structure are described in Fig.1-1 and Fig.1-2.

![Fig.1-1 Package outline](image1)

![Fig.1-2 Internal cross-section structure](image2)
Features:

- For P-side IGBTs
  - Drive circuit
  - High voltage level shift circuit
  - Control supply under voltage (UV) protection circuit (without fault signal output)
  - Built-in bootstrap diode with current limiting resistor

- For N-side IGBTs
  - Drive circuit
  - Short circuit (SC) protection circuit (by detecting sense current divided at N-side IGBT with external sense resistor)
  - Control supply under voltage (UV) protection circuit (with fault signal output)
  - Analog output of LVIC temperature

- Fault Signal Output
  - Corresponding to SC protection and N-side UV protection

- IGBT Drive Supply
  - Single DC15V power supply

- Control Input Interface
  - Schmitt-triggered 3V, 5V input compatible, High active logic

- UL Recognized
  - UL1557 File E323585

1.4 The Differences of Previous Series (600V Large DIPIPM Ver.4) and This Series

There are some differences between this Ver.6 series and former Ver.4 series (PS21A7*) as below Table 1-2.

<table>
<thead>
<tr>
<th>Item</th>
<th>Ver.4</th>
<th>Ver.6</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PS21A79</td>
<td>PS21A7A</td>
<td>PSS50SA2F6</td>
</tr>
<tr>
<td>Built-in IGBT</td>
<td>5th generation IGBT (LPT-CSTBT)</td>
<td>7th generation IGBT (LPT-CSTBT)</td>
<td>-</td>
</tr>
<tr>
<td>Bootstrap Di</td>
<td>Nothing</td>
<td>Built-in (with current limit R typ. 20Ω)</td>
<td>-</td>
</tr>
<tr>
<td>Temperature output (V_{OT} output)</td>
<td>typ. 3.63V (at LVIC temp. = 85°C)</td>
<td>typ. 2.36V (at LVIC temp. = 75°C)</td>
<td>with pull down resistor</td>
</tr>
<tr>
<td>Fault output current I_{FO}</td>
<td>max. 1mA</td>
<td>max. 5mA (Direct coupler drive is available)</td>
<td>Section 3.1.4</td>
</tr>
<tr>
<td>Arm shoot through blocking time</td>
<td>Min. 2.2μs</td>
<td>Min. 2.7μs</td>
<td>Min. 2.2μs</td>
</tr>
<tr>
<td>Tj</td>
<td>-20°C ~150°C</td>
<td>-30°C ~150°C</td>
<td></td>
</tr>
<tr>
<td>Tc</td>
<td>-20°C ~100°C</td>
<td>-30°C ~125°C</td>
<td></td>
</tr>
</tbody>
</table>

There are other differences. (e.g. electric characteristics, sense resistance for SC protection, allowable minimum pulse width and electrical potential of dummy terminals) Please refer each datasheet for more detail.
CHAPTER 2 SPECIFICATIONS AND CHARACTERISTICS

2.1 Specifications

The specifications are described below by using PSS75SA2F6 (75A/600V) as an example. Please refer to respective datasheet for the detailed description of other types.

2.1.1 Maximum Ratings

The maximum ratings of PSS75SA2F6 are shown in Table 2-1.

### INVERTER PART

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc</td>
<td>Supply voltage</td>
<td>Applied between P-NU,NV,NW</td>
<td>450</td>
<td>V</td>
</tr>
<tr>
<td>Vcc(surge)</td>
<td>Supply voltage (surge)</td>
<td>Applied between P-NU,NV,NW</td>
<td>500</td>
<td>V</td>
</tr>
<tr>
<td>Vces</td>
<td>Collector-emitter voltage</td>
<td></td>
<td>600</td>
<td>V</td>
</tr>
<tr>
<td>( \pm I )</td>
<td>Each IGBT collector current</td>
<td>( T_C = 25^\circ C )</td>
<td>75</td>
<td>A</td>
</tr>
<tr>
<td>( \pm ICP )</td>
<td>Each IGBT collector current (peak)</td>
<td>( T_C = 25^\circ C ), up to 1ms</td>
<td>150</td>
<td>A</td>
</tr>
<tr>
<td>Tj</td>
<td>Junction temperature</td>
<td></td>
<td>-30~+150</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Note 1:** Pulse width and period are limited due to junction temperature.

### CONTROL (PROTECTION) PART

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vd</td>
<td>Control supply voltage</td>
<td>Applied between ( V_{P1},V_{NC},V_{N1}-V_{NC} )</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>Vcs</td>
<td>Control supply voltage</td>
<td>Applied between ( V_{UPF},V_{US},V_{WP},V_{WS} )</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>vn</td>
<td>Input voltage</td>
<td>Applied between ( u_n, v_n, w_n-V_{NC} )</td>
<td>-0.5~0.5</td>
<td>V</td>
</tr>
<tr>
<td>Vfo</td>
<td>Fault output supply voltage</td>
<td>Applied between ( F_{0},V_{NC} )</td>
<td>-0.5~0.5</td>
<td>V</td>
</tr>
<tr>
<td>Ifo</td>
<td>Fault output current</td>
<td>Sink current at ( F_{0} ) terminal</td>
<td>5</td>
<td>mA</td>
</tr>
<tr>
<td>Vsc</td>
<td>Current sensing input voltage</td>
<td>Applied between ( C_{IN}-V_{NC} )</td>
<td>-0.5~0.5</td>
<td>V</td>
</tr>
</tbody>
</table>

### TOTAL SYSTEM

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc(pro)</td>
<td>Self protection supply voltage limit</td>
<td>( V_D = 13.5~16.5 \text{V}, \text{Inverter Part} )</td>
<td>400</td>
<td>V</td>
</tr>
<tr>
<td>Tc</td>
<td>Module case operation temperature</td>
<td>( T_{C} = 150^\circ \text{C}, \text{non-repetitive, up to 2us} )</td>
<td>-30~+125</td>
<td>°C</td>
</tr>
<tr>
<td>Tstg</td>
<td>Storage temperature</td>
<td></td>
<td>-40~+125</td>
<td>°C</td>
</tr>
<tr>
<td>Viso</td>
<td>Isolation voltage</td>
<td>60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate</td>
<td>2500</td>
<td>Vmax</td>
</tr>
</tbody>
</table>

**Note 2:** \( T_C \) measurement point

![Diagram](image)

**[Item explanation]**

1. **Vcc** The maximum P-N voltage in no switching state. Voltage suppressing circuit such as a brake circuit is necessary if the voltage exceeds this value.
2. **Vcc(surge)** The maximum P-N surge voltage in switching state. Snubber circuit is necessary if the voltage exceeds \( V_{cc} \).
3. **Vces** The maximum sustained collector-emitter voltage of built-in IGBT.
4. **Tj** The allowable current flowing into collect electrode (\( @T_{C}=25^\circ \text{C} \)). Pulse width and period are limited due to junction temperature \( Tj \).
5. **Tj** The maximum junction temperature rating is 150°C. Please design its junction temperature so that it doesn’t exceed 150°C including the ripple during continuous operation. Repetitive temperature variation \( \Delta Tj \) affects the life time of power cycle, so refer life time curves (Section 3.1.10) for safety design.
6. **Vcc(prot)** The maximum supply voltage for IGBT turning off safely in case of an SC fault. The power chip might be damaged if supply voltage exceeds this rating.
7. **Tj** (case temperature) is defined as the temperature just underneath the specified power chip. Please mount a thermocouple on the heat sink surface at above position to get proper temperature. Due to the control schemes (e.g. Different control between P and N-side like two phase modulation, high-side chopping), the highest \( Tj \) point may be different from above point. In such cases, it is necessary to change the measuring point to that under the highest power chip. (Refer Section 2.3.2)
2.1.2 Thermal Resistance

Table 2-2 shows the thermal resistance.

Table 2-2 Thermal resistance of PSS75SA2F6

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{th(j-c)}}$</td>
<td>Junction to case thermal resistance (Note 1)</td>
<td>Inverter IGBT part (per 1/6 module)</td>
<td>-</td>
<td>0.77 K/W</td>
</tr>
<tr>
<td>$R_{\text{th(j-f)}}$</td>
<td>Inverter FWDi part (per 1/6 module)</td>
<td>-</td>
<td>1.25 K/W</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Grease with good thermal conductivity and long-term endurance should be applied evenly with about $+100\mu \text{m}$ to $+200\mu \text{m}$ on the contacting surface of DIPIPM and heat sink. The contacting thermal resistance between DIPIPM case and heat sink $R_{\text{th(c-f)}}$ is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{\text{th(c-f)}}$ is about 0.2 K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0 W/m•K).

The above data shows the thermal resistance between chip junction and case at steady state. The thermal resistance goes into saturation in about 10s. The thermal resistance under 10s is called as transient thermal impedance which is shown in Fig.2-1. $Z_{\text{th(j-c)}}^*$ is the normalized value of the transient thermal impedance. ($Z_{\text{th(j-c)}}^* = Z_{\text{th(j-c)}} / R_{\text{th(j-c)}}$) For example, the IGBT transient thermal impedance of PSS75SA2F6 in 0.1s is $0.77 \times 0.5 = 0.39$ K/W.

The transient thermal impedance isn’t used for constantly current, but for short period current (ms order). (E.g. In the cases at motor starting, at motor lock...)

![Fig.2-1 Typical transient thermal impedance](image-url)
2.1.3 Electric Characteristics (Power Part)

Table 2-3 shows the typical static characteristics and switching characteristics.

### Table 2-3 Static characteristics and switching characteristics of PSS75SA2F6

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Collector-emitter saturation voltage</td>
<td>( V_{CE(sat)} = V_{CEB} = 15V, V_{BE} = 5V, I_{C} = 75A )</td>
<td>( T_{J} = 25^\circ C )</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{J} = 125^\circ C )</td>
<td>-</td>
</tr>
<tr>
<td>( V_{EC} )</td>
<td>FWDI forward voltage</td>
<td>( V_{EIN} = 0V, -I_{C} = 75A )</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>( t_{on} )</td>
<td>Switching times</td>
<td>( V_{CC} = 300V, V_{DB} = V_{D}= 15V )</td>
<td>( I_{C} = 75A, T_{J} = 125^\circ C, V_{IN(RN)} = 0\rightarrow 5V )</td>
<td>-</td>
</tr>
<tr>
<td>( t_{off} )</td>
<td></td>
<td>Inductive Load (upper-lower arm)</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>( t_{ss} )</td>
<td></td>
<td></td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>( I_{CES} )</td>
<td>Collector-emitter cut-off current</td>
<td>( V_{CES} = V_{CE} )</td>
<td>( T_{J} = 25^\circ C )</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{J} = 125^\circ C )</td>
<td>-</td>
</tr>
</tbody>
</table>

Switching time definition and performance test method are shown in Fig.2-2 and 2-3.

![Fig.2-2 Switching time definition](image)

![Fig.2-3 Evaluation circuit (inductive load)](image)

Short A for N-side IGBT, and short B for P-side IGBT evaluation

![Fig.2-4 Typical switching waveform](image)

Conditions: \( V_{CC}=300V, V_{DB}=V_{D}=15V, T_{J}=125^\circ C, I_{C}=75A \), Inductive load half-bridge circuit
### 2.1.4 Electric Characteristics (Control Part)

#### Table 2-4 Control (Protection) characteristics of PSS75SA2F6

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_0 )</td>
<td>Circuit current</td>
<td>Total of ( V_{P1}-V_{NC}, V_{N1}-V_{NC} ); ( V_{DC}=15V, V_{IN}=0V )</td>
<td>Min. 0 - Typ. (5.5)</td>
<td>Max. mA</td>
</tr>
<tr>
<td>( I_{DB} )</td>
<td>Each part of ( V_{UFB}-V_{FS}, V_{VFB}-V_{FS}, V_{WFB}-V_{FS} ); ( V_{DC}=V_{DB}=15V, V_{IN}=0V )</td>
<td>Min. 0 - Typ. (0.55)</td>
<td>Max. mA</td>
<td></td>
</tr>
<tr>
<td>( I_{SC} )</td>
<td>Short circuit trip level</td>
<td>Without outer shunt resistors to NU,NV,NW terminals (Note 1)</td>
<td>Min. 127 - Typ. - Max. A</td>
<td></td>
</tr>
<tr>
<td>( U_{VDB} )</td>
<td>P-side Control supply under-voltage protection(UV)</td>
<td>Trip level</td>
<td>Min. 10.0 - Typ. (12.0)</td>
<td>Max. V</td>
</tr>
<tr>
<td>( U_{VDB} )</td>
<td>P-side Control supply under-voltage protection(UV)</td>
<td>Reset level</td>
<td>Min. 10.5 - Typ. (12.5)</td>
<td>Max. V</td>
</tr>
<tr>
<td>( U_{VDB} )</td>
<td>N-side Control supply under-voltage protection(UV)</td>
<td>Trip level</td>
<td>Min. 10.3 - Typ. (12.5)</td>
<td>Max. V</td>
</tr>
<tr>
<td>( U_{VDB} )</td>
<td>N-side Control supply under-voltage protection(UV)</td>
<td>Reset level</td>
<td>Min. 10.8 - Typ. (13.0)</td>
<td>Max. V</td>
</tr>
<tr>
<td>( V_{FOH} )</td>
<td>Fault output voltage</td>
<td>( V_{NC}=0V, ; F_O ) terminal pulled up to 5V by 10k( \Omega )</td>
<td>Min. 4.9 - Typ. - Max. V</td>
<td></td>
</tr>
<tr>
<td>( V_{FOL} )</td>
<td>Fault output voltage</td>
<td>( V_{SC}=1V, ; I_{FO}=1mA )</td>
<td>Min. - - Typ. (0.95)</td>
<td>Max. V</td>
</tr>
<tr>
<td>( I_{IN} )</td>
<td>Input current</td>
<td>( V_{IN}=5V )</td>
<td>Min. 0.7 - Typ. (1.0)</td>
<td>Max. (1.5) mA</td>
</tr>
<tr>
<td>( V_{Ron} )</td>
<td>ON threshold voltage</td>
<td>Applied between ( U_{i}, ; V_{i} ), ( W_{i}, ; U_{NC}, ; V_{NC}, ; W_{NC} )</td>
<td>Min. - - Typ. (2.1)</td>
<td>Max. (2.6) V</td>
</tr>
<tr>
<td>( V_{Ron} )</td>
<td>OFF threshold voltage</td>
<td></td>
<td>Min. 0.8 - - Typ. -</td>
<td>Max. V</td>
</tr>
<tr>
<td>( V_{OC} )</td>
<td>Temperature output</td>
<td>LVIC temperature=75°C; Pull down ( R=5.1k\Omega ) (Note 3)</td>
<td>Min. 2.26 - Typ. (2.38)</td>
<td>Max. (2.51) V</td>
</tr>
<tr>
<td>( V_{F} )</td>
<td>Bootstrap Di forward voltage</td>
<td>( I_{F}=10mA ) including voltage drop by limiting resistor</td>
<td>Min. 0.5 - Typ. (0.9)</td>
<td>Max. (1.3) V</td>
</tr>
<tr>
<td>( R )</td>
<td>Built-in limiting resistance</td>
<td>Included in bootstrap Di</td>
<td>Min. 16 - Typ. (20)</td>
<td>Max. (24) ( \Omega )</td>
</tr>
</tbody>
</table>

**Note 1:** Short circuit protection detects sense current divided from main current at N-side IGBT and works for N-side IGBT only. In the case that outer shunt resistor is inserted into main current path, protection current level \( I_{SC} \) changes. For details, please refer the section about SC protection in this document.

**Note 2:** Fault signal is output when short circuit or N-side control supply under-voltage protection works. The fault output pulse-width \( t_{FO} \) depends on the capacitance \( C_{FO} \). \( C_{FO} \) (typ.) = \( t_{FO} \times (9.1 \times 10^{-6}) \) [F].

**Note 3:** DIPIPM doesn’t shut down IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIPIPM immediately.

*) Some specifications differs according to its rated current. For more details, please refer to the datasheet for each product.
2.1.5 Recommended Operating Conditions

The recommended operating conditions are described in Table 2-5. Although these conditions are the recommended but not the necessary ones, it is highly recommended to operate the modules within these conditions so as to ensure DIPIPM safe operation.

Table 2-5 Recommended operating conditions of PSS75SA2F6

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply voltage</td>
<td>Applied between P-NU, NV, NW</td>
<td>0 300 400</td>
<td>V</td>
</tr>
<tr>
<td>VD</td>
<td>Control supply voltage</td>
<td>Applied between VPI-VNC, VHI-VNC</td>
<td>13.5 15.0 16.5</td>
<td>V</td>
</tr>
<tr>
<td>VDB</td>
<td>Control supply voltage</td>
<td>Applied between VURB-VUS, VURB-VUS, VURB-VUS, VURB-VUS</td>
<td>13.0 15.0 18.5</td>
<td>V</td>
</tr>
<tr>
<td>ΔVDB</td>
<td>Control supply variation</td>
<td>-1 -1 +1</td>
<td>V/μs</td>
<td></td>
</tr>
<tr>
<td>tdead</td>
<td>Arm shoot-through blocking time</td>
<td>For each input signal</td>
<td>2.4 - -</td>
<td>μs</td>
</tr>
<tr>
<td>fPWM</td>
<td>PWM input frequency</td>
<td>Tc ≤ 100°C, TJ ≤ 125°C</td>
<td>- - 20</td>
<td>kHz</td>
</tr>
<tr>
<td>PWIN(on)</td>
<td>Minimum input pulse width</td>
<td>(Note 4)</td>
<td>1.5 - -</td>
<td>μs</td>
</tr>
<tr>
<td>PWIN(off)</td>
<td>Minimum input pulse width</td>
<td>(Note 5)</td>
<td>3.0 - -</td>
<td>μs</td>
</tr>
<tr>
<td>VNC</td>
<td>VNC variation</td>
<td>Between VNC-NU, NV, NW (including surge)</td>
<td>-5.0 - +5.0</td>
<td>V</td>
</tr>
</tbody>
</table>

Note 4: DIPIPM might not make response if the input signal pulse width is less than PWIN(on).

5: DIPIPM might make no response or delayed response (P-side IGBT only) for input pulse width less than PWIN(off).

Over rated collector current (Ic) operation, DIPIPM might make delayed response even if the input signal pulse width is more than PWIN(off).

About Delayed Response Against Shorter Input Off Signal Than PWIN(off) (P-side only)

*) Some specifications differs according to its rated current. For more details, please refer to the datasheet for each product.
2.1.6 Mechanical Characteristics and Ratings

The mechanical characteristics and ratings are shown in Table 2-6. Please refer to Section 2.4 for the detailed mounting instruction.

Table 2-6  Mechanical characteristics and ratings of PSS75SA2F6

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Reference</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mounting torque</td>
<td>Mounting screw : M4 (Note 6)</td>
<td>JEITA-ED-4701</td>
<td>0.98</td>
<td>1.18</td>
</tr>
<tr>
<td></td>
<td></td>
<td>402 method II</td>
<td>Max</td>
<td></td>
</tr>
<tr>
<td>Terminal strength pulling</td>
<td>Load 20N</td>
<td>JEITA-ED-4701</td>
<td>10</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>401 method I</td>
<td>Max</td>
<td></td>
</tr>
<tr>
<td>Terminal strength bending</td>
<td>Load 10N, 90deg. bend</td>
<td>JEITA-ED-4701</td>
<td>2</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>401 method III</td>
<td>Max</td>
<td></td>
</tr>
<tr>
<td>Weight</td>
<td></td>
<td></td>
<td>-</td>
<td>46</td>
</tr>
<tr>
<td>Heat radiation part flatness</td>
<td></td>
<td></td>
<td>-50</td>
<td>-</td>
</tr>
</tbody>
</table>

Note 6: Plain washers (ISO 7089~7094) are recommended.

Measurement point of heat-sink flatness

Diagram showing measurement position.
2.2 Protective Functions and Operating Sequence

There are SC protection, UV protection and outputting LVIC temperature function in this series. The detailed information is described below.

2.2.1 Short Circuit Protection

This series apply the detection method of small sense current, which is divided at N-side IGBT, to SC protection. So high wattage type shunt resistor isn't necessary for SC protection. (Fig.2-5)

![SC protection circuit](image)

*) This wattage of sense resistor is described as a guide, so it is recommended to evaluate on your real system well.

SC protection works by inputting the potential, which is generated by sense current flowing into the sense resistor, to the CIN terminal. Table 2-7 describes specified sense resistance and minimum SC protection current in that case for each products.

When SC protection works, DIPIPM shuts down all N-side IGBTs hardly and outputs Fo signal. Its pulse width (t_{Fo}) is set by C_{Fo} capacitor (C_{Fo} = t_{Fo} x 9.1 x 10^{-6} [F]). To prevent malfunction, it is recommended to insert RC filter before inputting to CIN terminal and set the time constant to shut down within 2μs when short circuit occurs. (Time constant 1.5μ-2.0μs is recommended.) Also it is necessary to set the resistance of RC filter to ten or more times of the sense resistor R_{s}.(Hundred times is recommended.)

Table 2-7 SC protection trip level (Not connecting outer shunt resistors to NU,NV,NW terminals.)

<table>
<thead>
<tr>
<th>Type name</th>
<th>Rs</th>
<th>Min.</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSS75SA2F6</td>
<td>20.0Ω</td>
<td>127A</td>
</tr>
<tr>
<td>PSS50SA2F6</td>
<td>31.6Ω</td>
<td>85A</td>
</tr>
</tbody>
</table>

For sense resistor, its large fluctuation leads to large fluctuation of SC trip level. So it is necessary to select small variation and good temperature characteristic type (within +/-1% is recommended). Wattage of the sense resistor can be estimated in view of the fact that the maximum split ratio between the main and sense currents is about 4000:1. (In this case maximum sense current flows.)
The estimation example for PSS75SA2F6 is described as below.

**[Estimation example]**

(1) Normal operation state
It is assumed that the maximum main current for normal operation is 75A (rated current, for keeping a margin) and the sense resistance is 20.0Ω.

In this case, the maximum sense current flows through the sense resistor is calculated as below.

\[ I = \frac{75A}{4000} = 18.8mA \]

And the loss at the sense resistor is

\[ P = I^2 \cdot R \cdot t = (18.8mA)^2 \cdot 20.0\Omega = 7.0mW \]

(2) Short circuit state
When short circuit occurs, its current depends on the condition, but up to IGBT saturation current (about 10 times of the rated current =350A) flows. So the sense current is

\[ I = \frac{750A}{4000} = 187.5mA \]

But this current shut down within 2μs by SC protection. And the average loss at the sense resistor is

\[ P = I^2 \cdot R \cdot t = (187.5mA)^2 \cdot 20.0\Omega \cdot 2\mu s / 1s = 0.0014mW \]

And drop voltage of this sense resistor is

\[ V = 187.5mA \cdot 20.0\Omega = 3.8V \]

As explained above, over 0.03W wattage resistor will be suitable, but it is necessary to confirm on your real system finally.

**[Remarks]**

It takes more time (Table 2-8) from inputting over threshold voltage to CIN terminal to shutting down IGBTs. (Because of IC’s transfer delay)

Table 2-8 Internal time delay of IC

<table>
<thead>
<tr>
<th>Item</th>
<th>typ</th>
<th>max</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC transfer delay time</td>
<td>0.5</td>
<td>1.0</td>
</tr>
</tbody>
</table>

Therefore, the total delay time from short circuit occurring to shutting down IGBTs is the sum of the delay by the outer RC filter and this IC delay.

**[SC protection (N-side only)]**

a1. Normal operation: IGBT ON and outputs current.
a2. Short circuit current detection (SC trigger) (It is recommended to set RC time constant 1.5~2.0μs so that IGBT shut down within 2.0μs when SC.)
a3. All N-side IGBTs’ gates are hard interrupted.
a4. All N-side IGBTs turn OFF.
a5. Fo outputs with a fixed pulse width determined by the external capacitance C_{FO}.
a7. Fo finishes output, but IGBTs don’t turn on until inputting next ON signal (L→H).

(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
a8. Normal operation: IGBT ON and outputs current.

![Fig.2-6 SC protection timing chart](image-url)
[About Short Circuit Protection by Sense IGBT]

This function aims to protect from Short Circuit like arm short or load short. If high accuracy of protection current level (e.g. protection for demagnetizing motor) is necessary, it is recommended to apply the method by detecting the voltage at outer shunt resistors into main current path. In that case, the current split ratio between main and sense currents varies, thus minimum SC protection trip level changes from the value in Table 2-7. Therefore, adjustment of the sense resistance will be needed. The example of minimum SC trip level with outer shunt resistor is described in Table 2-9 (PSS75SA2F6, at sense resistance 20.0Ω). Please contact us about selecting sense resistance in the case of inserting outer shunt resistors.

<table>
<thead>
<tr>
<th>Outer shunt resistance</th>
<th>Minimum SC trip level</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nothing</td>
<td>127A</td>
</tr>
<tr>
<td>3mΩ</td>
<td>100A</td>
</tr>
</tbody>
</table>

It is recommended to set outer shunt resistance to the value as shown in Table 2-10 or less because too large shunt resistance causes decrease of IGBT saturation current by decreasing gate voltage at large current. (Large current makes large voltage drop at shunt resistor.) For shunt resistor, select low parasitic inductance resistor like surface mounted device type and pattern the wiring from the N-side emitter (NU, NV, NW) terminals as short as possible because of reducing surge by shutdown at large short circuit current.

<table>
<thead>
<tr>
<th>Type name</th>
<th>Rs</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSS75SA2F6</td>
<td>5mΩ</td>
</tr>
<tr>
<td>PSS50SA2F6</td>
<td>7mΩ</td>
</tr>
</tbody>
</table>

As a method that combines short circuit and over current protection function, there is a method which doesn't use sense resistor too. It is the same method as former DIIPM Ver.3 and the example of protection circuit is described in Fig.2-7.

The SC protection trip level is needed to set to double the rated current or less. And it is recommended to set the reference voltage of comparators to about 0.5V and select the shunt resistance in order that the SC trip level becomes double the rated current or less. (e.g. In the case that the protection level is set to double the rated current for PSS75SA2F6, R=0.5V/150A=3.3mΩ or more)

When this protection method is applied, the rated sense resistor Rs should be connected between Vsc terminal and GND for protecting from surge too. (Don't leave it open.)
Note:
- It is necessary to set the time constant $R_C$ of external comparator input so that IGBT can stop within 2μs when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on. If additional RC filter is inserted into OR output, it is necessary to consider its delay too.
- The threshold voltage $V_{ref}$ is recommended to set about 0.5V.
- Select the shunt resistance so that SC trip-level is less than double the rated current.
- To avoid malfunction, the wiring A, B, C should be as short as possible.
- The point D at which the wiring to comparator is divided should be near the terminal of shunt resistor.
- OR output high level should be over 1V at all temperature range.
2.2.2 Control Supply UV Protection

The UV protection is designed for preventing unexpected operating behavior as described in Table 2-11. Both P-side and N-side have UV protecting function. However, fault signal (Fo) output only corresponds to N-side UV protection. Fo output continuously during UV state.

In addition, there is a noise filter (typ. 10μs) integrated in the UV protection circuit to prevent instantaneous UV erroneous trip. Therefore, the control signals are still transferred in the initial 10μs after UV happened.

<table>
<thead>
<tr>
<th>Control supply voltage</th>
<th>Operating behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-4V (P, N)</td>
<td>Equivalent to zero power supply. UV function is inactive, no Fo output. Normally IGBT does not work. But, external noise may cause DIPIPM malfunction (turns ON), so DC-link voltage need to turn on after control supply turning on. (Avoid inputting ON-sIGNALS to DIPIPM before the control supply coming up to 13.5V)</td>
</tr>
<tr>
<td>4-UV trip level (P, N)</td>
<td>UV function becomes active and output Fo (N-side only). Even if control signals are applied, IGBT does not work UV trip level-13.5V(N),13.0V(P) IGBT can work. However, conducting loss and switching loss will increase, and result extra temperature rise at this state.</td>
</tr>
<tr>
<td>13.5-16.5V (N), 13.0-18.5V (P)</td>
<td>Recommended conditions. (Normal operation)</td>
</tr>
<tr>
<td>16.5-20V (N),18.5-20V (P)</td>
<td>IGBT works. However, switching speed becomes fast and saturation current becomes large at this state, increasing SC broken risk.</td>
</tr>
<tr>
<td>20V- (P, N)</td>
<td>Over maximum voltage rating. The control circuit will be destroyed.</td>
</tr>
</tbody>
</table>

Ripple Voltage Limitation of Control Supply

If high frequency precipitous noise is superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem happens, line ripple voltage should meet the following specifications:

\[ \frac{dV}{dt} \leq \pm 1V/\mu s, \quad V_{\text{ripple}} \leq 2V_{p-p} \]
N-side UV Protection Sequence
a1. Control supply voltage $V_D$ exceeds under voltage reset level ($UV_{Dr}$), but IGBT turns ON when inputting next ON signal ($L \rightarrow H$). (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
a2. Normal operation: IGBT turn on and carry current.
a3. $V_D$ level drops to under voltage trip level. ($UV_{Dr}$).
a4. All N-side IGRTs turn OFF in spite of control input condition.
a5. Fo outputs for the period determined by the capacitance $C_{FO}$, but output is extended during $V_D$ keeps below $UV_{Dr}$.
a6. $V_D$ level reaches $UV_{Dr}$.
a7. Normal operation: IGBT ON and carry current.

![Fig.2-8 Timing chart of N-side UV protection](image)

P-side UV Protection Sequence
b1. Control supply voltage $V_{DB}$ rises. After the voltage reaches under voltage reset level $UV_{DBr}$, IGBT can turn on when inputting next ON signal ($L \rightarrow H$).
b2. Normal operation: IGBT ON and outputs current.
b3. $V_{DB}$ level drops to under voltage trip level ($UV_{DBt}$).
b4. IGBT of corresponding phase only turns OFF in spite of control input signal level, but there is no Fo signal output.
b5. $V_{DB}$ level reaches $UV_{DBr}$.

![Fig.2-9 Timing Chart of P-side UV protection](image)
2.2.3 Temperature Output Function

This function measures the temperature of control LVIC by built in temperature detecting circuit on LVIC. The heat generated at IGBT and FWDi transfers to LVIC through mold package and inner and outer heat sink. So that LVIC temperature cannot respond to rapid temperature change of power chips effectively. (e.g. motor lock, short current) It is recommended to use this function for protecting from excessive temperature rise by such cooling system down and continuance of overload operation. (Replacement from the thermistor which has been set on outer heat sink currently)

Also DIPIPM cannot shutdown IGBT and output fault signal automatically when temperature rises excessively. When temperature exceeds the defined protect level, controller (MCU) should stop the DIPIPM.

(1) $V_{OT}$ terminal circuit and outer additional circuit

$V_{OT}$ output circuit, which is described in Fig.2-10, is the output of OP amplifier circuit. The current capability of $V_{OT}$ output is described as Table 2-12. Refer Fig.2-14 about output characteristics.

<table>
<thead>
<tr>
<th>Source</th>
<th>Sink</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.7mA</td>
<td>0.1mA</td>
</tr>
</tbody>
</table>

Source : Current flow from $V_{OT}$ to outside.
Sink : Current flow from outside to $V_{OT}$.

Table 2-12 Output capability

(Tc=-30°C ~125°C)

- **In the case of detecting lower temperature than room temperature**

It is recommended to insert 5.1kΩ pull down resistor for getting linear output characteristics at lower temperature than room temperature. When the pull down resistor is inserted between $V_{OT}$ and $V_{NC}$(control GND), the extra current calculated by $V_{OT}$ output voltage / pull down resistance flows as LVIC circuit current continuously. In the case of only using $V_{OT}$ for detecting higher temperature than room temperature, it isn't necessary to insert the pull down resistor.
In the case of using with low voltage controller (MCU)

In the case that $V_{OT}$ output will be input to a low voltage controller (e.g. 3.3V MCU), $V_{OT}$ output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and this output for preventing over voltage.

![Fig.2-12 $V_{OT}$ output circuit in the case of using with low voltage controller](image)

And if it is needed to set the trip level of $V_{OT}$ output to the control supply voltage (e.g. 3.3V) or more, there is the method of dividing the $V_{OT}$ output by resistance voltage divider circuit and then inputting to A/D converter on MCU (Fig.2-13). In that case, sum of the resistances of divider circuit should be 5.1kΩ. About the necessity of clamp diode, we consider that the divided output will not exceed the supply voltage of controller generally, so it will be unnecessary to insert the clamp diode. But it should be judged by the divided output level finally.

![Fig.2-13 $V_{OT}$ output circuit in the case with high protection level](image)
(2) $V_{OT}$ output characteristics

The characteristics of $V_{OT}$ output vs. LVIC temperature is described as Fig.2-14.

The heat of power chips transfers to LVIC through the heat sink and package, so the relationship between LVIC temperature: $T_{ic}$ ($=V_{OT}$ output), case temperature: $T_c$ (under the chip defined on datasheet), and junction temperature: $T_j$ depends on the system cooling condition, heat sink, control strategy, etc.

This relationship may be different due to the cooling conditions. So when setting the threshold temperature for protection, it is necessary to get the relationship between them on your real system. And when setting threshold temperature $T_{ic}$, it is important to consider the protection temperature assures; $T_c \leq 125^\circ C$ and $T_j \leq 150^\circ C$. 

Fig.2-14 $V_{OT}$ output vs. LVIC temperature

(These minimum and maximum curves are based on theoretical designed value excluding LVIC temperature=75°C limits.)
(3) How to use V\text{OT} output

As mentioned above, the heat of power chips transfers to LVIC through the package and heat sink, and the relationship between LVIC temperature: Tic(=V\text{OT} output), case temperature: Tc(measuring point is defined on the datasheet), and junction temperature: Tj depend on the system cooling condition, heat sink, control strategy, etc.

For example, the evaluation result about the relationship between IGBT loss and these temperature is described as Fig.2-15. This relationship may be different due to the cooling conditions. So when setting the threshold temperature for protection, it is necessary to get the relationship between them on your real system and consider the protection temperature keeps Tj \leq 150^\circ C.

![Diagram](image)

**Fig.2-15 IGBT loss vs. Tj, Tc, Tic(Typical) (Ta=80°C)**

Procedure about setting the protection level by using Fig.2-15 is described as below.

| Table 2-13 Procedure for setting protection level |
|---------------------------------|-----------------|
| Procedure | Setting value example |
| 1) Set the protection Tj temperature | Set Tj to 130°C as protection level. |
| 2) Get LVIC temperature Tic that matches to above Tj of the protection level from the relationship of Tj-Tic in Fig.2-16. | Tic=87.5°C (at Tj=130°C) |
| 3) Get V\text{OT} value from the V\text{OT} output characteristics in Fig.2-17 and the Tic value which was obtained at 2). | V\text{OT}=2.70V (at Tic=87.5°C) is decided as the protection level. |

As above procedure, the setting value for V\text{OT} output is decided to 2.70V. But V\text{OT} output has some data spread, so it is important to confirm whether the protection temperature fluctuation of Tj is not Tj>150°C due to the data spread of V\text{OT} output. Procedure about the confirmation of temperature fluctuation is described in Table 2-14.

| Table 2-14 Procedure for confirmation of temperature fluctuation |
|---------------------------------|-----------------|
| Procedure | Confirmation example |
| 4) Confirm the region of Tic fluctuation at above V\text{OT} from Fig.2-17. | Tic=82°C~94°C (at V\text{OT}=2.70V) |
| 5) Confirm the region of Tj fluctuation at above region of Tic from Fig.2-16. | Tj=106°C~147°C (\leq 150°C, No problem)  
In this case, fluctuation of Tc is Tc=90°C~111°C |
The relationship between Tic, Tc(measuring) and Tj(calculated by loss) depends on the system cooling condition and control strategy, and so on. So please evaluate about these temperature relationship on your real system when considering the protection level.

If necessary, it is available to prepare the sample with the individual data of V_{OT} vs. LVIC temperature.
2.3 Package Outlines

2.3.1 Outline Drawing

Fig.2-18 Outline drawing
2.3.2 Power Chip Position

Fig.2-19 indicates the center position of the each power chips. (This figure is the view from laser marked side.)

![Power chip position diagram](image)

2.3.3 Marking Position

The laser marking specification is described in Fig.2-20. Company name, Country of origin, Type name, Lot number, and 2D code are marked in the upper side of module.

![Laser marking view](image)

The Lot number indicates production year, month, running number and country of origin. The detailed is described as below.

(Example) 05 AA1

- Running number
- Product month (however O: October, N: November, D: December)
- Last figure of Product year (e.g. 2020)
2.3.4 Terminal Description

<table>
<thead>
<tr>
<th>No.</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>U_P</td>
<td>U-phase P-side control input terminal</td>
</tr>
<tr>
<td>3</td>
<td>V_P1</td>
<td>U-phase P-side control supply positive terminal</td>
</tr>
<tr>
<td>4</td>
<td>V_PFB</td>
<td>U-phase P-side drive supply positive terminal</td>
</tr>
<tr>
<td>6</td>
<td>V_PFS</td>
<td>U-phase P-side drive supply GND terminal</td>
</tr>
<tr>
<td>7</td>
<td>V_P</td>
<td>V-phase P-side control input terminal</td>
</tr>
<tr>
<td>9</td>
<td>V_P1</td>
<td>V-phase P-side control supply positive terminal</td>
</tr>
<tr>
<td>10</td>
<td>V_VF</td>
<td>V-phase P-side drive supply positive terminal</td>
</tr>
<tr>
<td>12</td>
<td>V_VF</td>
<td>V-phase P-side drive supply GND terminal</td>
</tr>
<tr>
<td>13</td>
<td>W_P</td>
<td>W-phase P-side control input terminal</td>
</tr>
<tr>
<td>14</td>
<td>V_P1</td>
<td>W-phase P-side control supply positive terminal</td>
</tr>
<tr>
<td>15</td>
<td>V_PC</td>
<td>P-side control supply GND terminal</td>
</tr>
<tr>
<td>16</td>
<td>V_WFB</td>
<td>W-phase P-side drive supply positive terminal</td>
</tr>
<tr>
<td>18</td>
<td>V_WFS</td>
<td>W-phase P-side drive supply GND terminal</td>
</tr>
<tr>
<td>19</td>
<td>V_SC</td>
<td>Sense current detecting terminal</td>
</tr>
<tr>
<td>21</td>
<td>V_N1</td>
<td>N-side control supply positive terminal</td>
</tr>
<tr>
<td>22</td>
<td>V_NC</td>
<td>N-side control supply GND terminal</td>
</tr>
<tr>
<td>23</td>
<td>V_OT</td>
<td>LVIC temperature output terminal</td>
</tr>
<tr>
<td>24</td>
<td>CIN</td>
<td>SC trip voltage detect terminal</td>
</tr>
<tr>
<td>25</td>
<td>CFO</td>
<td>Fault pulse output width set terminal</td>
</tr>
<tr>
<td>26</td>
<td>F_O</td>
<td>Fault signal output terminal</td>
</tr>
<tr>
<td>27</td>
<td>U_N</td>
<td>U-phase N-side control input terminal</td>
</tr>
<tr>
<td>28</td>
<td>V_N</td>
<td>V-phase N-side control input terminal</td>
</tr>
<tr>
<td>29</td>
<td>W_N</td>
<td>W-phase N-side control input terminal</td>
</tr>
<tr>
<td>34</td>
<td>NW</td>
<td>W-phase N-side IGBT emitter terminal</td>
</tr>
<tr>
<td>35</td>
<td>NV</td>
<td>V-phase N-side IGBT emitter terminal</td>
</tr>
<tr>
<td>36</td>
<td>NU</td>
<td>U-phase N-side IGBT emitter terminal</td>
</tr>
<tr>
<td>37</td>
<td>W</td>
<td>W-phase output terminal</td>
</tr>
<tr>
<td>38</td>
<td>V</td>
<td>V-phase output terminal</td>
</tr>
<tr>
<td>39</td>
<td>U</td>
<td>U-phase output terminal</td>
</tr>
<tr>
<td>40</td>
<td>P</td>
<td>Inverter DC-link positive terminal</td>
</tr>
</tbody>
</table>
Table 2-16 Detailed description of input and output terminals

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-side drive supply positive terminal</td>
<td>$V_{UFB}$- $V_{UFS}$</td>
<td>Drive supply terminals for P-side IGBTs.</td>
</tr>
<tr>
<td>P-side drive supply GND terminal</td>
<td>$V_{WFB}$- $V_{WFS}$</td>
<td>Abnormal operation might happen if the $V_D$ supply is not aptly stabilized or has insufficient current capability. In order to prevent malfunction caused by such instability as well as noise and ripple in supply voltage, a bypass capacitor with favorable frequency and temperature characteristics should be mounted very closely to each pair of these terminals.</td>
</tr>
<tr>
<td>P-side control supply terminal</td>
<td>$V_{PI}$</td>
<td>Inserting a Zener diode (24V/1W) between each pair of control supply terminals is helpful to prevent control IC from surge destruction.</td>
</tr>
<tr>
<td>N-side control supply terminal</td>
<td>$V_{NI}$</td>
<td>In order to prevent malfunction caused by noise and ripple in the supply voltage, a bypass capacitor with favorable frequency characteristics should be mounted very closely to these terminals.</td>
</tr>
<tr>
<td>N-side control GND terminal</td>
<td>$V_{PC}$</td>
<td>Carefully design the supply so that the voltage ripple caused by noise or by system operation is within the specified minimum limitation.</td>
</tr>
<tr>
<td>Control input terminal</td>
<td>$U_P, V_P, W_P$</td>
<td>It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.</td>
</tr>
<tr>
<td>$U_N, V_N, W_N$</td>
<td></td>
<td>Ensure that line current of the power circuit does not flow through this terminal in order to avoid noise influences.</td>
</tr>
<tr>
<td>Sense current detect terminal</td>
<td>$V_{SC}$</td>
<td>The sense current split at N-side IGBT flows out from this terminal. For SC protection, connect predefined resistor here.</td>
</tr>
<tr>
<td>Short-circuit trip voltage detecting terminal</td>
<td>$CIN$</td>
<td>The sense current split at N-side IGBT flows out from this terminal. For SC protection, connect predefined resistor here.</td>
</tr>
<tr>
<td>Fault signal output terminal</td>
<td>$F_O$</td>
<td>The terminal is for setting the fault pulse output width.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>An external capacitor should be connected between this terminal and $V_{NC}$.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>When 22nF capacitor is connected, then the $F_O$ pulse width becomes 2.4ms.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_{FO} = 10 \times 9.1 \times 10^{-6}$ (F)</td>
</tr>
<tr>
<td>Fault pulse output width setting terminal</td>
<td>$CFO$</td>
<td>The terminal is for setting the fault pulse output width.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>An external capacitor should be connected between this terminal and $V_{NC}$.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>When 22nF capacitor is connected, then the $F_O$ pulse width becomes 2.4ms.</td>
</tr>
<tr>
<td>Temperature output terminal</td>
<td>$V_{OT}$</td>
<td>LVIC temperature is output by analog signal. It is output of OP amplifier internally.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>It is recommended to connect 5.1kΩ pulldown resistor if output linearity is necessary under room temperature.</td>
</tr>
<tr>
<td>Inverter DC-link positive terminal</td>
<td>$P$</td>
<td>DC-link positive power supply terminal.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Internally connected to the collectors of all P-side IGBTs.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>To suppress surge voltage caused by DC-link wiring or PCB pattern inductance, smoothing capacitor should be inserted very closely to the P and N terminal. It is also effective to add small film capacitor with good frequency characteristics.</td>
</tr>
<tr>
<td>Inverter DC-link negative terminal</td>
<td>$NU, NV, NW$</td>
<td>Open emitter terminal of each N-side IGBT</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If usage of common emitter is needed, connect these terminals together at the point as close from the package as possible.</td>
</tr>
<tr>
<td>Inverter output terminal</td>
<td>$U, V, W$</td>
<td>Inverter output terminals for connection to inverter load (e.g. AC motor).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Each terminal is internally connected to the intermediate point of the corresponding IGBT half bridge arm.</td>
</tr>
</tbody>
</table>

Note: Use oscilloscope to check voltage waveform of each power supply terminals and P&N terminals, the time division of OSC should be set to about 1μs/div. Please ensure the voltage (including surge) not exceed the specified limitation.
2.4 Mounting Method

This section shows the electric spacing and mounting precautions.

2.4.1 Electric Spacing

The electric spacing specification is shown in Table 2-17

<table>
<thead>
<tr>
<th>Clearance (mm)</th>
<th>Creepage (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Between live power terminals with high potential</td>
<td>7.1</td>
</tr>
<tr>
<td>Between live control terminals with high potential</td>
<td>3.1</td>
</tr>
<tr>
<td>Between terminals and heat sink</td>
<td>3.7</td>
</tr>
</tbody>
</table>

2.4.2 Mounting Method and Precautions

When installing the module to the heat sink, excessive or uneven fastening force might apply stress to inside chips. Then it will lead to a broken or degradation of the chips or insulation structure. The recommended fastening procedure is shown in Fig.2-21. When fastening, it is necessary to use the torque wrench and fasten up to the specified torque. And pay attention to the foreign particle on the contact surface between the module and the heat sink. Even if the fixing of heatsink was done by proper procedure and condition, there is a possibility of damaging the package because of tightening by unexpected excessive torque or tucking particle. For ensuring safety it is recommended to conduct the confirmation test(e.g. insulation inspection) on the final product after fixing the DIPIPM with the heatsink.

Table 2-18 Mounting torque and heat sink flatness specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mounting torque</td>
<td>Recommended 1.18N·m, Screw : M4</td>
<td>0.98</td>
<td>1.18</td>
<td>1.47</td>
<td>N·m</td>
</tr>
<tr>
<td>Flatness of outer heat sink</td>
<td>Refer Fig.2-22</td>
<td>-50</td>
<td>-</td>
<td>+100</td>
<td>μm</td>
</tr>
</tbody>
</table>

Fig.2-21 Recommended screw fastening order

(1) → (2)

Temporary fastening
(1) → (2)

Permanent fastening
(1) → (2)

Note: Generally, the temporary fastening torque is set to 20-30% of the maximum torque rating. Not care the order of fastening (1) or (2), but need to fasten alternately.

Fig.2-22 Measurement point of heat sink flatness

In order to get effective heat dissipation, it is necessary to keep the contact area as large as possible to minimize the contact thermal resistance. Regarding the heat sink flatness (warp, concavity and convexity) on the module installation surface, the surface finishing-treatment should be within Rz12. Evenly apply thermally conductive grease with 100μ-200μm thickness over the contact surface between the module and the heat sink, which is also useful for preventing corrosion. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.2K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m·k). When
applying grease and fixing heat sink, pay attention not to take air into grease. It might lead to make contact thermal resistance worse or loosen fixing in operation.

Pay attention to the selection of thermal conductive grease. The grease thickness after fixing the heatsink may increase due to the properties of the grease (contained filler diameter, viscosity, amount of application and so on). And it may cause increase of contact thermal resistance or package crack. Please contact thermal conductive grease manufacturer for its detailed characteristics.

2.4.3 Soldering Conditions

The recommended soldering condition is mentioned as below.
(Note: The reflow soldering cannot be recommended for DIPIPM.)

(1) Flow (wave) Soldering
DIPIPM is tested on the condition described in Table 2-19 about the soldering thermosability, so the recommended conditions for flow (wave) soldering are soldering temperature is up to 265°C and the immersion time is within 11s. However, the condition might need some adjustment based on flow condition of solder, the speed of the conveyer, and the land pattern and the through hole shape on the PCB, etc.

It is necessary to confirm whether it is appropriate or not for your real PCB finally.

Table 2-19 Reliability test specification

<table>
<thead>
<tr>
<th>Item</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Soldering Thermosability</td>
<td>260±5°C, 10±1s</td>
</tr>
</tbody>
</table>

(2) Hand soldering
Since the temperature impressed upon the DIPIPM may changes based on the soldering iron types (wattages, shape of soldering tip, etc.) and the land pattern on PCB, we cannot suggest the recommended temperature condition for hand soldering.

As a general requirement of the temperature profile for hand soldering, the temperature of the root of the DIPIPM terminal should be kept lower than 150°C for considering glass transition temperature (Tg) of the package molding resin and the thermal withstand capability of internal chips. Therefore, it is necessary to check the DIPIPM terminal root temperature, solderability and so on in your real PCB, when configure the soldering temperature profile. (It is recommended to set the soldering time as short as possible.)

For reference, the evaluation example of hand soldering with 50W soldering iron is described as below.

[Evaluation method]

a. Sample: Large DIPIPM Ver.6
b. Evaluation procedure
   - Put the soldering tip of 50W iron (temperature set to 400°C) on the terminal within 1mm from the toe. (The lowest heat capacity terminal (=control terminal) is selected.)
   - Measure the temperature rise of the terminal root part by the thermocouple installed on the terminal root.

[NOTE] For soldering iron, it is recommended to select one for semiconductor soldering (12~24V low voltage type, and the earthed iron tip) and with temperature adjustment function.
CHAPTER 3 SYSTEM APPLICATION HIGHLIGHT

3.1 Application Guidance
This chapter states usage and interface circuit design hints.

3.1.1 System Connection

C1: Electrolytic type with good temperature and frequency characteristics.
Note: the capacitance also depends on the PWM control strategy of the application system
C2: 0.5μ-2μF ceramic capacitor with good temperature, frequency and DC bias characteristics
C3: 0.1μ-0.2μF Film capacitor (for snubber)
D1: Zener diode 24V/1W for surge absorber

Fig. 3-1 Application System block diagram
3.1.2 Interface Circuit (Direct Coupling Interface example) 

Fig.3-2 shows a typical application circuit of connecting with MCU or DSP directly.

**Note**

1. If control GND and power GND are patterned by common wiring, it may cause malfunction by fluctuation of power GND level. It is recommended to connect control GND and power GND at only a N1 point at which NU, NV, NW are connected to power GND line.

2. It is recommended to insert a Zener diode D1 (24V/1W) between each pair of control supply terminals to prevent surge destruction.

3. To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally inserting a 0.1μ~0.22μF snubber capacitor C3 between the P-N1 terminals is recommended.

4. R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp -compensated type. The time constant R1C4 should be set so that SC current is shut down within 2μs. (1.5μs~2μs is general value.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is recommended. If R1 is too small, it may leads to delay of protection. So R1 should be min. 10 times larger resistance than Rs. (100 times is recommended.)

5. To prevent erroneous operation, the wiring of A, B, C should be as short as possible.

6. For sense resistor, the variation within 1%(including temperature characteristics), low inductance type is recommended. And the over 0.03W is recommended, but it is necessary to evaluate in your real system finally.

7. To prevent erroneous SC protection, the wiring from Vsc terminal to CIN filter should be divided at the point D that is close to the terminal of sense resistor. And the wiring should be patterned as short as possible.

8. All capacitors should be mounted as close to the terminals of the DIPIPM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2: 0.01μ~2.0μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.) Input drive is High-active type. There is a min. 3.3kΩ pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. And it is recommended to insert RC filter (e.g. R3=100Ω and C5=1000pF) and confirm the input signal level to meet the turn-on and turn-off threshold voltage. Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.

9. Error signal output width (tFo) can be set by the capacitor connected to C0 terminal. C0 typ.) \( = I_{fo} \times 9.1 \times 10^{-6} \) (F)

10. If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause erroneous operation. To avoid such problem, voltage ripple of control supply line should meet dV/dt ≤+/-1V/μs, Vripples2Vp-p.

11. For DIPIPM, it isn’t recommended to drive same load by parallel connection with other phase IGBT or other DIPIPM.
3.1.3 Interface Circuit (Opto-coupler Isolated Interface)

Fig.3-3 Interface circuit example with opto-coupler

Note:

(1) High speed (high CMR) opto-coupler is recommended.
(2) Set the current limiting resistance to make \( I_{FO} \) sink current \( I_{FO} \leq 5\text{mA} \) or less when the opto-coupler is driven by \( Fo \) output directly. To assure \( I_{FO} \leq 5\text{mA} \), it will be needed to pull up to 15V supply since \( Fo \) output may be max 4.75V (@\( I_{FO} \leq 5\text{mA}, 25^\circ C \)).
(3) To prevent malfunction, it is strongly recommended to insert RC filter (e.g. \( R3=100\Omega \) and \( C5=1000\text{pF} \)) and confirm the input signal level to meet turn-on and turn-off threshold voltage.
(4) About comparator circuit at \( V_{OT} \) output, it is recommended to design the input circuit with hysteresis because of preventing output chattering.
3.1.4 Circuits of Signal Input terminals and Fo Terminal

Input logic is high-active. A 3.3kΩ (min) pull-down resistor is built-in each input circuit of the DIPIPM as shown in Fig.3-4, so external pull-down resistor is not needed.

This series have same package as 1200V large DIPIPM Ver.4 series (PS22A7*) and 1200V large DIPIPM Ver.6 series (PSS**SA2FT), however, they have different input threshold voltage. When using same PCB between these series, it needs to give attention to the difference.

![Fig.3-4 Internal structure of control input terminals](image)

**Table 3-1 Input threshold voltage ratings (Tj=25°C)**

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turn-on threshold</td>
<td>Vth(on)</td>
<td>(U_{IP}, U_{WP}, U_{PC})</td>
<td>-</td>
<td>2.1</td>
<td>2.6</td>
<td>V</td>
</tr>
<tr>
<td>Turn-off threshold</td>
<td>Vth(off)</td>
<td>(U_{IN}, U_{WN}, U_{NC})</td>
<td>0.8</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
</tbody>
</table>

The wiring of each input should be patterned as short as possible and it is recommended to insert RC filter. There are limits for the minimum input pulse width in the DIPIPM. DIPIPM might make no response or delayed response, if the input pulse width (both on and off) is shorter than the specified value. (Refer Table 3-2)

![Fig.3-5 Control input connection in the case of direct connection with MCU](image)

Note: Design for input RC filter depends on the PWM control scheme used in the application and the wiring impedance of the printed circuit board. It is recommended to insert RC filter. (Time constant: over 100ns, e.g. 100Ω, 1000pF)

DIPIPM input signal interface integrates a 3.3kΩ (min.) pull-down resistor. Therefore, when using RC filter, be careful to satisfy the turn-on threshold voltage requirement.
Table 3-2 Allowable minimum input pulse width

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Type Name</th>
<th>Minimum value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>On signal</td>
<td>PWIN(on)</td>
<td>PSS50SA2F6</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PSS75SA2F6</td>
<td></td>
</tr>
<tr>
<td>Off signal</td>
<td>PWIN(off)</td>
<td>PSS50SA2F6</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PSS75SA2F6</td>
<td></td>
</tr>
</tbody>
</table>

- DIPIPM might not make response if the input signal pulse width is less than PWIN(on).
- DIPIPM might make no response or delayed response (P-side IGBT only) for input pulse width less than PWIN(off).
- Over rated collector current (Ic) operation, DIPIPM might make delayed response even if the input signal pulse width is more than PWIN(off).

Refer Fig.3-6 about delayed response.

![Diagram](image-url)

Fig.3-6 Delayed response with shorter input off (P-side only)
(2) Internal Circuit of Fo Terminal

Fo terminal is an open drain type. When Fo output is input into MCU (controller) directly, it is necessary to note the dependency of $V_{FO}$ on $I_{FO}$ ($V_{FO}=\text{max}0.95\text{V} @ I_{FO}=1\text{mA}, 25^\circ\text{C}$) and set pull up resistance so that Fo signal level fits to the input threshold voltage of MCU. In the case of pulling up to 5V supply, it is recommended to pull up by 10kΩ resistor.

When the opto-coupler is driven by Fo output directly, the maximum Fo sink current becomes 5mA or less. To assure $I_{FO}=5\text{mA}$, it will be needed to pull up to 15V supply since Fo output may be max 4.75V ($@ I_{FO}=5\text{mA}, 25^\circ\text{C}$).

If max 5mA coupler driving current is not enough, it is necessary to apply buffer circuit for increasing driving current.

Fig.3-7 shows the typical V-I characteristics of Fo terminal.

<table>
<thead>
<tr>
<th>Table 3-3 Electric characteristics of Fo terminal</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Item</strong></td>
</tr>
<tr>
<td>Fault output voltage</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

Fig.3-7 Fo terminal typical V-I characteristics ($V_D=15\text{V}, T_j=25^\circ\text{C}$)

3.1.5 Snubber Circuit

In order to prevent DIPIPM from the surge destruction, the wiring length between the smoothing capacitor and DIPIPM P-N terminals should be as short as possible. Also, a 0.1μ~0.22μF/630V snubber capacitor should be mounted to the position between P and the connect point of NU, NV and NW terminals as close as possible as Fig.3-8.
3.1.6 Influence of Wiring

Influence of pattern wiring around the sense resistor for SC protection and GND is shown below.

![Fig.3-9 External protection circuit](image)

(1) Influence of the part-A wiring

The part-A wiring affects SC protection level. SC protection works by judging the voltage of the CIN terminals. If part-A wiring is too long, extra surge voltage generated by the wiring inductance will lead to fluctuation of SC protection level. This wiring should be as short as possible for limiting the surge voltage.

(2) Influence of the part-B wiring pattern

RC filter is added to remove noise influence occurring on the sense resistor. Filter effect will dropdown and noise will easily superimpose on the wiring, if part-B wiring (=after filtering part) is too long. Please install the RC filter near CIN, VNC terminals as close as possible.

(3) Influence of the part-C wiring pattern

Part-C wiring pattern gives influence to all the items described above, maximally shorten the GND wiring is expected. If control GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point at which NU, NV, NW are connected to power GND line.
3.1.7 Precaution for Wiring on PCB

The case example of trouble due to PCB pattern

<table>
<thead>
<tr>
<th>Case example</th>
<th>Matter of trouble</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>The surge, generated by the wiring pattern and di/dt of noncontiguous big current flows to power GND, transfers to control GND pattern. It causes the control GND level fluctuation, so that the input signal based on the control GND fluctuates too. Finally the arm short occurs.</td>
</tr>
</tbody>
</table>
| 2            | Long wiring pattern has big parasitic inductance and generates high surge when switching. This surge causes the matter as below.  
- HVIC malfunction due to VS voltage (output terminal potential) dropping excessively.  
- LVIC surge destruction |
| 3            | IC surge destruction or malfunction occurs. |
| 4            | Cross talk noise might be transferred through the capacitance between these floating supply lines and input lines to DIPIPM. Then incorrect signals are input to DIPIPM input, and arm short (short circuit) might occur. |
3.1.8 SOA of DIPIPM

The following describes the SOA (Safety Operating Area) of DIPIPM.

- $V_{CES}$: Maximum rating of IGBT collector-emitter voltage
- $V_{CC}$: Supply voltage applied on P-N terminals
- $V_{CC(surge)}$: The total amount of $V_{CC}$ and the surge voltage generated by the wiring inductance and the DC-link capacitor.
- $V_{CC(Prot)}$: DC-link voltage that DIPIPM can protect itself.

In case of switching

$V_{CES}$ represents the maximum voltage rating (600V) of the IGBT. By subtracting the surge voltage (100V or less) generated by internal wiring inductance from $V_{CES}$ is $V_{CC(surge)}$, that is 500V. Furthermore, by subtracting the surge voltage (50V or less) generated by the wiring inductor between DIPIPM and DC-link capacitor from $V_{CC(surge)}$ derives $V_{CC}$, that is 450V.

In case of short-circuit

$V_{CES}$ represents the maximum voltage rating (600V) of the IGBT. By subtracting the surge voltage (100V or less) generated by internal wiring inductance from $V_{CES}$ is $V_{CC(surge)}$, that is, 500V. Furthermore, by subtracting the surge voltage (100V or less) generated by the wiring inductor between the DIPIPM and the electrolytic capacitor from $V_{CC(surge)}$ derives $V_{CC}$, that is, 400V.
3.1.9 SCSOA

Fig.3-13 and Fig.3-14 show the typical SCSOA performance curves.

Conditions: Vcc=400V, Tj=150°C at initial state, Vcc(surge)≤500V(surge included), non-repetitive, 2m load.

In the case of PSS50SA2F6 (50A rating) it means DIPIPM can shutdown maximum 490A(@V_D=16.5V) short circuit current safely if IGBT turn on period is within 4.0μs(typical).

Since the SCSOA operation area will vary with the control supply voltage, DC-link voltage, and etc, it is necessary to set time constant of RC filter with a margin.
3.1.10 Power Life Cycles

When DIPIPM is in operation, repetitive temperature variation will happen on the IGBT junctions (\(\Delta T_j\)). The amplitude and the times of the junction temperature variation affect the device lifetime.

Fig.3-15 shows the IGBT power cycle curve as a function of average junction temperature variation (\(\Delta T_j\)). (The curve is a regression curve based on 3 points of \(\Delta T_j=46, 88, 98\)K with regarding to failure rate of 0.1%, 1% and 10%. These data are obtained from the reliability test of intermittent conducting operation.)
3.2 Power Loss and Thermal Dissipation Calculation

3.2.1 Power Loss Simulation

For calculating power loss and temperature rising, the power loss simulator "Melcosim" is prepared in our WEB site. This simulator can make the calculation of inverter loss and temperature rise easy.

The 'Melcosim' can be downloaded from http://www.mitsubishielectric.com/semiconductors/

Simple expressions for calculating average power loss are given below:

- **Scope**
  The power loss calculation intends to provide users a way of selecting a matched power device for their VVVF inverter application. However, it is not expected to use for limit thermal dissipation design.

- **Assumptions**
  1. PWM controlled VVVF inverter with sinusoidal output;
  2. PWM signals are generated by the comparison of sine waveform and triangular waveform.
  3. Duty amplitude of PWM signals varies between \( \frac{1-D}{2} \sim \frac{1+D}{2} \) (%/100), (D: modulation depth).
  4. Output current various with Icp-sinx and it does not include ripple.
  5. Power factor of load output current is cos\( \theta \), ideal inductive load is used for switching.

- **Expressions Derivation**
  PWM signal duty is a function of phase angle \( x \) as \( \frac{1+D \times \sin x}{2} \) which is equivalent to the output voltage variation. From the power factor cos\( \theta \), the output current and its corresponding PWM duty at any phase angle \( x \) can be obtained as below:

  \[
  \text{Output current} = Icp \times \sin x
  \]
  \[
  \text{PWM Duty} = \frac{1 + D \times \sin(x + \theta)}{2}
  \]

  Then, \( V_{CE(sat)} \) and \( V_{EC} \) at the phase \( x \) can be calculated by using a linear approximation:

  \[
  V_{ce(sat)} = V_{ce(sat)}(@ Icp \times \sin x)
  \]
  \[
  V_{ec} = (-1) \times V_{ec}(@ Icp = Icp) \times \sin x
  \]

  Thus, the static loss of IGBT is given by:

  \[
  \frac{1}{2\pi} \int_{0}^{\pi} (Icp \times \sin x) \times V_{ce(sat)}(@ Icp \times \sin x) \times \frac{1 + D \sin(x + \theta)}{2} \cdot dx
  \]

  Similarly, the static loss of free-wheeling diode is given by:

  \[
  \frac{1}{2\pi} \int_{0}^{\pi} (-1) \times Icp \times \sin x)((-1) \times V_{ec}@ Icp \times \sin x) \times \frac{1 + D \sin(x + \theta)}{2} \cdot dx
  \]

  On the other hand, the dynamic loss of IGBT, which does not depend on PWM duty, is given by:

  \[
  \frac{1}{2\pi} \int_{0}^{\pi} (P_{sw(on)}(@ Icp \times \sin x) + P_{sw(off)}(@ Icp \times \sin x)) \times fc \cdot dx
  \]
FWDi recovery characteristics can be approximated by the ideal curve shown in Fig.3-16, and its dynamic loss can be calculated by the following expression:

\[
P_{SW} = \frac{I_{rr} \times V_{cc} \times t_{rr}}{4}
\]

Recovery occurs only in the half cycle of the output current, thus the dynamic loss is calculated by:

\[
\int_{\pi}^{2\pi} \frac{I_{rr}(@ I_{cp} \times \sin x) \times V_{cc} \times t_{rr}(@ I_{cp} \times \sin x) \times f_{c} \cdot dx}{4} \\
= \int_{\rho}^{2\pi} \frac{I_{rr}(@ I_{cp} \times \sin x) \times V_{cc} \times t_{rr}(@ I_{cp} \times \sin x) \times f_{c} \cdot dx}{8}
\]

- **Attention of applying the power loss simulation for inverter designs**
  - Divide the output current period into fine-steps and calculate the losses at each step based on the actual values of PWM duty, output current, \(V_{CE(sat)}\), \(V_{EC}\), and \(P_{sw}\) corresponding to the output current. The worst condition is most important.
  - PWM duty depends on the signal generating way.
  - The relationship between output current waveform or output current and PWM duty changes with the way of signal generating, load, and other various factors. Thus, calculation should be carried out on the basis of actual waveform data.
  - \(V_{CE(sat)}, V_{EC}\) and \(P_{sw(on, off)}\) should be the values at \(T_j=125^\circ C\).
3.2.2 Temperature Rise Considerations and Calculation Example

Fig.3-17 shows the typical characteristics of allowable motor rms current versus carrier frequency under the following inverter operating conditions based on power loss simulation results.

Conditions: $V_{CC}=300V$, $V_D=15V$, $V_{CE(sat)}=Typ.$, P.F=0.8, Switching loss=Typ., $T_j=125^\circ C$, $T_c=100^\circ C$, $R_{th(j-c)}=Max.$, 3-phase PWM modulation, 60Hz sine waveform output.

The inverter loss can be calculated by the free power loss simulation software will be uploaded on the Mitsubishi Electric web site. (URL: http://www.mitsubishielectric.com/semiconductors/)
3.3 Noise and ESD Withstand Capability

3.3.1 Evaluation Circuit of Noise Withstand Capability

DIPIPM have been confirmed to be with over +/-2.0kV noise withstand capability by the noise evaluation under the conditions shown in Fig.3-19. However, noise withstand capability greatly depends on the test environment, the wiring patterns of control substrate, parts layout, and other factors, an additional confirmation on prototype is necessary.

![Fig.3-19 Noise withstand capability evaluation circuit](image)

**Note:** C1: AC line common-mode filter 4700pF, PWM signals are input from microcomputer by using opto-couplers, 15V single power supply, Test is performed with IM

**Test conditions**

- \( V_{CC} = 300V, V_\text{D} = 15V, Ta = 25°C, \) no load
- Scheme of applying noise: From AC line (R, S, T), Period \( T = 16\text{ms} \), Pulse width \( tw = 0.05-1 \mu s \), input in random.

3.3.2 Countermeasures and Precautions

DIPIPM improves noise withstand capabilities by means of reducing parts quantity, lowering internal wiring parasitic inductance, and reducing leakage current. But when the noise affects on the control terminals of DIPIPM (due to no good wiring pattern on PCB), the short circuit or malfunction of SC protection may occur. In that case, the countermeasures are recommended.

![Fig.3-20 Example of countermeasures](image)
3.3.3 Static Electricity Withstand Capability

DIPIPM has been confirmed to be with typical +/-1kV or more withstand capability against static electricity from the following tests shown in Fig.3-21, 22. HBM method: C=100pF, R=1.5 kΩ.

![Surge test circuit example](image)

**Fig.3-21 Surge test circuit example**(VN1 terminal)  **Fig.3-22 Surge test circuit example**(VP1 terminal)
CHAPTER 4 Bootstrap Circuit Operation

4.1 Bootstrap Circuit Operation

For three phase inverter circuit driving, normally four isolated control supplies (three for P-side driving and one for N-side driving) are necessary. But using floating control supply with bootstrap circuit can reduce the number of isolated control supplies from four to one (N-side control supply).

Bootstrap circuit consists of a bootstrap diode (BSD), a bootstrap capacitor (BSC) and a current limiting resistor. It uses the BSC as a control supply for driving P-side IGBT. The BSC supplies gate charge when P-side IGBT turning ON and circuit current of logic circuit on P-side driving IC. (Fig.4-2) Since a capacitor is used as substitute for isolated supply, its supply capability is limited. This floating supply driving with bootstrap circuit is suitable for small supply current products like DIPIM.

Charge consumed by driving circuit is re-charged from N-side 15V control supply to BSC via current limiting resistor and BSD when voltage of output terminal (U, V or W) goes down to GND potential in inverter operation. But there is the possibility that enough charge doesn't perform due to the conditions such as switching sequence, capacitance of BSC, limiting resistance and so on. Deficient charge leads to low voltage of BSC and might work under voltage protection (UV). This situation makes the loss of P-side IGBT increase by low gate voltage or stop switching. So it is necessary to consider and evaluate enough for designing bootstrap circuit. For more detail information about driving by the bootstrap circuit, refer the DIPIM application note “Bootstrap Circuit Design Manual”.

The built-in BSD characteristics of this series and the circuit current characteristics in switching situation of P-side IGBT are described as below.

![Bootstrap Circuit Diagram](image1)

![Bootstrap Circuit Diagram](image2)
4.2 Bootstrap Supply Circuit Current at Switching State

Bootstrap supply circuit current $I_{DB}$ at steady state is maximum 0.55mA for this series. But at switching state, because gate charge and discharge are repeated by switching, the circuit current will exceed 0.55mA and increases proportional to carrier frequency. For reference, Fig.4-3 and Fig.4-4 show the circuit current $I_{DB}$ for P-side IGBT driving supply - carrier frequency $f_c$ typical characteristics for each products.

Conditions: $V_D=V_{DB}=15V$, $T_J=150^\circ C$, $V_{CC}=450V$

---

![Fig.4-3 $I_{DB}$ vs. Carrier frequency for PSS50SA2F6](image1)

![Fig.4-4 $I_{DB}$ vs. Carrier frequency for PSS75SA2F6](image2)
4.3 Note for designing the bootstrap circuit

When each device for bootstrap circuit is designed, it is necessary to consider various conditions such as temperature characteristics, change by lifetime, variation and so on. Note for designing these devices are listed as below. For more detail information about driving by the bootstrap circuit, refer the DIPIPM application note “Bootstrap Circuit Design Manual”

(1) Bootstrap capacitor
Electrolytic capacitors are used for BSC generally. And recently ceramic capacitors with large capacitance are also applied. But DC bias characteristic of the ceramic capacitor when applying DC voltage is considerably different from that of electrolytic capacitor. (Especially large capacitance type) Some differences of capacitance characteristics between electrolytic and ceramic capacitors are listed in Table 4-1.

<table>
<thead>
<tr>
<th>Temperature characteristics (Ta: -20 ~ 85°C)</th>
<th>Electrolytic capacitor</th>
<th>Ceramic capacitor (large capacitance type)</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Aluminum type:</td>
<td></td>
<td>Different due to temp. characteristics rank</td>
</tr>
<tr>
<td>Low temp.: -10% High temp: +10%</td>
<td></td>
<td>Low temp.: -5%~0%</td>
</tr>
<tr>
<td>• Conductive polymer aluminum solid type:</td>
<td></td>
<td>High temp.: -5%~10%</td>
</tr>
<tr>
<td>Low temp.: -5% High temp: +10%</td>
<td></td>
<td>(in the case of B,X5R,X7R ranks)</td>
</tr>
</tbody>
</table>

DC bias characteristic of electrolytic capacitor is not matter. But it is necessary to note ripple capability by repetitive charge and discharge, life time which is greatly affected by ambient temperature and so on. Above characteristics are just example data which are obtained from the WEB, please refer to the capacitor manufacturers about detailed characteristics.

(2) Bootstrap diode
This series integrate bootstrap diodes for P-side driving supply. This BSD incorporates current limiting resistor (typ. 20Ω). The $V_F$-$I_F$ characteristics (including voltage drop by built-in current limiting resistor) is shown in Fig.4-5 and Table 4-2.

![Fig.4-5 V_F-I_F curve for bootstrap Diode (The right figure is enlarged view)](image)

Table 4-2 Electric characteristics of built-in bootstrap diode

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bootstrap Di forward voltage</td>
<td>$V_F$</td>
<td>$I_F=10mA$ including voltage drop by limiting resistor</td>
<td>0.5</td>
<td>0.9</td>
<td>1.3</td>
<td>V</td>
</tr>
<tr>
<td>Built-in limiting resistance</td>
<td>$R$</td>
<td>Included in bootstrap Di</td>
<td>16</td>
<td>20</td>
<td>24</td>
<td>Ω</td>
</tr>
</tbody>
</table>
4.4 Initial charging in bootstrap circuit

In the case of applying bootstrap circuit, it is necessary to charge to the BSC initially because voltage of BSC is 0V at initial state or it may go down to the trip level of under voltage protection after long suspending period (even 1s). BSC charging is performed by turning on all N-side IGBT normally. When outer load (e.g. motor) is connected to the DIPIPM, BSC charging may be performed by turning on only one phase N-side IGBT since potential of all output terminals will go down to GND level through the wiring in the motor. But its charging efficiency might become lower due to some cause. (e.g. wiring resistance of motor)

There are mainly two procedures for BSC charging. One is performed by one long pulse, and another is conducted by multiple short pulses. Multi pulse method is used when there are some restriction like control supply capability and so on.

![Initial charging root](image)

Fig.4-6 Initial charging root

Initial charging needs to be performed until voltage of BSC exceeds recommended minimum supply voltage 13V. (It is recommended to charge as high as possible with consideration for voltage drop between the end of charging and start of inverter operation.)

After BSC was charged, it is recommended to input one ON pulse to the P-side input for reset of internal IC state before starting system. Input pulse width is needed to be longer than allowable minimum input pulse width PWIN(on). (e.g. 1.5μs)
CHAPTER 5 PACKAGE HANDLING

5.1 Packaging Specification

Spacers are inserted into the top and bottom of the box. If there is some space on top of the box, additional buffer materials are also inserted.

Fig.5-1 Packaging Specification

Quantities:
- 6pcs per 1 tube
- Tube Quantity: 5 × 6 = 30 pcs
- IPM Quantity: 30 × 6 = 180 pcs

Total amount in one box (max):
- Tube Quantity: 5 × 6 = 30 pcs
- IPM Quantity: 30 × 6 = 180 pcs

When it isn’t fully filled by tubes at top stage, cardboard spacers or empty tubes are inserted for filling the space of top stage.

Weight (max):
- About 46g per 1 pcs
- About 380g per 1 tube
- About 13kg per 1 box

Packaging box

Plastic Tube

DIPIM

5 columns

6 stages

Spacers are inserted into the top and bottom of the box. If there is some space on top of the box, additional buffer materials are also inserted.
## 5.2 Handling Precautions

<table>
<thead>
<tr>
<th>Cautions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Transportation</strong></td>
</tr>
<tr>
<td>- Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged.</td>
</tr>
<tr>
<td>- Throwing or dropping the packaging boxes might cause the devices to be damaged.</td>
</tr>
<tr>
<td>- Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.</td>
</tr>
<tr>
<td><strong>Storage</strong></td>
</tr>
<tr>
<td>- We recommend temperature and humidity in the ranges 5-35°C and 45-75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above.</td>
</tr>
<tr>
<td><strong>Long storage</strong></td>
</tr>
<tr>
<td>- When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior.</td>
</tr>
<tr>
<td><strong>Surroundings</strong></td>
</tr>
<tr>
<td>- Keep modules away from places where water (including dew condensation) or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems.</td>
</tr>
<tr>
<td><strong>Flame resistance</strong></td>
</tr>
<tr>
<td>- The epoxy resin of case material is flame-resistant type (UL standard 94V-0), but they are not noninflammable.</td>
</tr>
<tr>
<td><strong>Anti-electrostatic Measures</strong></td>
</tr>
<tr>
<td>- ICs and power chips with MOS gate structure are used for the DIPIPM power modules. Please keep the following notices to prevent modules from being damaged by static electricity.</td>
</tr>
<tr>
<td>(1) Precautions against the device destruction caused by the ESD</td>
</tr>
<tr>
<td>When the ESD of human bodies, packaging and etc. are applied to terminal, it may damage and destroy devices. The basis of anti-electrostatic is to inhibit generating static electricity possibly and quick dissipation of the charged electricity.</td>
</tr>
<tr>
<td>*Containers that charge static electricity easily should not be used for transit and for storage.</td>
</tr>
<tr>
<td>*Terminals should be always shorted with a carbon cloth or the like until just before using the module. Never touch terminals with bare hands.</td>
</tr>
<tr>
<td>*Should not be taking out DIPIPM from tubes until just before using DIPIPM and never touch terminals with bare hands.</td>
</tr>
<tr>
<td>*During assembly and after taking out DIPIPM from tubes, always earth the equipment and your body. It is recommended to cover the work bench and its surrounding floor with earthed conductive mats.</td>
</tr>
<tr>
<td>*When the terminals are open on the printed circuit board with mounted modules, the modules might be damaged by static electricity on the printed circuit board.</td>
</tr>
<tr>
<td>*If using a soldering iron, earth its tip.</td>
</tr>
<tr>
<td>(2) Notice when the control terminals are open</td>
</tr>
<tr>
<td>*When the control terminals are open, do not apply voltage between the collector and emitter. It might cause malfunction.</td>
</tr>
<tr>
<td>*Short the terminals before taking a module off.</td>
</tr>
<tr>
<td>Anti-overvoltage Measures</td>
</tr>
<tr>
<td>- Precautions for overvoltage destruction. It should be noted that overvoltage destruction of DIPIPM might be caused by applying surges to inner chips (power chips and ICs) when surges are impressed to DIPIPM package directly or indirectly via the circuit board by surge discharging due to mis-operation on the in-circuit inspection process (e.g. plug off the connector of test board before discharging its capacitor, imperfect contact of the connector, and so on).</td>
</tr>
</tbody>
</table>
## Revision Record

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Points</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>August 26, 2020</td>
<td>New</td>
</tr>
</tbody>
</table>
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