MITSUBISHI ELECTRIC

< DIPIPM >

Compact DIPIPM Series APPLICATION NOTE PSSxxSF1F6

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CHAPTER 1 INTRODUCTION

1.1 Features of Compact DIPIPM

Compact DIPIPM is an intelligent power module with transfer mold packages favorable for larger mass production. Power chips, drive and protection circuits are integrated in the module, which makes it easy for AC400-440V class low power motor inverter control. Compared to the conventional Mini DIPIPM Ver.7 series (20, 30, 50A / 600V) supporting an isolation withstand voltage of 2500 Vrms, an equivalent isolation withstand voltage is realized, and by applying RC-IGBTs to the power chips, the number of built-in chips is reduced, thereby achieving further package downsizing. Main features of this series are as below.

- *By applying RC-IGBTs, approximately a 50% reduction in package size is achieved compared with Mini DIPIPM.*
- *By applying a high heat-dissipation sheet, a rated current of 50 A equivalent to that of Mini DIPIPM is secured.*
- *The operating junction temperature range is up to 150°C, and the maximum junction temperature is 175°C, supporting instantaneous current conduction during overload operation.*
- *Continuous operation down to a lower temperature limit of −40°C is supported.*
- *Protection circuits equal to or greater than those of Mini DIPIPM series are incorporated, and an interlock function is newly added.*
- *A terminal-to-heatsink distance equivalent to that of Mini DIPIPM is secured.*

About detailed differences, please refer Section 1.5.
Fig.1-1-1 and Fig.1-1-2 show the outline and internal cross-section structure respectively.

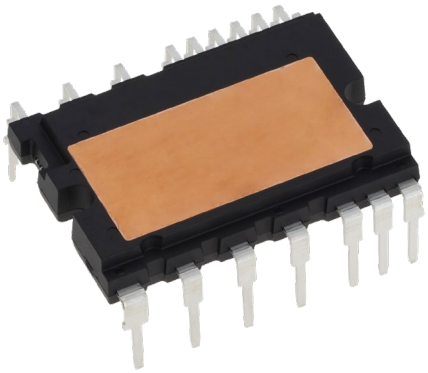


Fig.1-1-1 Package image

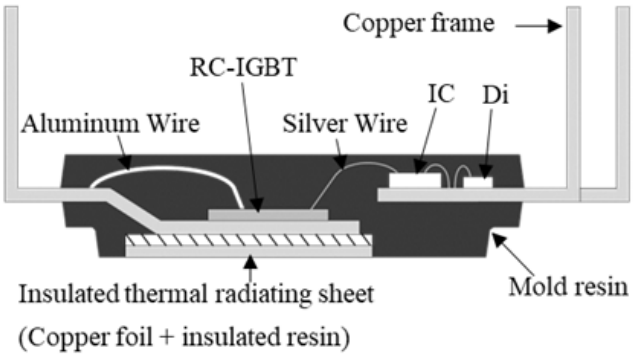


Fig.1-1-2 Internal cross-section structure

1.2 Functions

Compact DIPIPM has following functions. Its inner block diagram is described in Fig.1-2-1.

- For P-side IGBTs:
  - Drive circuit; high voltage level shift circuit.
  - Control supply under voltage (UV) lockout circuit (without fault signal output).
  - Built-in bootstrap diode (BSD) with current limiting resistor
- For N-side IGBTs:
  -Drive circuit.
  -Short circuit (SC) protection circuit (by inserting external shunt resistor into main current path)
  -Control supply under voltage (UV) lockout circuit (with fault signal output)
  -Outputting LVIC temperature by analog signal (No self over temperature protection)
- Fault Signal Output
  - Corresponding to N-side IGBT SC, N-side UV and OT protection.
- Arm short protection
  - Interlock function (IL)
- IGBT Drive Supply
  -Single DC15V power supply (in the case of using bootstrap method)
- Control Input Interface
  -Schmitt-triggered 3V, 5V input compatible, high active logic.
- UL recognized: UL1557 File E323585

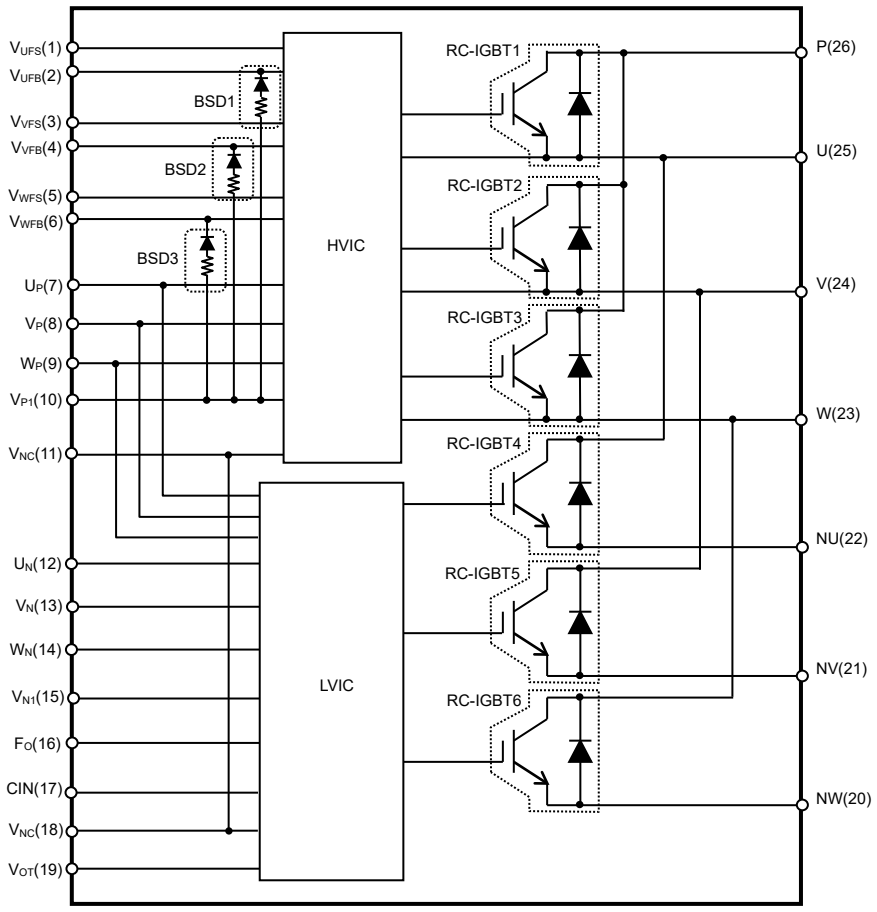


Fig.1-2-1 Inner block diagram

1.3 Target Applications

Motor drives for consumer and industrial applications

1.4 Product Line-up

Table 1-4-1 Compact DIPIPM Line-up

Type Name	Rated current	Motor Rating [1)]	Isolation Voltage
PSS30SF1F6	30A/600V	2.2kW	V_{iso} = 2500Vrms (Sine 60Hz, 1min All shorted pins-heat sink)
PSS50SF1F6	50A/600V	3.7kW	

1) The motor ratings are calculation results. It will depend on the conditions of operation.

1.5 The Differences between Compact DIPIPM and Mini DIPIPM Series

Compact DIPIPM has some differences against Mini DIPIPM series (PSSxxS71FT・PSSxxS73F6). Main differences are described in the following tables.

For more details and the other characteristics, please refer to the datasheet or application note for each product.

Table 1-5-1 Differences in specifications

Items	Symbol	PSSxxS71F6	PSSxxS73F6	PSSxxSF1F6	Ref.
		Mini DIPIPM with BSD	Mini DIPIPM Ver.7	Compact DIPIPM	
Junction temperature	T_j	-20~+150°C	-	-	-
Junction operating temperature	T_{jop}	-	-30~+150°C 1)	-40~+150°C 1)	-
Maximum junction temperature	T_{jmax}	-	Max. 175°C 1)	Max. 175°C 1)	-
Module case operation temperature	T_C	-20~+100℃	-30~+125°C 1)	-40~+125°C 1)	-
V_{OT} output 2) (LVIC temp. output)	V_{OT}	typ. 2.64V LVIC temp. =85°C	←	typ. 2.80V LVIC temp. =90°C	Section 2.2.3
Interlock function	IL	-	-	Built-in	Section 2.2.4

1) Compact DIPIPM series specifies the chip junction temperature by the junction operating temperature T_{jop} and the maximum junction temperature T_{jmax}. The maximum junction temperature rating of built-in power chips is 175°C(@Tc≤125°C). However, to ensure safe operation of DIPIPM, the average junction temperature should be limited to $T_{j(Ave)}$≤150°C (@Tc≤125°C).

2) V_{OT} function cannot shutdown by itself when LVIC temperature exceeds protection level. So, it is necessary for system controllers to monitor this V_{OT} output and shutdown when the temperature reached the protection level.

<About max.175°C guarantee>

Maximum junction temperature T_{jmax}=175°C is set assuming a short-term temperature rise (e.g. motor lock). When designing your system for its continual operation, the average junction temperature should be set less than $T_{j(Ave)}$≤150°C.

Please also note that repeated temperature changes affect the lifetime.

Table 1-5-2 Differences of specifications and recommended operating conditions

Items	Symbol	PSSxxS71F6	PSSxxS73F6	PSSxxSF1F6
		Mini DIPIPM with BSD	Mini DIPIPM Ver.7	Compact DIPIPM
Circuit current for IC (Low voltage part)	I_D	Max. 6.00mA	←	Max. 4.00mA
Short circuit trip level	$V_{SC(ref)}$	0.45~0.51V	←	0.455~0.505V
P-side Control supply under-voltage protection (UV)	UV_{DBt}	10.0~12.0V	←	10.2~12.9V
	UV_{DBr}	10.5~12.5V	←	10.2~12.9V
N-side Control supply under-voltage protection (UV)	UV_{Dt}	10.3~12.5V	←	10.3~12.5V
	UV_{Dr}	10.8~13.0V	←	←
Fault output pulse width 1)	t_{Fo}	Typ. 2.4ms (CFo=22nF)	←	Min. 200μs

1) Compact DIPIPM, unlike Mini DIPIPM series, does not have a CFo terminal. The fault output pulse width is a minimum of 200 μs.

CHAPTER 2 SPECIFICATIONS AND CHARACTERISTICS

2.1 Compact DIPIPM Specifications

Compact DIPIPM specifications are described below by using PSS30SF1F6 (30A/600V) as an example. Please refer to respective datasheet for the detailed description of other types.

2.1.1 Maximum Ratings

The maximum ratings of PSS30SF1F6 (30A/600V) are shown in Table 2-1-1.

Table 2-1-1 Maximum Ratings (Tj = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit	
V_{CC}	Supply voltage	Applied between P-NU, NV, NW	450	V	(1)
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-NU, NV, NW	500	V	(2)
V_{CES}	Collector-emitter voltage		600	V	(3)
$\pm I_C$	Each IGBT collector current	T_C=25°C (Note1)	30	A	(4)
$\pm I_{CP}$	Each IGBT collector current (peak)	T_C= 25°C, less than 1ms	60	A	
T_{jop}	Operation junction temperature	Continuous operation (Note2)	-40~+150	°C	
T_{jmax}	Maximum junction temperature	Only IGBT, temporally operation (e.g. overload)	175	°C	(5)

Note1: Pulse width and period are limited due to junction temperature.
Note2: The maximum junction temperature rating of built-in power chips is 175°C(@Tc≦125°C). However, to ensure safe operation of DIPIPM, the average junction temperature should be limited to Tj(Ave)≦150 C(@Tc≦125°C)

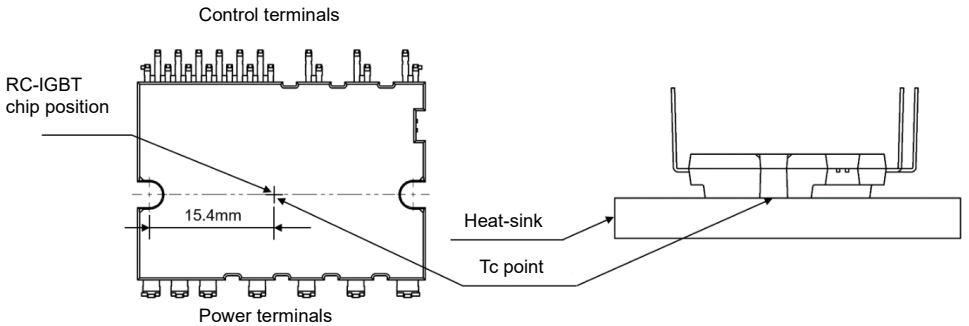
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	20	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	20	V
V_{IN}	Input voltage	Applied between U_P, V_P, W_P-V_{NC}, U_N, V_N, W_N-V_{NC}	-0.5~V_D+0.5	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	-0.5~V_D+0.5	V
I_{FO}	Fault output current	Sink current at F_O terminal	5	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	-0.5~V_D+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit	
$V_{CC(PROT)}$	Self-protection supply voltage limit (Short circuit protection capability)	V_D = 13.5~16.5V, Inverter Part T_j = 150°C, non-repetitive, less than 2μs	400	V	(6)
T_C	Module case operation temperature	Measurement point of Tc is described below	-40~+125	°C	
T_{stg}	Storage temperature		-40~+125	°C	
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	2500	V_{rms}	

Tc measurement position



(7)

NOTES:

(1) Vcc — The maximum voltage can be biased between P-N. A voltage suppressing circuit such as a brake circuit is necessary if P-N voltage exceeds this value.

(2) Vcc(surge) — The maximum P-N surge voltage in switching state. If P-N voltage exceeds this voltage, a snubber circuit is necessary to absorb the surge under this voltage.

(3) V_{CES} — The maximum sustained collector-emitter voltage of built-in IGBT and FWDi.

(4) +/-I_C — The allowable continuous current flowing at collect electrode (Tc=25°C) Pulse width and period are limited due to junction temperature.

(5) Tjop — The maximum junction temperature rating is 175°C at Tc=25°C. But for safe operation, it is recommended to limit the average junction temperature up to 150°C. Repetitive temperature variation ΔTj affects the life time of power cycle, so refer to lifetime curves for safety design.

(6) Vcc(prot) — The maximum supply voltage for turning off IGBT safely in the case of an SC or OC faults. The power chip might not be protected and break down in the case that the supply voltage is higher than this specification.

(7) Tc position — Tc (case temperature) is defined as the temperature just beneath the specified power chip. Please mount a thermocouple on the heat sink surface at the defined position to get accurate temperature information. In some control schemes, temperature measurement point at the following may not be highest case temperature. In such cases, it is necessary to change the measurement point to that under the highest power chip. (Refer previous figure of power chip position.)

[Power chip position]

Fig.2-1-1 indicate the position of the each power chips. (This figure is the view from laser marked side.)

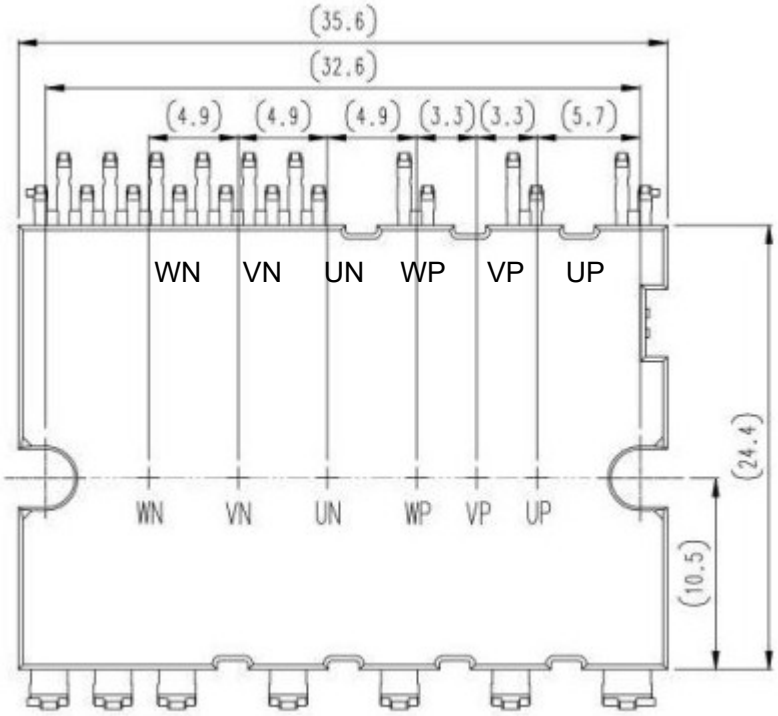


Fig.2-1-1 Power chip position (PSSxxSF1F6) (Unit: mm)

2.1.2 Thermal Resistance

Table 2-1-2 shows the thermal resistance of PSS30SF1F6 (30A/600V).

Table 2-1-2 Thermal resistance of PSS30SF1F6

THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note)	Inverter RC-IGBT part (per 1/6 module)	-	-	1.05	K/W

Note: Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100μm~+200μm on the contacting surface of DIPIPM and heat sink. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.3K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m•k).

The above data shows the thermal resistance between chip junction and case at steady state. The thermal resistance goes into saturation within about 10 seconds. The unsaturated thermal resistance is called transient thermal impedance which is shown in Fig.2-1-2. Zth(j-c)* is the normalized value of the transient thermal impedance. (Zth(j-c)*= Zth(j-c) / Rth(j-c)max)

For example, the IGBT transient thermal impedance of PSS30SF1F6 in 0.1s is 1.05×0.93≒0.98K/W.

The transient thermal impedance isn't used for constant current, but for short period current (ms order). (e.g. in the cases at motor starting, at motor lock・・・)

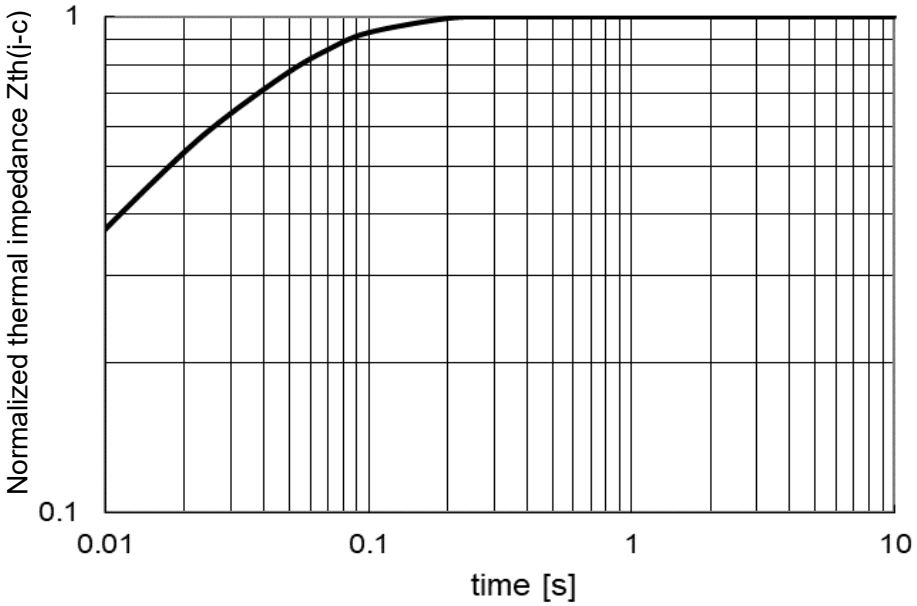


Fig.2-1-2 Typical transient thermal impedance (PSSxxSF1F6)

2.1.3 Electric Characteristics and Recommended Conditions

Table 2-1-3 shows the typical static characteristics and switching characteristics of PSS30SF1F6 (30A/600V).

Table 2-1-3 Static and switching characteristics of PSS30SF1F6 (Tj = 25°C, unless otherwise noted)

INVERTER PART (T_j = 25°C, unless otherwise noted)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_D = V_{DB} = 15V, V_{IN} = 5V, I_C = 30A	-	1.27	1.57	V
V_{EC}	FWDi forward voltage	V_{IN} = 0V, -I_C = 30A	-	1.35	1.64	V
t_{on}	Switching times	V_{CC} = 300V, V_D = V_{DB} = 15V I_C = 30A, T_j = 25°C, V_{IN} = 0↔5V Inductive Load（upper-lower arm）	0.57	1.00	1.45	μs
$t_{C(on)}$			-	0.29	0.54	μs
t_{off}			-	1.20	1.64	μs
$t_{C(off)}$			-	0.16	0.37	μs
t_{rr}			-	0.19	-	μs
I_{CES}	Collector-emitter cut-off current	V_{CE} = V_{CES}	-	-	1	mA

Switching time definition and performance test method are shown in Fig.2-1-3 and 2-1-4. Switching characteristics are measured by half bridge circuit with inductance load.

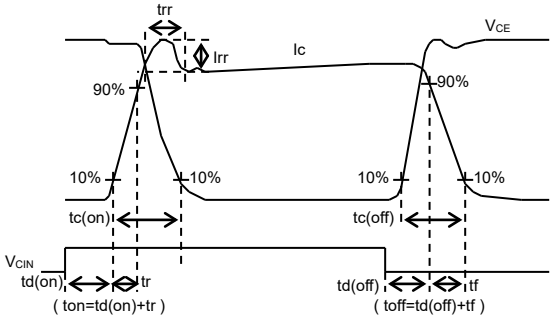


Fig.2-1-3 Switching time definition

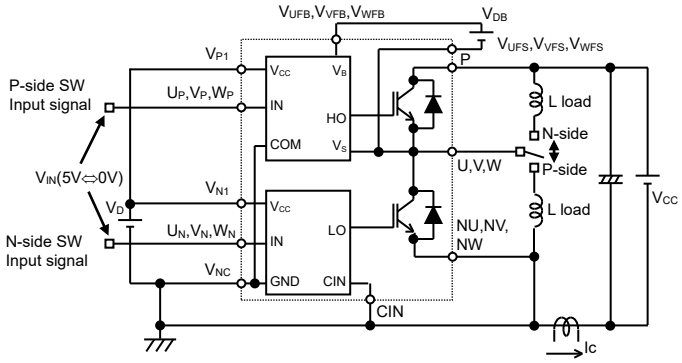


Fig.2-1-4 Evaluation circuit (inductive load)

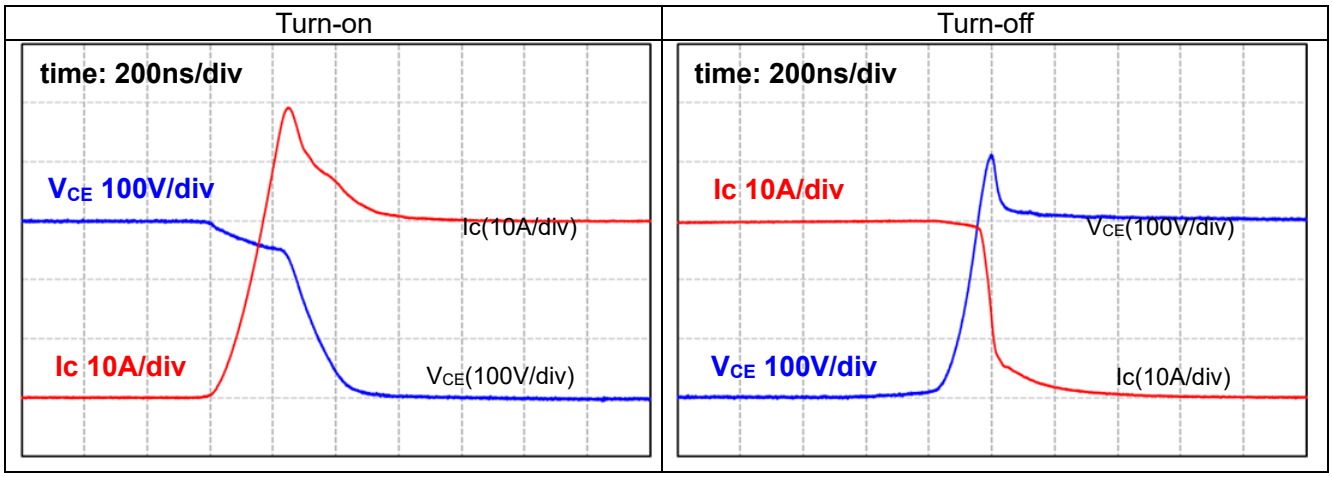


Fig.2-1-5 Typical switching waveform (PSS30SF1F6)
Conditions: V_{CC}=300V, V_D=V_{DB}=15V, Tj=125°C, Ic=30A, Inductive load half-bridge circuit

Table 2-1-4 shows the typical control part characteristics of PSS30SF1F6 (30A/600V).

Table 2-1-4 Control (Protection) characteristics of PSS30SF1F6 (T_j = 25°C, unless otherwise noted)

CONTROL (PROTECTION) PART (T_j = 25°C, unless otherwise noted)

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit current	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	V_D=15V, V_{IN}=0V	-	-	4.00	mA
			V_D=15V, V_{IN}=5V	-	-	4.00	
I_{DB}		Each part of V_{UFB}- V_{UFS}, V_{VFB}- V_{VFS}, V_{WFB}- V_{WFS}	V_D=V_{DB}=15V, V_{IN}=0V	-	-	0.55	
			V_D=V_{DB}=15V, V_{IN}=5V	-	-	0.55	
$V_{SC(ref)}$	Short circuit trip level	V_D = 15V (Note 1)		0.455	0.480	0.505	V
UV_{DBt}	P-side Control supply under-voltage protection (UV)	T_j ≤125°C	Trip level	10.2	-	12.9	V
UV_{DBr}			Reset level	10.2	-	12.9	V
UV_{Dt}	N-side Control supply under-voltage protection (UV)		Trip level	10.3	-	12.5	V
UV_{Dr}			Reset level	10.8	-	13.0	V
V_{OT}	Temperature output	Pull down R=5.1kΩ (Note 2)	LVIC Temperature=90°C	2.63	2.80	2.97	V
V_{FOH}	Fault output voltage	V_{SC} = 0V, F_O terminal pulled up to 5V by 10kΩ		4.9	-	-	V
V_{FOL}		V_{SC} = 1V, I_{FO} = 1mA		-	-	0.95	V
t_{FO}	Fault output pulse width	(Note 3)		200	-	-	µs
I_{IN}	Input current	V_{IN} = 5V		0.70	1.00	1.50	mA
$V_{th(on)}$	ON threshold voltage	Applied between U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}		-	2.20	2.60	V
$V_{th(off)}$	OFF threshold voltage			0.80	1.40	-	
$V_{th(hys)}$	ON/OFF threshold hysteresis voltage			0.35	0.80	-	
V_F	Bootstrap Di forward voltage	I_F=10mA including voltage drop by limiting resistor		0.5	0.9	1.3	V
R	Built-in limiting resistance	I_F=300mA		16	20	24	Ω

Note 1 : SC protection works only for N-side IGBT. Please select the external shunt resistance such that the SC trip-level is less than 2 times of the current rating.
Note 2 : DIPIPM don't shutdown IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIPIPM.
3 : Fault signal Fo outputs when SC or UV protection works. Fo pulse width is different for each protection modes. At SC failure, Fo pulse width is a fixed width (=minimum 200µs), but at UV failure, Fo outputs continuously until recovering from UV state.

Recommended operating conditions for PSS30SF1F6 (30A/600V) are given in Table 2-1-5. It is highly recommended to operate the modules within these conditions so as to ensure DIPIPM safe operation.

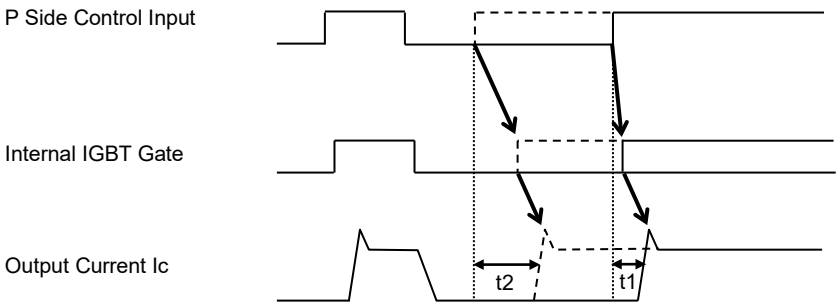
Table 2-1-5 Recommended operating conditions of PSS30SF1F6

RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage	Applied between P-NU, NV, NW	0	300	400	V
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	13.0	15.0	18.5	V
ΔV_D, ΔV_{DB}	Control supply variation		-1	-	+1	V/µs
t_{dead}	Arm shoot-through blocking time	For each input signal	1.5	-	-	µs
f_{PWM}	PWM input frequency	T_C ≤ 125°C, T_j ≤ 150°C	-	-	20	kHz
PWIN(on)	Minimum input pulse width	(Note 1)	0.7	-	-	µs
PWIN(off)		(Note 2)	1.5	-	-	
V_{NC}	V_{NC} variation	Between V_{NC}-NU, NV, NW (including surge)	-5.0	-	+5.0	V

Note1: DIPIPM might not make response if the input signal pulse width is less than PWIN(on).
Note2: DIPIPM might make no response or delayed response (P-side IGBT only) for input pulse width less than PWIN(off). Over rated collector current (Ic) operation, DIPIPM might make delayed response even if the input signal pulse width is PWIN(off) or more. The timing charts are described as below.

Delayed Response Against Shorter Input Off Signal Than PWIN(off) (P-side only, above rated current)



Real line: off pulse width > PWIN(off); turn on time t1
Broken line: off pulse width < PWIN(off); turn on time t2
(t1:Normal switching time)

About Control supply variation

If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet the following specifications:

$dV/dt \leq +/-1V/\mu s$, $Vripple \leq 2Vp\text{-}p$

2.1.4 Mechanical Characteristics and Ratings

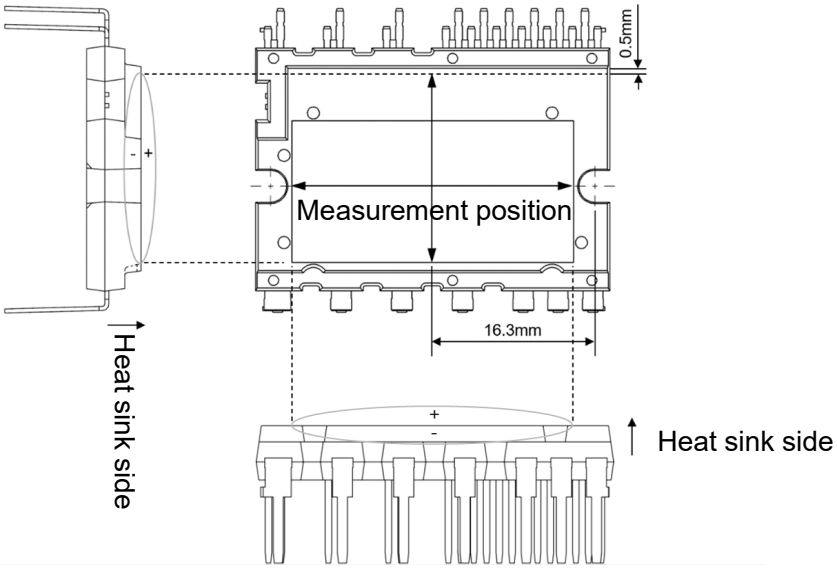
The mechanical characteristics and ratings are shown in Table 2-1-6.
Please refer to Section 2.4 for the detailed mounting instruction of Compact DIPIPM.

Table 2-1-6 Mechanical characteristics and ratings of PSS30SF1F6

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition	Reference	Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3 (Note 1)	JEITA-ED-4701 402 Method Ⅱ	0.59	0.69	0.78	N·m
Terminal pulling strength	Control terminal: Load 2.3N Power terminal: Load 2.3N	JEITA-ED-4701 401 Method Ⅰ	30	-	-	s
Terminal bending strength	15deg. Bend	JEITA-ED-4701 401 Method Ⅲ	1	-	-	times
Weight		-	-	10.3	-	g
Heat-sink flatness	(Note 2)	-	-30	-	100	μm

Note 1: Plain washers (ISO7089-7094) are recommended.
Note 2: Measurement point of heat radiation part flatness



2.2 Protective Functions and Operating Sequence

Compact DIPIPM has short circuit (SC), Under Voltage of control supply (UV), temperature output (VOT) and Interlock (IL) for protection function. The operating principle and sequence are described below.

2.2.1 Short Circuit Protection

(1) General

Compact DIPIPM Ver.7 uses external shunt resistor for the current detection as shown in Fig.2-2-1. The internal protection circuit inside the IC captures the excessive large current by comparing the CIN voltage generated at the shunt resistor with the referenced SC trip voltage and perform protection automatically. The threshold voltage trip level of the SC protection Vsc(ref) is typ. 0.48V.

In case of SC protection happens, all the gates of N-side three phase IGBTs will be interrupted together with a fault signal output. To prevent DIPIPM erroneous protection due to normal switching noise and/or recovery current, it is necessary to set an RC filter (time constant: 1.5μ~2μs) to the CIN terminal input (Fig.2-2-1, 2-2-2). Also, please make the pattern wiring around the shunt resistor as short as possible.

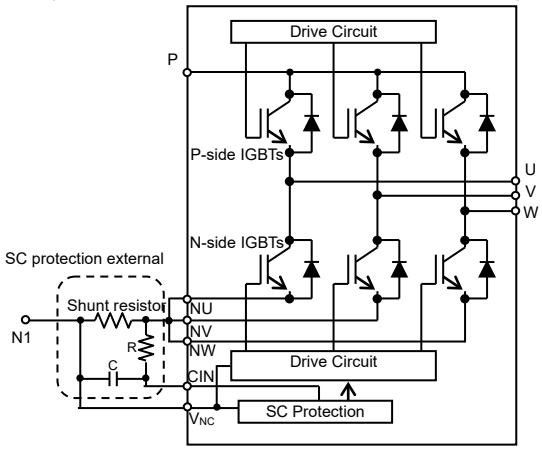


Fig.2-2-1 SC protecting circuit

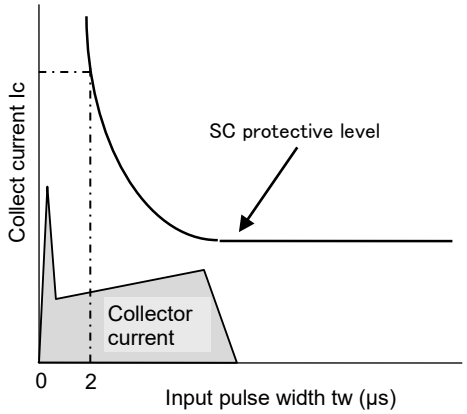


Fig.2-2-2 Filter time constant setting

(2) SC protection Sequence

SC protection (N-side only with the external shunt resistor and RC filter)

a1. Normal operation: IGBT ON and carrying current.

a2. Short circuit current detection (SC trigger).
It is necessary to set RC time constant so that IGBT shut down within 2.0μs when SC. (1.5~2.0μs is recommended generally.)

a3. All N-side IGBTs' gate are hard interrupted.

a4. All N-side IGBTs turn OFF.

a5. F_O outputs for t_{Fo}=minimum 200μs.

a6. Input = "L". IGBT OFF

a7. Fo finishes output, but IGBTs don't turn on until inputting next ON signal (L→H).
IGBT of each phase can return to normal state by inputting ON signal to each phase.

a8. Normal operation: IGBT ON and outputs current.

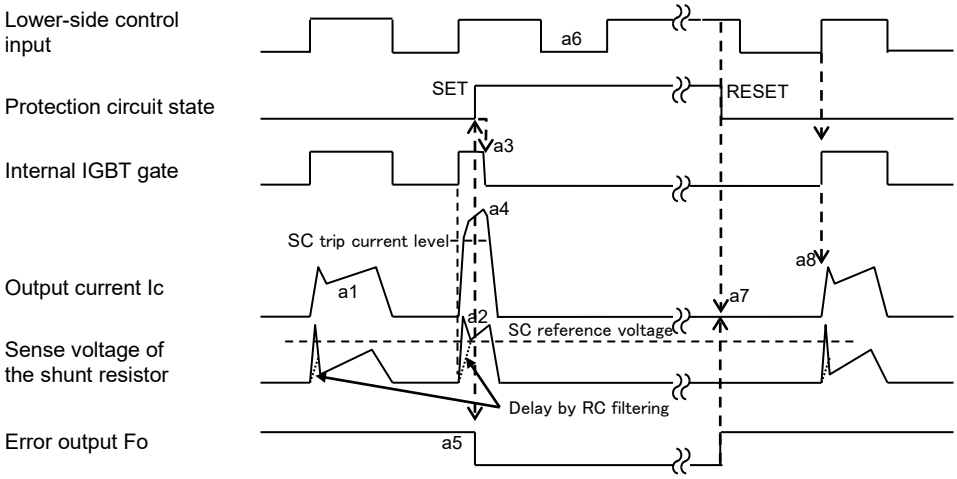


Fig.2-2-3 SC protection timing chart

(3) Determination of Shunt Resistance

1. Shunt resistance

The value of current sensing resistance is calculated by the following formula:

$$R_{Shunt} = V_{SC(ref)}/SC$$

where $V_{SC(ref)}$ is the SC trip voltage.

The maximum SC trip level SC(max) should be set less than the IGBT minimum saturation current which is 2.0 times as large as the rated current. For example, the SC(max) of PSS30SF1F6 should be set to 30x2=60A. The parameters ($V_{SC(ref)}$, R_{Shunt}) dispersion should be considered when designing the SC trip level.

For example of PSS30SF1F6, the spec of $V_{SC(ref)}$ as shown in Table 2-2-1.

Table 2-2-1 Specification for $V_{SC(ref)}$

Condition	Min	Typ	Max	Unit
Tj=25°C, V_D=15V	0.455	0.480	0.505	V

Then, the range of SC trip level can be calculated by the following expressions:

$R_{Shunt(min)}=V_{SC(ref)\ max}$ /SC(max)
$R_{Shunt(typ)}= R_{Shunt(min)}$ / 0.95* then SC (typ) = $V_{SC(ref)\ typ}$ / $R_{Shunt(typ)}$
$R_{Shunt(max)}= R_{Shunt(typ)}$ x 1.05* then SC (min)= $V_{SC(ref)\ min}$ / $R_{Shunt(max)}$
*) This is the case that shunt resistance dispersion is within +/-5%.

So, the SC trip level range is described as Table 2-2-2:

Table 2-2-2 Operative SC Range (R_{Shunt}=8.4mΩ (min), 8.9mΩ (typ), 9.3mΩ (max)) (Calculated Value*)

Condition	min.	typ.	Max.	Unit
Tj=25°C, V_D=15V	48.9	54.2	60	A

(e.g. 12.8mΩ ($R_{shunt(min)}$) = 0.51V (=$V_{SC(max)}$) / 40A(=SC(max))

There is the possibility that the actual SC protection level becomes less than the calculated value. This is considered due to the resonant signals caused mainly by parasitic inductance and parasitic capacity. It is recommended to make a confirmation of the resistance by prototype experiment.
*) The above shunt resistance values are calculated values. For actual selection, refer to standard values such as the E-series specified in IEC standards.

2. RC Filter Time Constant

It is necessary to set an RC filter in the SC sensing circuit to prevent malfunction of SC protection due to noise interference. The RC time constant is determined depending on the applying time of noise interference and the SCSOA of the DIPIPM.

When the voltage drop on the external shunt resistor exceeds the SC trip level, the time (t1) that the CIN terminal voltage rises to the referenced SC trip level can be calculated by the following expression:

$$V_{SC} = R_{shunt} \cdot I_c \cdot (1 - \varepsilon^{-\frac{t1}{\tau}})$$

$$t1 = -\tau \cdot \ln(1 - \frac{V_{SC}}{R_{shunt} \cdot I_c})$$

Vsc: the CIN terminal input voltage, Ic : the peak current, τ : the RC time constant

On the other hand, the typical time delay t2 (from Vsc voltage reaches Vsc(ref) to IGBT gate shutdown) of IC is shown in Table 2-2-3.

Table 2-2-3 Internal time delay of IC

Item	Min	typ	max	Unit
IC transfer delay time	-	-	0.6	μs

Therefore, the total delay time from an SC level current happened to the IGBT gate shutdown becomes:

t_{TOTAL}=t1+t2

2.2.2 Control Supply UV Protection

(1) General

The UV protection is designed to prevent unexpected operating behavior as described in Table 2-2-4.

Both P-side and N-side have UV protecting function; however, fault signal (Fo) output only corresponds to N-side UV protection. Fo output continuously during UV state.

In addition, there is a noise filter (typ. 7μs) integrated into the UV protection circuit to prevent instantaneous UV erroneous trip. Therefore, the control signals are still transferred in the initial 7μs after UV happened.

Table 2-2-4 DIPIPM operating behavior versus control supply voltage

Control supply voltage	Operating behavior
0 - 4V (P, N-side)	In this voltage range, built-in control IC may not work properly. Normal operating of each protection function (UV, Fo output etc.) is not also assured. Normally IGBT does not work. But external noise may cause DIPIPM malfunction (turns ON), so DC-link voltage needs to start up after control supply starts-up.
4 - UV_{Dt} (N-side), 4 - UV_{DBt} (P-side)	UV function becomes active and output Fo (N-side only). Even if control signals are applied, IGBT does not work
UV_{Dt} - 13.5V (N-side), UV_{DBt} -13.0V (P-side)	IGBT can work. However, conducting loss and switching loss will increase, and result in extra temperature rise at this state.
13.5 - 16.5V (N-side), 13.0 - 18.5V (P-side)	Recommended conditions.
16.5 - 20V (N-side), 18.5 - 20V (P-side)	IGBT works. However, switching speed becomes fast and saturation current becomes large at this state, increasing SC broken risk.
20V- (P, N-side)	The control circuit might be destroyed.

Ripple Voltage Limitation of Control Supply

If high frequency noise is superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem happens, line ripple voltage should meet the following specifications:

$$dV/dt \leq +/-1V/\mu s,\ Vripple \leq 2Vp\text{-}p$$

(2) UV protection Sequence

[N-side UV Protection Sequence]

a1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but IGBT turns ON by next ON signal (L→H). (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
a2. Normal operation: IGBT ON and carrying current.
a3. V_D level dips to under voltage trip level. (UV_{Dt}).
a4. All N-side IGBTs turn OFF in spite of control input condition.
a5. Fo outputs for tFo=minimum 200μs, but output is extended during VD keeps below UVDr.
a6. V_D level reaches UV_{Dr}.
a7. Normal operation: IGBT ON and outputs current.

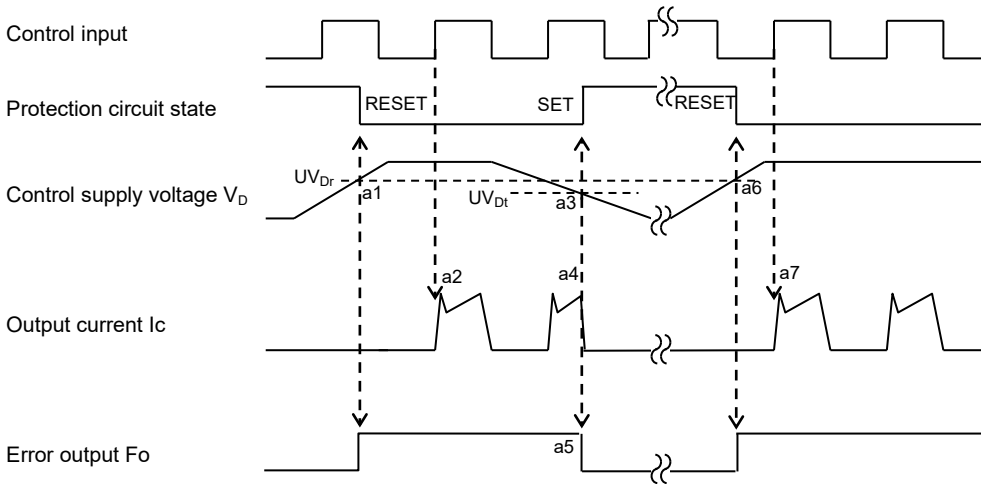


Fig.2-2-4 Timing chart of N-side UV protection

[P-side UV Protection Sequence]

a1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr}, IGBT turns on by next ON signal (L→H).
a2. Normal operation: IGBT ON and outputs current.
a3. V_{DB} level drops to under voltage trip level (UV_{DBt}).
a4. IGBT of the corresponding phase only turns OFF in spite of control input signal level, but there is no F_O signal output.
a5. V_{DB} level reaches UV_{DBr}.
a6. Normal operation: IGBT ON and outputs current.

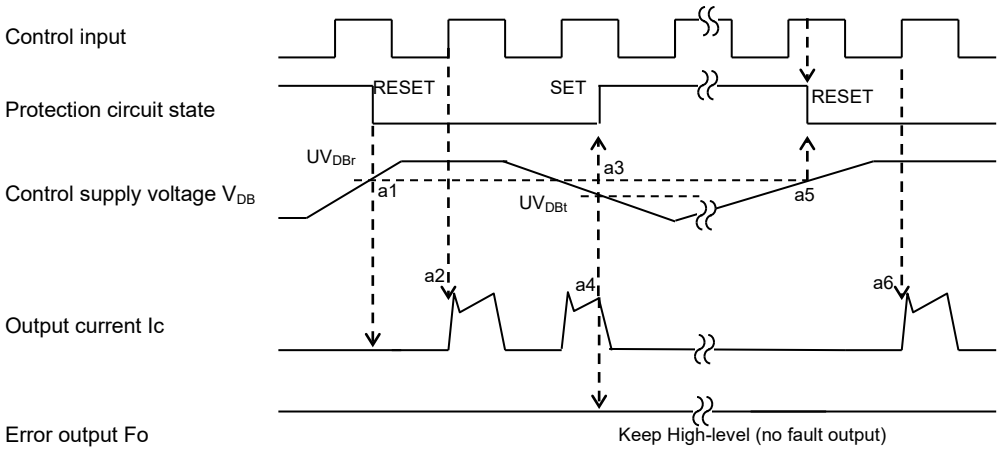


Fig.2-2-5 Timing Chart of P-side UV protection

2.2.3 Temperature output function V_{OT}

(1) Usage of this function

This function measures the temperature of control LVIC by built in temperature sensor on LVIC. The heat generated at IGBT and FWDi transfers to LVIC through molding resin of package and outer heat sink. So LVIC temperature cannot respond to rapid temperature rise of those power chips effectively. (e.g. motor lock, short circuit) It is recommended to use this function for protecting from slow excessive temperature rise by such cooling system down and continuance of overload operation. (Replacement from the thermistor which was mounted on outer heat sink currently.)

[Note]

In this function, DIPIPM cannot shut down IGBT and output fault signal by itself when temperature rises excessively. When temperature exceeds the defined protection level, controller (MCU) should stop the DIPIPM.

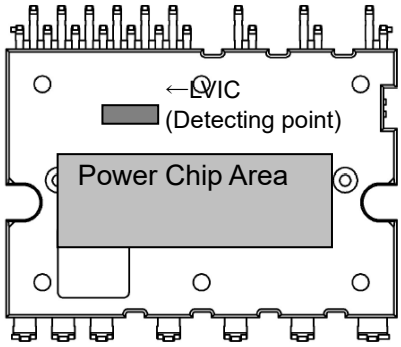


Fig.2-2-6 Temperature detecting point

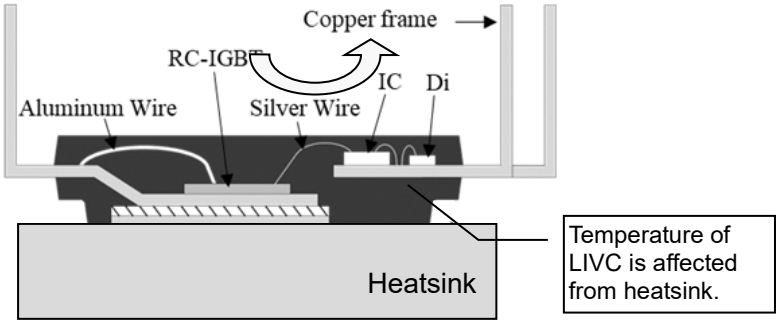


Fig.2-2-7 Thermal conducting from power chips

(2) V_{OT} characteristics

V_{OT} output circuit, which is described in Fig.2-2-8, is the output of OP amplifier circuit. The current capability of V_{OT} output is described as Table 2-2-6. The characteristics of V_{OT} output vs. LVIC temperature is linear characteristics described in Fig.2-2-12. There are some cautions for using this function as below.

Table 2-2-6 Output capability

(Tc=-20°C ~100°C)

	min.
Source	1.7mA
Sink	0.1mA

Source: Current flow from V_{OT} to outside.

Sink : Current flow from outside to V_{OT}.

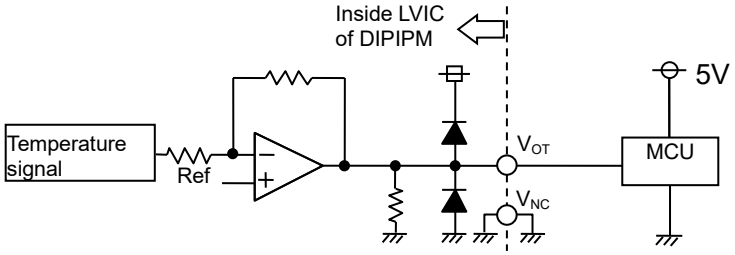


Fig.2-2-8 V_{OT} output circuit

• <u>In the case of detecting lower temperature than room temperature</u>

It is recommended to insert 5.1kΩ pull down resistor for getting linear output characteristics at lower temperature than room temperature. When the pull down resistor is inserted between V_{OT} and V_{NC} (control GND), the extra current calculated by V_{OT} output voltage / pull down resistance flows as LVIC circuit current continuously. In the case of only using V_{OT} for detecting higher temperature than room temperature, it isn't necessary to insert the pull down resistor.

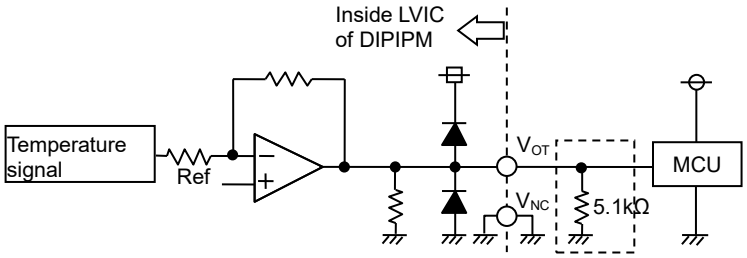


Fig.2-2-9 V_{OT} output circuit in the case of detecting low temperature

• In the case of using with low voltage controller (MCU)

In the case of using V_{OT} with low voltage controller (e.g. 3.3V MCU), V_{OT} output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and this output for preventing over voltage.

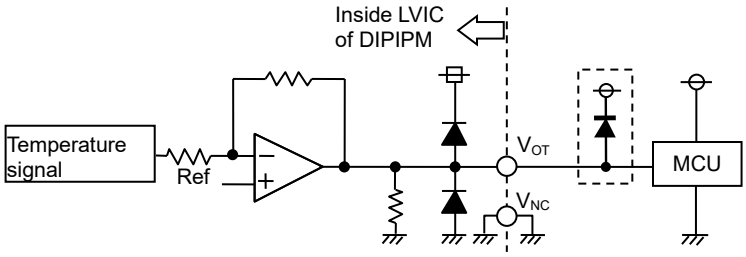


Fig.2-2-10 V_{OT} output circuit in the case of using with low voltage controller

• In the case that the protection level exceeds control supply of the controller

In the case of using low voltage controller like 3.3V MCU, if it is necessary to set the trip V_{OT} level to control supply voltage (e.g. 3.3V) or more, there is the method of dividing the V_{OT} output by resistance voltage divider circuit and then inputting to A/D converter on MCU (Fig.2-2-11). In that case, sum of the resistances of divider circuit should be almost 5.1kΩ. About the necessity of clamp diode, we consider that the divided output will not exceed the supply voltage of controller generally, so it will be unnecessary to insert the clump diode. But it should be judged by the divided output level finally.

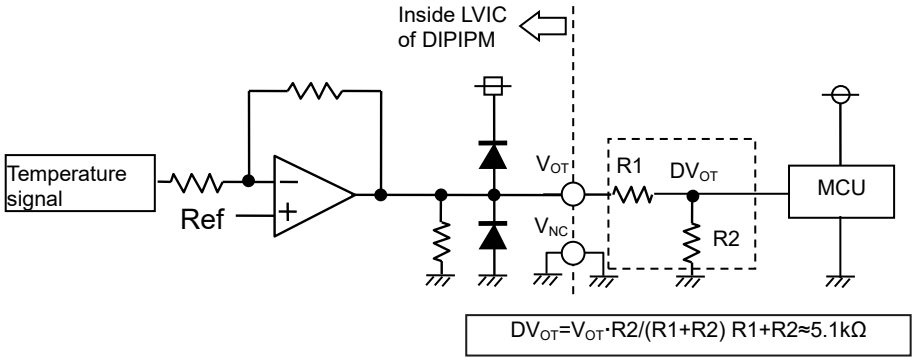


Fig.2-2-11 V_{OT} output circuit in the case with high protection level

Please handle the following characteristics of VOT output vs. LVIC temperature as reference data to set over temperature protection. These curves are based on theoretical designed value excluding specified value in the target specification.

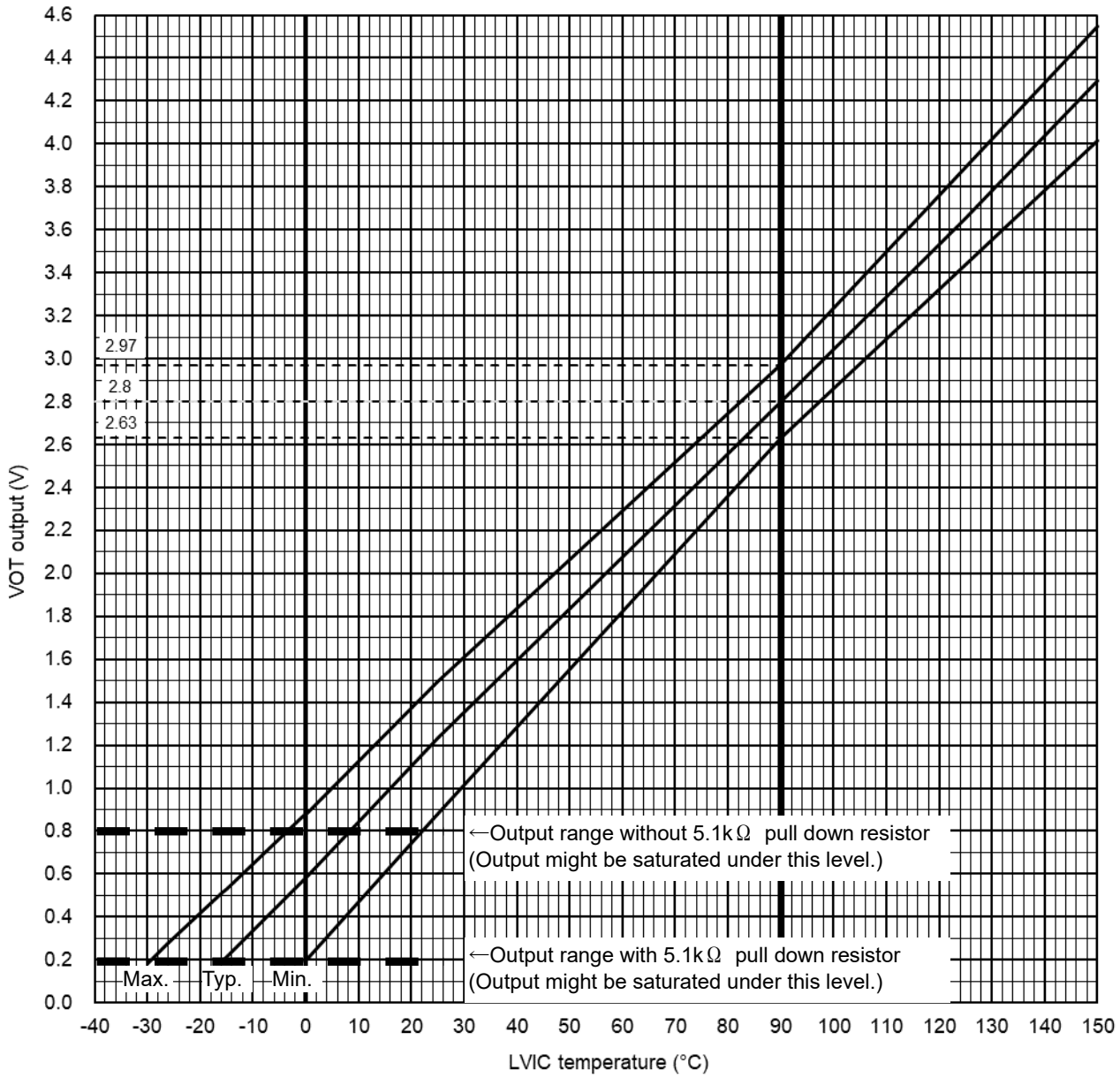


Fig.2-2-12 V_{OT} output vs. LVIC temperature (PSSxxSF1F6)

As mentioned above, the heat of power chips transfers to LVIC through the heat sink and package, so the relationship between LVIC temperature: Tic (=VOT output), case temperature: Tc (under the chip defined on datasheet), and junction temperature: Tj depends on the system cooling condition, heat sink, control strategy, etc. This relationship may be different due to the cooling conditions. So, when setting the threshold temperature for protection, it is necessary to get the relationship between them on your real system. And when setting threshold temperature Tic, it is important to consider the protection temperature assures T_j =150°C.

2.2.4 Interlock function

(1) General

This interlock function detects simultaneous ON of P-side and N-side in the same phase by the control IC (LVIC) and prevents arm short circuit. The LVIC compares P-side control input and N-side control input in the same phase. When the simultaneous ON signals are input, the N-side output is kept OFF state regardless of its input state.
(Fo signal is not output) P-side IGBTs output keeps following input signal.

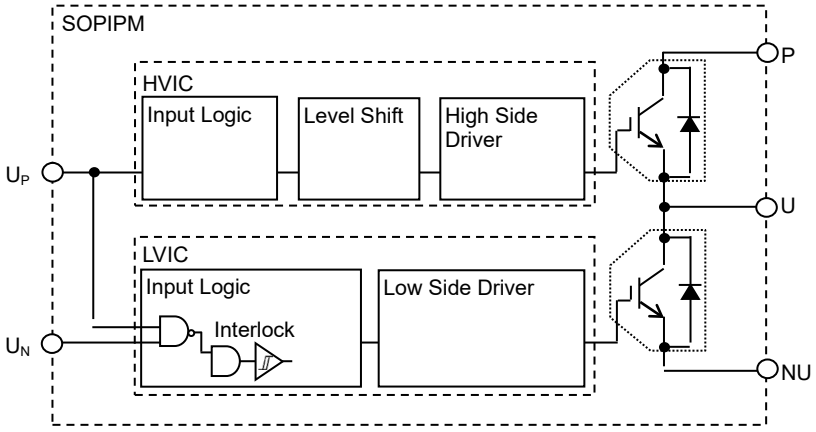


Fig.2-2-13 Interlock function block diagram (typical example: U phase)

(2) Interlock Sequence

[Interlock Sequence]

a1. When N-side is ON state(H), P-side turn ON(L→H) ····· N-side shut off (Note1)
a2. When P-side is ON state(H), N-side turn ON(L→H) ····· N-side shut off
a3. P-side turn OFF(H→L) and N-side is ON state(H) ····· N-side turn ON (Note1)

Note1: When a1 and a3 are active, a small-time-period through current may flow due to the difference in transmission delay between the control inputs on the P-side and N-side and the internal IGBT gate signal.

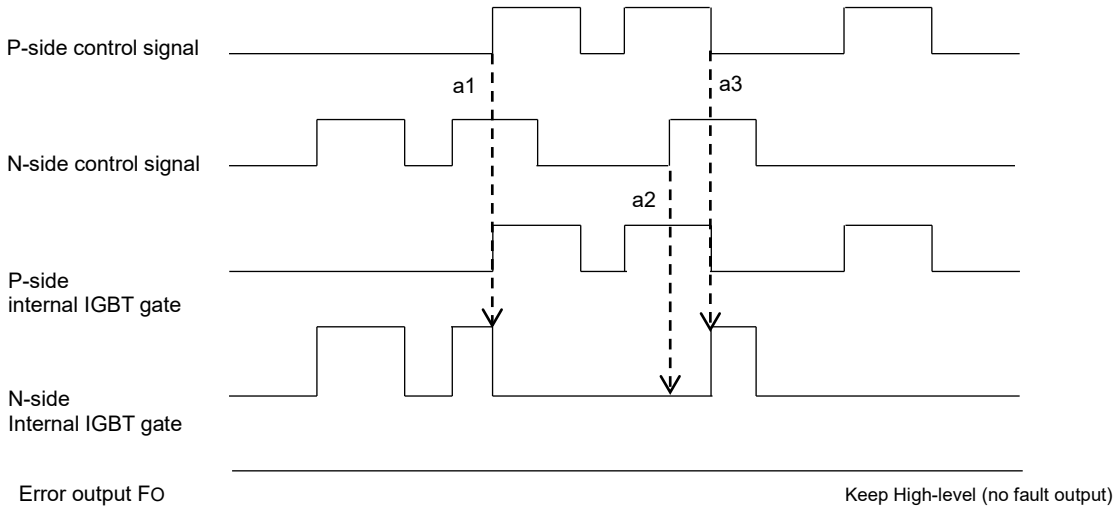


Fig.2-2-14 Timing Chart of Interlock function

2.3 Package Outlines

2.3.1 Package outlines and PCB Through-hole Pattern

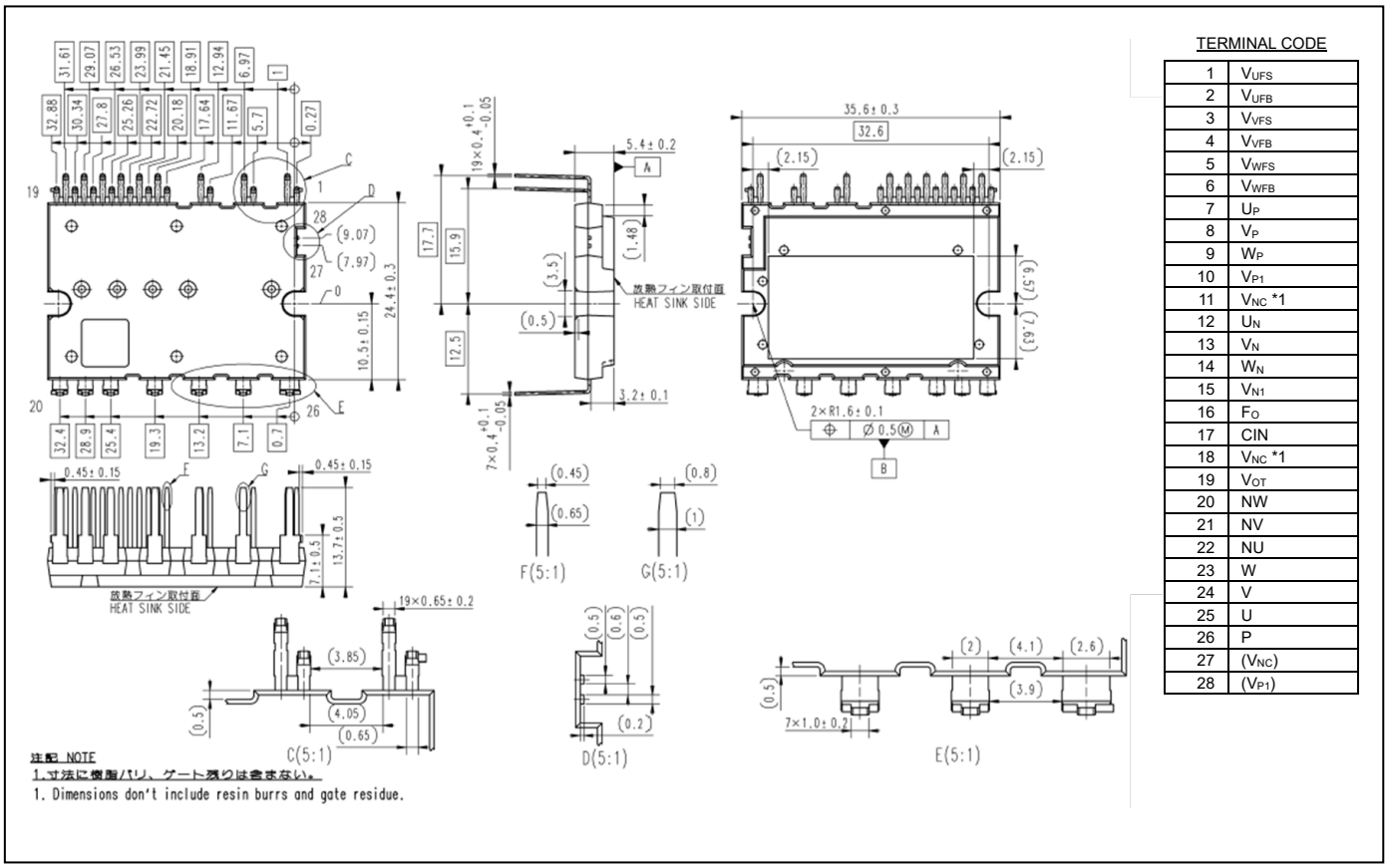


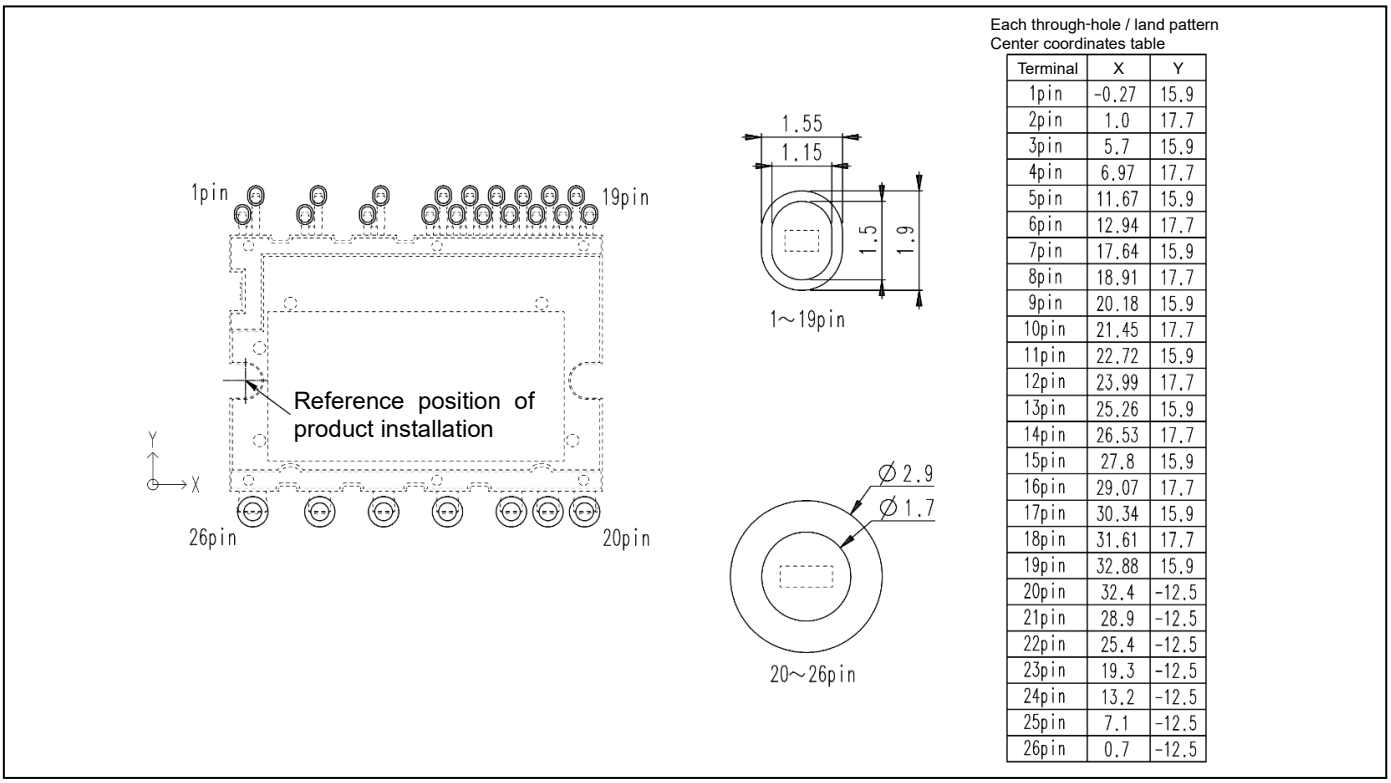
Fig.2-3-1 PSSxxSF1F6 package outline drawing (Dimension in mm)

Note: () pins are used internally. Please leave them NC (no connection).

Note: Pins 11 and 18 of the VNC (control power GND terminal) are internally connected. Use only one pin; leave the other pin in the NC (no connection) state.

Fig 2-3-2 shows the layout of recommended through-hole locations and diameters for PSSxxSF1F6.

[Dimension: mm]



Each through-hole / land pattern Center coordinates table

Terminal	X	Y
1pin	-0.27	15.9
2pin	1.0	17.7
3pin	5.7	15.9
4pin	6.97	17.7
5pin	11.67	15.9
6pin	12.94	17.7
7pin	17.64	15.9
8pin	18.91	17.7
9pin	20.18	15.9
10pin	21.45	17.7
11pin	22.72	15.9
12pin	23.99	17.7
13pin	25.26	15.9
14pin	26.53	17.7
15pin	27.8	15.9
16pin	29.07	17.7
17pin	30.34	15.9
18pin	31.61	17.7
19pin	32.88	15.9
20pin	32.4	-12.5
21pin	28.9	-12.5
22pin	25.4	-12.5
23pin	19.3	-12.5
24pin	13.2	-12.5
25pin	7.1	-12.5
26pin	0.7	-12.5

Fig.2-3-2 PCB through-hole pattern of PSSxxSF1F6 (Reference Figure)

2.3.2 Marking

The laser marking specifications of Compact DIPIPM series is described in Fig.2-3-3. Company name, Country of origin, Type name, Lot number, and 2D code mark are marked in the upper side of module.

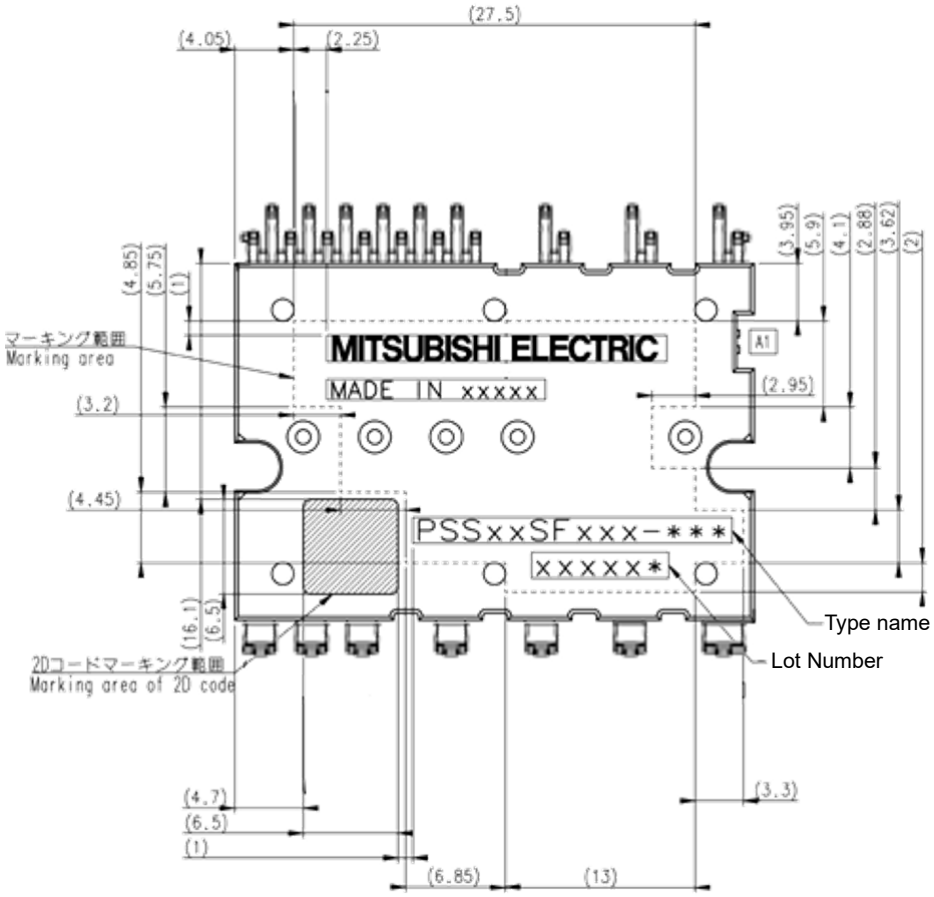


Fig.2-3-3 Laser marking view PSSxxSF1F6 (Dimension in mm)

The Lot number indicates production year, month, running number and country of origin.
The details are described below.

(Example) H 0 N AA1

- AA1 → Running number
- N → Product month (however O: October, N: November, D: December)
- 0 → Last figure of Product year (e.g. 2020)
- H → Factory identification
  H: Manufactured at the factory in China

2.3.3 Terminal Description

Table 2-3-1 Terminal description (PSSxxSF1F6)

No.	Symbol	Description
1	V_{UFS}	U-phase P-side drive supply GND terminal
2	V_{UFB}	U-phase P-side drive supply positive terminal
3	V_{VFS}	V-phase P-side drive supply GND terminal
4	V_{VFB}	V-phase P-side drive supply positive terminal
5	V_{WFS}	W-phase P-side drive supply GND terminal
6	V_{WFB}	W-phase P-side drive supply positive terminal
7	U_P	U-phase P-side control input terminal
8	V_P	V-phase P-side control input terminal
9	W_P	W-phase P-side control input terminal
10	V_{P1}	P-side control supply positive terminal
11	V_{NC} *1	P-side control supply GND terminal (connected to No.18 terminal internally)
12	U_N	U-phase N-side control input terminal
13	V_N	V-phase N-side control input terminal
14	W_N	W-phase N-side control input terminal
15	V_{N1}	N-side control supply positive terminal
16	Fo	Fault signal output terminal
17	CIN	SC trip voltage detecting terminal
18	V_{NC} *1	N-side control supply GND terminal (connected to No.11 terminal internally)
19	V_{OT}	Temperature output
20	NW	W-phase N-side IGBT emitter
21	NV	V-phase N-side IGBT emitter
22	NU	U-phase N-side IGBT emitter
23	W	W-phase output terminal (connected to No.5 terminal internally)
24	V	V-phase output terminal (connected to No.3 terminal internally)
25	U	U-phase output terminal (connected to No.1 terminal internally)
26	P	Inverter DC-link positive terminal
27	(V_{NC}) *2	Inner used terminal. Keep no connection It has control GND potential.
28	(V_{P1}) *2	Inner used terminal. Keep no connection. It has control supply potential.

1) Pins 11 and 18 of the VNC (control power GND terminal) are internally connected. Use only one pin; leave the other pin in the NC (no connection) state.
2) Dummy pin has some potential like gate voltage. Don't connect dummy-pins to any other terminals or PCB pattern.

Table 2-3-2 Detailed description of input and output terminals

Item	Symbol	Description
P-side drive supply positive terminal P-side drive supply GND terminal	V_{UFB}- V_{UFS} V_{VFB}- V_{VFS} V_{WFB}- V_{WFS}	• Drive supply terminals for P-side IGBTs. • By virtue of applying the bootstrap circuit scheme, individual isolated power supplies are not needed for the DIPIPM P-side IGBT drive. Each bootstrap capacitor is charged by the N-side V_D supply during ON-state of the corresponding N-side IGBT in the loop. • Abnormal operation might happen if the V_D supply is not aptly stabilized or has insufficient current capability. In order to prevent malfunction caused by such unstability as well as noise and ripple in supply voltage, a bypass capacitor with favorable frequency and temperature characteristics should be mounted very closely to each pair of these terminals. • Inserting a Zener diode (24V/1W) between each pair of control supply terminals is helpful to prevent control IC from surge destruction.
P-side control supply terminal N-side control supply terminal	V_{P1} V_{N1}	• Control supply terminals for the built-in HVIC and LVIC. • In order to prevent malfunction caused by noise and ripple in the supply voltage, a bypass capacitor with good frequency characteristics should be mounted very closely to these terminals. • Design the supply carefully so that the voltage ripple caused by operation keep within the specification. (dV/dt ≤ +/-1V/μs, Vripple≤2Vp-p) • It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
N-side control GND terminal	V_{NC}	• Control ground terminal for the built-in HVIC and LVIC. • Ensure that line current of the power circuit does not flow through this terminal in order to avoid noise influences.
Control input terminal	U_P,V_P,W_P U_N,V_N,W_N	• Control signal input terminals. • Voltage input type. These terminals are internally connected to Schmitt trigger circuit and pulled down by min 3.3kΩ resistor internally • The wiring of each input should be as short as possible to protect the DIPIPM from noise interference. • Use RC coupling in case of signal oscillation. Pay attention to threshold voltage of input terminal, because input circuit has pull down resistor.
Short-circuit trip voltage detecting terminal	CIN	• For short circuit protection, input the potential of external shuint resistor to CIN terminal through RC filter (for the noise immunity). • The time constant of RC filter is recommended to be up to 2μs.
Fault signal output terminal	F_O	• Fault signal output terminal. • Fo signal line should be pulled up to the logic supply. (In the case pulling up to 5V supply, over 5kΩ resistor is needed for limitting the Fo sink current I_{Fo} up to 1mA. Normally 10kΩ is recommended.)
Temperature output terminal	V_{OT}	• LVIC temperature is ouput by analog signal. • This terminal is connected to the ouput of OP amplifer internally. • It is recommended to connect 5.1kΩ pulldown resistor if output linearlity is necessary under room temperature.
Inverter DC-link positive terminal	P	• DC-link positive power supply terminal. • Internally connected to the collectors of all P-side IGBTs. • To suppress surge voltage caused by DC-link wiring or PCB pattern inductance, smoothing capacitor should be inserted very closely to the P and N terminal. It is also effective to add small film capacitor with good frequency characteristics.
Inverter DC-link negative terminal	NU,NV,NW	• Open emitter terminal of each N-side IGBT • These terminals are connected to the power GND through individual shunt resistor.
Inverter power output terminal	U, V, W	• Inverter output terminals for connection to inverter load (e.g. AC motor). • Each terminal is internally connected to the intermidiate point of the corresponding IGBT half bridge arm.

Note: Use oscilloscope to check voltage waveform of each power supply terminals and P&N terminals, the time division of OSC should be set to about 1μs/div. Please ensure the voltage (including surge) not exceed the specified limitation.

2.4 Mounting Method

This section shows the electric spacing and mounting precautions of Compact DIPIPM.

2.4.1 Electric Spacing

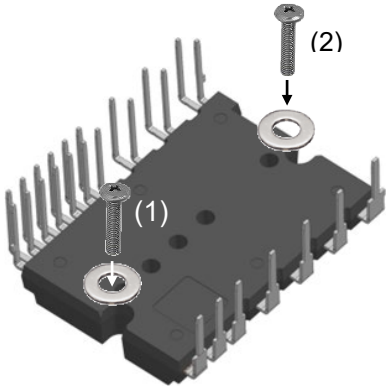
The electric spacing specification of Compact DIPIPM series is shown in Table 2-4-1

Table 2-4-1 Minimum insulation distance of PSSxxSF1F6 (minimum value)

Clearance(mm)		Creepage(mm)	
Between power terminals	3.0	Between power terminals	4.0
Between control terminals	3.0	Between control terminals	4.0
Between terminals and heat sink	3.0	Between terminals and heat sink	4.0

2.4.2 Mounting Method and Precautions

When installing the module to the heat sink, excessive or uneven fastening force might apply stress to inside chips. Then it will lead to a broken or degradation of the chips or insulation structure. The recommended fastening procedure is shown in Fig.2-4-1. When fastening, it is necessary to use the torque wrench and fasten up to the specified torque. And pay attention not to have any foreign particle on the contact surface between the module and the heat sink. Even if the fixing of heatsink was done by proper procedure and condition, there is a possibility of damaging the package because of tightening by unexpected excessive torque or tucking particle. For ensuring safety it is recommended to conduct the confirmation test (e.g. insulation inspection) on the final product after fixing the DIPIPM with the heatsink.



Temporary fastening
(1)→(2)

Permanent fastening
(1)→(2)

Note: Generally, the temporary fastening torque is set to 20-30% of the maximum torque rating.
Not care the order of fastening (1) or (2), but need to fasten alternately.

Fig.2-4-1 Recommended screw fastening order

Table 2-4-2 Mounting torque and heat sink flatness specifications

Item	Condition	Min.	Typ.	Max.	Unit
Mounting torque	Screw : M3	0.59	0.69	0.78	N·m
Flatness of outer heat sink	Refer Fig.2-4-3	-30	—	+100	μm

Note: Recommend using plain washer (ISO7089-7094) in fastening the screws.

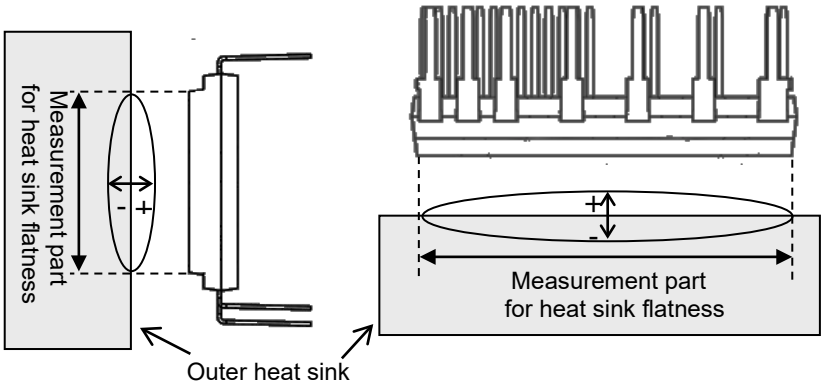


Fig.2-4-2 Measurement point of heat sink flatness

For effective heat dissipation, it is necessary to enlarge the contact area as much as possible to minimize the contact thermal resistance. Regarding the heat sink flatness (warp/concavity and convexity) on the module installation surface, the surface finishing-treatment should be within Rz12.

Evenly apply thermally conductive grease with 100μ-200μm thickness over the contact surface between a module and a heat sink, which is also useful for preventing corrosion. Furthermore, the grease should be with stable quality and long-term endurance within wide operating temperature range. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.3K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m·k). When applying grease and fixing heat sink, pay attention not to take air into grease. It might lead to make contact thermal resistance worse or loosen fixing in operation.

2.4.3 Soldering Conditions

The recommended soldering condition is mentioned as below.
(Note: The reflow soldering cannot be recommended for DIPIPM.)

(1) Flow (wave) Soldering

DIPIPM is tested on the condition described in Table 2-4-3 about the soldering thermostability, so the recommended conditions for flow (wave) soldering are soldering temperature is up to 270°C±5°C and the immersion time is within 9s.

However, the condition might need some adjustment based on flow condition of solder, the speed of the conveyer, the land pattern and the through hole shape on the PCB, etc.

It is necessary to confirm whether it is appropriate or not for your real PCB finally.

Table 2-4-3 Reliability test specification

Item	Condition
Soldering thermostability	270 ± 5°C, max. 9s

(2) Hand soldering

Since the temperature impressed upon the DIPIPM may change based on the soldering iron types (wattages, shape of soldering tip, etc.) and the land pattern on PCB, the unambiguous hand soldering condition cannot be decided.

As a general requirement of the temperature profile for hand soldering, the temperature of the root of the DIPIPM terminal should be kept under 150°C for considering glass transition temperature (Tg) of the package molding resin and the thermal withstand capability of internal chips. Therefore, it is necessary to check the DIPIPM terminal root temperature, solderability and so on in your real PCB, when configuring the soldering temperature profile. (It is recommended to set the soldering time as short as possible.)

For reference, the evaluation example of hand soldering with 50W soldering iron is described as below.

[Evaluation method]
a. Sample: PSSxxSF1F6
b. Evaluation procedure
- Put the soldering tip of 50W iron (temperature set to 400°C) on the terminal within 1mm from the toe. (The lowest heat capacity terminal (=control terminal) is selected.)
- Measure the temperature rise of the terminal root part by the thermocouple installed on the terminal root.

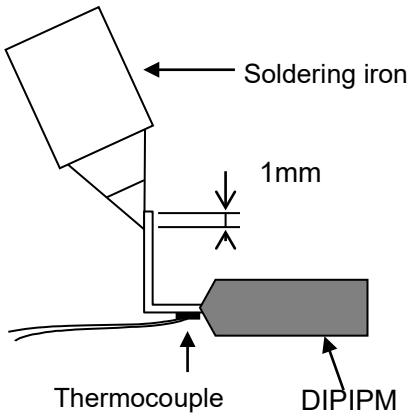


Fig.2-4-3 Heating and measuring point

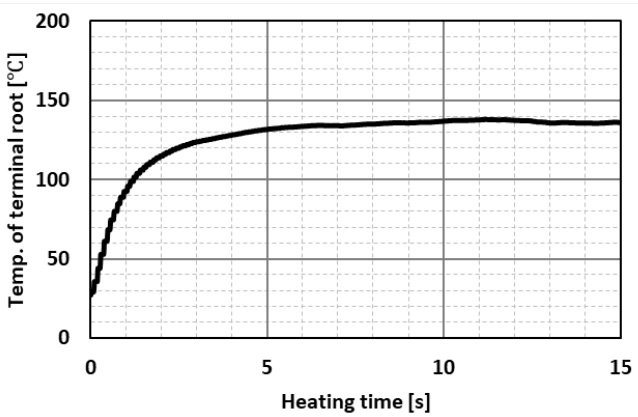


Fig.2-4-4 Temperature alteration of the terminal root (Example)

[Note]
For soldering iron, it is recommended to select one for semiconductor soldering (12~24V low voltage type, and the earthed iron tip) and with temperature adjustment function.

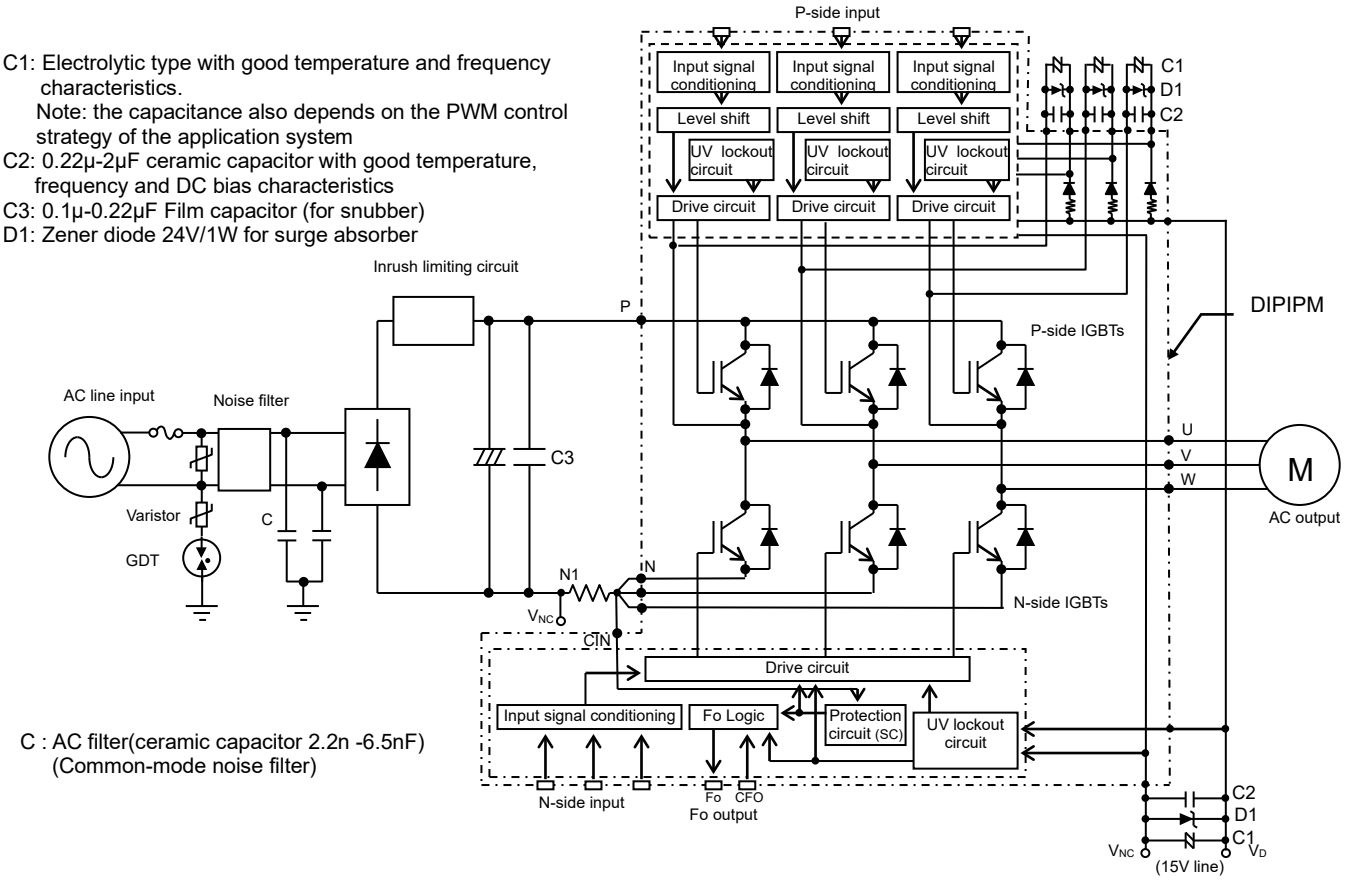
CHAPTER 3 SYSTEM APPLICATION GUIDANCE

3.1 Application Guidance

This chapter states Compact DIPIPM application method and interface circuit design hints.

3.1.1 System connection

C1: Electrolytic type with good temperature and frequency characteristics.
Note: the capacitance also depends on the PWM control strategy of the application system
C2: 0.22μ-2μF ceramic capacitor with good temperature, frequency and DC bias characteristics
C3: 0.1μ-0.22μF Film capacitor (for snubber)
D1: Zener diode 24V/1W for surge absorber



C : AC filter(ceramic capacitor 2.2n -6.5nF)
(Common-mode noise filter)

Fig.3-1-1 System block diagram (Example)

3.1.2 Interface Circuit (Direct Coupling Interface example for using one shunt resistor)

Fig.3-1-2 shows a typical application circuit of interface schematic, in which control signals are transferred directly input from a controller (e.g. MCU, DSP).

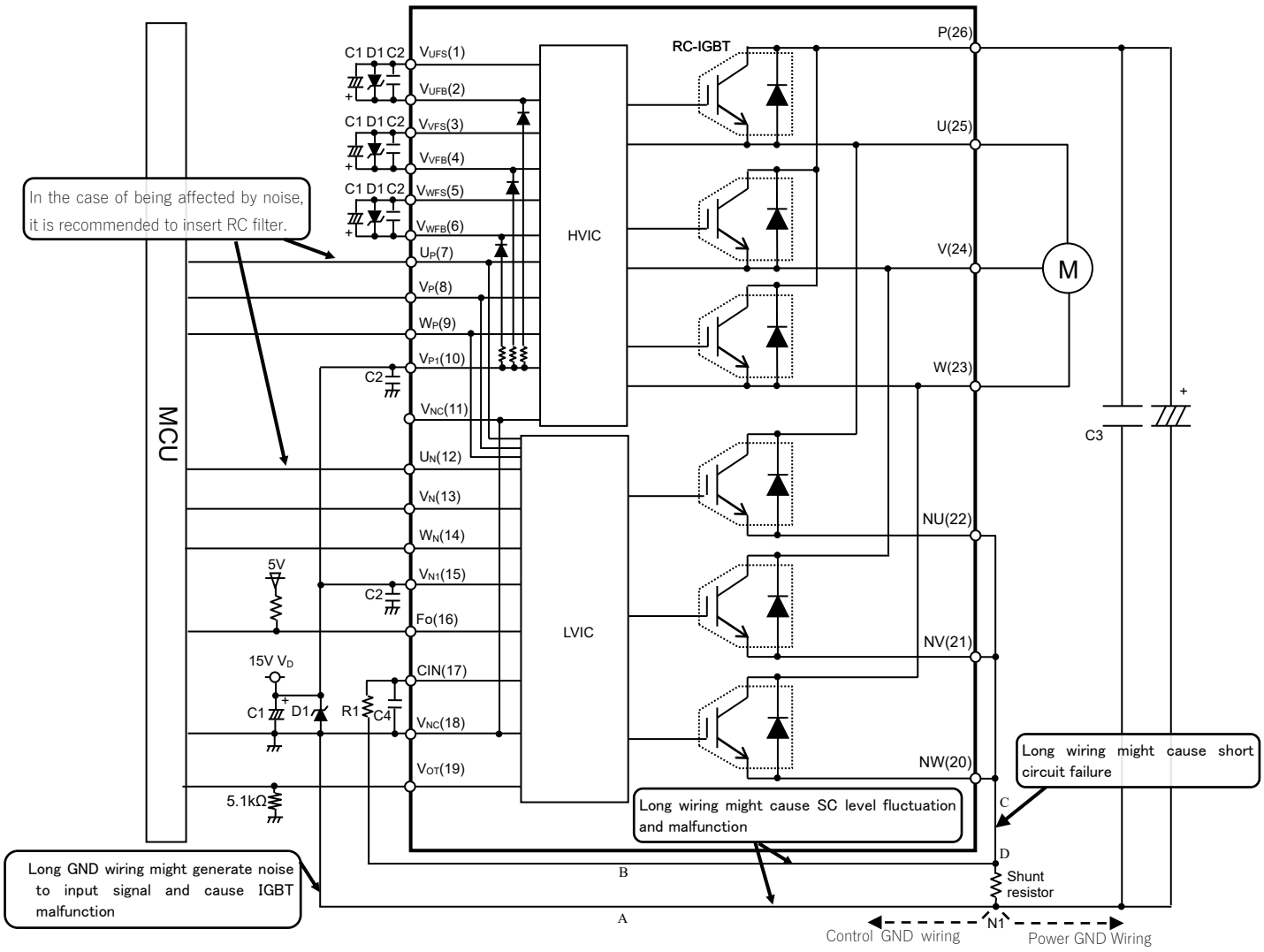


Fig.3-1-2 Interface circuit example except for common emitter type

(1) If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point N1 (near the terminal of shunt resistor).
(2) It is recommended to insert a Zener diode D1(24V/1W) between each pair of control supply terminals to prevent surge destruction.
(3) To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1μF or more snubber capacitor C3 between the P-N1 terminals is recommended.
(4) R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2μs. (1.5μs~2μs is recommended generally.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is necessary.
(5) To prevent malfunction, the wiring of A, B, C should be as short as possible.
(6) The point D at which the wiring to CIN filter is divided should be near the terminal of shunt resistor. NU, NV, NW terminals should be connected at near NU, NV, NW terminals when it is used by one shunt operation. Low inductance SMD type with tight tolerance, temp-compensated type is recommended for shunt resistor.
(7) All capacitors should be mounted as close to the terminals as possible. (C1: good temperature, frequency characteristic electrolytic type and C2:0.22μ-2μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.)
(8) Input logic is High-active. There is a 3.3kΩ(min.) pull-down resistor in the input circuit of IC. To prevent malfunction, the input wiring should be as short as possible. When using RC coupling, make the input signal level meet the turn-on and turn-off threshold voltage.
(9) Fo output is open drain type. It should be pulled up to power supply of MCU (e.g. 5V, 3.3V) by a resistor that makes I_{Fo} up to 1mA. (I_{FO} is estimated roughly by the formula of control power supply voltage divided by pull-up resistance. In the case of pulled up to 5V, 10kΩ (5kΩ or more) is recommended.)
(10) Thanks to built-in HVIC, direct coupling to MCU without any optocoupler or transformer isolation is possible.
(11) Pins 11 and 18 of the VNC (control power GND terminal) are internally connected. Use only one pin; leave the other pin in the NC (no connection) state.
(12) If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet dV/dt ≤+/-1V/μs, Vripple≤2Vp-p.
(13) For DIPIPM, it isn't recommended to drive same load by parallel connection with other phase IGBT or other DIPIPM.

3.1.3 Interface Circuit (Example of Opto-coupler Isolated Interface)

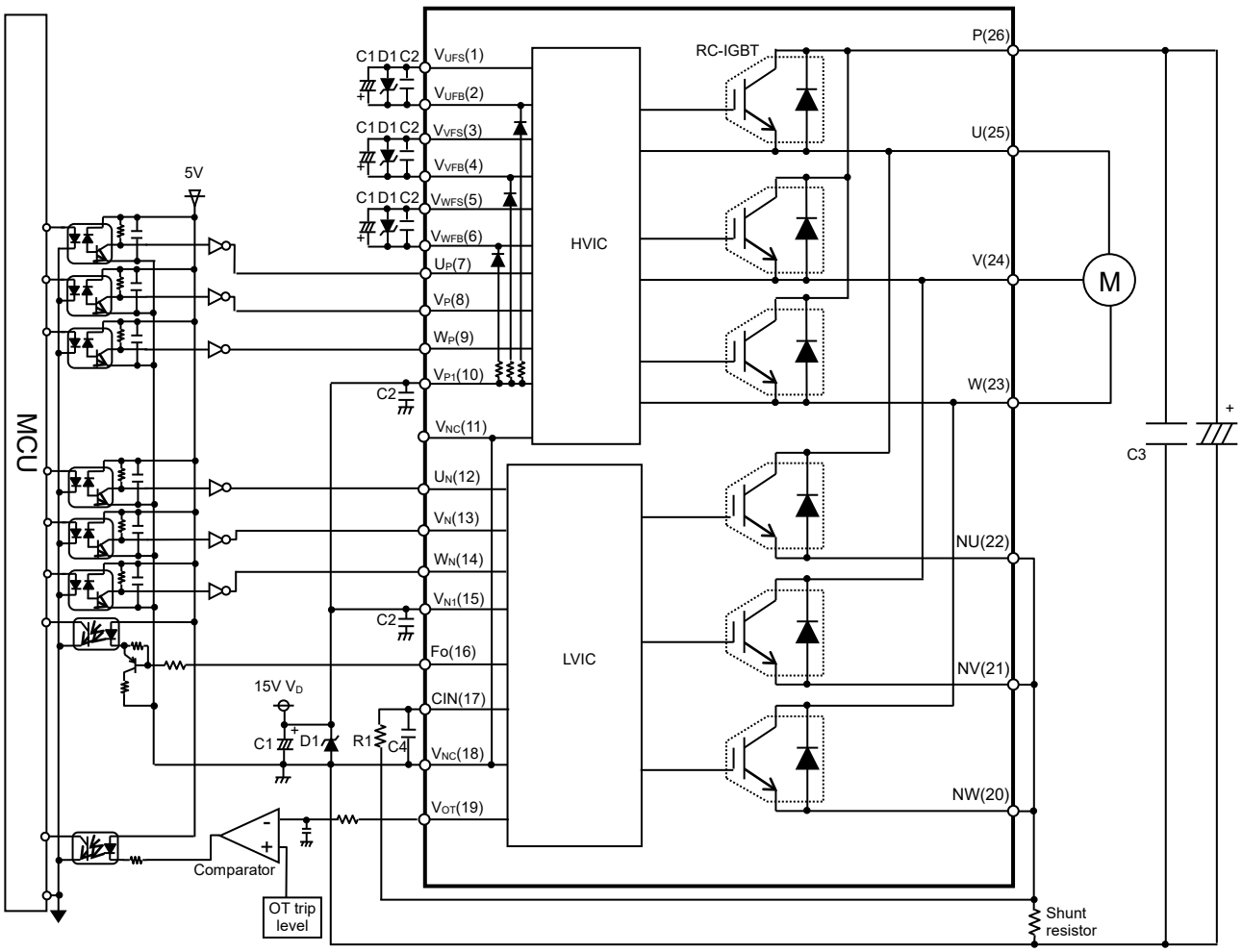


Fig.3-1-3 Interface circuit example with opto-coupler

Note:
(1) High speed (high CMR) opto-coupler is recommended.
(2) Fo terminal sink current for inverter part is max.5mA. It is recommended for driving coupler to apply buffer. To prevent Fo output from malfunctioning, it is recommended to make wiring from Fo terminal to buffer Tr and coupler as short as possible.
(3) About comparator circuit at V_{OT} output, it is recommended to design the input circuit with hysteresis because of preventing output chattering.

3.1.4 External SC Protection Circuit with Using Three Shunt Resistors

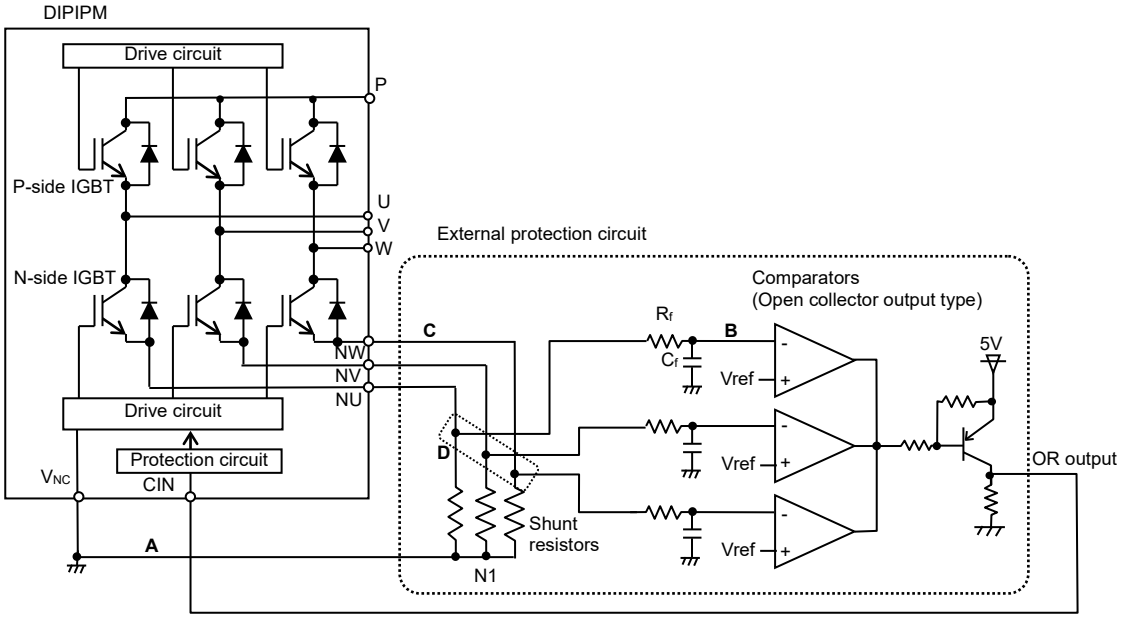


Fig.3-1-4 Interface circuit example

Note:

(1) It is necessary to set the time constant R_fC_f of external comparator input so that IGBT stops within 2μs when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on.
(2) The threshold voltage Vref should be set up the same rating of short circuit trip level (Vsc(ref) typ. 0.48V).
(3) Select the external shunt resistance so that SC trip-level is less than specified value.
(4) To avoid malfunction, the wiring A, B, C should be as short as possible.
(5) The point D at which the wiring to comparator is divided should be near the terminal of shunt resistor.
(6) OR output high level should be over 0.505V (=maximum Vsc(ref)).
(7) GND of Comparator, GND of Vref circuit and Cf should be not connected to power GND but to control GND wiring.

3.1.5 Circuits of Signal Input Terminals and Fo Terminal

(1) Internal Circuit of Control Input Terminals

DIPIPM is high-active input logic. 3.3kΩ(min) pull-down resistor is built-in each input circuits of the DIPIPM as shown in Fig.3-1-5, so external pull-down resistor is not needed.

Furthermore, by lowering the turn on and turn off threshold value of input signal as shown in Table 3-1-1, a direct coupling to 3V class microcomputer or DSP becomes possible.

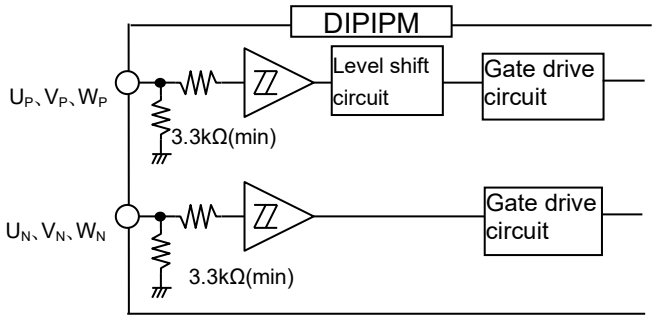


Fig.3-1-5 Internal structure of control input terminals

Table 3-1-1 Input threshold voltage ratings (Tj=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn-on threshold voltage	Vth(on)	U_P,V_P,W_P-V_{NC} terminals U_N,V_N,W_N-V_{NC} terminals	-	2.2	2.6	V
Turn-off threshold voltage	Vth(off)		0.8	1.4	-	
Threshold voltage hysterisis	Vth(hys)		0.35	0.8	-	

The wiring of each input should be patterned as short as possible. And if the pattern is long and the noise is imposed on the pattern, it may be effective to insert RC filter. There are limits for the minimum input pulse width in DIPIPM. The DIPIPM might make no response or delayed response, if the input pulse width (both on and off) is shorter than the specified value. For allowable minimum input pulse width, please refer to the datasheet for each product in detail.

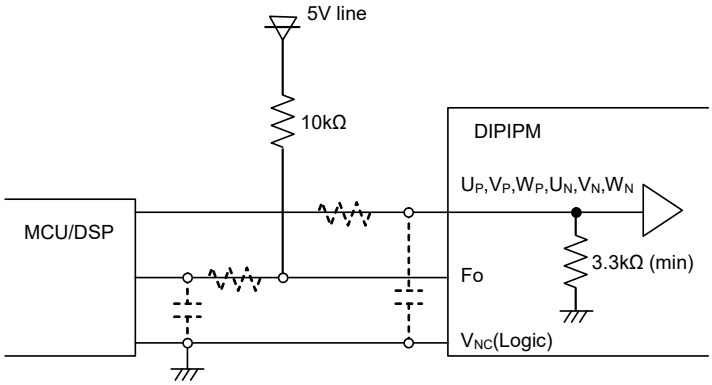


Fig.3-1-6 Control input connection

Note: The RC coupling (parts shown in the dotted line) at each input depends on user's PWM control strategy and the wiring impedance of the printed circuit board.
The DIPIPM signal input section integrates a 3.3kΩ(min) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

(2) Internal Circuit of Fo Terminal

F_O terminal is an open drain type, it should be pulled up to a 5V supply as shown in Fig.3-1-6. Fig.3-1-7 shows the typical V-I characteristics of Fo terminal. The maximum sink current of Fo terminal is 5mA. If opto-coupler is applied to this output, please pay attention to the opto-coupler drive ability.

Table 3-1-2 Electric characteristics of Fo terminal

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output voltage	V_{FOH}	V_{SC}=0V, Fo=10kΩ,5V pulled up	4.9	-	-	V
	V_{FOL}	V_{SC}=1V, Fo=1mA	-	-	0.95	V

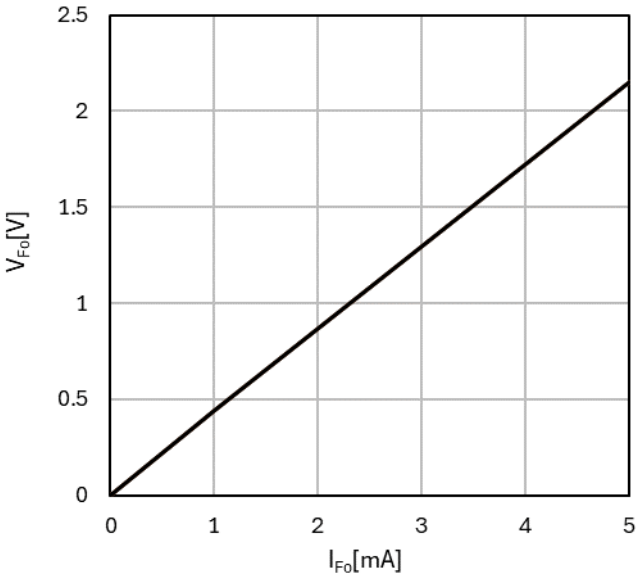


Fig.3-1-7 Fo terminal typical V-I characteristics (V_D=15V, T_j=25°C)

3.1.6 Snubber Circuit

To prevent DIPIPM from destruction by extra surge, the wiring length between the smoothing capacitor and P terminal (DIPIPM) – N1 points (shunt resistor terminal) should be as short as possible. Also, a 0.1μ~0.22μF/630V snubber capacitor should be mounted in the DC-link and near to P, N1.

Normally there are two positions ((1) or (2)) to mount a snubber capacitor as shown in Fig.3-1-8. Snubber capacitor should be installed in the position (2) to suppress surge voltage effectively. However, the charging and discharging currents generated by the wiring inductance and the snubber capacitor will flow through the shunt resistor, which might cause erroneous protection if this current is large enough.

To suppress the surge voltage maximally, the wiring at part-A (including shunt resistor parasitic inductance) should be as small as possible. A better wiring example is shown in location (3).

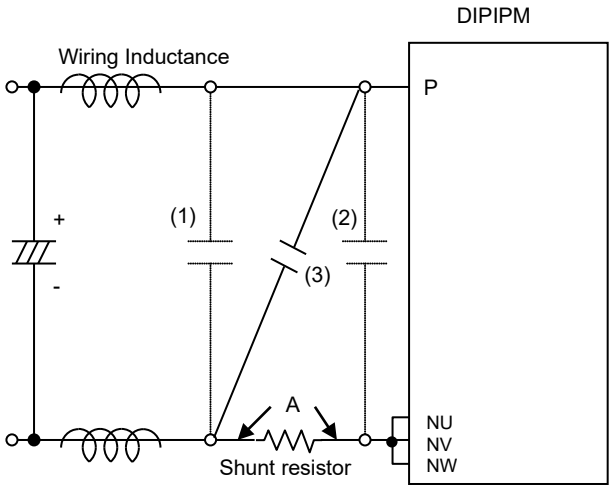


Fig.3-1-8 Recommended snubber circuit location

3.1.7 Recommended Wiring Method around Shunt Resistor

External shunt resistor is employed to detect short-circuit accident. A longer wiring between the shunt resistor and DIPIPM causes so much large surge that might damage built-in IC. To decrease the pattern inductance, the wiring between the shunt resistor and DIPIPM should be as short as possible and using low inductance type resistor such as SMD resistor instead of long-lead type resistor.

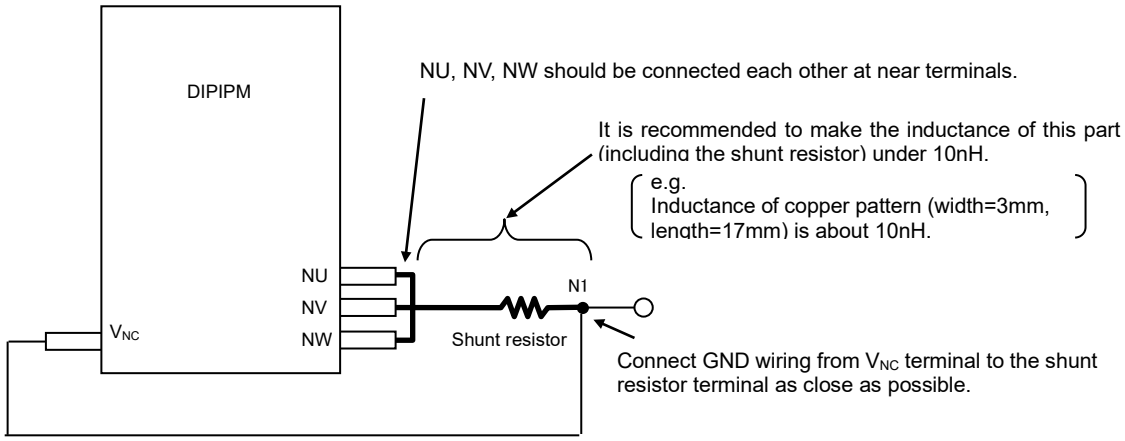


Fig.3-1-9 Wiring instruction (In the case of using with one shunt resistor)

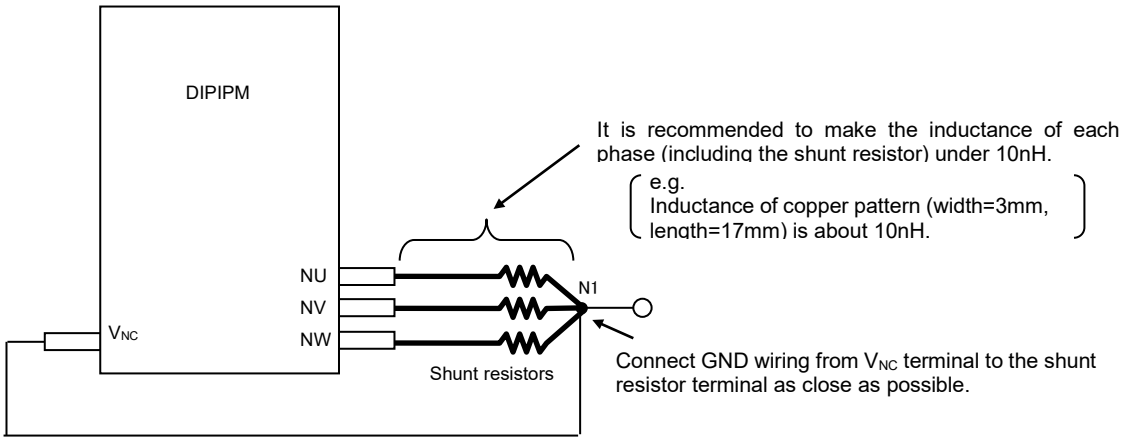


Fig.3-1-10 Wiring instruction (In the case of using with three shunt resistors)

Pattern wiring around the shunt resistor affects many influence for its DIPIPM operation. Please note that the wiring should be designed as short as possible to reduce its wiring inductance.

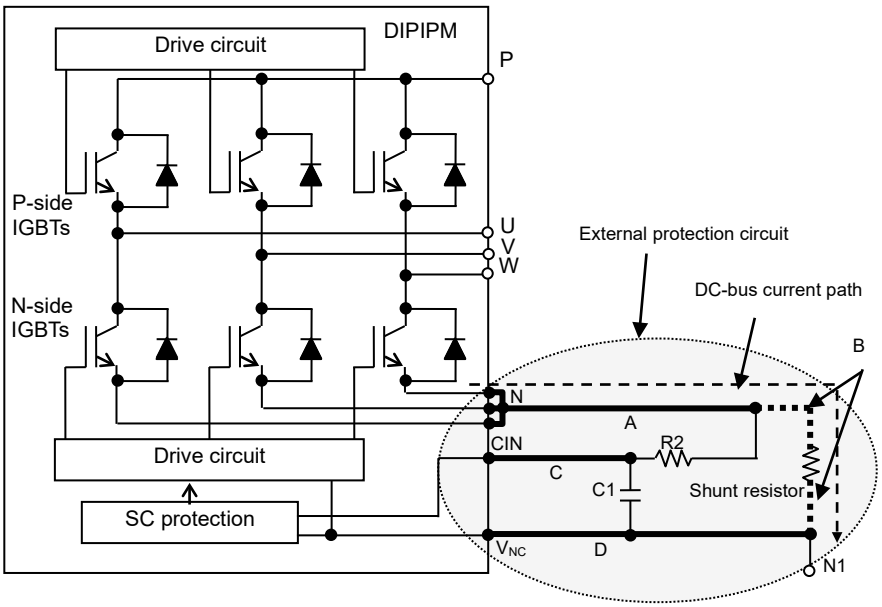


Fig.3-1-11 External protection circuit

(1) Influence of the part-A wiring

The ground of N-side IGBT gate is V_{NC}. If part-A wiring pattern in Fig.3-1-11 is too long, extra voltage generated by the wiring parasitic inductance will result the potential of IGBT emitter variation during switching operation. Please install shunt resistor as close to the N terminal as possible.

(2) Influence of the part-B wiring

The part-B wiring affects SC protection level. SC protection works by detecting the voltage of the CIN terminals. If part-B wiring is too long, extra surge voltage generated by the wiring inductance will lead to deterioration of SC protection level. It is necessary to connect CIN and V_{NC} terminals directly to the two ends of shunt resistor and avoid long wiring.

(3) Influence of the part-C wiring pattern

C1R2 filter is added to remove noise influence occurring on shunt resistor. Filter effect will dropdown and noise will easily superimpose on the wiring if part-C wiring is too long. It is necessary to install the C1R2 filter near CIN, V_{NC} terminals as close as possible.

(4) Influence of the part-D wiring pattern

Part-D wiring pattern gives influence to all the items described above, maximally shorten the GND wiring is expected.

3.1.8 Precaution for Wiring on PCB

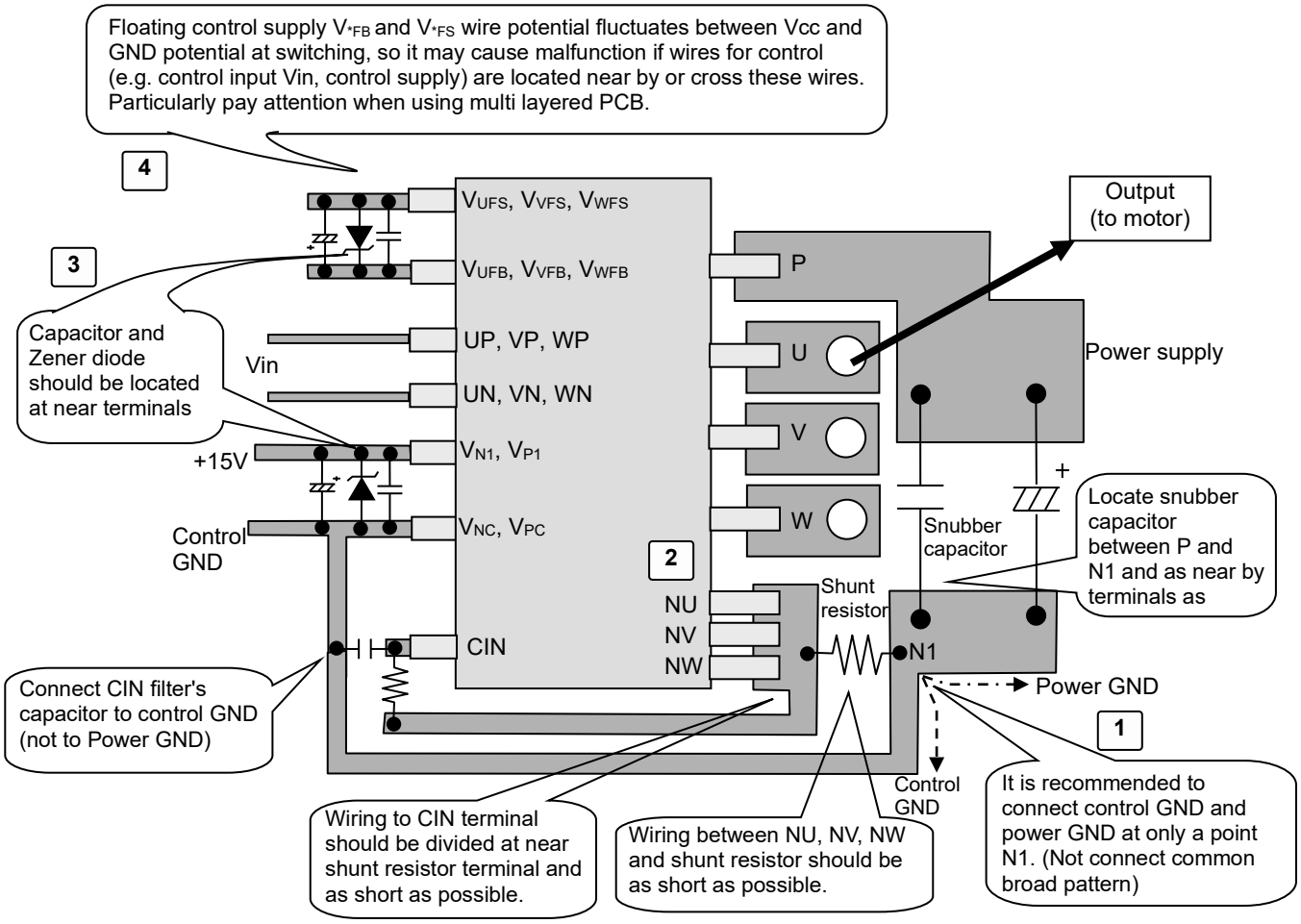


Fig.3-1-12 Precaution for wiring on PCB

The case example of trouble due to PCB pattern

	Case example	Matter of trouble
1	•Control GND pattern overlaps power GND pattern.	The surge, generated by the wiring pattern and di/dt of noncontiguous big current flows to power GND, transfers to control GND pattern. It causes the control GND level fluctuation, so that the input signal based on the control GND fluctuates too. Then the arm short might occur.
	•Ground loop pattern exists.	Stray current flows to GND loop pattern, so that the control GND level and input signal level (based on the GND) fluctuates. Then the arm short might occur.
2	•Large inductance of wiring between N and N1 terminal	Long wiring pattern has big parasitic inductance and generates high surge when switching. This surge causes the matter as below. •HVIC malfunction due to VS voltage (output terminal potential) dropping excessively. •LVIC surge destruction
3	Capacitors or zener diodes are nothing or located far from the terminals.	IC surge destruction or malfunction might occur.
4	The input lines are located parallel and close to the floating supply lines for P-side drive.	Cross talk noise might be transferred through the capacitance between these floating supply lines and input lines to DIPIPM. Then incorrect signals are input to DIPIPM input, and arm short (short circuit) might occur.

3.1.9 Parallel operation of DIPIPM

Fig.3-1-13 shows the circuitry of parallel connection of two DIPIPMs. Route (1) and (2) indicate the gate charging path of low-side IGBT in DIPIPM No.1 & 2 respectively. In the case of DIPIPM 1, the parasitic inductance becomes large by long wiring and it might have a negative effect on DIPIPM's switching operation. (Chare operation of bootstrap capacitor for high-side might be affected too.) Also, such a wiring makes DIPIPM be affected by noise easily, then it might lead to malfunction. If more DIPIPMs are connected in parallel, GND pattern becomes longer and the influence to other circuit (protection circuit etc.) by the fluctuation of GND potential is conceivable, therefore parallel connection is not recommended.

Because DIPIPM doesn't consider the fluctuation of characteristics between each phase definitely, it cannot be recommended to drive same load by parallel connection with other phase IGBT or IGBT of other DIPIPM.

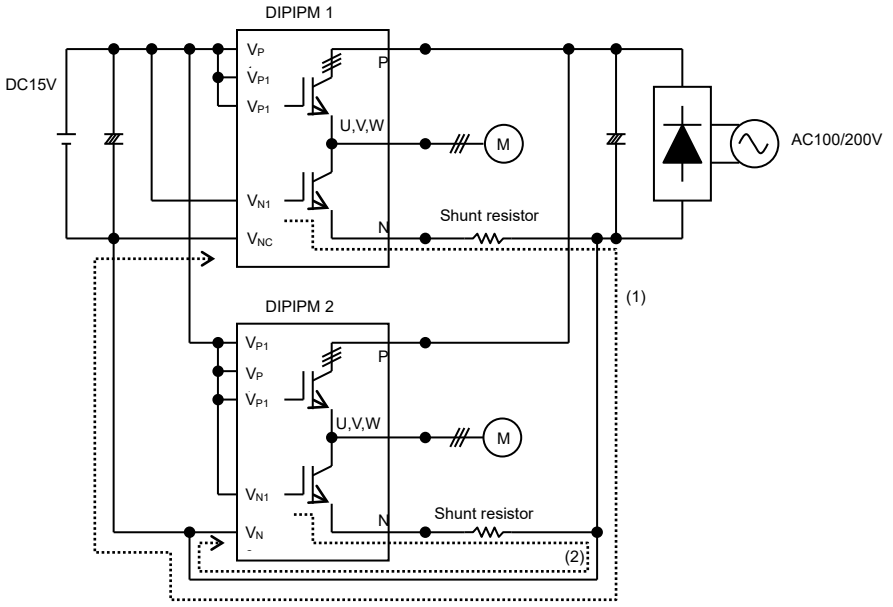


Fig.3-1-13 Parallel operation

3.1.10 SOA of Compact DIPIPM

The following describes the SOA (Safety Operating Area) of the Compact DIPIPM.

V_{CES}: Maximum rating of IGBT collector-emitter voltage

V_{CC}: Supply voltage applied on P-N terminals

$V_{CC(surge)}$: Total amount of V_{CC} and surge voltage generated by the wiring inductance and the DC-link capacitor

$V_{CC(PROT)}$: DC-link voltage that DIPIPM can protect itself

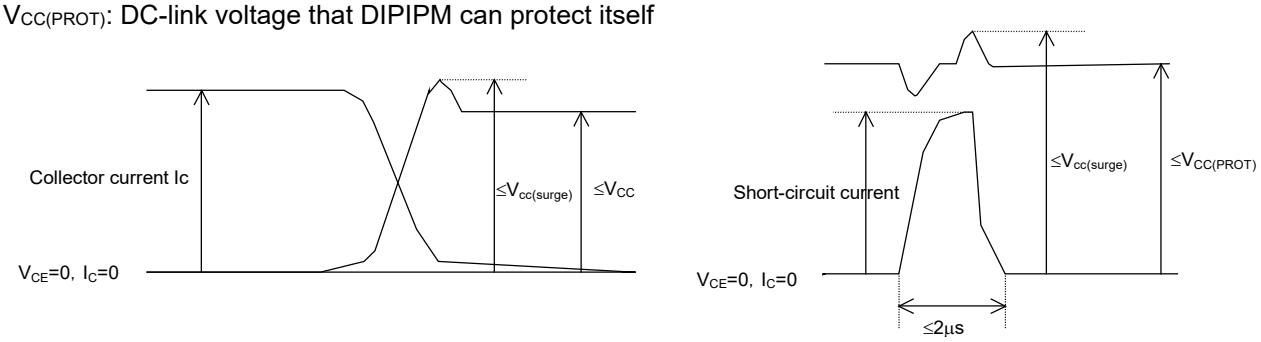


Fig.3-1-14 SOA at switching mode and short-circuit mode

In case of Switching

V_{CES} represents the maximum voltage rating (600V) of the IGBT. By subtracting the surge voltage (100V or less) generated by internal wiring inductance from V_{CES} is $V_{CC(surge)}$, that is 500V. Furthermore, by subtracting the surge voltage (50V or less) generated by the wiring inductor between DIPIPM and DC-link capacitor from $V_{CC(surge)}$ derives V_{CC}, that is 450V.

In case of Short-circuit

V_{CES} represents the maximum voltage rating (600V) of the IGBT . By Subtracting the surge voltage (100V or less) generated by internal wiring inductor from V_{CES} is $V_{CC(surge)}$, that is, 500V. Furthermore, by subtracting the surge voltage (100V or less) generated by the wiring inductor between the DIPIPM and the electrolytic capacitor from $V_{CC(surge)}$ derives V_{CC}, that is, 400V.

3.1.11 SCSOA

Fig.3-1-15~16 shows the typical SCSOA performance curves of each product.
(Conditions: Vcc=400V, Tj=150°C at initial state, V_{CES}≤600V, $V_{CC(surge)}$≤500V(surge included), non-repetitive, 2m load.)

In the case of PSS30SF1F6, it can shutdown safely an SC current that is about 9 times of its current rating under the conditions if the IGBT conducting period is less than about 2.7μs. Since the SCSOA operation area will vary with the control supply voltage, DC-link voltage, and etc, it is necessary to set time constant of RC filter with a margin.

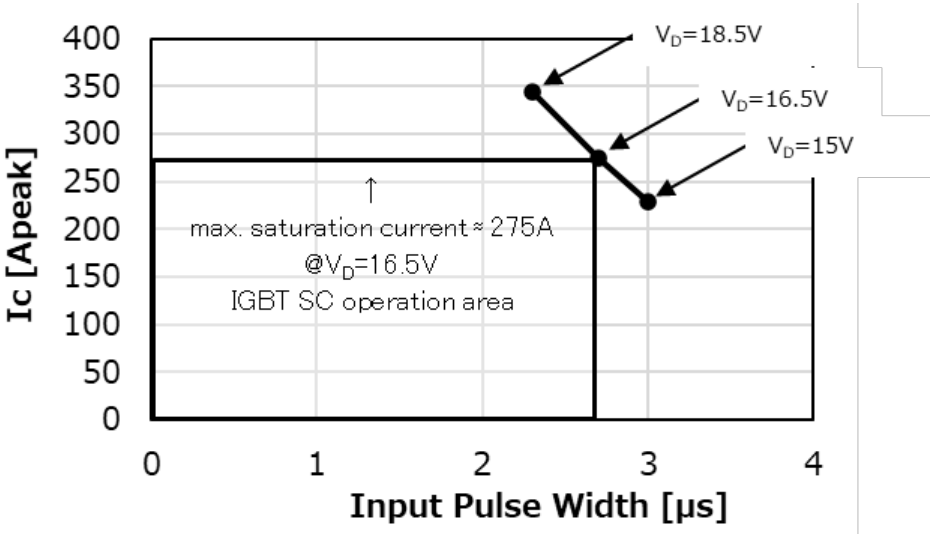


Fig.3-1-15 Typical SCSOA curve of PSS30SF1F6

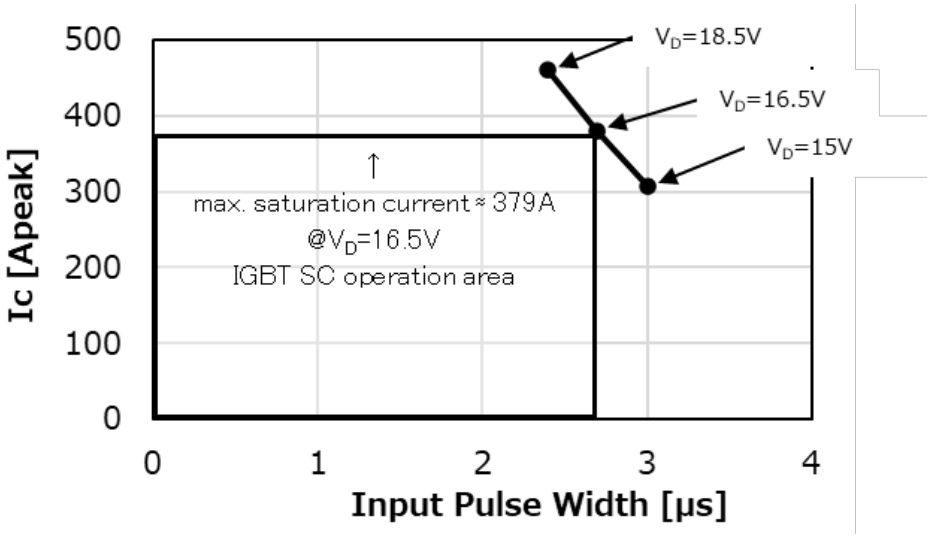


Fig.3-1-16 Typical SCSOA curve of PSS50SF1F6

3.1.12 Power Life Cycles

When DIPIPM is in operation, repetitive temperature variation will happen on the IGBT junctions (ΔTj). The amplitude and the times of the junction temperature variation affect the device lifetime.

Fig.3-1-17 shows the IGBT power cycle curve as a function of average junction temperature variation (ΔTj).

(The curve is a regression curve based on 3 points of ΔTj=46, 88, 98K regarding failure rate of 0.1%, 1% and 10%. These data are obtained from the reliability test of intermittent conducting operation)

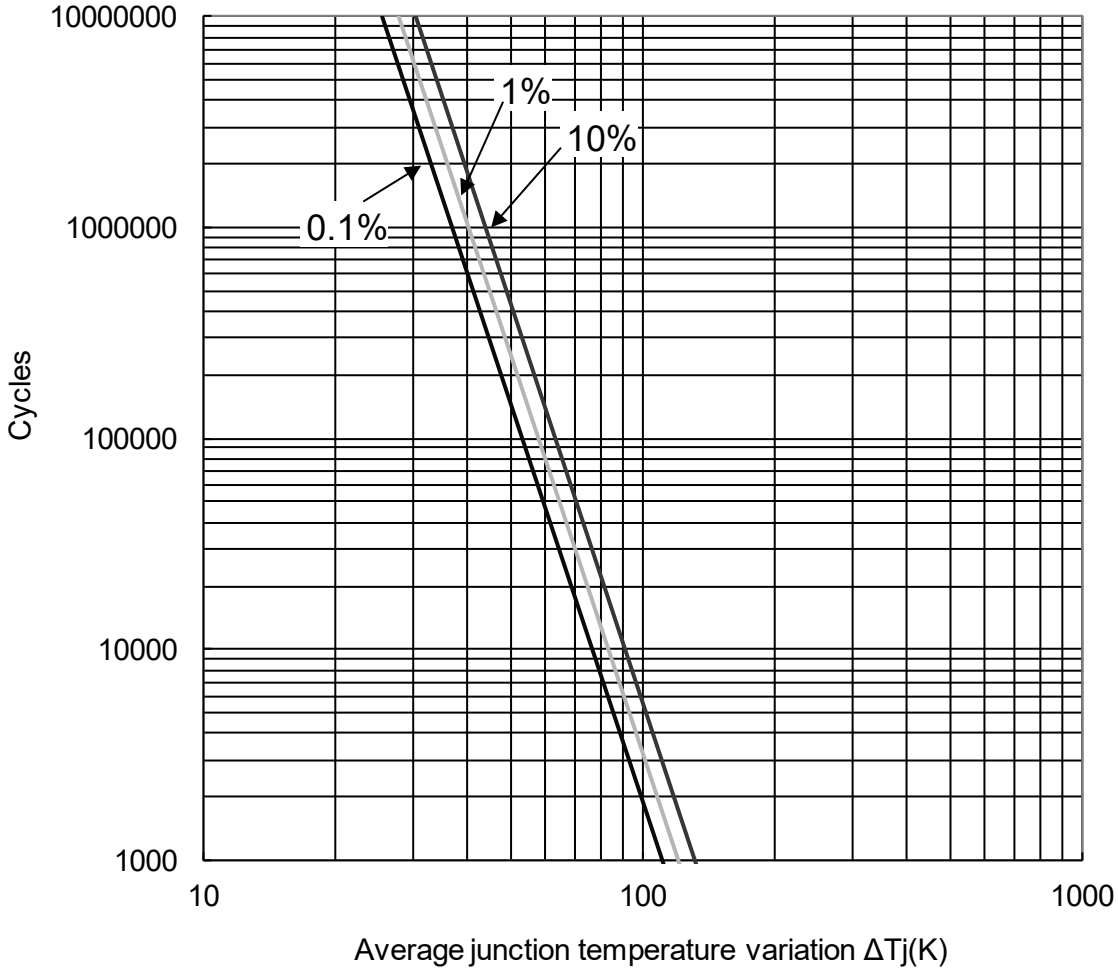


Fig.3-1-17 Power cycle curve

3.2 Power Loss and Thermal Dissipation Calculation

3.2.1 Power Loss Calculation

Simple expressions for calculating average power loss are given below:

● Scope

The power loss calculation intends to provide users a way of selecting a matched power device for their VVVF inverter application. However, it is not expected to use for limit thermal dissipation design.

● Assumptions

(1) PWM controlled VVVF inverter with sinusoidal output;
(2) PWM signals are generated by the comparison of sine waveform and triangular waveform.
(3) Duty amplitude of PWM signals varies between $\frac{1-D}{2} \sim \frac{1+D}{2}$ (%/100), (D: modulation depth).
(4) Output current various with Icp·sinx and it does not include ripple.
(5) Power factor of load output current is cosθ, ideal inductive load is used for switching.

● Expressions Derivation

PWM signal duty is a function of phase angle x as $\frac{1+\mathrm{D}\times\sin\mathrm{x}}{2}$ which is equivalent to the output voltage variation. From the power factor cosθ, the output current and its corresponding PWM duty at any phase angle x can be obtained as below:

$$Output\ \ current = Icp \times \sin x$$

$$PWM\ \ \ Duty = \frac{1+D\times\sin(x+\theta)}{2}$$

Then, $V_{CE(sat)}$ and V_{EC} at the phase x can be calculated by using a linear approximation:

$$Vce(sat) = Vce(sat)(@\,Icp \times \sin x)$$
$$Vec = (-1) \times Vec(@\,Iecp(=Icp) \times \sin x)$$

Thus, the static loss of IGBT is given by:

$$\frac{1}{2\pi}\int_0^{\pi}(Icp \times sin\,x) \times Vce(sat)(@Icp \times sin\,x) \times \frac{1+D\,sin(x+\theta)}{2} \cdot dx$$

Similarly, the static loss of free-wheeling diode is given by:

$$\frac{1}{2\pi}\int_{\pi}^{2\pi}((-1) \times Icp \times sin\,x)((-1) \times Vec(@Icp \times sin\,x) \times \frac{1+D\,sin(x+\theta)}{2} \cdot dx$$

On the other hand, the dynamic loss of IGBT, which does not depend on PWM duty, is given by:

$$\frac{1}{2\pi}\int_0^{\pi}(Psw(on)(@Icp \times sin\,x) + Psw(off)(@Icp \times sin\,x)) \times fc \cdot dx$$

FWDi recovery characteristics can be approximated by the ideal curve shown in Fig.3-2-1, and its dynamic loss can be calculated by the following expression:

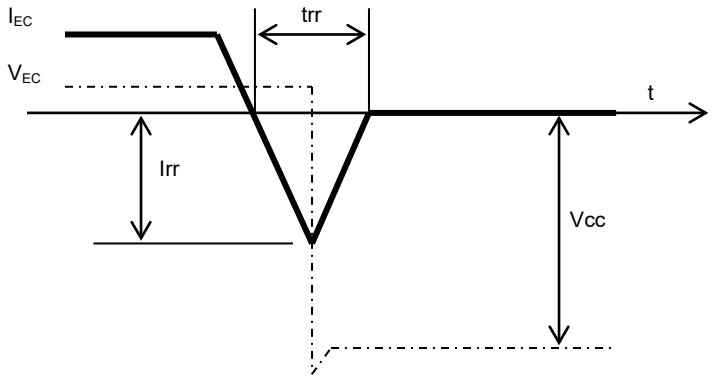


Fig.3-2-1 Ideal FWDi recovery characteristics curve

$$Psw = \frac{Irr \times Vcc \times trr}{4}$$

Recovery occurs only in the half cycle of the output current, thus the dynamic loss is calculated by:

$$\frac{1}{2}\int_{\pi}^{2\pi} \frac{Irr(@Icp \times \sin x) \times Vcc \times trr(@Icp \times \sin x)}{4} \times fc \cdot dx$$

$$= \frac{1}{8}\int_{\rho}^{2\pi} Irr(@Icp \times \sin x) \times Vcc \times trr\,(@Icp \times \sin x) \times fc \cdot dx$$

- Attention of applying the power loss simulation for inverter designs
  - Divide the output current period into fine-steps and calculate the losses at each step based on the actual values of PWM duty, output current, $V_{CE(sat)}$, V_{EC}, and Psw corresponding to the output current. The worst condition is most important.
  - PWM duty depends on the signal generating way.
  - The relationship between output current waveform or output current and PWM duty changes with the way of signal generating, load, and other various factors. Thus, calculation should be carried out on the basis of actual waveform data.
  - $V_{CE(sat)}$,V_{EC} and Psw(on, off) should be the values at Tj=125°C.

3.2.2 Temperature Rise Considerations and Calculation Example

Fig.3-2-2 shows the typical characteristics of allowable motor rms current versus carrier frequency under the following inverter operating conditions based on power loss simulation results.

Conditions: V_{CC}=300V, V_D=V_{DB}=15V, PF=0.8, M=1.0, Typ value, Tj=125°C, Tc=100°C, ΔT(j-c)=25K, Rth(j-c)=Max., 3-phase PWM modulation, 60Hz sine waveform output

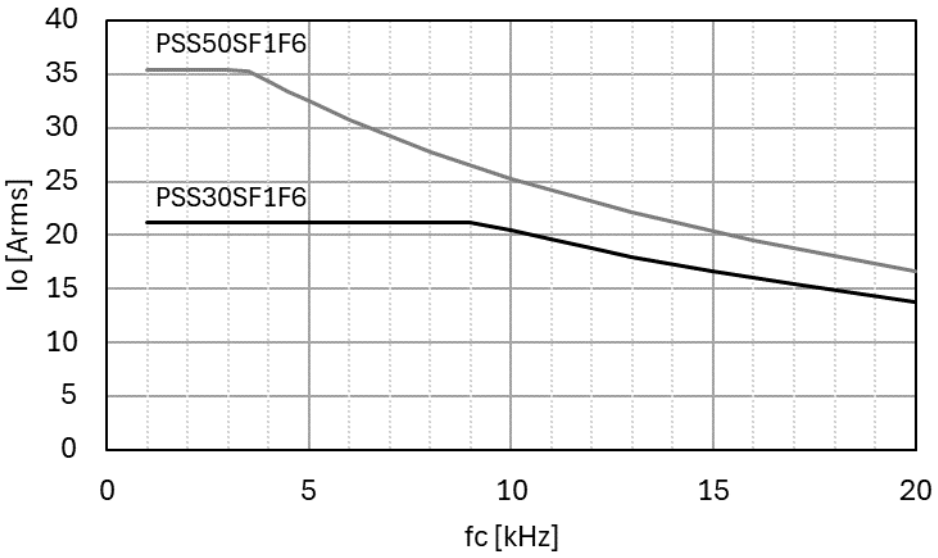


Fig.3-2-2 Effective current-carrier frequency characteristics

Fig.3-2-2 shows an example of estimating allowable inverter output rms current under different carrier frequency and permissible maximum operating temperature condition (Tc=100°C. Tj=125°C). The results may change for different control strategy and motor types. Anyway please ensure that there is no large current over device rating flowing continuously.

The inverter loss can be calculated by the free power loss simulation software is uploaded to the web site. URL: http://www.MitsubishiElectric.com/semiconductors/

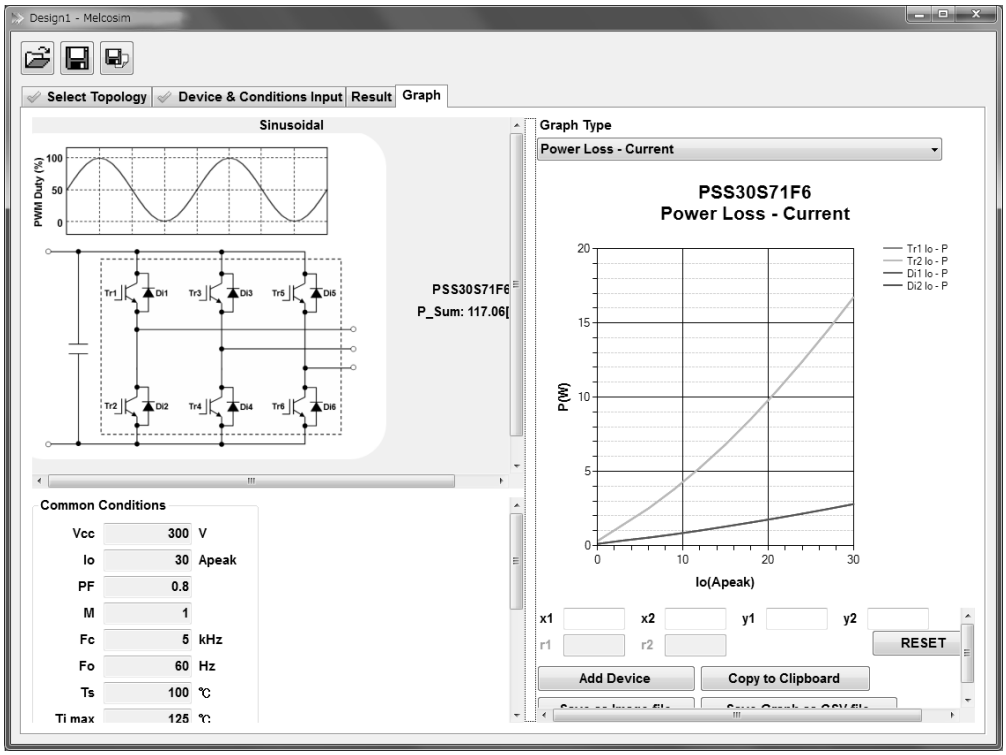


Fig.3-2-3 Loss simulator screen image

3.2.3 Installation of thermocouple

Installation of thermocouple for measurement of DIPIPM case temperature is shown below.

Point for installing thermocouple in heat sink is shown in Fig.3-2-4. In some control schemes, temperature measurement point at the following may not be highest case temperature. In such cases, it is necessary to change the measurement point to that under the highest power chip. (Refer previous figure of power chip position.)

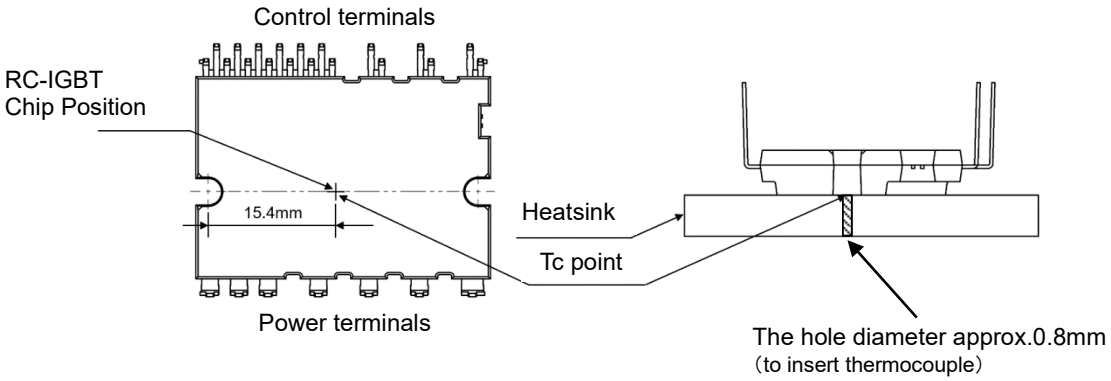


Fig. 3-2-4 Point for installing thermocouple in external heat sink

Installation of thermocouple is shown in Fig. 3-2-5. After making a hole under the chip with largest loss into the heat sink, the thermocouple is inserted in this hole and fixed by hammering around the hole with a centerpunch. After fixing the thermocouple, please sandpaper the thermocouple installing surface to make flat surface.

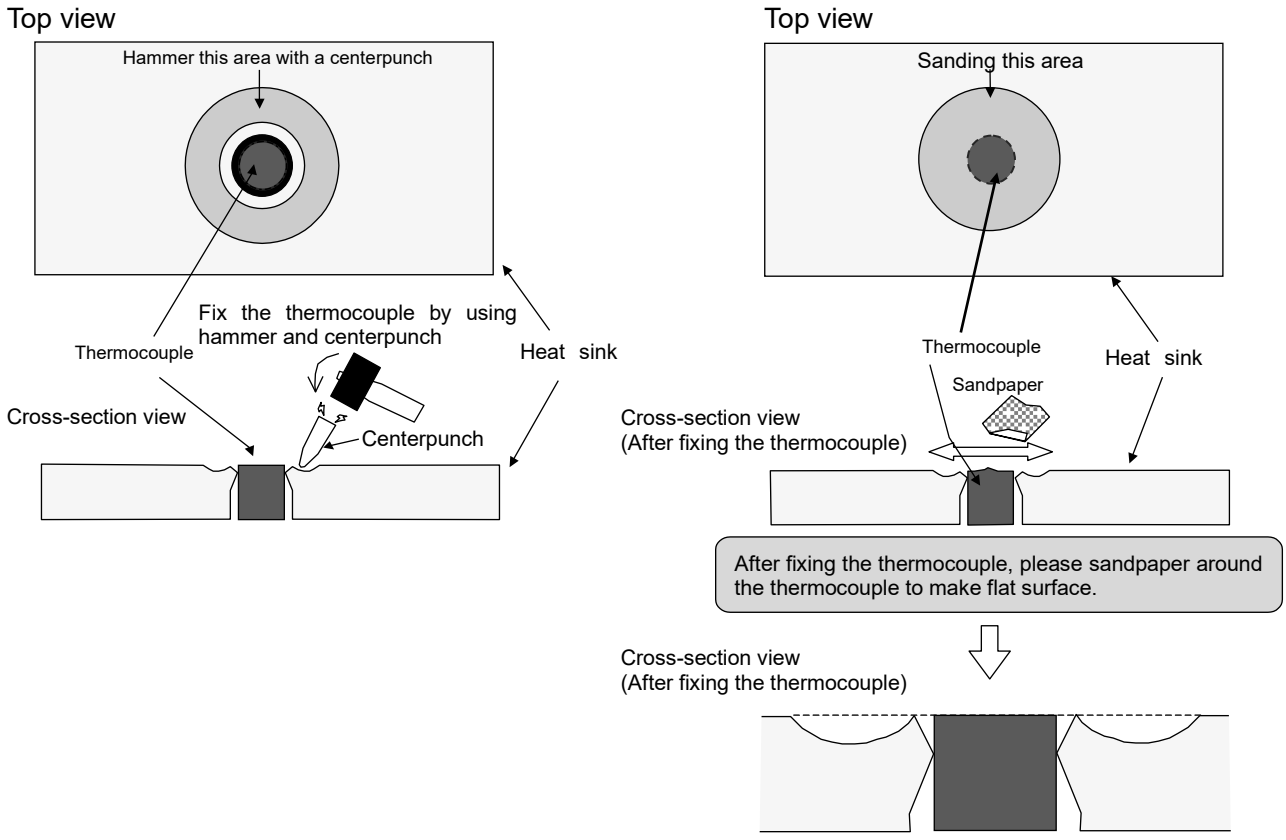


Fig. 3-2-5 Example of installation of thermocouple

3.3 Noise and ESD Withstand Capability

3.3.1 Evaluation Circuit of Noise Withstand Capability

Compact DIPIPM series have been confirmed to be with over +/-2.0kV noise withstand capability by the noise evaluation under the conditions shown in Fig.3-3-1. However, noise withstand capability greatly depends on the test environment, the wiring patterns of control substrate, parts layout, and other factors; therefore, an additional confirmation on prototype is necessary.

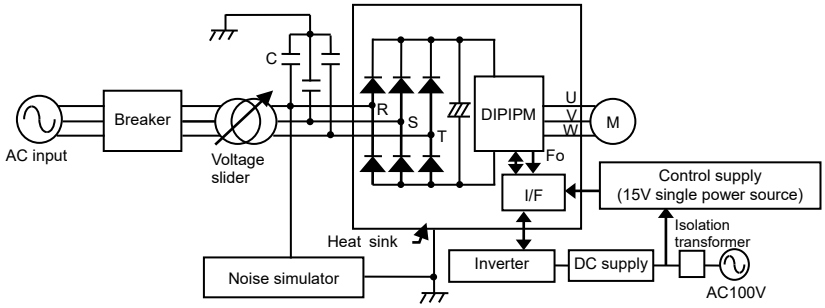


Fig.3-3-1 Noise withstand capability evaluation circuit

Note:

C1: AC line common-mode filter 4700pF, PWM signals are input from microcomputer by using opto-couplers, 15V single power supply, Test is performed with IM

Test conditions

V_{CC}=300V, V_D=15V, Ta=25°C, no load

Scheme of applying noise: From AC line (R, S, T), Period T=16ms, Pulse width tw=0.05-1μs, input in random

3.3.2 Countermeasures and Precautions

DIPIPM improves noise withstand capabilities by reducing parts quantity, lowering internal wiring parasitic inductance, and reducing leakage current. But when the noise affects on the control terminals of DIPIPM (due to wiring pattern on PCB), the short circuit or malfunction of SC protection may occur. In that case, countermeasures below are recommended.

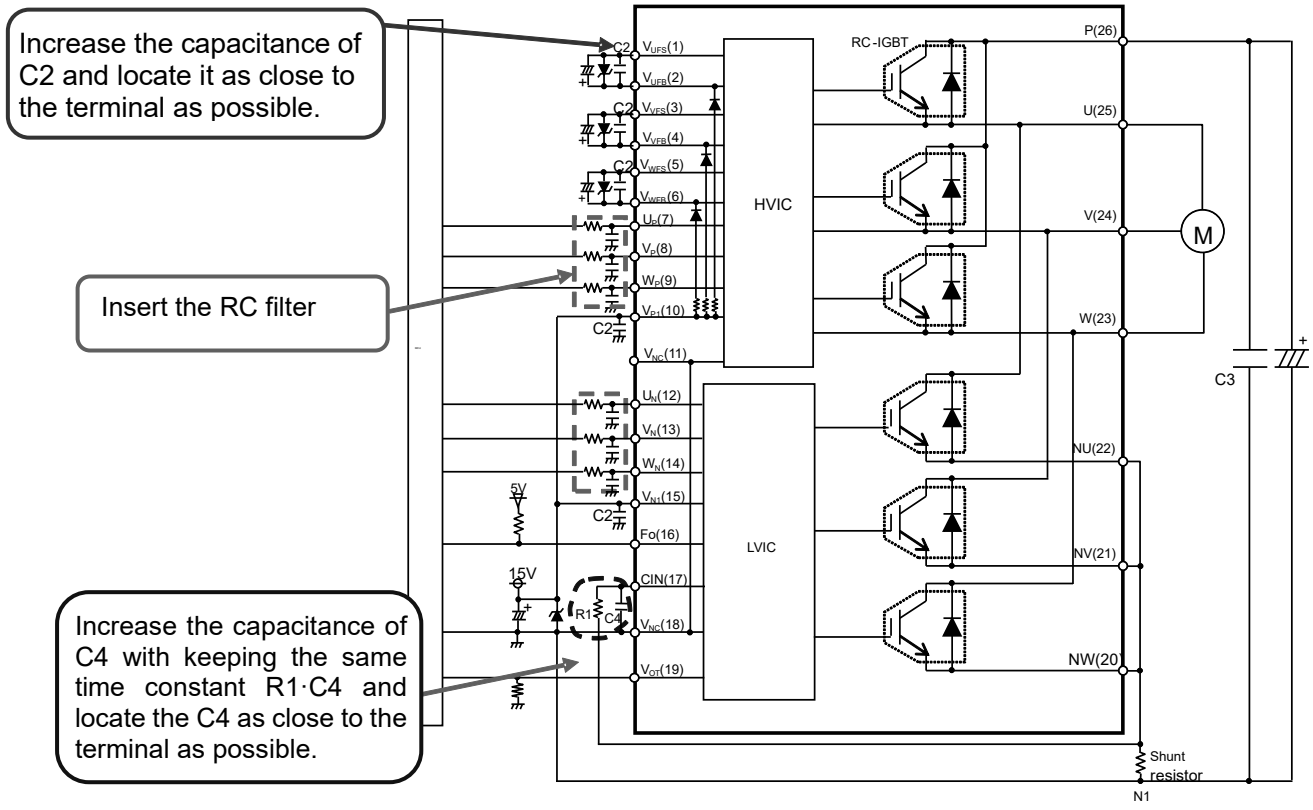


Fig.3-3-2 Example of countermeasures for inverter part

3.3.3 Static Electricity Withstand Capability

DIPIPM has been confirmed to be with typical +/-1kV or more withstand capability against static electricity from the following tests shown in Fig. 3-3-3, 4. HBM method: C=100pF, R=1.5kΩ.

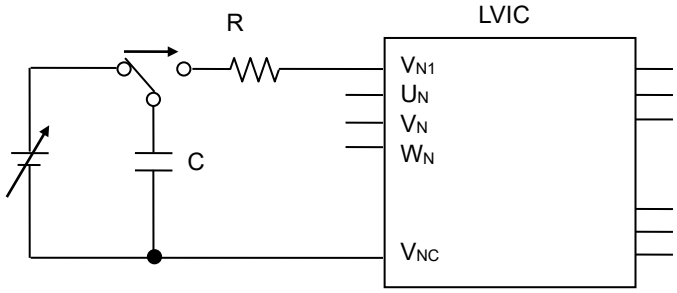


Fig.3-3-3 LVIC terminal Surge Test circuit

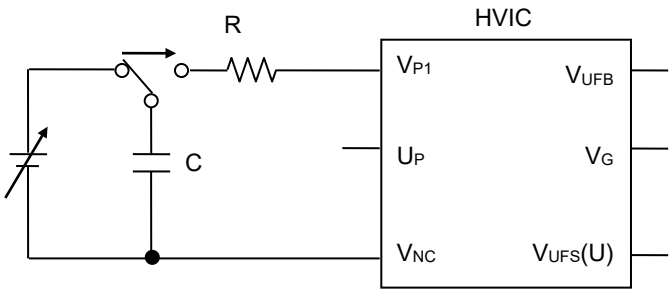


Fig.3-3-4 HVIC terminal Surge Test circuit

Conditions: Surge voltage is increased by 0.1kV step and only one surge pulse is impressed at each voltage. (Limit voltage of surge simulator: ±4.0kV, Judgment method; change in V-I characteristic)

CHAPTER 4 Bootstrap Circuit Operation

4.1 Bootstrap Circuit Operation

For three phase inverter circuit driving, normally four isolated control supplies (three for P-side driving and one for N-side driving) are necessary. But using floating control supply with bootstrap circuit can reduce the number of isolated control supplies from four to one (N-side control supply).

Bootstrap circuit consists of a bootstrap diode (BSD), a bootstrap capacitor (BSC) and a current limiting resistor. (Compact DIPIPM series integrates BSD and limiting resistor and can make bootstrap circuit by adding outer BSC only.) It uses the BSC as a control supply for driving P-side IGBT. The BSC supplies gate charge when P-side IGBT turning ON and circuit current of logic circuit on P-side driving IC. (Fig.4-1-2) Since a capacitor is used as substitute for isolated supply, its supply capability is limited. This floating supply driving with bootstrap circuit is suitable for small supply current products like DIPIPM.

Charge consumed by driving circuit is re-charged from N-side 15V control supply to BSC via current limiting resistor and BSD when voltage of output terminal (U, V or W) goes down to GND potential in inverter operation. But there is the possibility that enough charge doesn't perform due to the conditions such as switching sequence, capacitance of BSC and so on. Deficient charge leads to low voltage of BSC and might work under voltage protection (UV). This situation makes the loss of P-side IGBT increase by low gate voltage or stop switching. So, it is necessary to consider and evaluate enough for designing bootstrap circuit. For more detailed information about driving by the bootstrap circuit, refer the DIPIPM application note "*Bootstrap Circuit Design Manual*"

The BSD characteristics for Compact DIPIPM series and the circuit current characteristics in switching situation of P-side IGBT are described as below.

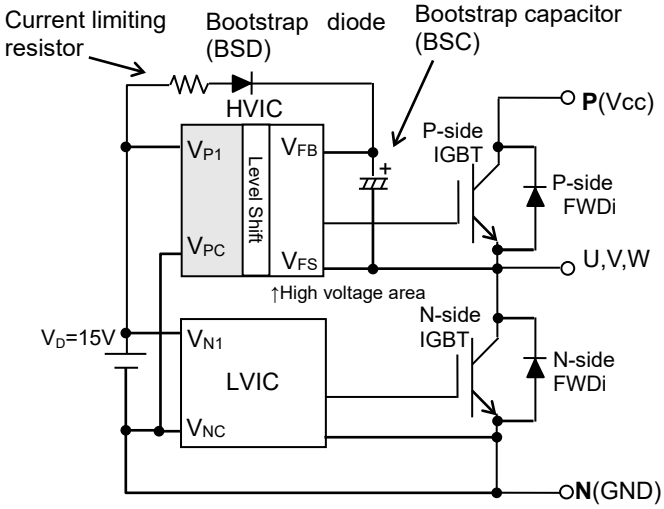


Fig.4-1-1 Bootstrap Circuit Diagram

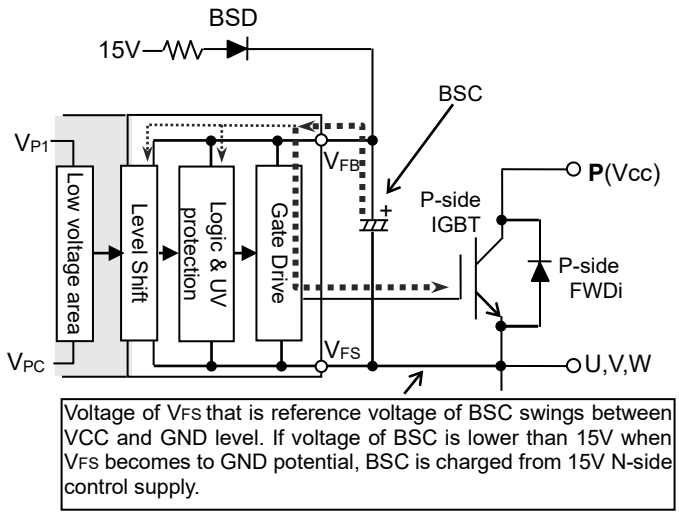


Fig.4-1-2 Bootstrap Circuit Diagram

4.2 Bootstrap Supply Circuit Current at Switching State

Bootstrap supply circuit current I_{DB} at steady state is maximum 0.55mA. But at switching state, because gate charge and discharge are repeated by switching, the circuit current exceeds 0.55mA and increases proportional to carrier frequency. For reference, Fig.4-2-1, 4-2-2 show typical I_{DB} - carrier frequency fc characteristics for PSSxxSF1F6.
(Conditions: V_D=V_{DB}=15V, Tj=125°C, Vcc=450V)

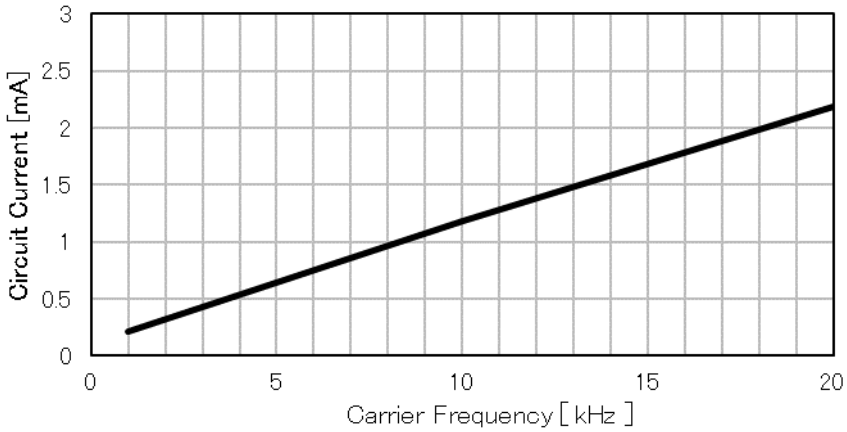


Fig.4-2-1 I_{DB} vs. Carrier frequency for PSS30SF1F6

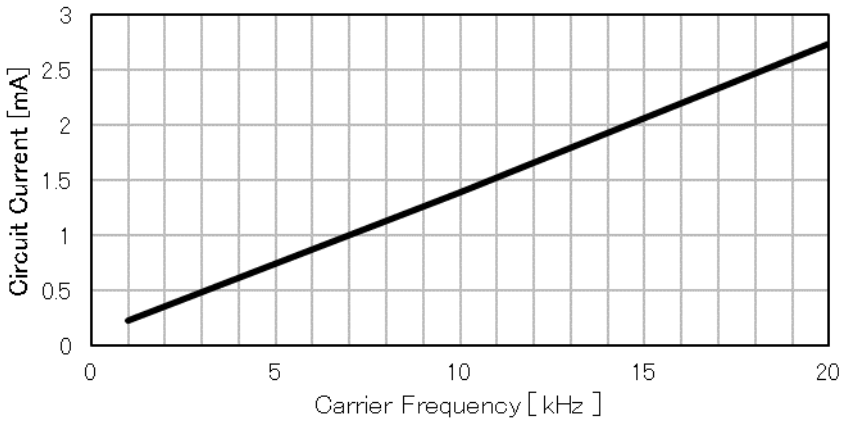


Fig.4-2-2 I_{DB} vs. Carrier frequency for PSS50SF1F6

4.3 Note for designing the bootstrap circuit

When each device for bootstrap circuit is designed, it is necessary to consider various conditions such as temperature characteristics, change by lifetime, variation and so on. Note for designing these devices are listed as below. For more detailed information about driving by the bootstrap circuit, refer the DIPIPM application note "*Bootstrap Circuit Design Manual*"

(1) Bootstrap capacitor

Electrolytic capacitors are used for BSC generally. And recently ceramic capacitors with large capacitance are also applied. But DC bias characteristic of the ceramic capacitor when applying DC voltage is considerably different from that of electrolytic capacitor. (Especially large capacitance type) Some differences of capacitance characteristics between electrolytic and ceramic capacitors are listed in Table 4-3-1.

Table 4-3-1 Differences of capacitance characteristics between electrolytic and ceramic capacitors

	Electrolytic capacitor	Ceramic capacitor (large capacitance type)
Temperature characteristics (Ta: -20~ 85°C)	•Aluminum type: Low temp.: -10% High temp: +10% •Conductive polymer aluminum solid type: Low temp.: -5% High temp: +10%	Different due to temp. characteristics rank Low temp.: -5%~0% High temp.: -5%~-10% (in the case of B, X5R, X7R ranks)
DC bias characteristics (Applying DC15V)	Nothing within rating voltage	Different due to temp. characteristics, rating voltage, package size and so on **-70%**~-15%

DC bias characteristic of electrolytic capacitor is not matter. But it is necessary to note ripple capability by repetitive charge and discharge, lifetime which is greatly affected by ambient temperature and so on. Above characteristics are just example data which are obtained from the WEB, please refer to the capacitor manufacturers about detailed characteristics.

(2) Bootstrap diode

Compact DIPIPM integrates bootstrap diodes for P-side driving supply. This BSD incorporates current limiting resistor (typ. 20Ω). The V_F-I_F characteristics (including voltage drop by built-in current limiting resistor) are shown in Fig.4-3-1 and Table 4-3-2.

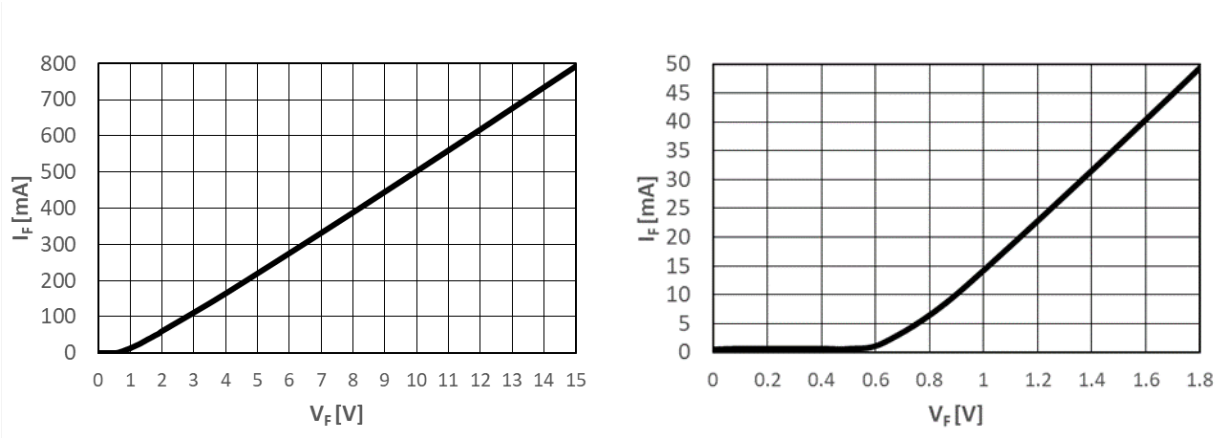


Fig.4-3-1 V_F-I_F curve for bootstrap Diode (The right figure is enlarged view)

Table 4-3-2 Electric characteristics of built-in bootstrap diode

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Bootstrap Di forward voltage	V_F	I_F=10mA including voltage drop by limiting resistor	0.5	0.9	1.3	V
Built-in limiting resistance	R	I_F=300mA	16	20	24	Ω

4.4 Initial charging in bootstrap circuit

In the case of applying bootstrap circuit, it is necessary to charge the BSC initially because voltage of BSC is 0V at initial state or it may go down to the trip level of under voltage protection after long suspending period (even 1s). BSC charging is performed by turning on all N-side IGBT normally. When outer load (e.g. motor) is connected to the DIPIPM, BSC charging may be performed by turning on only one phase N-side IGBT since potential of all output terminals will go down to GND level through the wiring in the motor. But its charging efficiency might become lower due to some cause. (e.g. wiring resistance of motor)

There are mainly two procedures for BSC charging. One is performed by one long pulse, and another is conducted by multiple short pulses. Multi pulse method is used when there are some restrictions like control supply capability and so on.

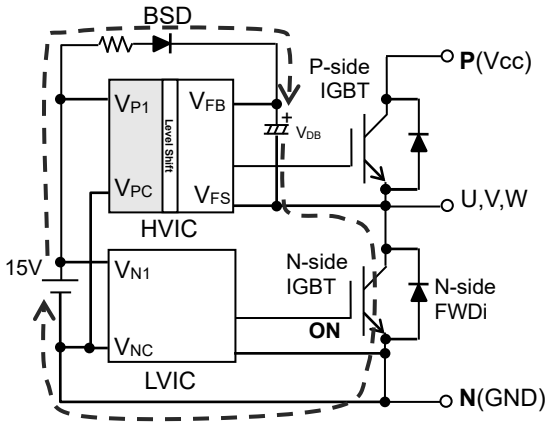


Fig.4-4-1 Initial charging root

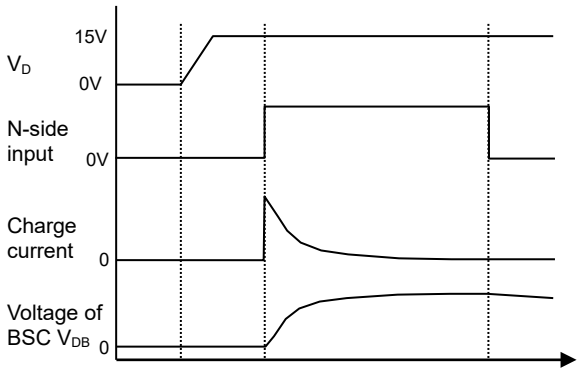


Fig.4-4-2 Example of waveform by one charging pulse

Initial charging needs to be performed until voltage of BSC exceeds recommended minimum supply voltage 13V. (It is recommended to charge as high as possible with consideration for voltage drop between the end of charging and start of inverter operation.)

After BSC was charged, it is recommended to input one ON pulse to the P-side input for reset of internal IC state before starting system. Input pulse width is needed to be longer than allowable minimum input pulse width PWIN(on). (e.g. 0.7μs or more for PSSxxSF1F6. Refer the datasheet for each product.)

CHAPTER 5 Interface Demo Board

5.1 Compact DIPIPM Interface Demo Board

This chapter describes the interface demo board (EVA25-COMP) for Compact DIPIPM series. Please use the demo board for not only first evaluation but also reference design of your actual PCB pattern.

(1) Demo Board Outline

The demo board can mount the minimum necessary components of Compact DIPIPM interface shown in Fig.5-1-1.

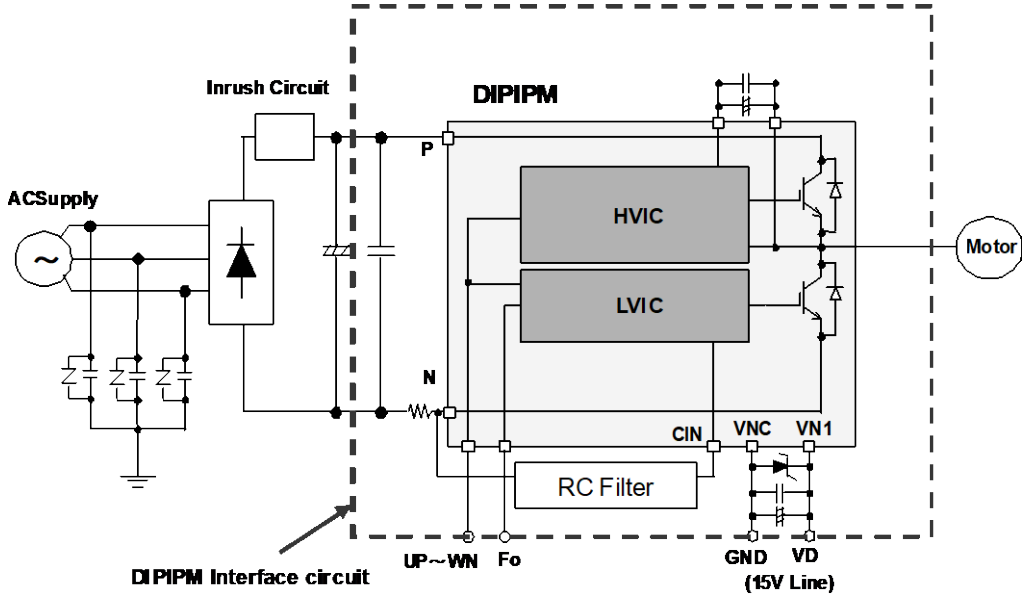
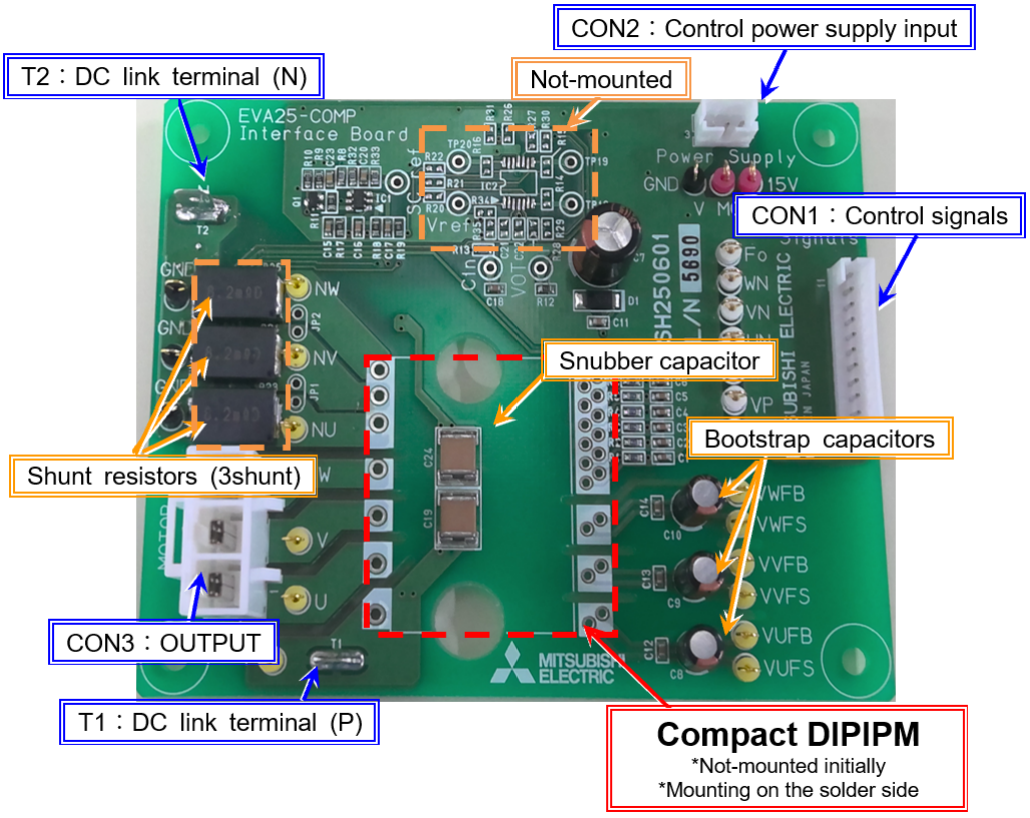


Fig.5-1-1 Demo board interface circuit (EVA25-COMP)

(2) Precautions of interface demo board evaluation

- EVA25-COMP is a common interface demo board for Compact DIPIPM series. Depending on the product series and your usage, it is necessary to change the connection or some parts on the board. Refer its user guide in detail.
- SC protection of EVA25-COMP hires comparator IC1 to detect output current with three shunt resistors. Please select the external shunt resistance such that the SC trip-level is less than 2 times of the current rating. For SC protection with one shunt resistor, insert jumper wires J1 and J2 to contact NU, NV and NW terminals. For common emitter configuration, it is recommended to monitor the shunt resistor voltage with Cin terminal directly, instead of using the initial overcurrent detection comparator IC1.
- EVA25-COMP has current monitor output circuit for shunt resistors through high speed OP-amp. 3 shunt current can be detected by mounting additional OP-amp IC2 and peripheral components.
- When driving DIPIPM with the interface board, connect the board to the signal source such as MCU as short as possible.
- This evaluation board is for your quick and temporary evaluation, and the following patterns and parts list are examples. We cannot guarantee the proper operation of this PCB in all cases. When selecting parts and design patterns for your PCB, please comply with your design standard and consider lifetime, reliability and so on.

(3) Demo Board Photo
(Board size: 110mmx80mm, Cupper pattern thickness: 70μm)



(Note) The circuit components and printings on the board are subject to be changed without notice.

Fig.5-1-2 Demo board EVA25-COMP photo

5.2 Circuit Schematic, Parts List and Board pattern,

(1) Circuit Schematic

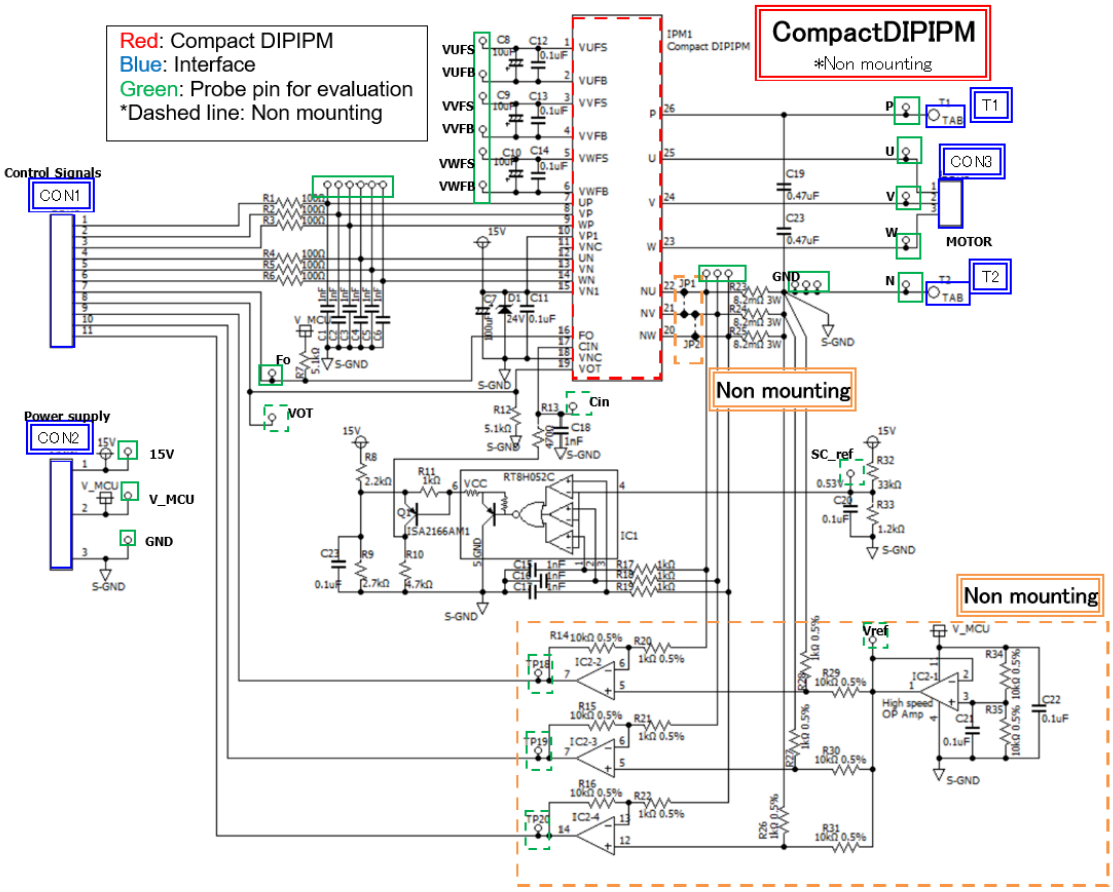


Fig.5-2-1 Demo board circuit schematic

The protection Zener diode for the P-side floating control power supply is not shown. However, in an actual system board, it is recommended to mount Zener diodes between the V_{UFB}–U, V_{VFB}–V, and V_{WFB}–W terminals.

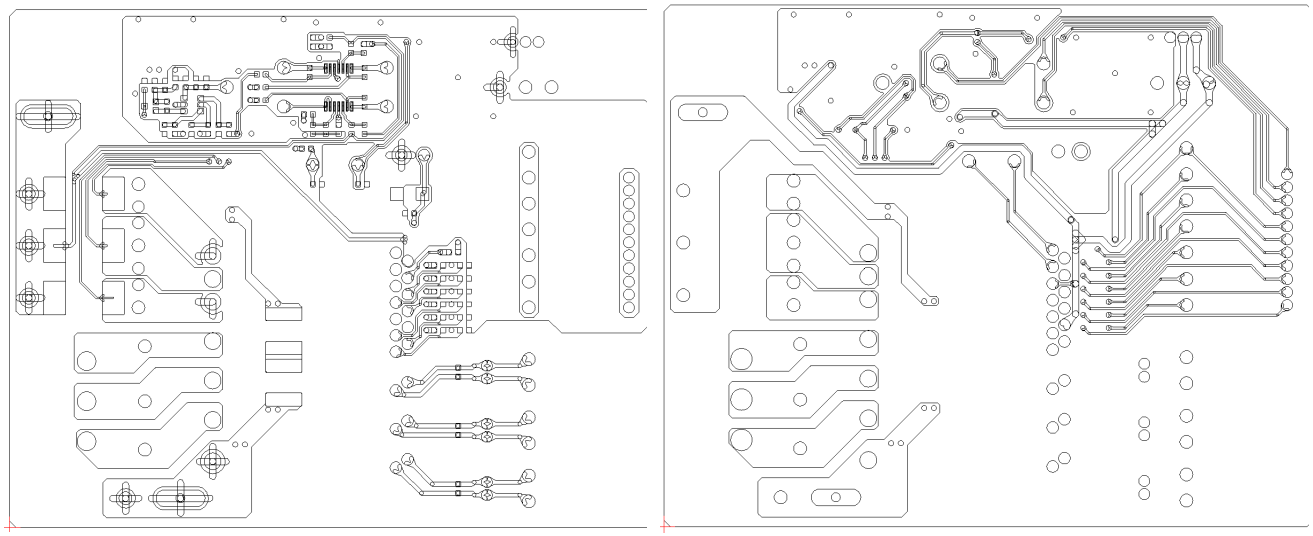
(2) Parts List

Table 5-3-1 Parts list (only for reference)

No.	Mark	Parts	Specification	Maker	Type	Qty
1	IPM1	DIPIPM	Compact DIPIPM	Mitsubishi	pss**SF1F7	1
2	C1-6,15-18	Capacitor	1nF 50V, 1.6 x 0.8	Murata	GRJ188R71H102KE11D	10
3	C7	Capacitor	100uF 50V,φ8 x H11.5	Nichicon	UPS1H101MPD	1
4	C8-10	Capacitor	10uF 50V,φ5 x H11	Nichicon	UPS1H100MDD	3
5	C11-14,20,23	Capacitor	0.1uF 50V, 1.6 x 0.8	Murata	GRJ188R71H104KE11D	6
6	C21-22	Capacitor	0.1uF 50V, 1.6 x 0.8	Murata	GRJ188R71H104KE11D	2
7	C19,24	Capacitor	0.22uF 630V,5.7 x 5.0	Murata	GRJ55DR72J224KWJ1L	2
8	CON1	Connector	2mm pitch	JST	B9B-PH-K-S	1
9	CON2	Connector	2mm pitch	JST	B3B-PH-K-S	1
10	CON3	Connector	3.96mm pitch	JST	B3P-VH-B	1
11	D1	Zener Diode	24V 1W	ROHM	PTZTE2524B	1
12	IC1	Comparator	Overcurrent protection IC	ISAHAYA	RT8H052C	1
13	IC2	OP Amp	SR=9V/μs, SSOP14	JRC	NJU7048	1
14	JP1,2	Jumper	2.5mm pitch, THφ1			2
15	Q1	Transistor	-0.5A -60V	ISAHAYA	ISA2166AM1	1
16	R1-6	Resistor	100Ω 0.1W ±1%	KOA	RK73H1J1000F	6
17	R7,12	Resistor	5.1kΩ 0.1W ±1%	KOA	RK73H1J5101F	2
18	R8	Resistor	2.2kΩ 0.1W ±1%	KOA	RK73H1J2201F	1
19	R9	Resistor	2.7kΩ 0.1W ±1%	KOA	RK73H1J2701F	1
20	R10	Resistor	4.7kΩ 0.1W ±1%	KOA	RK73H1J4701F	1
21	R11,17-19	Resistor	1kΩ 0.1W ±1%	KOA	RK73H1J1001F	4
22	R13	Resistor	470Ω 0.1W ±1%	KOA	RK73H1J4700F	1
23	R14-16,29-31,34-35	Resistor	10kΩ 0.1W ±0.5%	KOA	RK73H1J1002D	8
24	R20-22,26-28	Resistor	1kΩ 0.1W ±0.5%	KOA	RK73H1J1001D	6
25	R23-25	Resistor	8.2Ω 3W ±1%	KOA	SLN3TTE16LF	3
26	R32	Resistor	33kΩ 0.1W ±1%	KOA	RK73H1J3302F	1
27	R33	Resistor	1.2kΩ 0.1W ±1%	KOA	RK73H1J1201F	1
28	T1,2	Tab	187 series	Kyoushin	TP42097-21	2

(Note1) Compact DIPIPM (No.1), C21~26 (No.6), IC2 (No.13), JP1, 2 (No.14), R14~16, 29~31, 34~35 (No.23) and R20~22, 26~28 (No.24) are not mounted. The connectors (with 100 mm lead wires) for CON1 (No.8), CON2 (No.9) and CON3 (No.10) are supplied as accessories.

(3) Pattern diagram

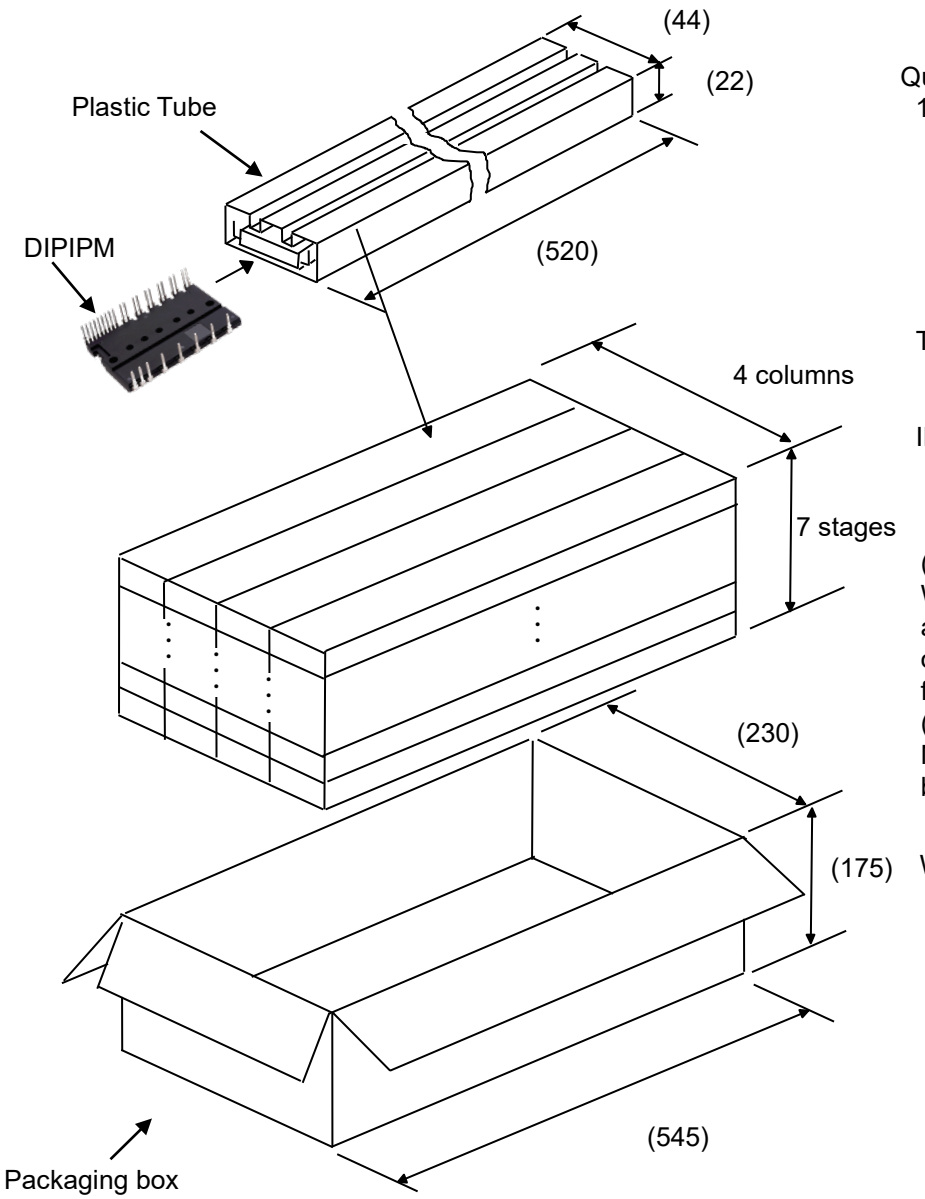


Component side　　Back side

Fig.5-2-1 Demo board component layout (DIPIPM is mounted to back side.)

CHAPTER 6 PACKAGE HANDLING

6.1 Packaging Specification



Quantity:
13pcs per 1 tube

Total amount in one box (max):
Tube Quantity: 4 × 7=28pcs

IPM Quantity(max.):
28 × 13=364pcs

(note1)
When it isn't fully filled by tubes at top stage, cardboard spacers or empty tubes are inserted for filling the spcae of top stage.
(note2)
Multiple lots may be mixed in one box.

Weight (max):
About 10.3g per 1pcs of DIPIPM
About 240g per 1 tube
About 7.6kg per 1 box

Spacers are put on the top and bottom of the box. If there is some space on top of the box, additional buffer materials are also inserted.

Fig.6-1 Packaging Specification

6.2 Handling Precautions

⚠ Cautions	
Transportation	·Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged. ·Throwing or dropping the packaging boxes might cause the devices to be damaged. ·Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.
Storage	·We recommend temperature and humidity in the ranges 5-35°C and 45-75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above.
Long storage	·When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior.
Surroundings	·Keep modules away from places where water (including dew condensation) or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems.
Flame resistance	·The epoxy resin and the case materials are flame-resistant type (UL standard 94-V0), but they are not noninflammable.
Static electricity	·ICs and power chips with MOS gate structure are used for the DIPIPM power modules. Please keep the following notices to prevent modules from being damaged by static electricity. (1)Precautions against the device destruction caused by the ESD The ESD of human bodies and packaging and/or excessive voltage applied across the gate to emitter may damage and destroy devices. The basis of anti-electrostatic is to inhibit generating static electricity possibly and quick dissipation of the charged electricity. ·Containers that charge static electricity easily should not be used for transit and for storage. ·Terminals should be always shorted with a carbon cloth or the like until just before using the module. Never touch terminals with bare hands. ·Should not be taking out DIPIPM from tubes until just before using DIPIPM and never touch terminals with bare hands. ·During assembly and after taking out DIPIPM from tubes, always earth the equipment and your body. It is recommended to cover the work bench and its surrounding floor with earthed conductive mats. ·When the terminals are open on the printed circuit board with mounted modules, the modules might be damaged by static electricity on the printed circuit board. ·If using a soldering iron, earth its tip. (2)Notice when the control terminals are open ·When the control terminals are open, do not apply voltage between the collector and emitter. It might cause malfunction. ·Short the terminals before taking a module off.

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