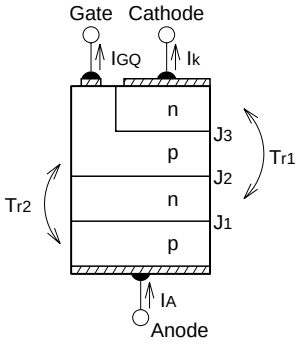
FEATURE AND APPLICATION OF GATE TURN-OFF THYRISTORS

Gate turn-off (GTO) thyristors are able to not only turn on the main current but also turn it off, provided with a gate drive circuit. Unlike conventional thyristors, they have no commutation circuit, downsizing application systems while improving efficiency. They are the most suitable for high-current, high-speed switching applications, such as inverters and chopper circuits.

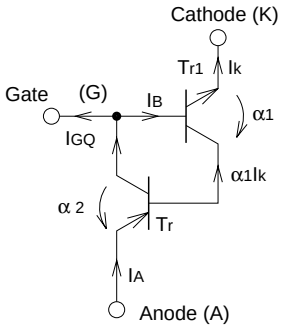
1. GTO thyristor operation principles

A GTO thyristor consists of four layers, pnpn, as like conventional thyristors. Functions except for turn-off are the same as those of conventional thyristors, therefore, we mainly describe the turn-off operation here.

When a GTO thyristor is in the on-stats, the central base regions are filled with holes supplied from the anode and electrons supplied from the cathode. If reverse bias is applied to make the gate negative in respect to the cathode, part of holes in the p-base layer are extracted through the gate, suppressing the injection of electrons from the cathode. In response to this suppression, more hole current is extracted through the gate, further suppressing the electron injection. In the course of this process, the cathode emitter junction (J_3) is put into a reverse-bias state entirely, GTO thyristor is turned off. Fig. 1 illustrates the turn-off operation, using a two-transistor model.



(a) Base unit



(b) Two-transistor model equivalent circuit

Fig. 1 GTO Transistor Operation Principle

Suppose that a GTO thyristor is divided into npn transistor Tr_1 on the cathode side and pnp transistor Tr_2 on the anode side, and that they are connected as shown in Fig. 1(b). In this figure, the current amplification factor of transistor Tr_1 is called α_1, and that of transistor Tr_2, α_2. If reverse current I_{GQ} flows through the gate, base current I_B at transistor Tr_1 is reduced when I_{GQ} is increased. This relationship can be expressed by the following equation:

$$I_B = \alpha_2 \cdot I_A - I_{GQ}$$

On the other hand, electron current I_{RB}, which disappears due to the recombination in the Tr_1 base layer, can be expressed as follows:

$$I_{RB} = (1 - \alpha_1) \cdot I_K$$

The relationship between GTO thyristor anode current (I_A) and cathode current (I_K) is expressed by the following equation:

$$I_A = I_K + I_{GQ}$$

To turn off the GTO thyristor, I_B must be smaller than I_{RB}. The magnitude of the reverse-bias current I_{GQ} that satisfies this condition can be calculated by the following equation:

$$I_{GQ} = (\alpha_1 + \alpha_2 - 1) \cdot I_A/\alpha_1$$

As can be seen from what has been discussed, it is possible in theory that a GTO thyristor can carry out the turn-off if an adequate magnitude of reverse bias current is supplied to the gate. Actually, however sheet resistance exists in the Tr_1 base region, making it difficult to turn off the on state current flowing at the emitter junction that is far from the gate. To minimize the resistance, GTO thyristors for high power applications are finely patterned: unit constructions as illustrated in Fig. 1 are placed in parallel with one another in whole silicon area. (See Fig. 2.)

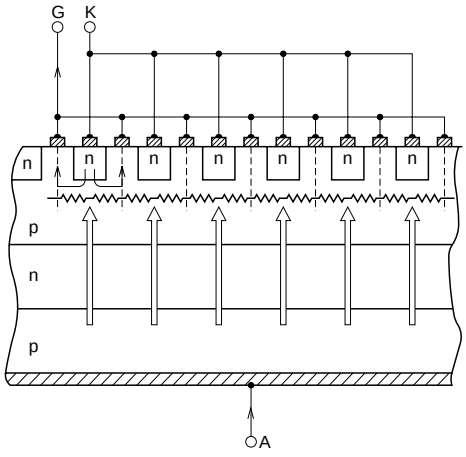


Fig. 2 GTO Thyristor Fine Pattern

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2. GTO thyristor: types and structure

The GTO thyristor unit construction is as shown in Fig. 1. Mitsubishi has two types of GTO thyristors, from which a more suitable one should be selected for a given application.

(1) Anode short GTO thyristor

The structure is as shown in Fig. 3 below:

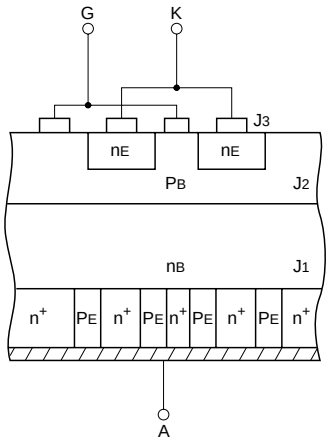

Fig. 3 Anode short GTO Thyristor Structure

At the J_1 junction, the anode is partially shorted due to the n^+ layers, so that the reverse voltage of the GTO thyristor is as small as that of the J_3 junction (around 15V normally). However, excess carriers are extracted from the gate and from the n^+ layer during the turn-off, enabling high-speed switching.

This type of thyristor is suitable for applications that require high-speed switching but do not need high reverse voltage, such as voltage source inverters.

(2) Reverse conducting GTO thyristor

The structure is as shown in Fig. 4 below.

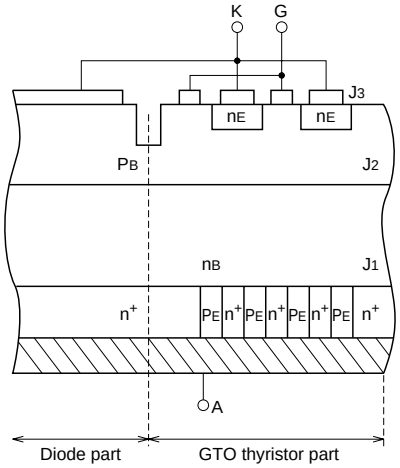

Fig. 4 Reverse conducting GTO Thyristor

This product consists of a fast recovery diode part and the anode short GTO thyristor part, the former of which is connected in parallel to the latter. The thyristor is the same type as the one described in (1) above. This product is suitable for application to voltage source inverters for example, where a GTO thyristor requires Flywheel diode. No additional diode is necessary if this GTO thyristor is used, reducing the system size and weight.

3. GTO thyristor operating waveform and definition of each parameter

Fig. 5 gives the GTO thyristor on-off switching waveforms, along with the definition of the parameters in each waveform.

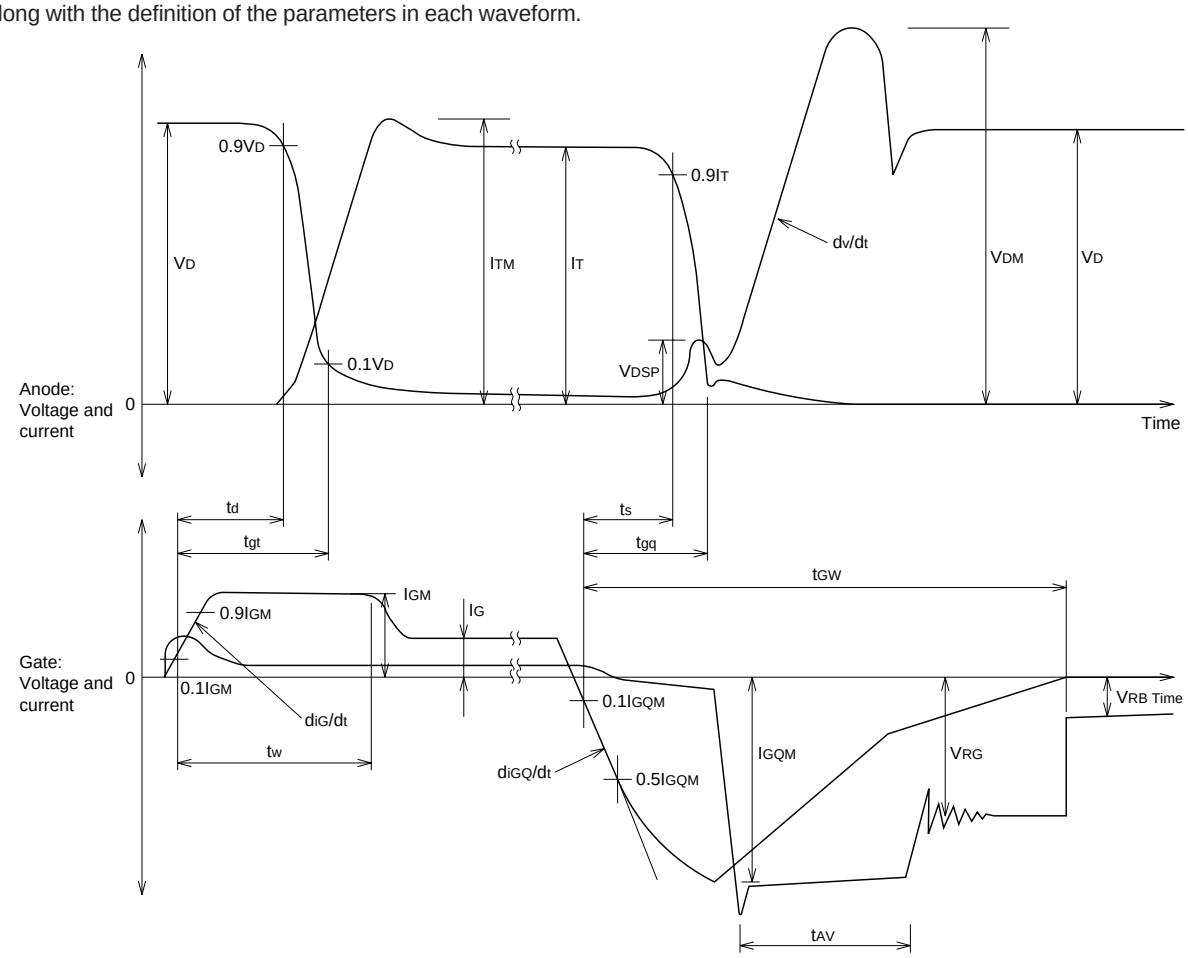

Fig. 5 GTO Thyristor Operation Waveforms and the Definition of Each Parameter

The anode voltage and current waveforms and gate voltage and current waveforms are the same between GTO thyristors and conventional thyristors during the turn-on operation. The gate current first increases up to I_{GM}, and then lowers to the I_G level, on which the current is retained for the time being. The difference between GTO thyristors and conventional thyristors is that, with the former, the current stays on the I_G level as long as on state current flows.

To carry out the turn-off, the gate drive circuit should be able to supply gate current whose increasing rate (di_{GQ}/dt) is higher than specified. The circuit should have also enough capability to increase the current higher than I_{GQM} easily. On the other hand, as the GTO thyristor is turned off, anode current is shifted to the snubber circuit, generating spike voltage V_{DSP}. The magnitude of this voltage is dependent on the increasing current rate (di/dt) and snubber circuit inductance. Note that, if this voltage is high, the GTO thyristor fails to carry out the turn-off. When GTO is turned off, anode voltage increases at a constant rate of dv/dt ($\propto I/C$). When the voltage reaches peak voltage V_{DM}, it lowers to the main circuit supply voltage level. As can be seen from the anode current waveform, the anode current is abruptly decreased after storage period t_s. However, after the turn-off period (t_{gq}), tail current flows until excess carriers are completely diminished in the inside of the silicon (tail period). The gate voltage drops suddenly after the t_s period, and eventually becomes equal to the gate circuit power supply voltage, passing through the avalanche period (t_{AV}), which occurs due to the gate circuit inductance.

The gate reverse bias time (t_{gw}) is required for the GTO thyristor to turn off anode current. During the t_{gw} period, the gate circuit impedance should be retained on a low level and reverse bias should be applied between the gate (G) and cathode (K), to extract excess carriers from the inside of the silicon. Note that, if the gate circuit impedance is not adequately low, gate current generated by excess carriers in the silicon reduce the reverse gate bias voltage. As a result, if forward bias between G and K occurs, it causes a turn-off failure and the distruction of the device.

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4. GTO thyristor instructions

(1) Ratings and selection of the device

① Peak repetitive off state voltage V_{DRM}
Voltage must not exceed the V_{DRM} level. Considering the largest applicable voltage plus an adequate margin, according to the operating conditions, determine off state voltage to be appropriate, and select an adequate device.

② Peak repetitive reverse voltage V_{RRM}
The anode short GTO thyristor has a peak repetitive reverse voltage of about 17 – 19 V. Connect a diode by aniti-parallel connection so that reverse voltage will not be applied to the GTO thyristor.
If the reverse conducting GTO thyristor is used, this instruction shall not be applied because a diode is already connected by anti-parallel connection and the magnitude of reverse voltage is dependent on the diode characteristics.

③ Repetitive controllable on state current I_{TQRM}
GTO thyristor cannot turn off the current higher than the specified I_{TQRM} with specified snubber circuit & gate condition.
The device may be destroyed if it is tried to turn off current that is higher than I_{TQRM}.

④ Average on state current $I_{T(AV)}$
This current refers to the maximum conductible average on state current that is determined under the condition of 60-Hz single-phase half waves at the specified fin temperature.
About GTO thyristor, $I_{T(AV)}$ is usually about one-third of I_{TQRM}. Select the device in consideration with the current that is supplied continuously and the peak current that is to be turned off.

⑤ Surge on state current I_{TSM}
Surge on state current I_{TSM} can be flowed at a limited number of times by an accident etc.
If excessive current flows, the device may be destroyed. Note that it may be destroyed into pieces and they may be scattered, depending on the conditions.

(2) Snubber circuit

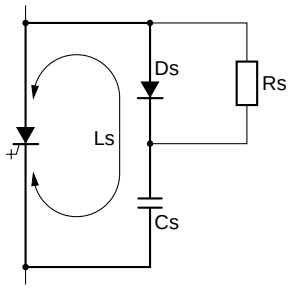
The snubber circuit in a GTO thyristor is almost to be equal to the commutation circuit in conventional thyristors. It must be capable of absorbing voltage fluctuation that occurs when the GTO thyristor turns off the current. Fig. 6 illustrates a typical snubber circuit that may be used in a GTO thyristor.
The snubber circuit must satisfy the following requirements:

① The circuit can conduct a large amount of current, and the voltage drop in the circuit must be swfficiently low.

② The circuit is connected by thick and short wires (as indicated with thick lines in Fig. 6) with a low inductance.

③ The snubber capacitor has a capacitance that is higher than a specified level. The inductance of capacitor must be sufficiently low.

④ The snubber diode has a low forward recovery voltage and low reverse recovery charge.



Ds : Snubber diode
Cs : Snubber capacitor
Rs : Snubber resistance
Ls : Snubber inductance

Fig. 6 GTO Thyristor Snubber Circuit

1) Snubber inductance L_S can be obtained as shown in Fig. 7. Remove the snubber resistance R_S from the circuit. Replace the GTO thyristor with switch SW. Fast switching thyristor etc. should be used as the switch. Apply DC voltage to snubber capacitor C_S. When switch SW is closed, a discharge waveform as shown below is obtained. Snubber circuit inductance L_S can be obtained using the following equation, based on the pulse width (t_w) of this current waveform.

$$L_S = (t_w/\pi)^2/C_S$$

Snubber circuit inductance L_S refers to the total inductance of the snubber circuit. It includes the inductance of diode D_S, capacitor C_S, and wiring.

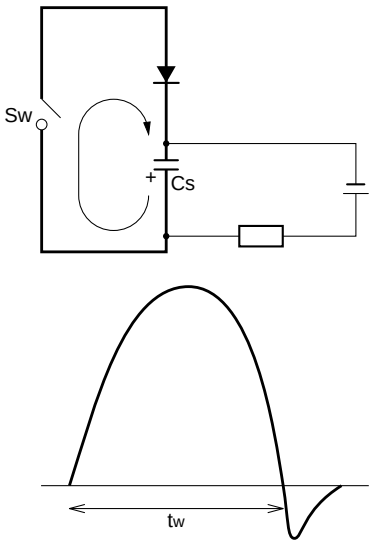


Fig. 7 Snubber Circuit Inductance Measuring Method

When L_S is large, spike voltage V_{dsp} is increased. The magnitude of this voltage is dependent on the di/dt rate of the current, which shifts to the snubber circuit during the turn-off operation. If V_{dsp} is too large, the turn-off failure occurred and the device is destroyed. Fig. 8 shows the typical dependency of the repetitive controllable on state current and snubber inductance of GTO thyristor by FG3000DV-90DA.

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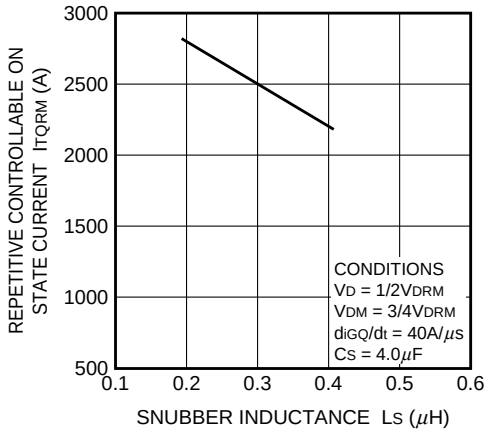
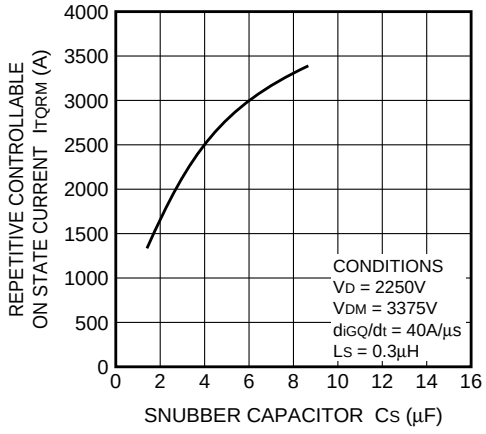
Fig. 8 Relationship between Repetitive Controllable ON State Current and Snubber Inductance



2) Snubber circuit capacitance is expressed as C_S. Anode voltage increasing rate dv/dt is proportional to the value of I/C_S (I: turn off current). Therefore, as C_S is decreased, dv/dt is increased, enlarging instantaneous power losses during the turn-off, controllable on state current is decreasesd as a result. To achieve the required controllable on state current, snubber capacitance C_S needs to be at least on a specified value. Fig. 9 shows the maximum data on dependance between snubber capacitance and repetitive controllable ON State current by FG3000DV-90DA.

Fig. 9 Relationship between Repetitive Controllable ON State Current and Snubber Capacitance



3) Snubber resistance is expressed as R_S. When R_S is large, snubber capacitor C_S discharge time constant $\tau(C_S R_S)$ becomes high when the GTO thyristor is turned on. It is required to increase the minimum on time ($t_{on\ mim}$).
We recommend that the minimum on time should be no less than 5τ. This is because capacitor C_S discharges electrically completely in a period that is five times time constant τ.
If the GTO thyristor is turned off when $t_{on\ mim}$ is less than 5τ, capacitor is not discharged completely, so that the remain charge voltage of capacitor is applied to the GTO thyristor. When this voltage is large, spike voltage is also increased, and in the worst case, the GTO thyristor is destroyed due to turn off failure. If snubber resistance R_S is small, C_S discharge current cannot be suppressed and becomes large, increasing turn-on losses. We recommend the resistance to be 5 – 10Ω.
Power losses P_W that occur at R_S are approximately calculated by the following equation:

$$P_W = \frac{1}{2} C_S f [V_D^2 + (V_{DM} - V_D)^2]$$

f: Switching frequency

According to the obtained value, determine power rating of R_S in actual operation to be sufficiently high value. Table 1 shows recommended snubber constants for each GTO thyristor.

(3) Diode selection

Select a snubber diode and flywheel diode for GTO thyristors to satisfy the following equations:

① Snubber diode D_S $\quad I_{F(AV)} \fallingdotseq \frac{1}{10} I_{TQRM}$ (GTO)
$\quad V_{RRM} = V_{DRM}$ (GTO)

② Flywheel diode D_F $\quad I_{F(AV)} \fallingdotseq I_{T(AV)}$ (GTO)
$\quad V_{RRM} = V_{DRM}$ (GTO)

where,
$I_{F(AV)}$: Diode average forward current
I_{TQRM}: GTO thyristor maximum turn-off current
V_{RRM}: Diode peak reverse voltage
V_{DRM}: GTO thyristor peak off state voltage
$I_{T(AV)}$: GTO thyristor average on state current
Table 1 shows recommended diodes for each GTO thyristor.
Fig. 10 shows the relationship between diode forward recovery voltage V_{FP} and increasing rate of forward current di/dt.
When snubber diode reverse recovery charge Q_{rr} of the snubber diode is large, anode (A)-cathode (K) voltage of the GTO thyristor drops considerably after the V_{DM} period, as shown in Fig. 11. It should be made certain that reverse voltage is not applied between A and K of the GTO thyristor. To ensure this, the snubber diode should have the characteristics of low forward recovery voltage V_{FP} and low reverse recovery charge Q_{rr}.
Table 1 also lists a number of recommended snubber diodes. A suitable one should be determined based on the operating conditions.

Flywheel diode D_F is often used in a stack, being combined with a GTO thyristor. In this case, the flywheel diode needs to be pressed with the same strength of force as that for the GTO thyristor, therefore, the pressure-mounting force tolerance for flywheel diodes should overlap that for GTO thyristors. Table 1 lists diodes with which a GTO thyristor can be pressed together, along with those that cannot be pressed together (marked *).
To combine a GTO thyristor and flywheel diode, pressure-mounting diameter is different. Construct the stack carefully so that the difference in the post diameter can be not effected to each other and that the pressure condition must be uniformed in the whole post of the device.

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Table 1. Recommended Snubber Constants and Flywheel Diodes for Each GTO Thyristor

GTO construction	Type	Snubber Constants			Flywheel Diode
		C_S (μF)	L_S (μH)	R_S (Ω)	
Anode short Type	FG1000BV-90DA	0.7	0.3	5 ~10	—
	FG2000FX-50DA	4.0	0.3	5 ~10	FD1000FH-50*
	FG2000JV-90DA	4.0	0.2	5 ~10	—
	FG3000GX-90DA	3.0	0.25	5 ~10	FD1000FX-90
	FG3000DV-90DA	6.0	0.3	5 ~10	FD1000FV-90
	FG3300AH-50DA	6.0	0.2	5 ~10	FD1000FH-50
	FG4000BX-90DA	3.0	0.25	5 ~10	1. FD1000FV-90 2. FD1500AV-90*
	FG4000CX-90DA	5.0	0.2	5 ~10	1. FD1000FV-90 2. FD1500AV-90
	FG4000EX-50DA	6.0	0.2	5 ~10	1. FD1000FH-50* 2. FD1500AV-90
	FG4000FX-90DA	3.0	0.25	5 ~10	FD1000FX-90
	FG4000GX-90DA	4.0	0.2	5 ~10	FD1000FX-90
	FG6000AU-120D	6.0	0.2	5 ~10	FD2000DU-120
Reverse conducting Type	FGR3000FX-90DA	6.0	0.2	5 ~10	—
	FGR3000CV-90DA	3.5	0.2	5 ~10	—

Fig. 10 Relationship between Forward Recovery Voltage and Increasing rate of Forward Current

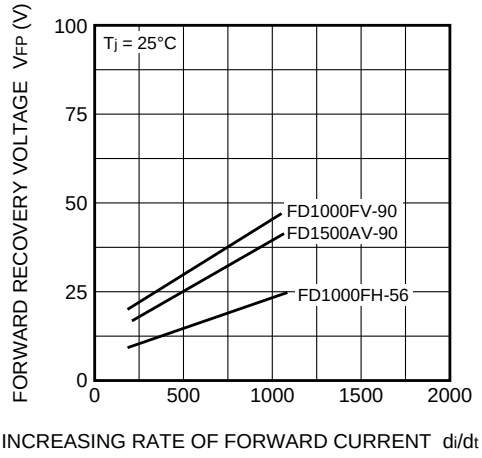
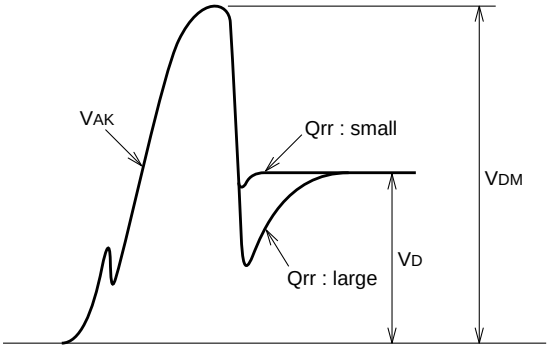


Fig. 11 Anode-Cathode Voltage Turn off Waveform in Case of Different Q_{rr} Value of Snubber Diode



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(4) GTO thyristor gate drive

1) Fig. 5 gives typical gate drive waveforms. Each parameter used in the figure is as defined below:

① On-gate current

I_{GM}: High on gate current

dig/dt: Increasing rate of on gate current (10% and 90%)

t_w: High on gate current pulse width

Pulse width t_w refers the width from 10% of initiation of gate current to the high gate current lowered to a specified level. It is usually recommended to set t_w to be two times of the turn-on time.

I_G: Steady-state on gate current

Steady-state on gate current that is supplied during the GTO thyristor on period should be no less than gate trigger current I_{GT}. Set I_{GT} considering that it is dependent on the junction temperature, as can be seen in Fig. 12.

② OFF gate current

di_{GQ}/dt: Increasing rate of turn off gate current (10%~50%)

t_{av}: Gate avalanche period

Because of $LgIg^2$ energy by turn-off gate current I_g and gate circuit inductance Lg, gate-cathode of GTO thyristor is put in an avalanche state. This period is called t_{av}. Set this period referring to the following conditions:

When t_{av} is extremely short, gate current sharply drops after the peak of turn-off gate current as shown in Fig. 13. Therefore, t_{av} must be longer than the value shown above. However, if t_{av} is too long, the period during which avalanche current flows is increased, and also rms gate current is increased. Therefore, adjust t_{av} must not be exceeded higher than 30μs.

V_{GR}: Turn-off gate voltage

After t_{av} in the turn-off period, voltage V_{GR} is applied between gate and cathode in a steady state. About GTO thyristor for turn-off, V_{GR} is needed to be high. However, it should be no more than peak gate reverse voltage V_{GRM}. In consideration with gate voltage fluctuation, set V_{GR} to be the highest possible value but not to exceed V_{GRM}.

V_{RB}: Steady-state bias voltage

To retain the GTO thyristor in an off state, reverse bias voltage of no less than 2V but no more than V_{GRM} should be applied between gate and cathode.

t_{GW}: Gate reverse bias time

During the off-gate pulse period (t_{GW}), it is necessary to apply V_{GR} at adequately low impedance, because the tail current must sufficiently flow during the disappering of excess carriers inside of the GTO thyristor.

If tail current is decreased to be a sufficiently low level, by applying V_{RB} between the gate and cathode the GTO thyristor is retained to be in an off state.

Fig. 12 Relationship between Gate Trigger Current and Junction Temperature

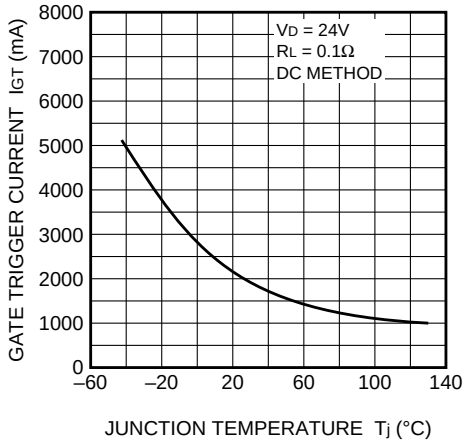
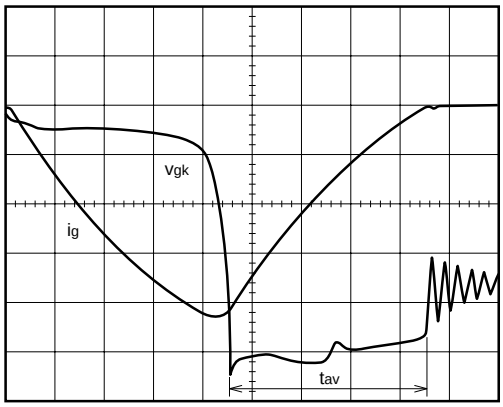
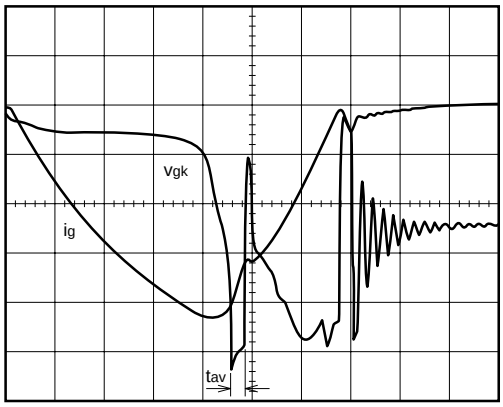


Fig. 13 Gate Current and Voltage Waveforms in case of Different t_{av} (GTO Thyristor Ratings: 2 kA, 4.5 kV)



When t_{av} = 20μs



When t_{av} = 2μs

ig : 100A/div.
vgk : 5V/div.
t : 5μs/div.

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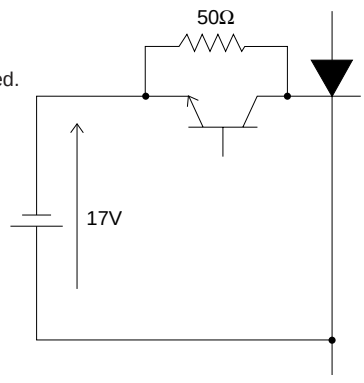
Table 2 Recommended Gate Drive Conditions for GTO Thyristors ($T_j \geq 0°C$)

Model		I_{GM}	dig/dt	tw	I_G (note)	di_{GQ}/dt	t_{av}	V_{GR}	V_{RB}	NOTE t_{GW}
		A	A/μs	μs	A	A/μs	μs	V	V	μs
FG1000BV-90DA	MIN	20	15	—	3.8	30	—	15	2	150
	TYP	—	—	20	—	—	15	—	—	—
	MAX	40	—	—	—	60	—	17	17	200
FG2000FX-50DA	MIN	30	10	—	3.8	30	—	15	2	150
	TYP	—	—	20	—	—	20	—	—	—
	MAX	50	—	—	—	60	—	17	17	200
FG2000JV-90DA	MIN	30	10	—	4.5	30	—	15	2	150
	TYP	—	—	20	—	—	20	—	—	—
	MAX	50	—	—	—	60	—	17	17	200
FG3000GX-90DA	MIN	25	20	—	3.8	40	—	15	2	150
	TYP	—	—	12	—	—	20	—	—	—
	MAX	50	—	—	—	60	—	17	17	200
FG3000DV-90DA	MIN	40	10	—	6.0	40	—	15	2	150
	TYP	—	—	20	—	—	20	—	—	—
	MAX	100	—	—	—	60	—	17	17	200
FG3300AH-50DA	MIN	40	10	—	6.0	40	—	15	2	150
	TYP	—	—	20	—	—	20	—	—	—
	MAX	100	—	—	—	60	—	17	17	200
FG4000BX-90DA	MIN	25	20	—	4.8	40	—	17	2	150
	TYP	—	—	12	—	—	20	—	—	—
	MAX	50	—	—	—	60	—	19	19	200
FG4000CX-90DA	MIN	40	20	—	6.0	50	—	17	2	150
	TYP	—	—	20	—	—	20	—	—	—
	MAX	100	—	—	—	70	—	19	19	200
FG4000EX-50DA	MIN	50	30	—	7.5	50	—	15	2	150
	TYP	—	—	20	—	—	20	—	—	—
	MAX	100	—	—	—	70	—	17	17	200
FG4000FX-90DA	MIN	25	20	—	4.8	40	—	17	2	150
	TYP	—	—	12	—	—	20	—	—	—
	MAX	50	—	—	—	60	—	19	19	200
FG4000GX-90DA	MIN	25	20	—	3.8	40	—	15	2	150
	TYP	—	—	12	—	—	20	—	—	—
	MAX	50	—	—	—	60	—	17	17	200
FG6000AU-120D	MIN	90	30	—	13	80	—	20	2	150
	TYP	—	—	12	—	—	20	—	—	—
	MAX	150	—	—	—	100	—	22	22	200
FGR3000FX-90DA	MIN	75	30	—	4.5	30	—	16	2	150
	TYP	—	—	20	—	—	20	—	—	—
	MAX	100	—	—	—	60	—	18	18	200
FGR3000CV-90DA	MIN	40	20	—	4.5	40	—	16	2	150
	TYP	—	—	20	—	—	20	—	—	—
	MAX	100	—	—	—	60	—	18	18	200

NOTE: Conditions: $V_D = \frac{1}{2} V_{DRM}$, gate circuit conditions are as follows.
These are the standard values.
In order to decide more detailed value, the fluctuation of V_D etc. must be considered.



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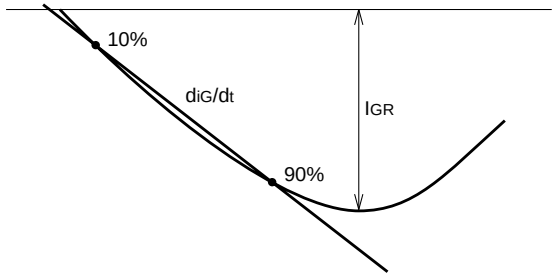
FEATURE AND APPLICATION OF GATE TURN-OFF THYRISTORS

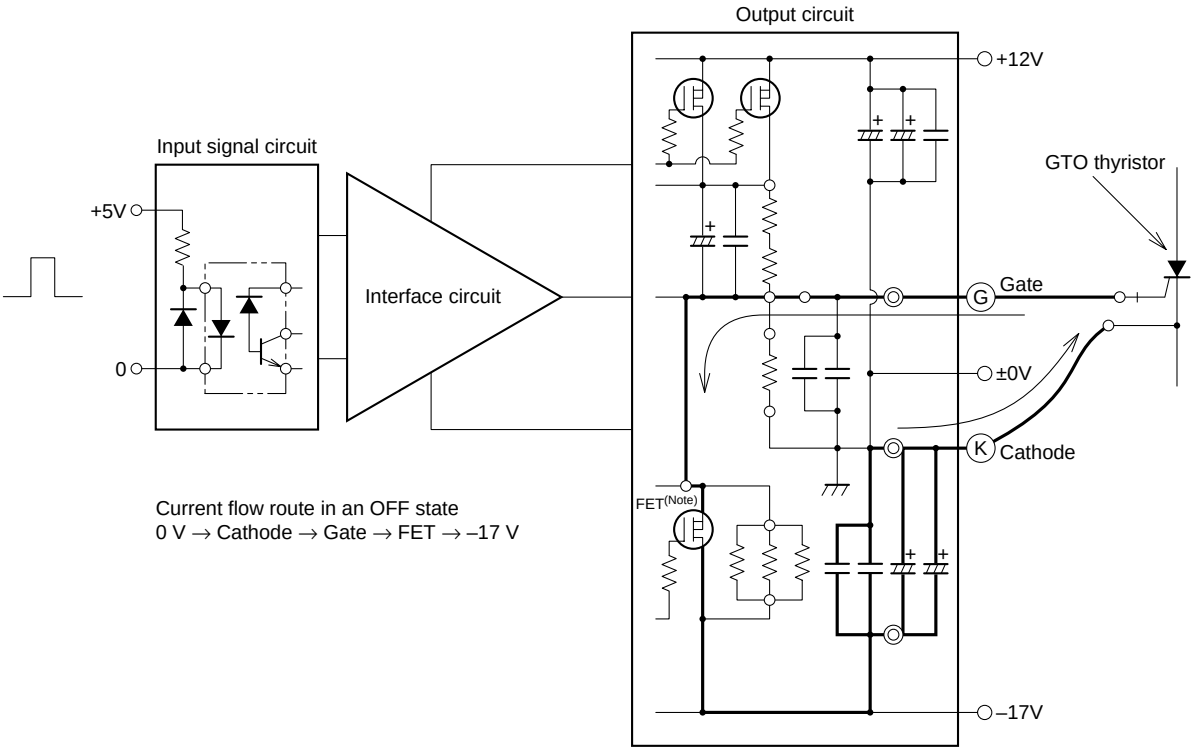
2) Fig. 14 shows a typical GTO thyristor gate drive circuit (block diagram).
The turn-off gate has a number of metal oxide semiconductor field-effect transistors (MOSFETs) having sufficiently low on resistance. Impedance through thick lines in the figure must keep to be low value.
The turn-off gate current is strongly dependent on the GTO thyristor turn-off characteristics. Current capability of drive circuit needs to be sufficiently high to completely extract excess carriers in the GTO thyristor. We recommend current capability of the gate driver to be achieved as shown below:

$I_{GR} \geq 1.2 \times I_{GQ}$ (I_{GQ}: Peak gate current that is necessary to turn off the maximum current)
$di_G/dt \geq di_{GQ}/dt$ (di_{GQ}/dt: Specified increasing rate of turn-off gate current)

The measurement is determined using the current waveform obtained by connecting the gate lead to the gate drive circuit, and short-circuiting both ends of the gate lead terminal (gate and cathode terminal). (See Fig. 15.)

Fig. 15 Gate Current Waveform Short-circuited Gate Driver





(Note) Connect a number of MOSFETs with low ON resistance.

Fig. 14 GTO Thyristor Gate Drive Circuit Example (Block Diagram)

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(5) GTO thyristor power loss

Fig. 16 shows power loss generated in GTO thyristor operation. Among these losses, the off-state loss is small and negligible.

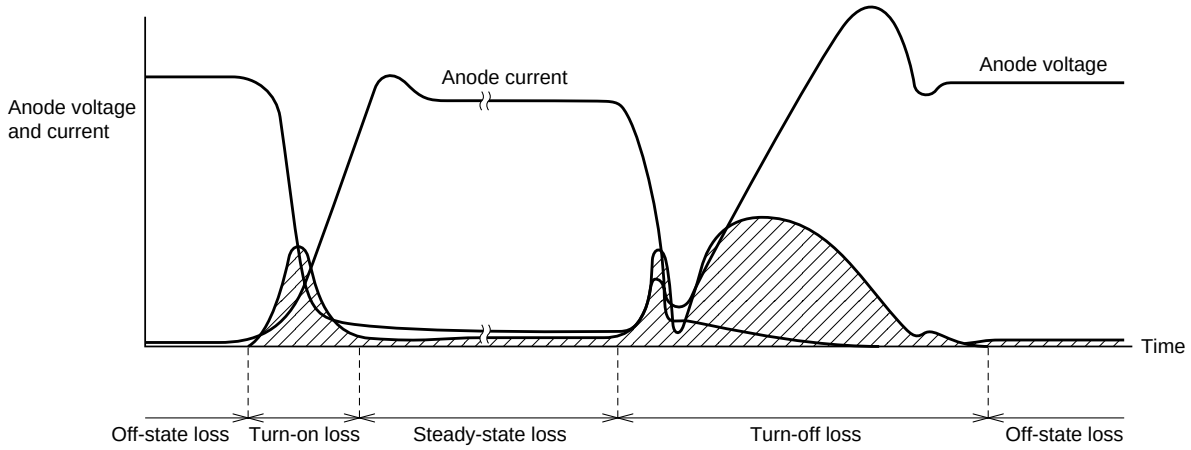


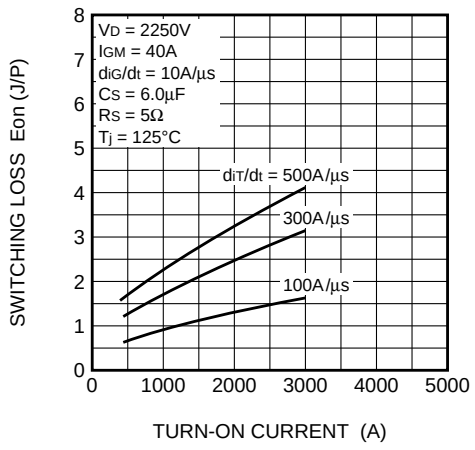
Fig. 16 GTO Thyristor Loss Location (the Shaded Portion)

When GTO thyristor is used at high frequency, switching losses during the turn-on operation and turn-off operation should be taken into account, along with steady-state losses that are determined with on state voltage and on state current. The relationship between the switching loss per pulse and turn on current is shown in this data book for each type.

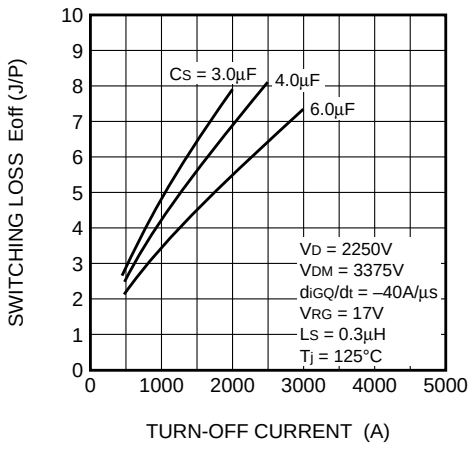
For the turn-on loss, increasing rate of turn on current di/dt is used as the parameter. For the turn-off loss, snubber capacitance C_S is used as the parameter. Switching losses can be calculated by multiplying these value by the switching frequency. Fig. 17 shows the typical data about FG3000DV switching losses.

Fig. 17 FG3000DV Switching Loss (Representative Data)

(a) Turn-on switching loss (maximum value)



(b) Turn-off switching loss (maximum value)



For example, the average of total losses (P_T) can be obtained as follows. (See Fig. 18.)

$t_{on} + t_{off} = 5ms$
Frequency = 200Hz
duty = $\frac{t_{on}}{t_{on} + t_{off}} = 0.3$
Snubber conditions: $C_S = 6\mu F$, $R_S = 5\Omega$, $L_S = 0.3\mu H$
Main circuit conditions; $I_T = 800$ A
$di/dt = 300A/\mu s$
$V_D = 2250V$
$V_{DM} = 3375V$

$P_T = I_T \times V_T$ ($\dot{I} = I_T$) $\times 0.3 + (E_{on} + E_{off}) \times f$
$= 800A \times 2.35V \times 0.3 + (1.55 + 3.0) \times 200Hz$
$= 1474W$

In actual operation, transient change of junction temperature must also be considered. It should be determined by more precise calculation in consideration of losses in each on period and transient thermal resistance values.

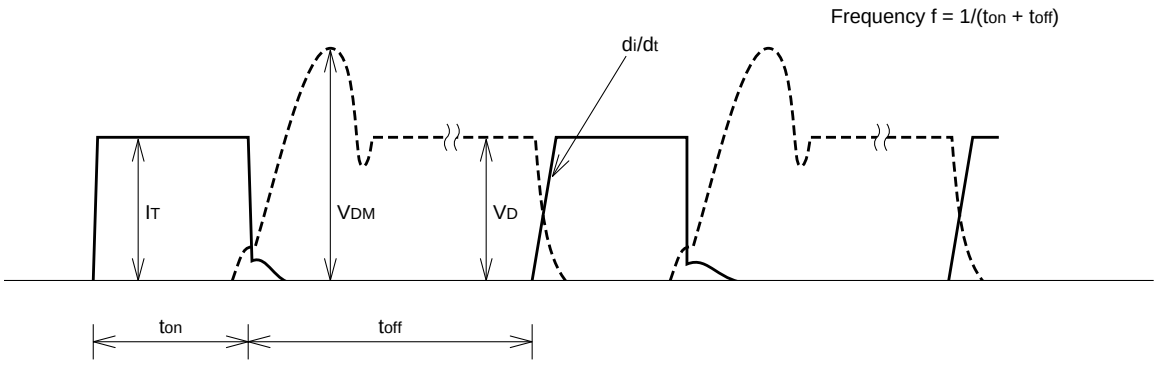


Fig. 18 GTO Thyristor Operation Waveform

FEATURE AND APPLICATION OF GATE TURN-OFF THYRISTORS

(6) Long term DC stability voltage

1) Outline

High-power semiconductors, such as GTO thyristors, have generally been used at a DC voltage that is no more than half of the blocking voltage rating. With recent advance in application technologies, however, supplied voltage to the semiconductor is increasing. Application with DC voltage that is higher than half of the blocking voltage rating is becoming increasingly popular.

When a DC high voltage is applied continuously over a long time, however, extremely powerful cosmic rays may enter the semiconductor device, destroying the device suddenly. This phenomenon is in recent years clarified by the locomotive application in Europe.

2) Device destruction

A semiconductor device may be destroyed abruptly, without current leakage increase either at the moment of device destruction or before and after it. Destruction occurs at random in the device, melting down the device on the spot.

When the destruction possibility is plotted on a Weibull chart, m equals 1, showing that destruction occurs accidentally. On the other hand, this destruction phenomenon is known to be related to voltage, and the failure rate is exponentially dependent on the applied voltage (electric field strength).

3) Countermeasures against device destruction due to cosmic rays that occur during high DC stability voltage application

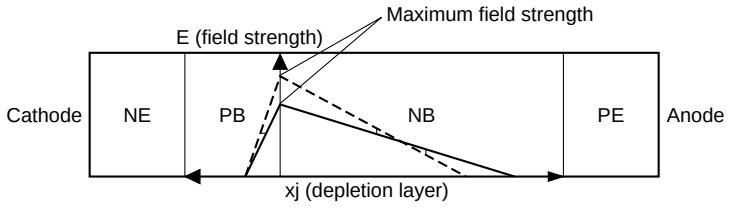
The GTO thyristor is a high-power semiconductor. By increasing the silicon resistivity, electric field strength can be decreased. Fig. 19 shows outlines of this device construction.

4) Mitsubishi semiconductor device made from silicon with high resistivity

Mitsubishi GTO thyristors with an device made from silicon with high resistivity are listed below. They have guaranteed long-term DC stability voltage V_{LTDS} that is as high as 2/3 of the blocking voltage rating.

FD1000FX-90 (high-frequency rectifier diode)
FG3000GX-90DA (anode short GTO thyristor)
FG4000FX-90DA (anode short GTO thyristor)
FG4000GX-90DA (anode short GTO thyristor)
FGR3000FX-90DA (reverse conducting GTO thyristor)
Note: V_{LTDS} refers to Long Term DC Stability voltage.

Fig. 20 shows typical dependency between DC voltage V_{DC} and the failure rate (FIT). V_{DC} value at 100 FIT failure rate is called V_{LTDS}. Conventional GTO thyristors with 4.5kV blocking voltage have V_{LTDS} of 2500V. For LTDS GTO thyristors with same blocking voltage, V_{LTDS} can be increased to 3,000V.



Note
1) Dotted line: Field strength of conventional device
2) Solid line: Field strength of device made from silicon with high resistivity

Fig. 19 Outline of an Device with Improved Long-term DC Stability Voltage

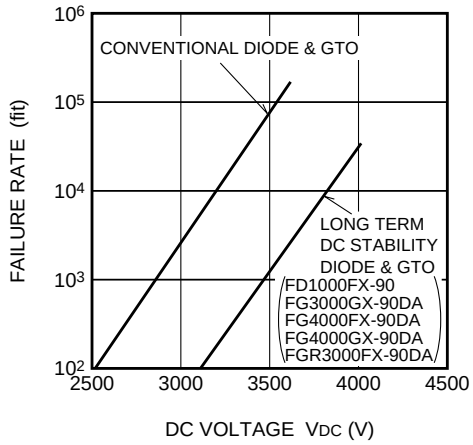


Fig. 20 Relationship between DC Voltage and Failure Rate

(7) GTO thyristor pressure mounting

In a GTO thyristor, each segment is independent each other. Functions such as turn-off are ensured by press of the whole device surface uniformly. Check the uniformity of the pressure condition of the surface by using pressure-sensitive paper.

Also pay attention to the cooling fin contact surface flatness, which is recommended to be within 10μm. To press the device of which diameter are different from the GTO thyristor design the stack structure carefully so that the difference in the pressure contact diameter will be absorbed when they are pressed together.

FEATURE AND APPLICATION OF GATE TURN-OFF THYRISTORS

5. GTO thyristor applications

Mitsubishi GTO thyristors have the excellent features as the power switching device. They are suitable for use as a main control device in inverters and choppers. Compared with conventional thyristors, GTO thyristors have the following advantages:

(1) With excellent switching characteristics, GTO thyristors help improving high frequency characteristics and efficiency.
(2) No commutation circuit is necessary, helping to reduce the system size and weight.
(3) All functions become available with semiconductors, enabling maintenance-free operation.
(4) Commutation current does not flow, minimizing the generation of noise and electromagnetic waves.

GTO thyristors are used in such devices as AC drive (VVVF invertors), DC drive (DC choppers), AC stabilizing power supplies (CVCF), and DC circuit breakers. Fig. 21 shows an example of applying a GTO thyristor to a pulse width modulation converter/inverter system. In this application, the converter/invertor system drives a 3-phase induction motor at variable speeds with a 3-phase AC power supply.

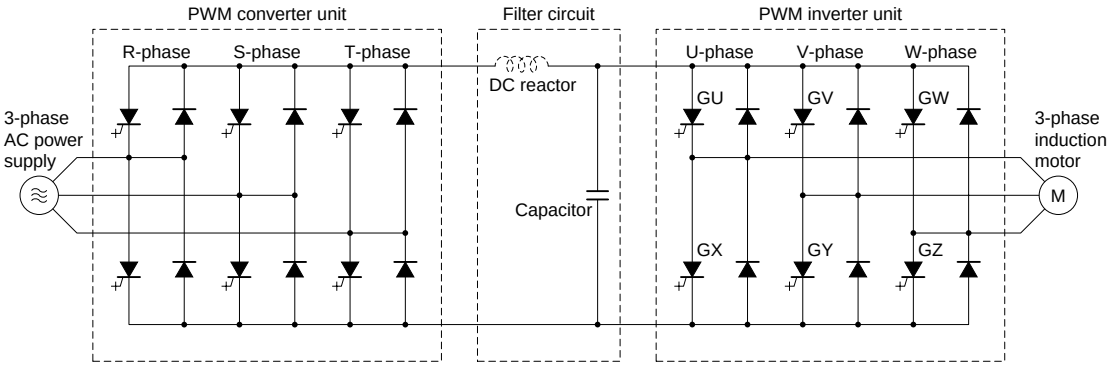


Fig. 21 Main Circuit of PWM Converter/Inverter System

(1) PWM converter
Regenerative operation is available by controlling GTO thyristor. High-efficiency operation is available by controlling power factor 1.

(2) Filter circuit
A filter circuit is constructed from an inverted L-type circuit consisting of a DC reactor and capacitor. It controls sixfold frequency ripples that are generated in the PWM converter and ripple current that comes from the PWM inverter.
The DC reactor is not always used.

(3) PWM inverter
Three-phase AC with variable voltage and frequency is generated by controlling the GTO thyristor, enabling variable speed operation of the three-phase inductive motor. Fig. 22 shows an inverter output voltage waveform for triangular wave modulation, for example.
Recently, GTO thyristors are often used in three-level converters and three-level inverters.
Fig. 23 shows an example of application to a three-level converter/inverter system.
A three-level inverter can generate voltage whose waveform is stepped on three levels of 0V, 1/2Vc, and Vc, diminishing noise and torque ripples.
Fig. 25 shows a three-level inverter output voltage waveform.

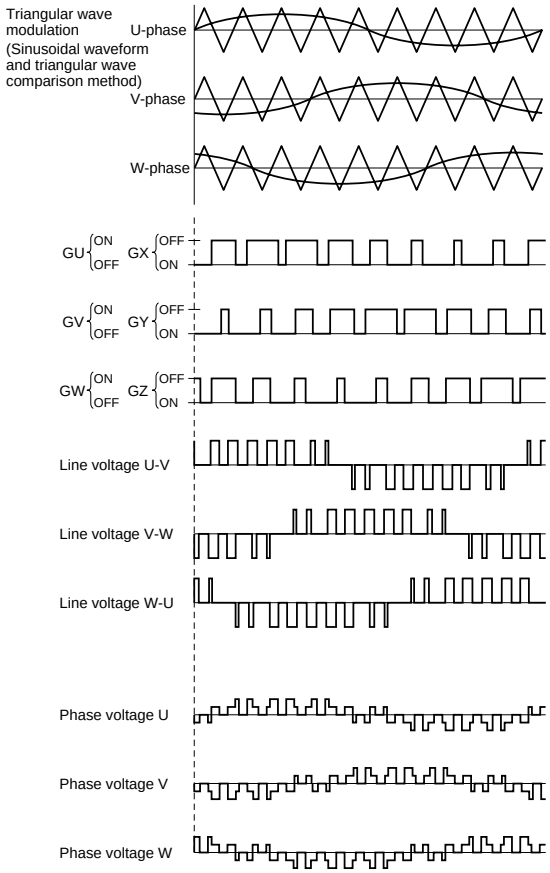


Fig. 22 Inverter Output Voltage

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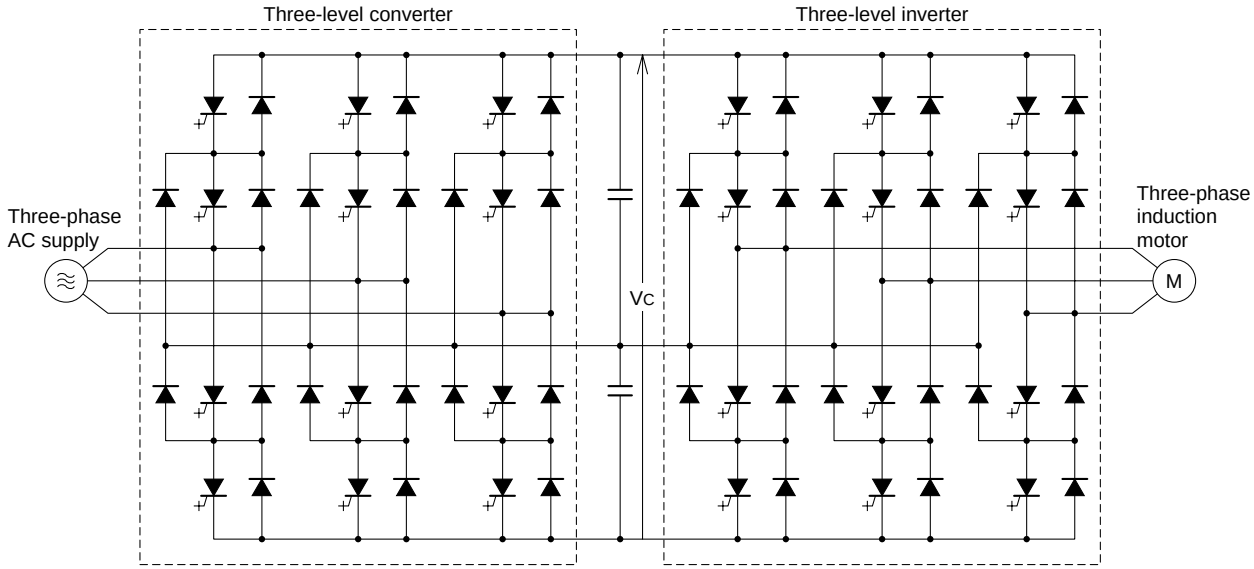


Fig. 23 Main Circuit of Three-level Converter/Inverter System

Phase switching state

GT1	GT2	GT3	GT4	Phase voltage	Mode
ON	ON	OFF	OFF	Vc	② ④
OFF	ON	ON	OFF	Vc/2	① ③
OFF	OFF	ON	ON	0	⑤ ⑥

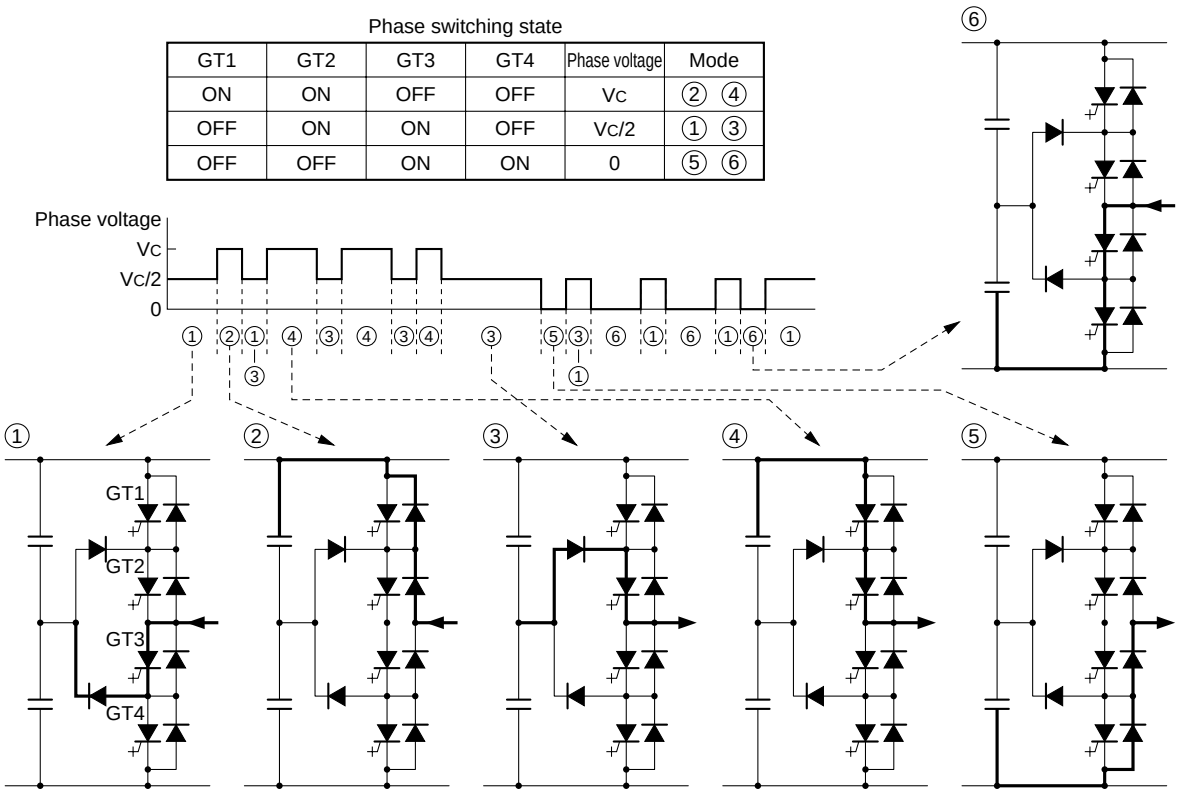
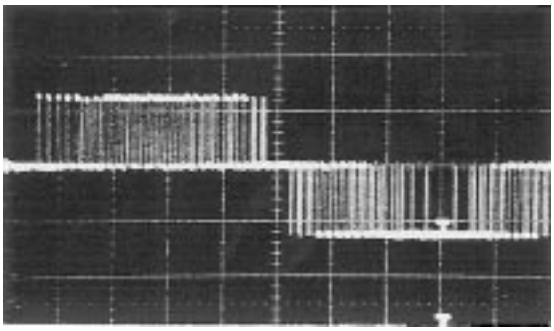
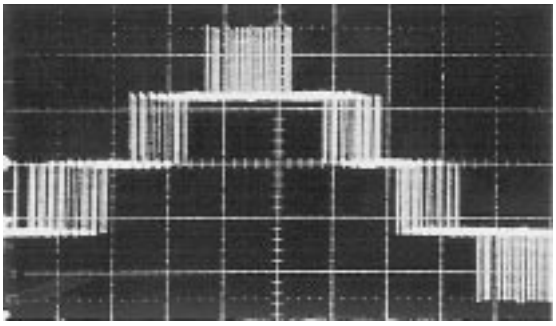


Fig. 24 Three-level Inverter Operation Mode



(a) Two-level output voltage waveform



(b) Three-level output voltage waveform

Fig. 25 Two-level & Three-level Inverter Output Voltage Waveform