

HVIC Application Note

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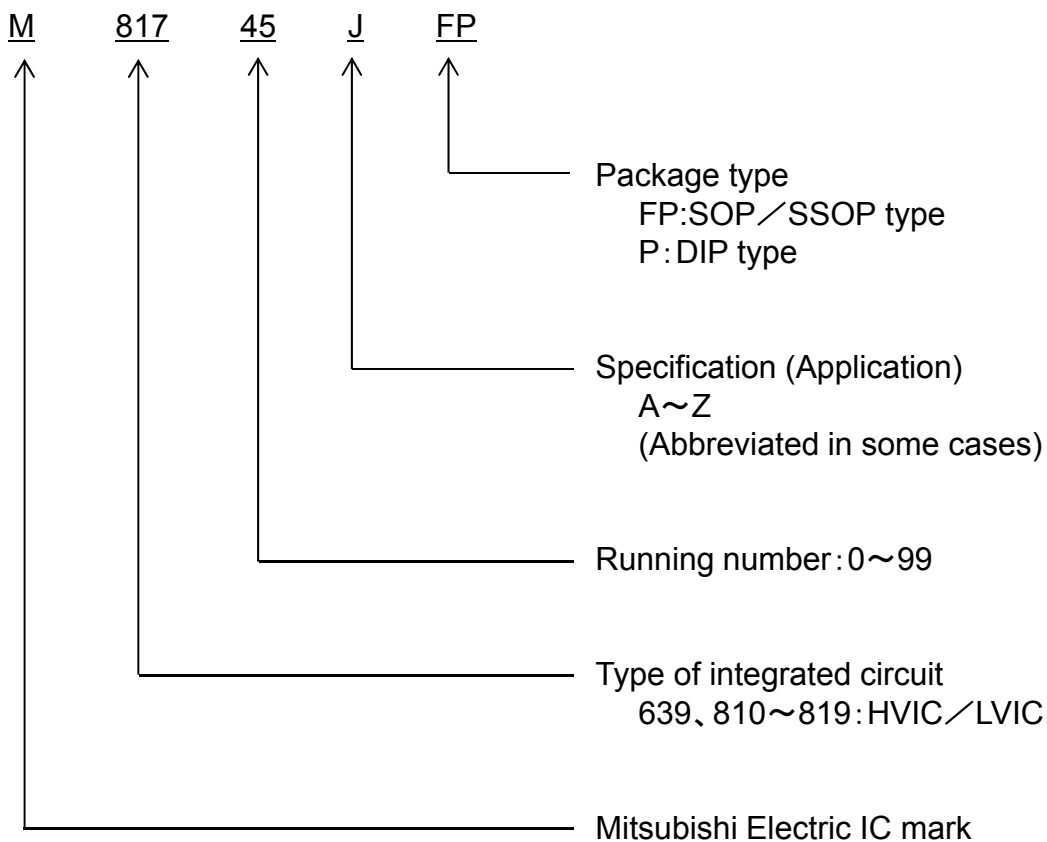
1. Introduction

1-1. Features

HVIC is a high voltage IC which drives gate of power MOSFET or IGBT directly in response to input signal from MCU, and HVIC is used in place of pulse transformer and photo coupler. Level-shift circuit obtains isolation on the semiconductor chip, and the reliability of the system is increased by protection functions (Under voltage lockout, interlock, input filter, fault output etc.). Mitsubishi electric has a lot of half-bridge type HVICs which are used for driving circuits, and are compliant with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) directive 2011/65/EU.

For more information, please refer to the datasheet and the catalog posted on Mitsubishi Electric semiconductor website(<http://www.MitsubishiElectric.com/>).

1-2. Product type name



1-3. Application circuit examples

(1) Gate driver for 3-phase motor(3-phase bridge)

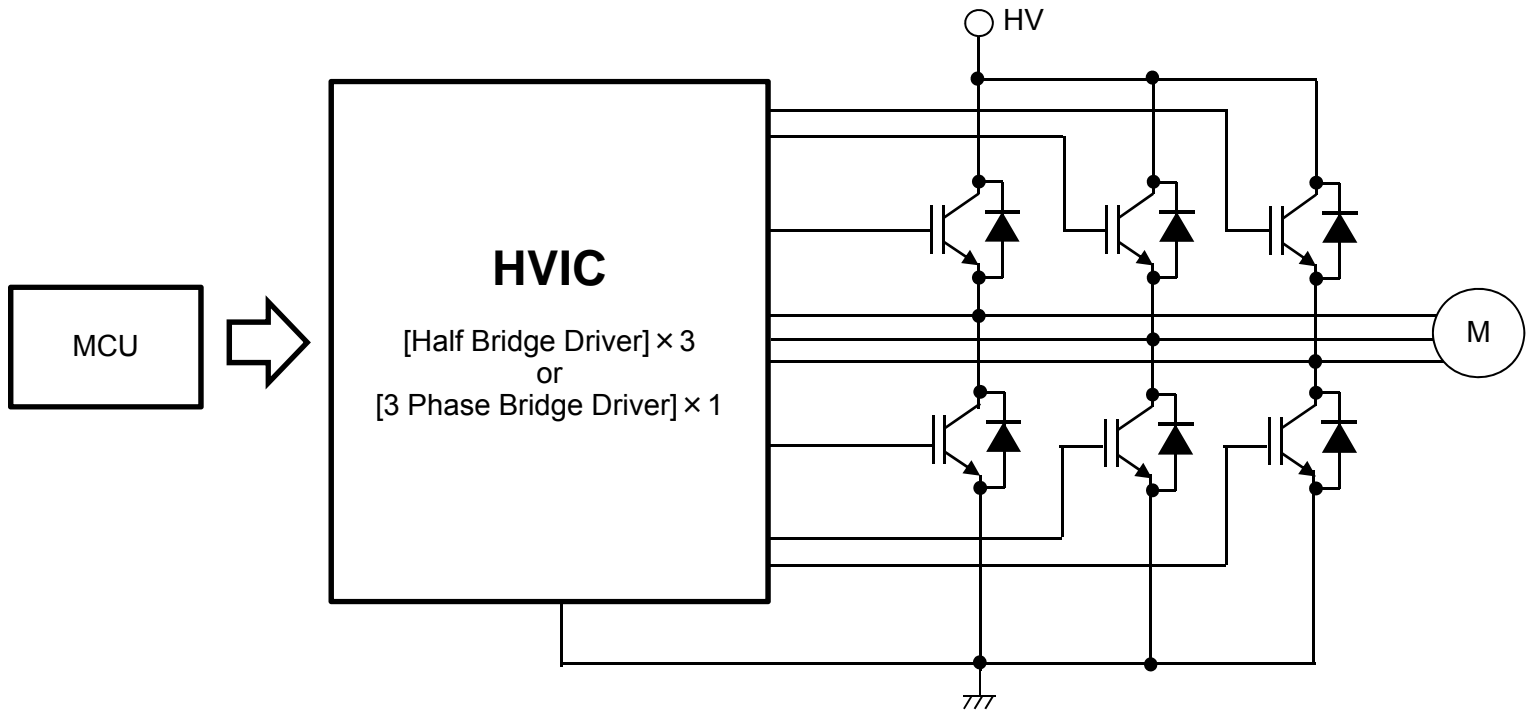


Fig.1 Gate driver for 3-phase motor(3-phase bridge)

(2) Gate driver for illumination lamp(Half bridge)

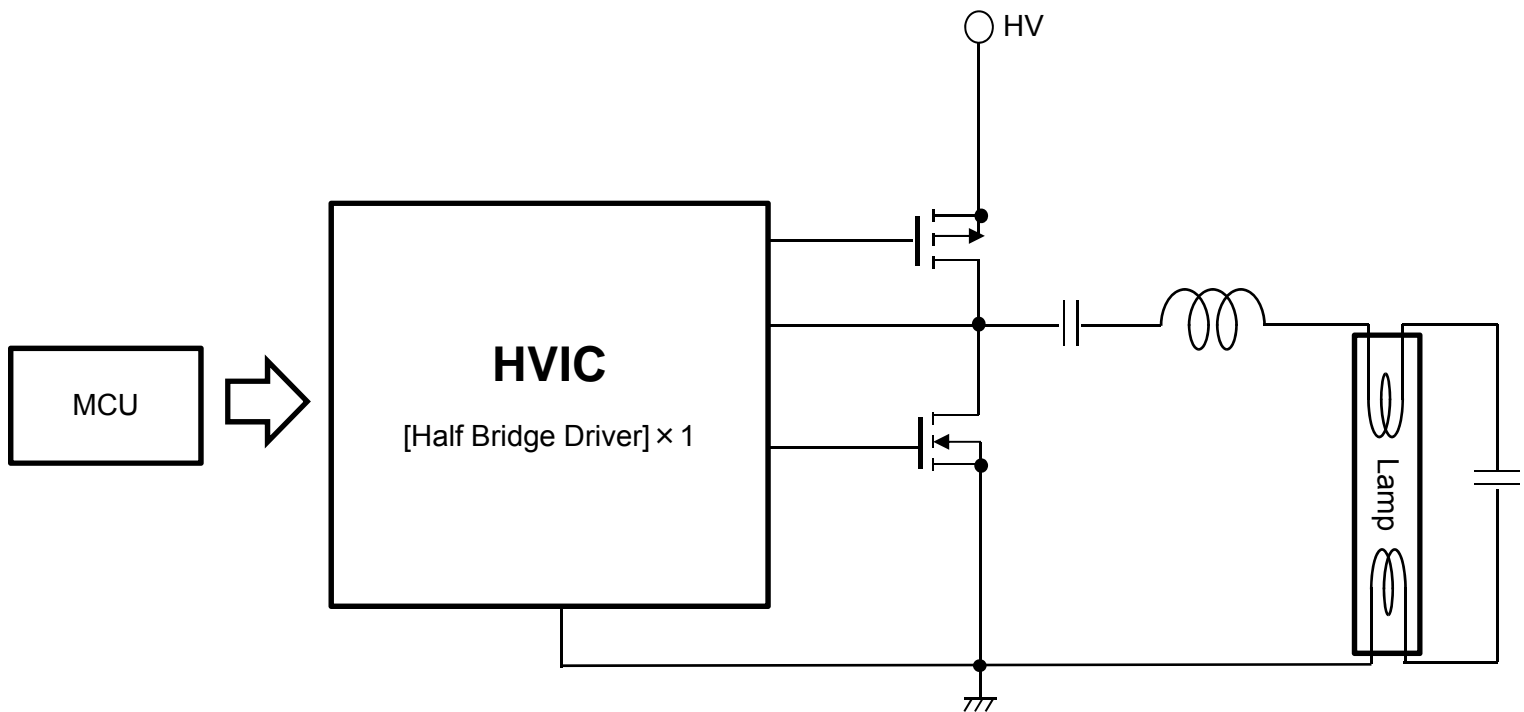


Fig.2 Gate driver for illumination lamp(Half bridge)

(3) Gate driver for DC-DC converter(High-side)

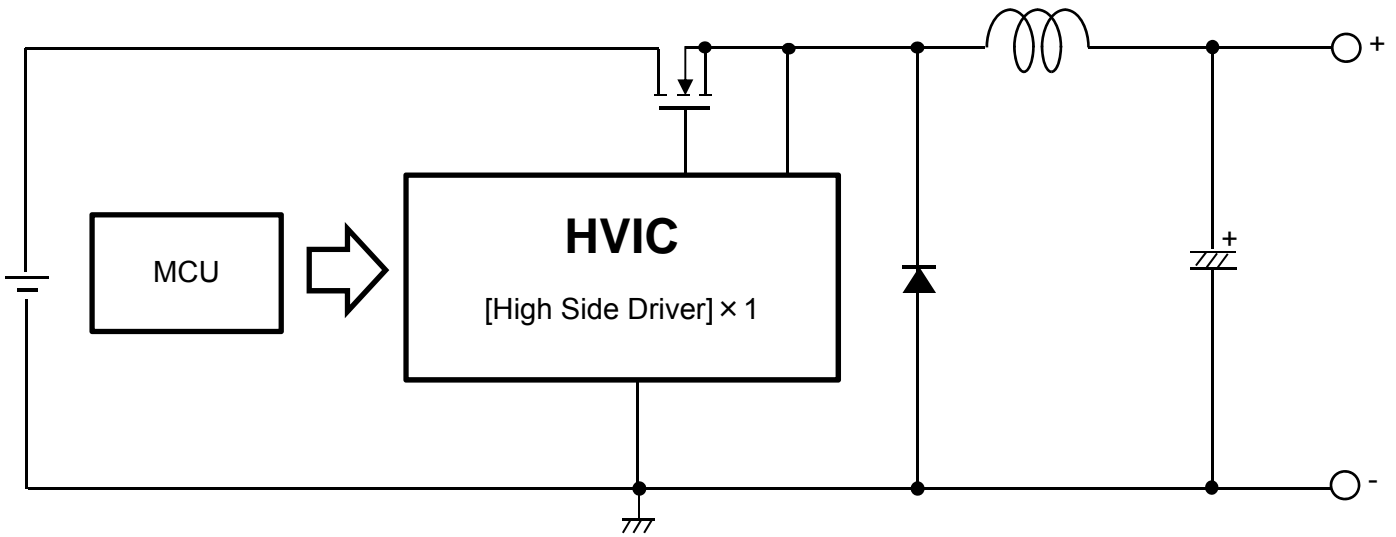


Fig.3 Gate driver for DC-DC converter(High-side)

(4) Gate driver for illumination lamp(Full bridge)

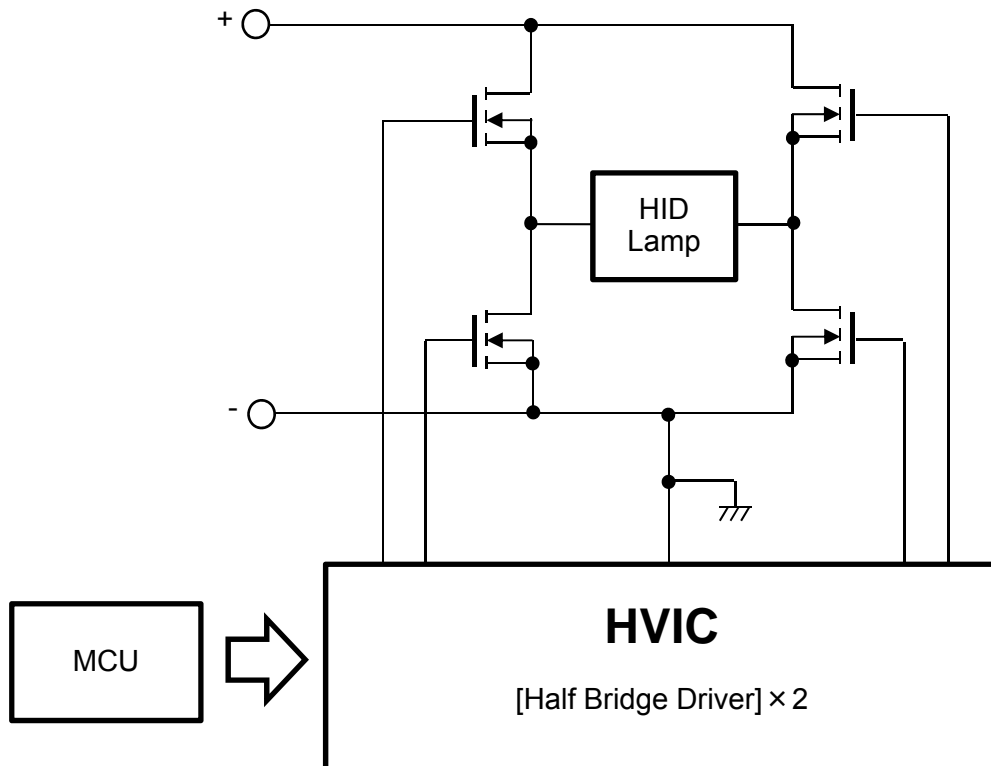


Fig.4 Gate driver for illumination lamp(Full bridge)

(5) Gate driver for IH cooking heater(Half-bridge)

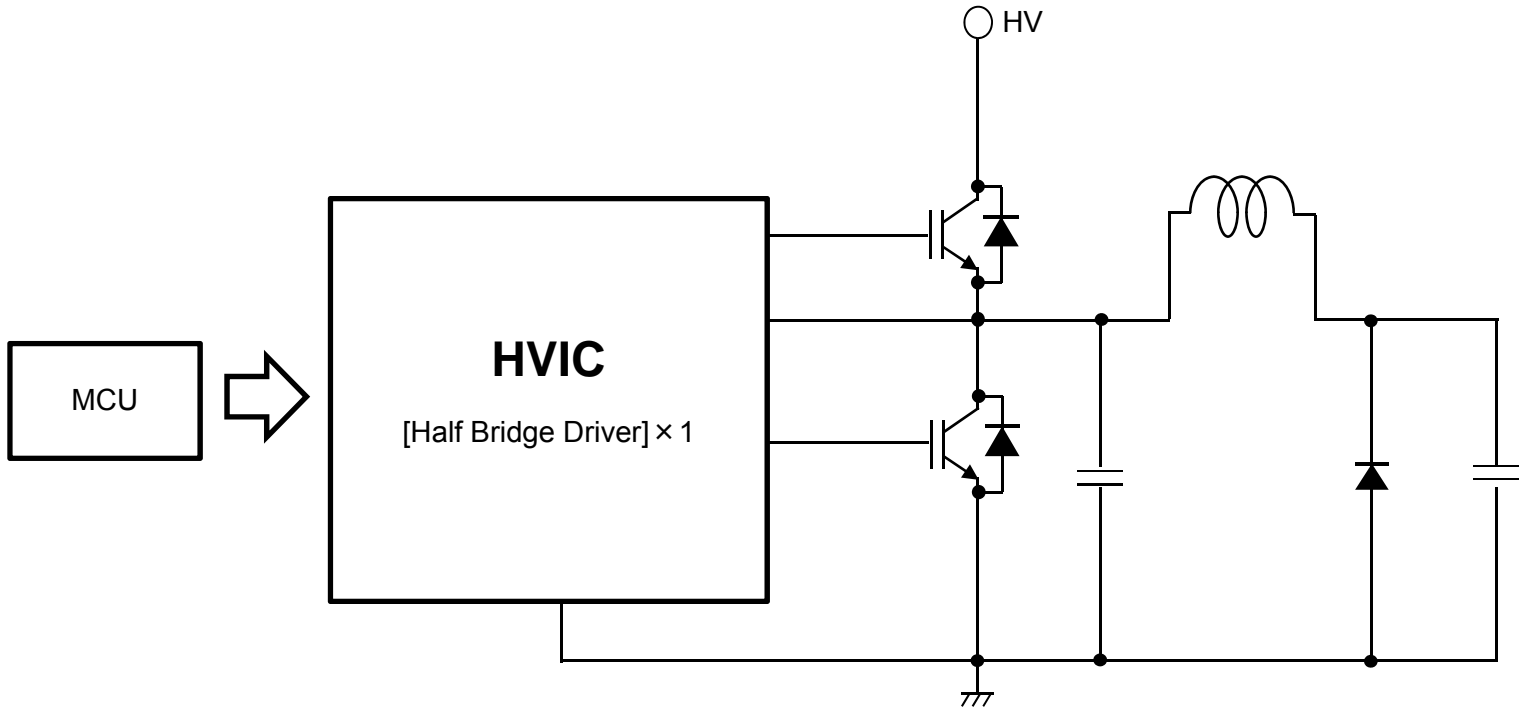


Fig.5 Gate driver for IH cooking heater(Half-bridge)

(6) Gate driver for PFC dual control(Low-side)

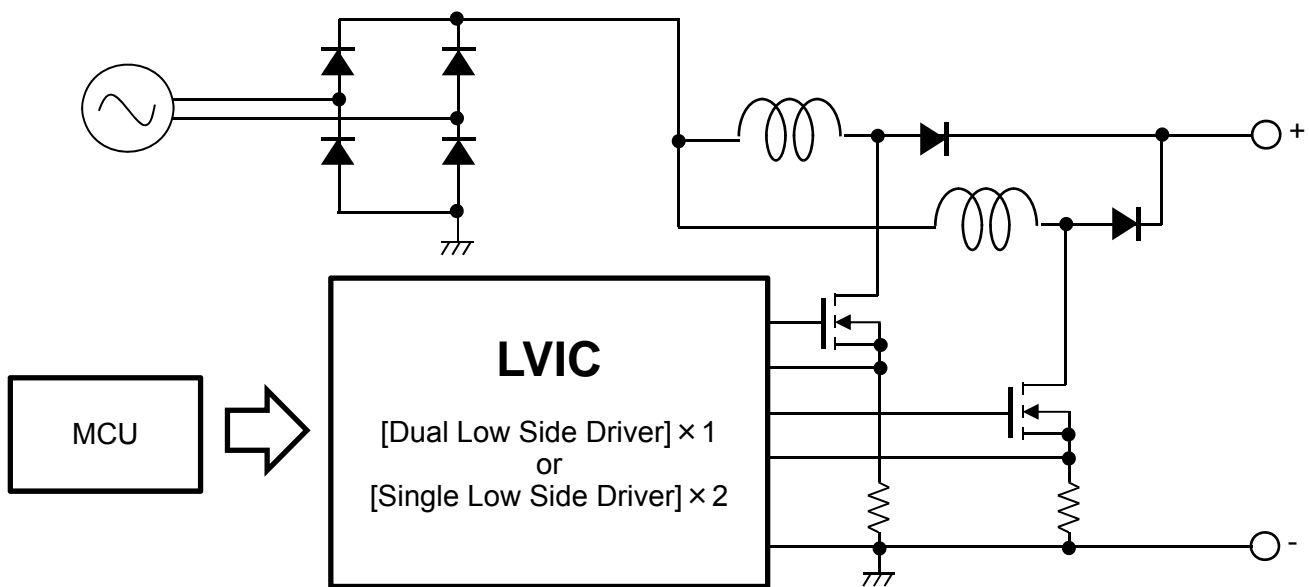


Fig.6 Gate driver for PFC dual control(Low-side)

(7) Gate driver for brake circuit(Low-side)

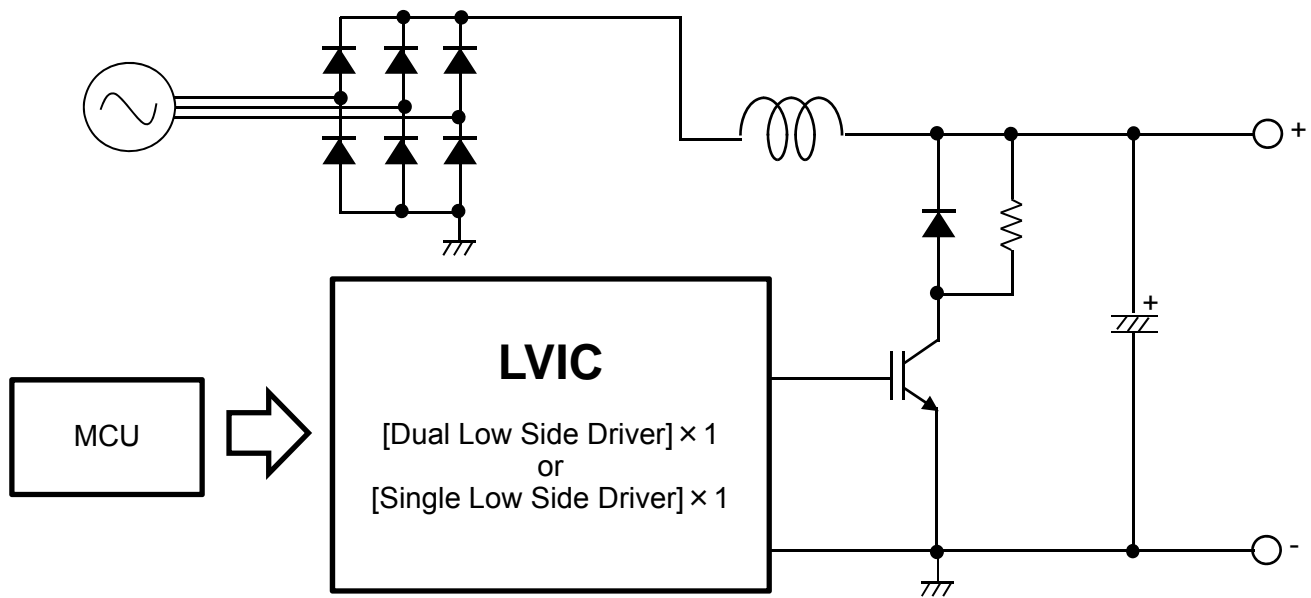


Fig.7 Gate driver for brake circuit(Low-side)

2. Attention points when using HVIC

2-1. Bootstrap circuit (For HVIC)

① Bootstrap circuit method and basic operation

The emitter/source potential of high-side IGBT/MOSFET referenced to GND changes to the voltage of the HV terminal from 0V when operating the application. Therefore, to drive high-side IGBT/MOSFET, the power supply of the high-side drive circuit of HVIC should have potential which is higher by VBS than the emitter/source potential of high-side IGBT/MOSFET. One of the methods to apply this voltage is the floating power supply method. Fig.8 shows the example of the floating power supply method.

Bootstrap circuit method is used in place of the floating power supply method. The bootstrap capacitor(C1) is charged through the resistor(R1) and bootstrap diode(D1) by VCC, and the high-side drive circuit of HVIC is driven by the voltage of the capacitor(C1). Fig.9 shows the example of the bootstrap circuit method.

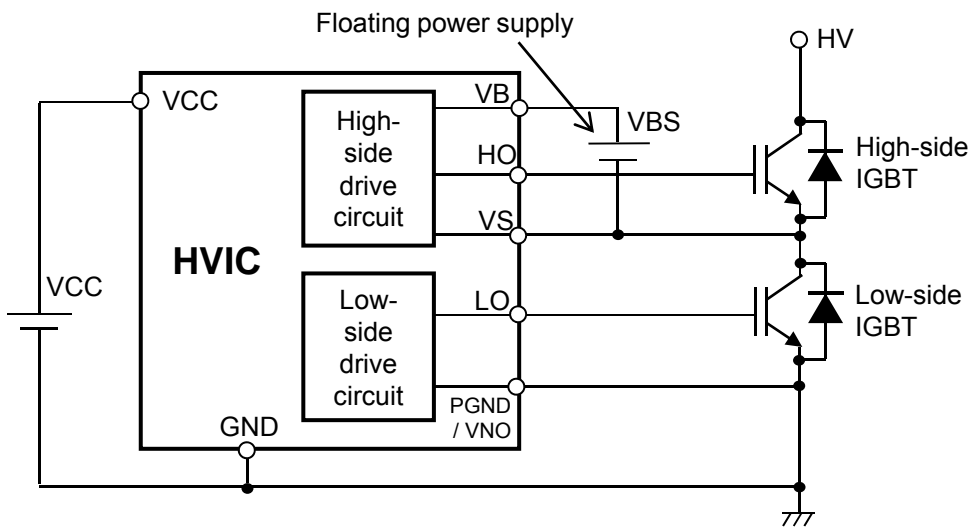


Fig.8 Floating power supply method

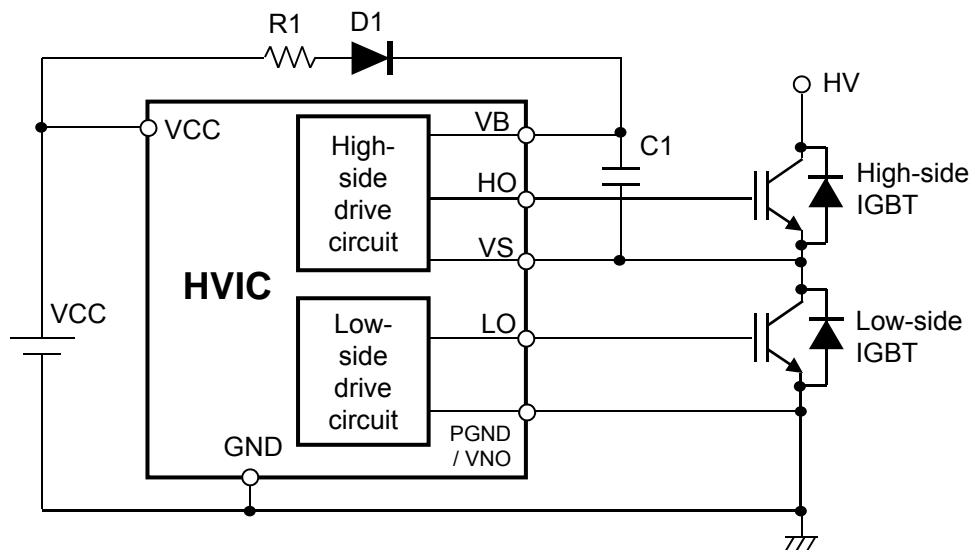


Fig.9 Bootstrap circuit method

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②Electrical charge and discharge current route when HVIC is operated

Fig.10 shows the electrical charge and discharge current route of C1 when HVIC is regularly operated.

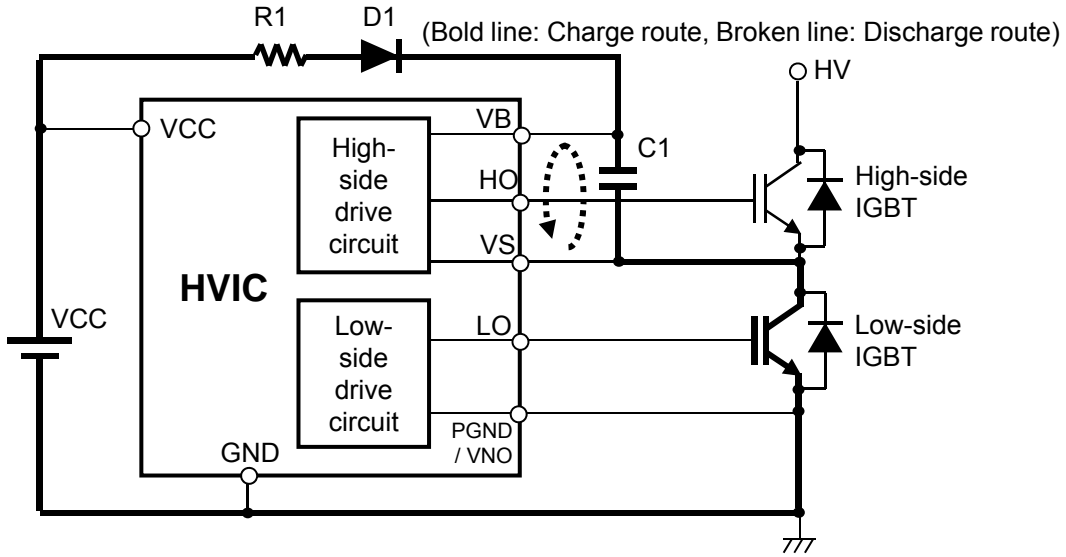


Fig.10 Electrical charge and discharge current route

③Initial charge and the voltage between the C1 terminals

Although it was shown that the high-side drive circuit of HVIC operates with the voltage between the C1 terminals in the preceding clause, it is necessary to charge the capacitor C1 up to a high enough voltage (more than the trip voltage of UV circuit of HVIC + margin) first of all to operate this high-side drive circuit after the power supply is applied to HVIC. This is called an initial charge of C1, and it is necessary for the initial charge of C1 to input the control signal that turns on low-side IGBT as shown in Fig.10.

Moreover, in regular operation of HVIC, while the low-side IGBT is off-state, the potential of C1 falls by the consumption current of the high-side drive circuit of HVIC, and the leak current of C1. Also, it is necessary to set off-time of the low-side IGBT so that the voltage of the C1 terminals doesn't become lower than the trip voltage of the UV circuit of HVIC. Fig.11 shows charge and discharge timing chart.

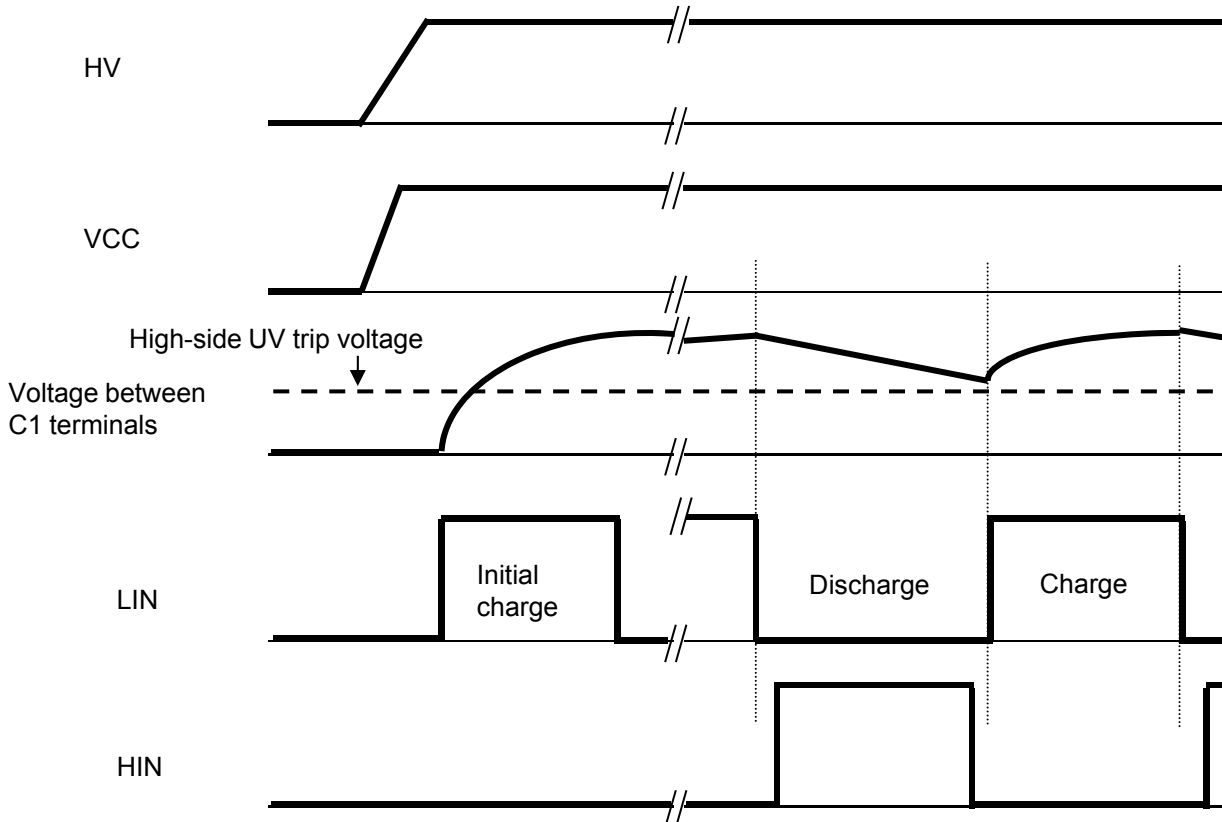


Fig.11 Charge and discharge timing chart in initial charge and regularity operation

④Setting of each constant value (R1,C1,D1) of the bootstrap circuit

• Setting of bootstrap capacitor (C1)

To drive high-side IGBT, the bootstrap capacitor is charged by turning on low-side IGBT. The charged voltage VC1 is shown below. (VF:Voltage between D1 terminals, Vce:Voltage between collector and emitter of low-side IGBT)

$$VC1 = VCC - VF - Vce \cdots (1)$$

The capacitance value C1 is shown below. (T1:Maximum on-time of high-side IGBT, IBS:High-side drive circuit consumption current of HVIC, ΔV:Electrical discharge allowance voltage between C1 terminals)

$$C1 = IBS \times T1 / \Delta V + \text{margin} \cdots (2)$$

IBS changes depending on gate capacitance of IGBT and carrier frequency. And (1) and (2) expression are simplified. So please set the capacitance value C1 based on evaluation of your system.

About the kind of capacitor, it recommends that the electrolysis capacitor which has excellent characteristics of temperature and frequency is connected in parallel with the ceramic capacitor for noise removal which has excellent characteristics of temperature and frequency.

• Setting of resistor (R1)

R1 is necessary to restrict inrush current during initial charge. Time to charge C1 is decided by C1 and R1. Therefore, when the minimum on-time of the low-side IGBT is set to T2, the value of R1 is set so that C1 can be charged by ΔV in the time of T2.

• Selection of diode (D1)

The high-speed recovery diode whose breakdown voltage is 600V/1200V or more is recommended.

2-2. Interlock circuit (For HVIC with a built-in interlock circuit)

Some of our HVICs contain an interlock circuit which prevents the high-side and low-side power semiconductors from simultaneously becoming high-state(Arm short) when high/low-side simultaneous turn-on signals are input. There are two types of interlock specifications as follows. For the type of the interlock built in each HVIC, please refer to the datasheet.

① Interlock for turning the high/low-side outputs to “low” in response to the input of simultaneous turn-on signals

• Active-High type

When HIN = LIN = “high” (ON), the logic circuit shown in Fig.12 turns the high-side and low-side outputs to “low” (OFF) thus preventing arm short of power semiconductors (IGBT/MOSFET).

• Active-Low type

The high/low-side outputs become ON when HIN = LIN = “low”, the circuit logic is inverse to that of the Active-High type described above. However, the simultaneous turn-on prevention circuit is configured according to the same principle as for the Active-High type.

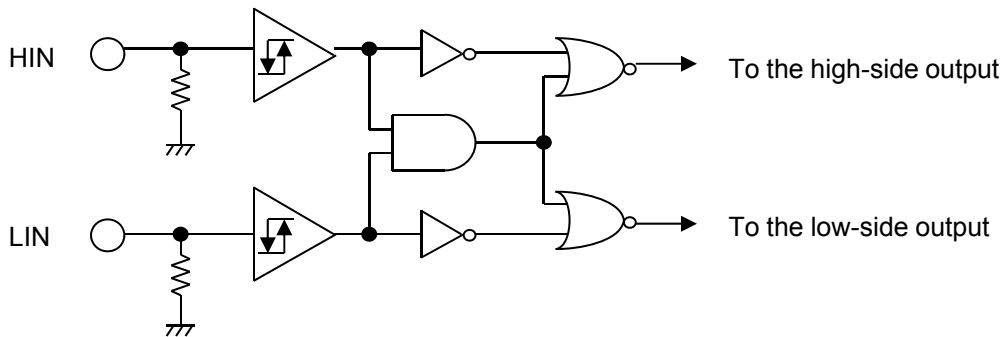


Fig.12 Interlock circuit (Output-Low type)

② Interlock for maintaining the high/low-side outputs in response to the input of simultaneous turn-on signals

• Active-High type

When HIN = LIN = “high” (ON), the logic circuit shown in Fig.13 keeps the high-side and low-side outputs in the same state as before the input of simultaneous turn-on signals thus preventing arm short of power semiconductors (IGBT/MOSFET).

• Active-Low type

The high/low-side outputs become ON when HIN = LIN = “low”, the circuit logic is inverse to that of the Active-High type described above. However, the simultaneous turn-on prevention circuit is configured according to the same principle as for the Active-High type.

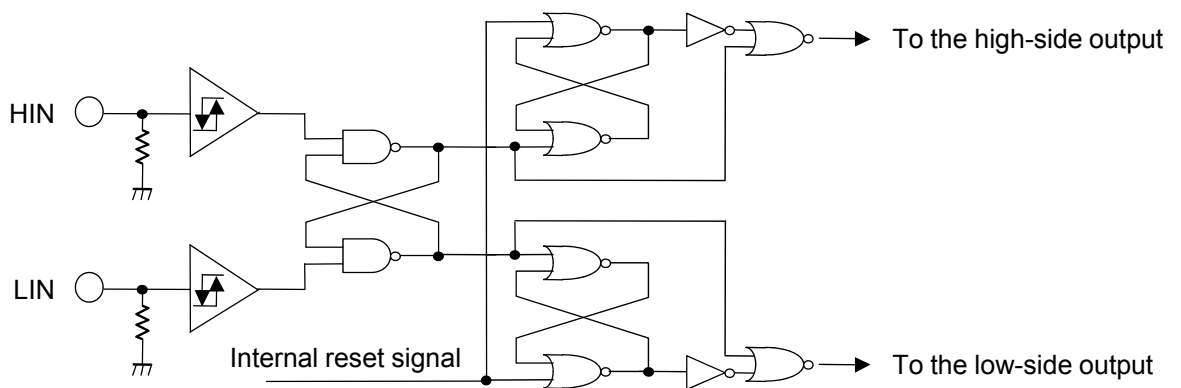


Fig.13 Interlock circuit (Output-maintaining type)

2-3. Malfunction due to Miller capacitance (For HVIC)

The gate voltage of the power semiconductor may change according to the influence of a parasitic element in the power semiconductor, the characteristic of HVIC and the mounting board condition when carrying out ON/OFF operation of the power semiconductor (IGBT/MOSFET) using HVIC and the malfunction may be caused. The mechanism and improvement plan of such a malfunction are shown below. The relation of malfunction by parasitic capacitor is shown in Fig.14(The bootstrap circuit is omitted.).

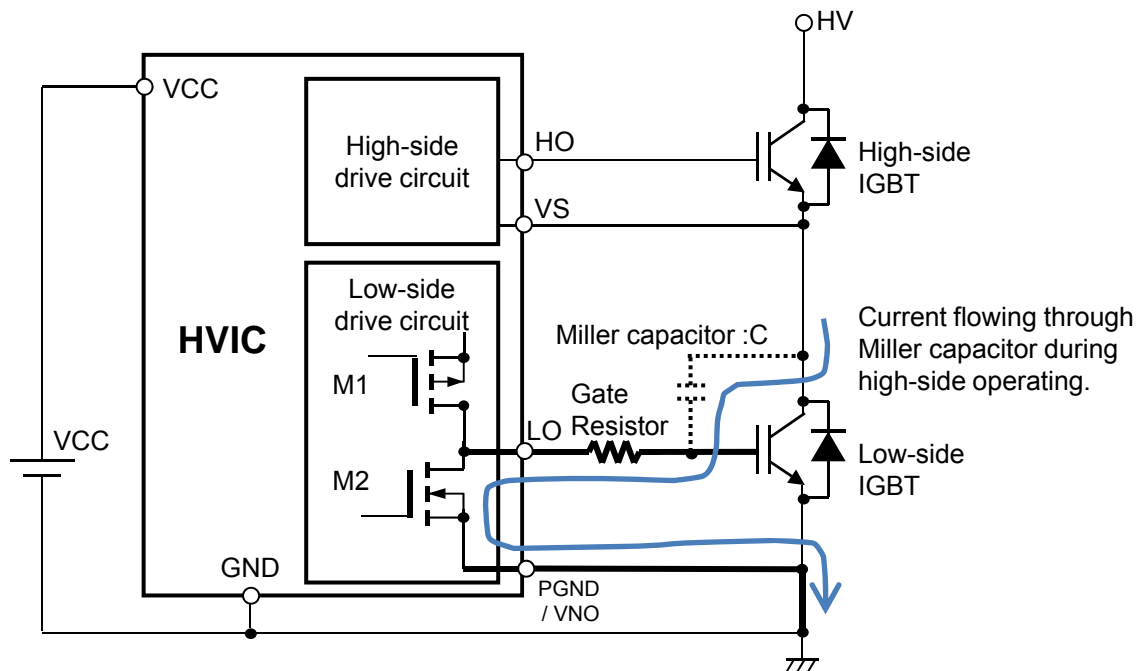


Fig.14 Relation between parasitic capacitor and malfunction of power semiconductor

• Mechanism of malfunction

When high-side IGBT turns on, dv/dt is caused at the emitter of high-side IGBT (The collector of low-side IGBT). At this time, transient current flows through the parasitic capacitor between collector and gate of low-side IGBT and the gate resistor. And the gate voltage of low-side IGBT increases. If the gate voltage exceeds the threshold voltage of low-side IGBT, arm short is caused at high/low-side IGBT.

• Improvement plan

- ① Select power semiconductor with small capacitance value of Miller capacitor C.
- ② Increase the gate resistor of high-side power semiconductor.
- ③ Decrease the gate resistor of low-side power semiconductor.
- ④ Shorten and widen the trace between power semiconductor and HVIC.
- ⑤ Select HVIC with a built-in Miller clamp circuit.

Miller clamp circuit creates a bypass to the emitter of low-side IGBT for the transient current, and restricts the gate voltage increase. Please refer to the datasheet for HVIC with a built-in Miller clamp circuit.

2-4. VS undershoot (For HVIC)

The voltage of VS terminal can be lower than that of GND terminal transiently because of the arrangement and the trace for the elements on the mounting board when carrying out ON/OFF operation of the power semiconductor (IGBT/MOSFET) using HVIC and the malfunction may be caused. The relation between malfunction and VS undershoot is shown in Fig.15.

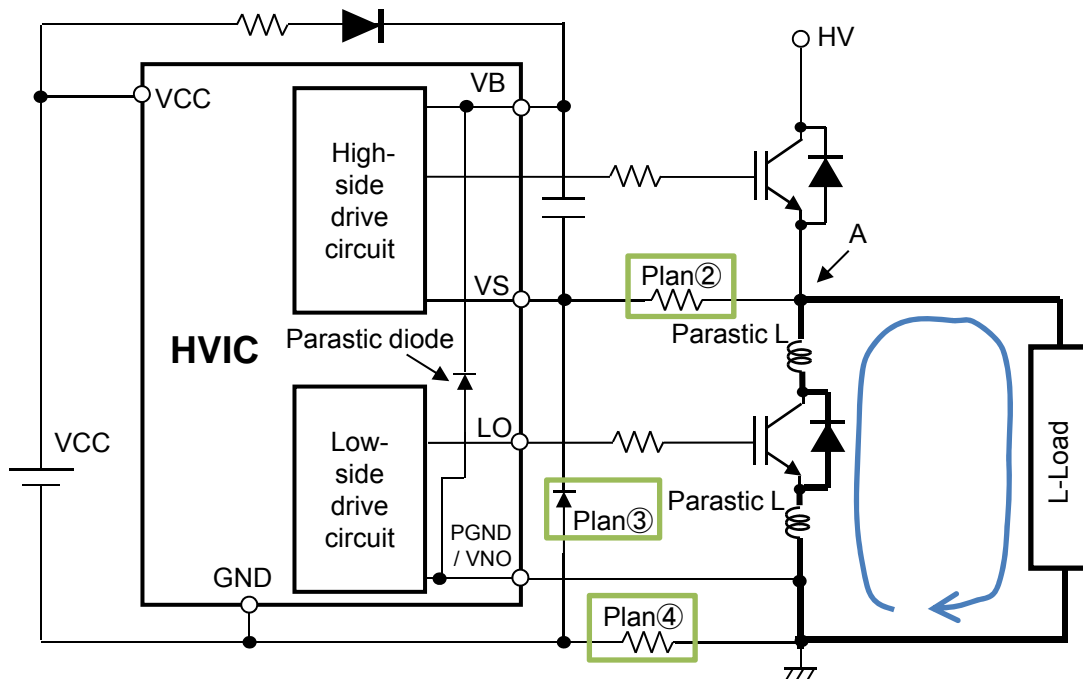


Fig.15 Malfunction in connecting L-Load

• Mechanism of malfunction

When high-side IGBT turns off, low-side IGBT enters a freewheeling mode. At this time, the potential of A point falls to less than that of GND; minus potential. The potential of the VS and VB terminal of HVIC becomes minus potential correspond with the potential of A point, too. When the VB terminal falls to minus potential, a parasitic diode in HVIC is turned on, and large current flows. HVIC may cause malfunction.

If high-side IGBT tries to turn on during VS minus period, the high-side output signal of HVIC cannot output. Please input ON-signal when VS voltage satisfies recommended operating conditions. Please refer to the datasheet for recommended operating conditions of HVIC.

• Improvement plan

- ① Increase the gate resistor of high-side power semiconductor, and decrease the transient current flowing through parasitic L.
- ② Add the resistor between A point and VS terminal, and restrict VS voltage decrease. However, this resistor is placed on the charge route of bootstrap capacitor. So the gate voltage of high-side IGBT increases, arm short can be caused. Please select appropriate resistance value.
- ③ Inserts a diode which has small VF between GND terminal and VS terminal.
- ④ Restrict the current flowing through the diode(Plan③) by adding the resistor between GND and PGND/VNO, and enhance the clamp effect of the diode.
- ⑤ Shorten and widen the trace of the bold line in Fig.15.

2-5. Minimum transmission VCC voltage (For HVIC)

Definition of minimum transmission VCC voltage:

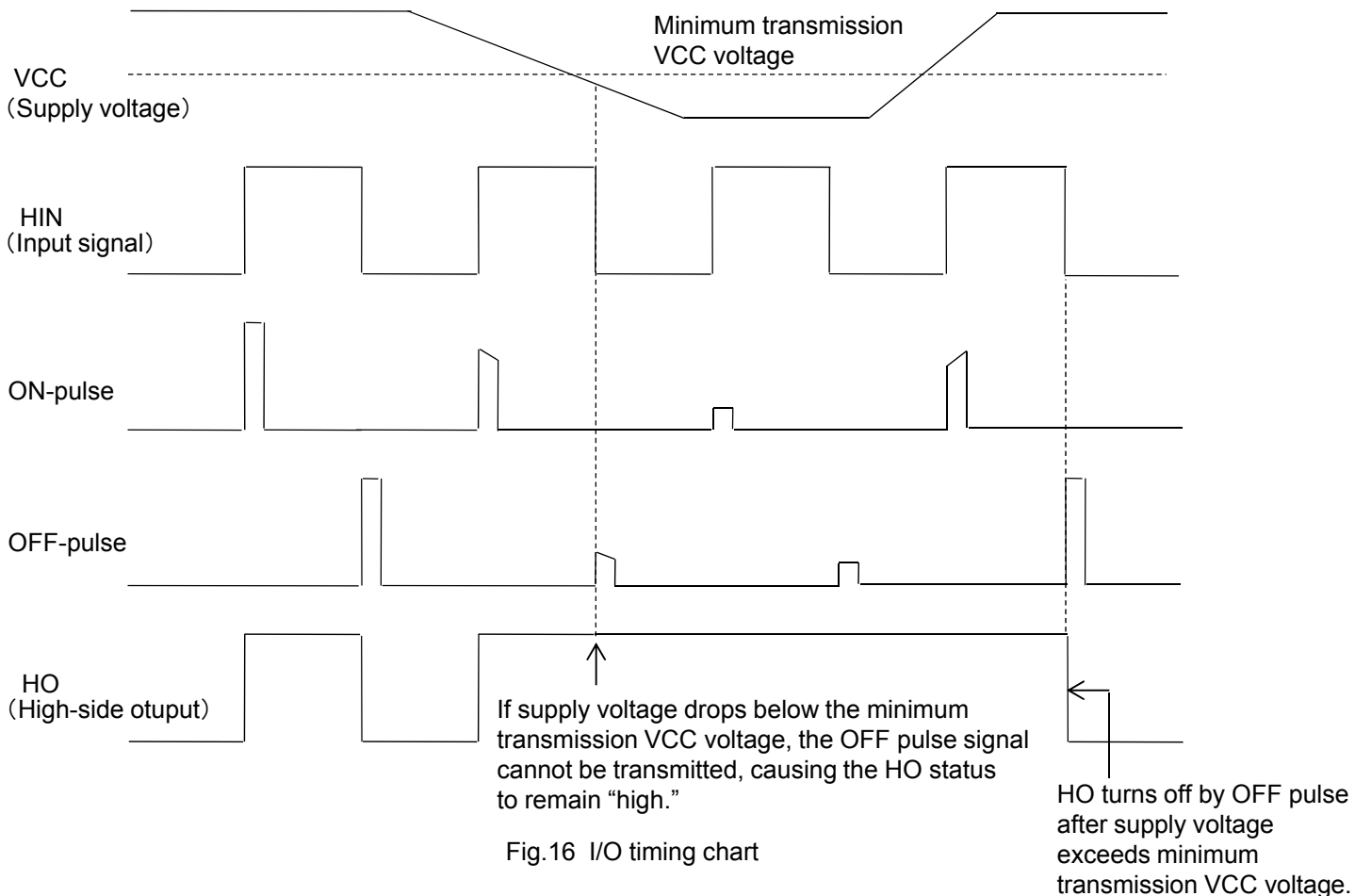
The “minimum transmission VCC voltage” is the minimum level of supply voltage required for signal transmission, and not the voltage at which the HVIC can meet all specified characteristic requirements, such as transmission time and output performance, under recommended operating conditions.

The phenomenon is explained below that the HVIC output is not reset (not turned off) despite the input of “low” signal (signal level to turn off the output) when VCC voltage drops while VB supply voltage is normal.

Fig.16 shows I/O timing chart. When the “high” signal is applied to the high-side input (HIN) pin, ON pulse occurs at the rising edge timing of the signal. The ON pulse enters the set input pin of the latch circuit. As a result, the output of the latch circuit becomes “high,” turning the high-side output (HO) status to “high.” Similarly, when the “low” signal is applied to the HIN pin, OFF pulse occurs at the falling edge timing of the signal. The OFF pulse enters the reset input pin of the latch circuit, causing its output to become “low,” turning the HO status to “low.”

As shown in Fig.16, if VCC voltage drops below the minimum level for signal transmission, OFF pulse signal might not be transmitted, causing the HO status to remain “high” even when the signal input to the HIN pin switches from “high” to “low”.

If the high-side supply voltage (VB) drops and activates the under voltage (UV) lockout circuit, the HO status becomes “low” regardless of the HIN status.



2-6. Narrow pulse input (For HVIC)

In high-side circuit, if narrow pulse signal is input, the overlap may occur between turn-off propagation delay time(Fig.17②) and dv/dt of VS voltage(Fig.17④). At this time, OFF signal may not be transmitted due to a logic filter circuit which prevents malfunction by dv/dt . Please set long enough pulse input.

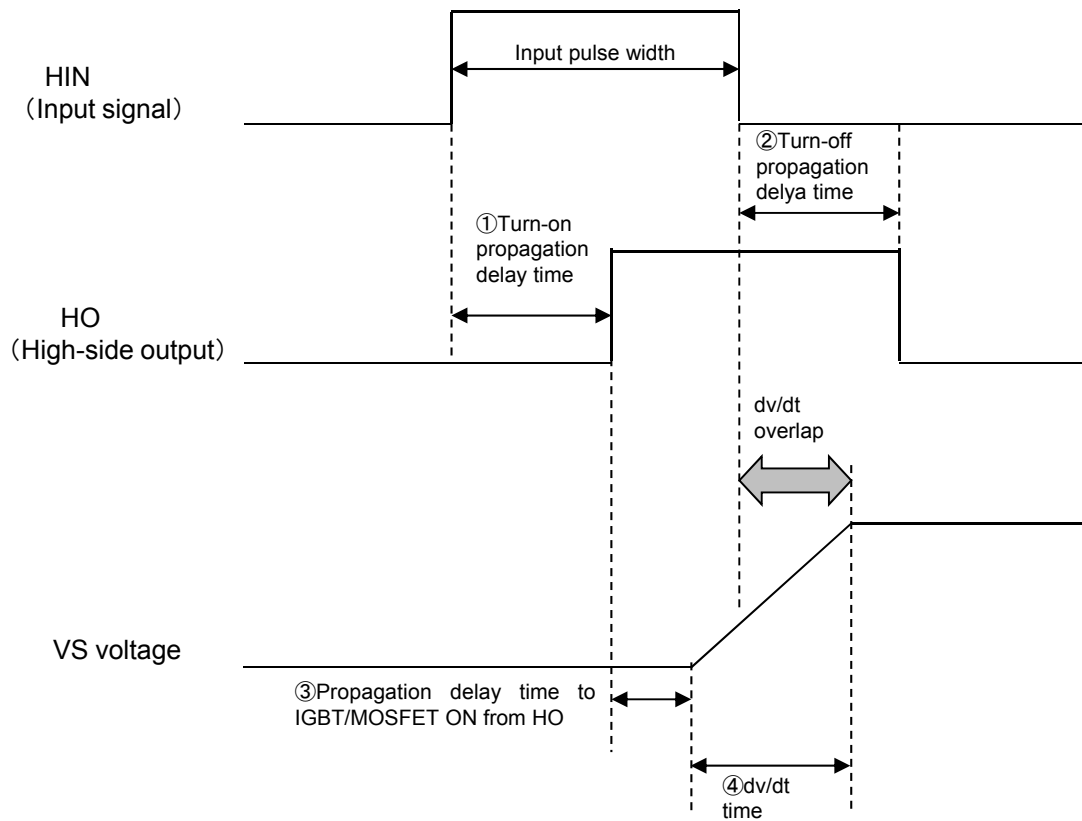


Fig.17 Malfunction timing chart due to narrow pulse input

2-7. Over-current protection (For HVIC with a built-in over-current protection circuit)

2-7-1. Sense resistor method (For HVIC with a built-in CIN over-current protection circuit)

Fig.18 shows connection example using sense resistor method. Fig.19 shows the timing chart.

The shunt resistor(For current sense) is set. The voltage which is caused by the current flowing through the shunt resistor feeds back CIN terminal of IC. And the over-current protection of power semiconductor can be carried out when the voltage of CIN terminal exceeds the threshold voltage(CIN trip voltage). At this time, the power semiconductor is shut down and fault signal(FO) is output. Please set RC filter to the CIN terminal to prevent malfunction due to noise and recovery current in switching. The shunt resistance value is set as below($V_{SC(REF)}$:CIN trip voltage, SC:Current to be shut down).

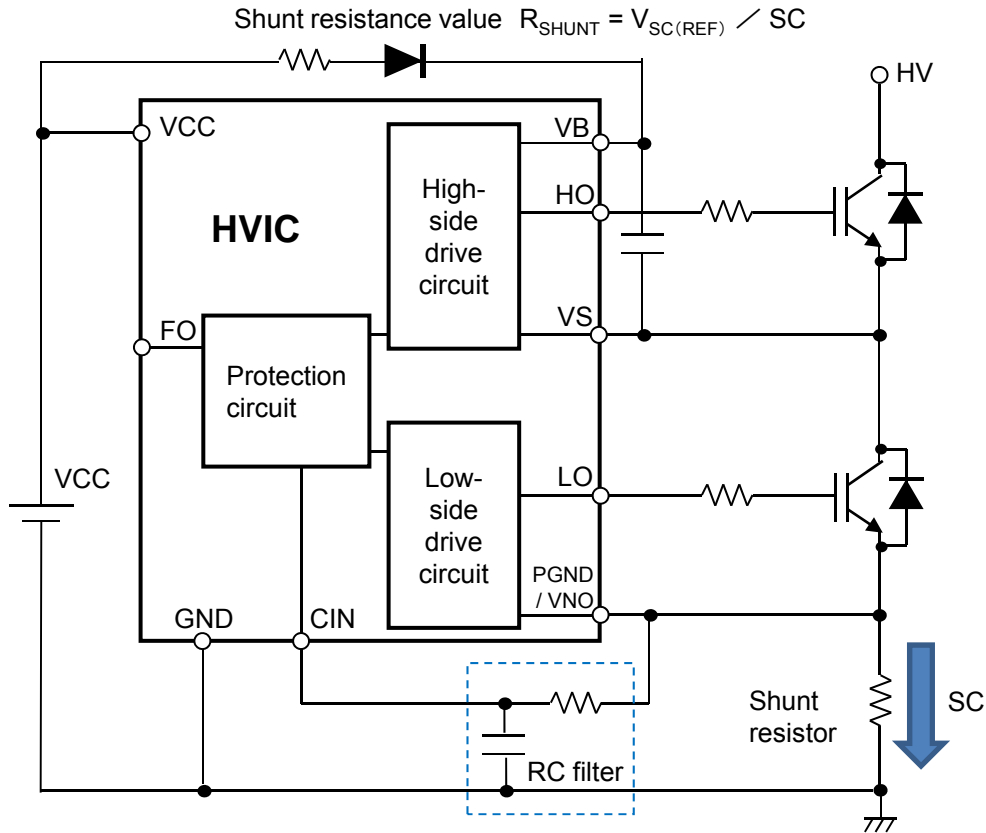


Fig.18 Connection exaple using sense resistor method

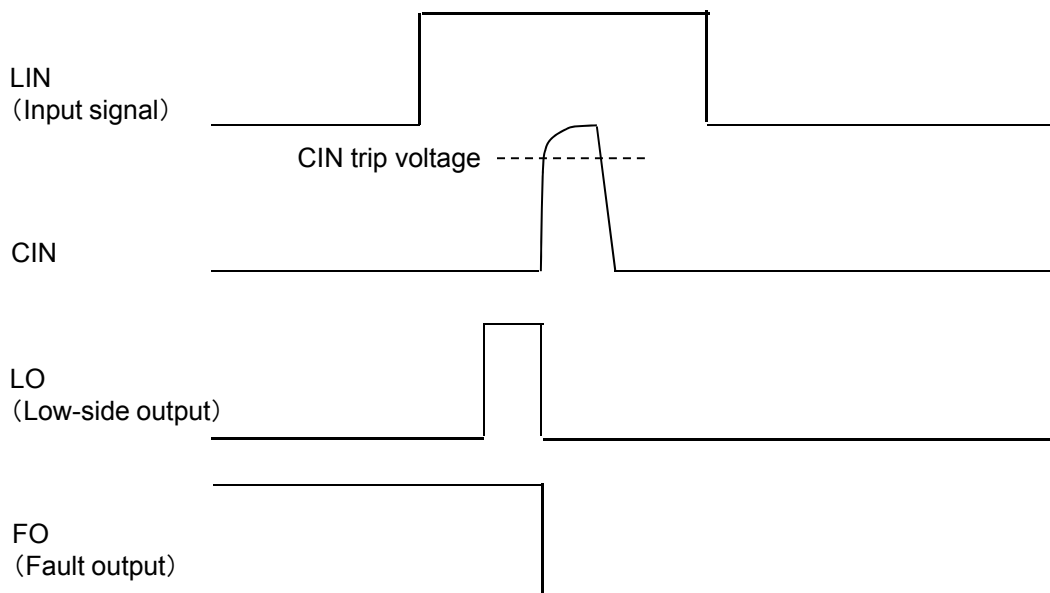


Fig.19 Timing chart using sense resistor method

2-7-2. Desaturatin method (For HVIC with a built-in DESAT over-current protection circuit)

Fig.20 shows connection example using desaturation method. Fig.21 shows the timing chart.

High voltage diode and blanking capacitor are connected to DESAT terminal. When IC output is "high" and power semiconductor is ON-state, the current flows from the DESAT terminal. When Vce of the power semiconductor is saturated, the current flows to the power semiconductor. On the other hand, when Vce of the power semiconductor is desaturated, the current charges the blanking capacitor. If the voltage of DESAT terminal exceeds the threshold voltage, the desaturation is detected. At this time, IC output is shut down and fault signal(FO) is output. Regarding the operating sequence, there is no difference between high-side and low-side.

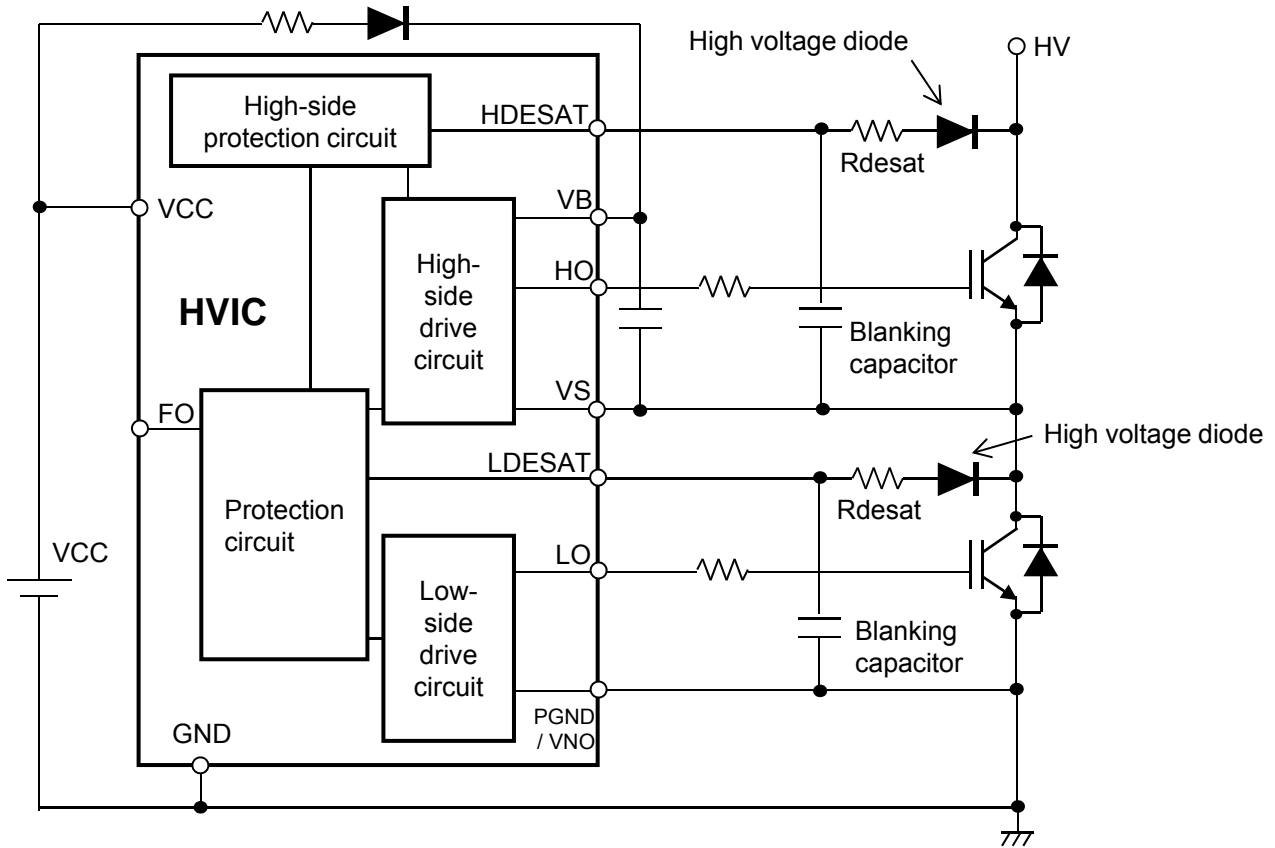


Fig.20 Connection example using desaturation method

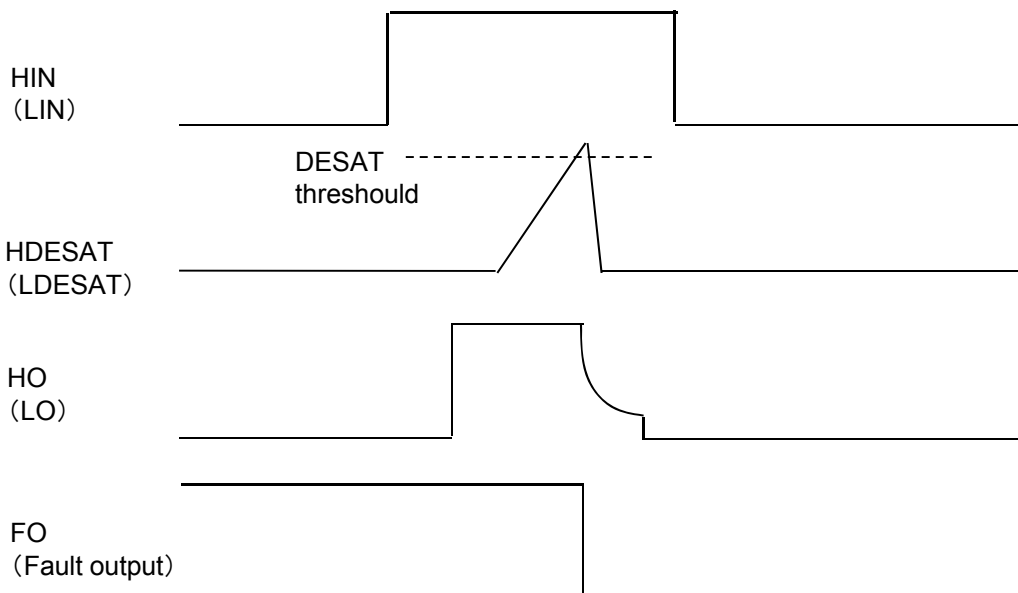


Fig.21 Timing chart using desaturation method

•Vce to detect desaturation

Vdesat which is monitored at DESAT terminal is shown below (Vce:Voltage between collector and emitter of IGBT, Idesat:Current flowing from DESAT terminal, Rdesat:Resistor connected to DESAT terminal).

$$V_{desat} = V_{ce} + I_{desat} \times R_{desat} \dots (1)$$

Please refer to the dataset for the DESAT threshold and Idesat. Vce is depending on IGBT. Please set Vce to detect desaturation according to the power semiconductor. And please set Rdesat using (1) expression.

•Blanking time

Desaturation is detected when IC output is "high". However, it is necessary that delay(Blanking) time is set to the detection of desaturation from IC output to prevent malfunction. The blanking time is shown below.

$$t_{BLANK} = C_{blank} \times V_{desat} / I_{desat} + t_0 \dots (2)$$

Cblank indicates the blanking capacitor in Fig.20. The t₀ blanking time is set in HVIC. So when Cblank equals 0(pF), the blanking time is t₀. Please refer to the DESAT threshold, Idesat and t₀. Please set the blanking capacitor using (2) expression according to the blanking time to be set.

2-8. Gate resistor (For HVIC)

Fig.22 shows gate drive circuit using HVIC. The gate resistor R_g is shown below (I_{source} : Source current of HVIC, I_{sink} : Sink current of HVIC, R_{on} : ON resistance for source output, R_{off} : OFF resistance for sink output).

$$R_g = VCC / I_{source} - R_{on}$$

$$R_g = VCC / I_{sink} - R_{off}$$

And the gate resistor R_g is shown below (t_{swon} : ON switching time, t_{swoff} : OFF switching time, Q_g Δ : Gate charge amount of IGBT).

$$R_g = VCC \times t_{swon} / Q_g - R_{on}$$

$$R_g = VCC \times t_{swoff} / Q_g - R_{off}$$

The expressions as shown above are simplified. When you set the gate resistance value, please evaluate your system with consideration for switchin time, loss and surge voltage.

Fig.22 shows low-side circuit. However high-side circuit is same as low-side circuit.

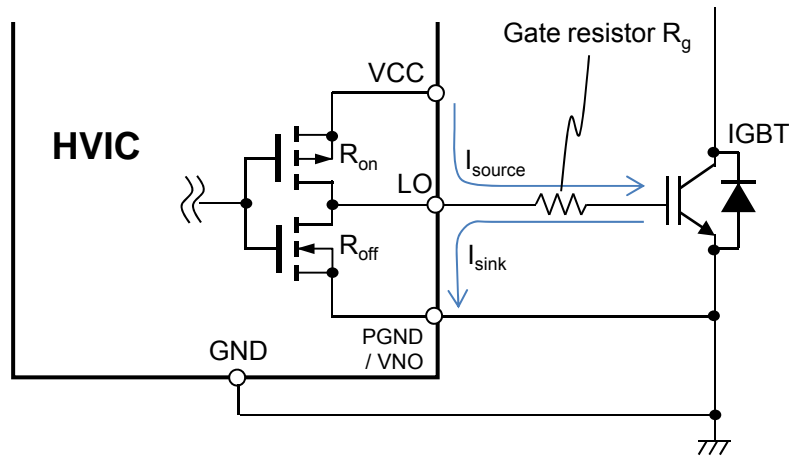


Fig.22 Gate drive circuit using HVIC

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2-9. Attention points of circuit board (For HVIC)

2-9-1. Sense resistor method (For HVIC with a built-in CIN over-current protection circuit)

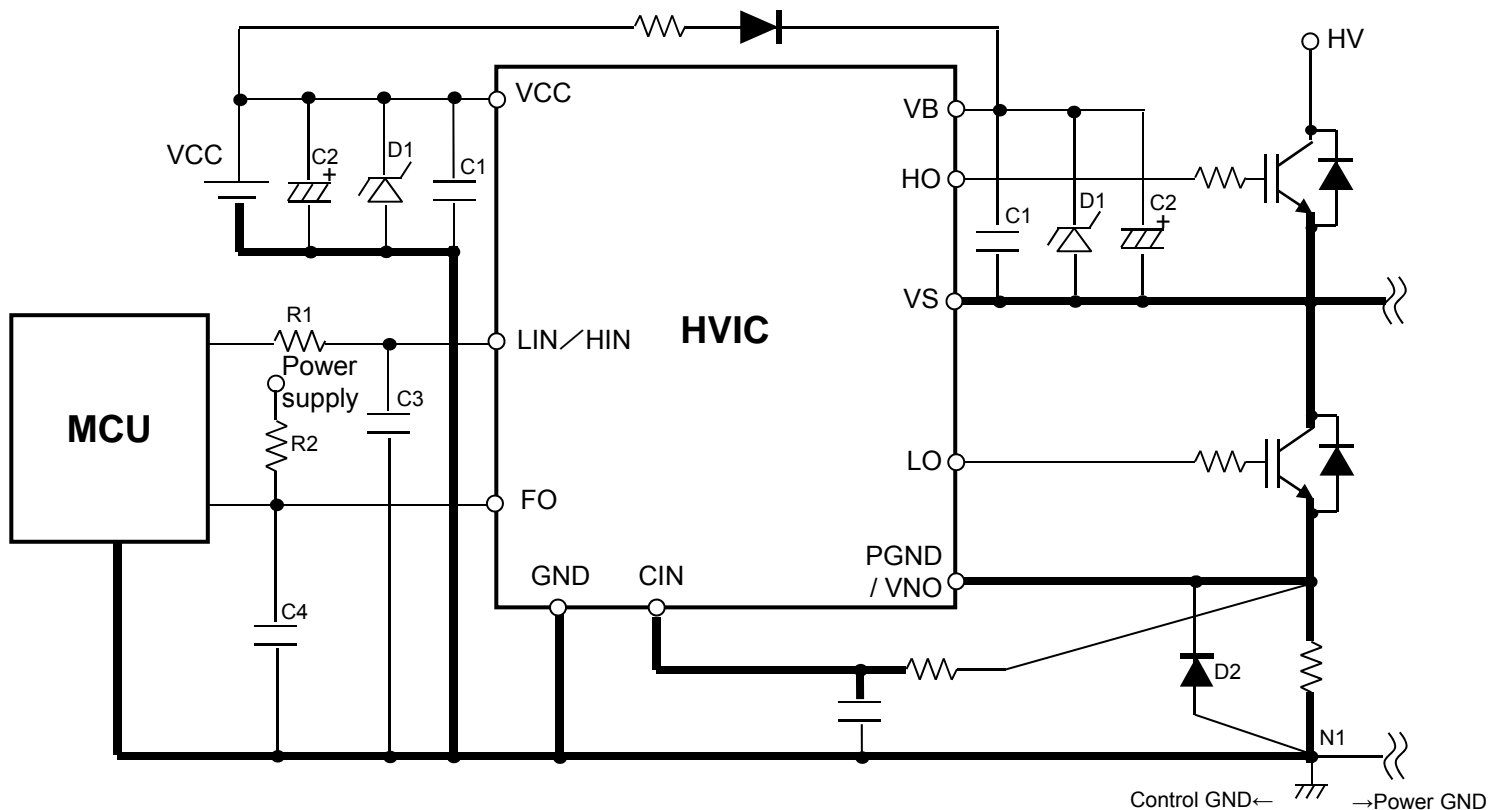


Fig.23 Attention points of circuit board using sense resistor method

- More moderate power supply noise than $\pm 1V/\mu s$ and smaller ripple voltage than 2V are recommended to prevent a malfunction. Even when the ripple voltage is less than 2V, recommended operating conditions have to be satisfied.
- Film or ceramic capacitor (C1: 0.22~2 μF) in parallel with electrolytic capacitor (C2) is recommended as power supply noise filter.
- Zener diode (D1) is recommended to absorb power supply surge. The zener voltage has to be less than the absolute maximum ratings of power supply terminal of HVIC.
- MCU is brought close to HVIC to decrease a line impedance.
- RC filter (R1, C3) is recommended in high noise condition.
- FO is connected to a pull-up resistor (R2) which makes a sink current less than 1mA. (Ex. 10k Ω @5V)
- Film capacitor (C4: 1nF) is recommended in high noise condition.
- The bold line in Fig.23 has a large effect on the operation of HVIC and power semiconductor. Shorten and widen the bold line in Fig.23 to decrease a line impedance.
- It is recommended to connect control GND and power GND at only a point N1.
- Diode (D2) between PGND/VNO and N1 is recommended in high noise condition.

2-9-2. Desaturatin method (For HVIC with a built-in DESAT over-current protection circuit)

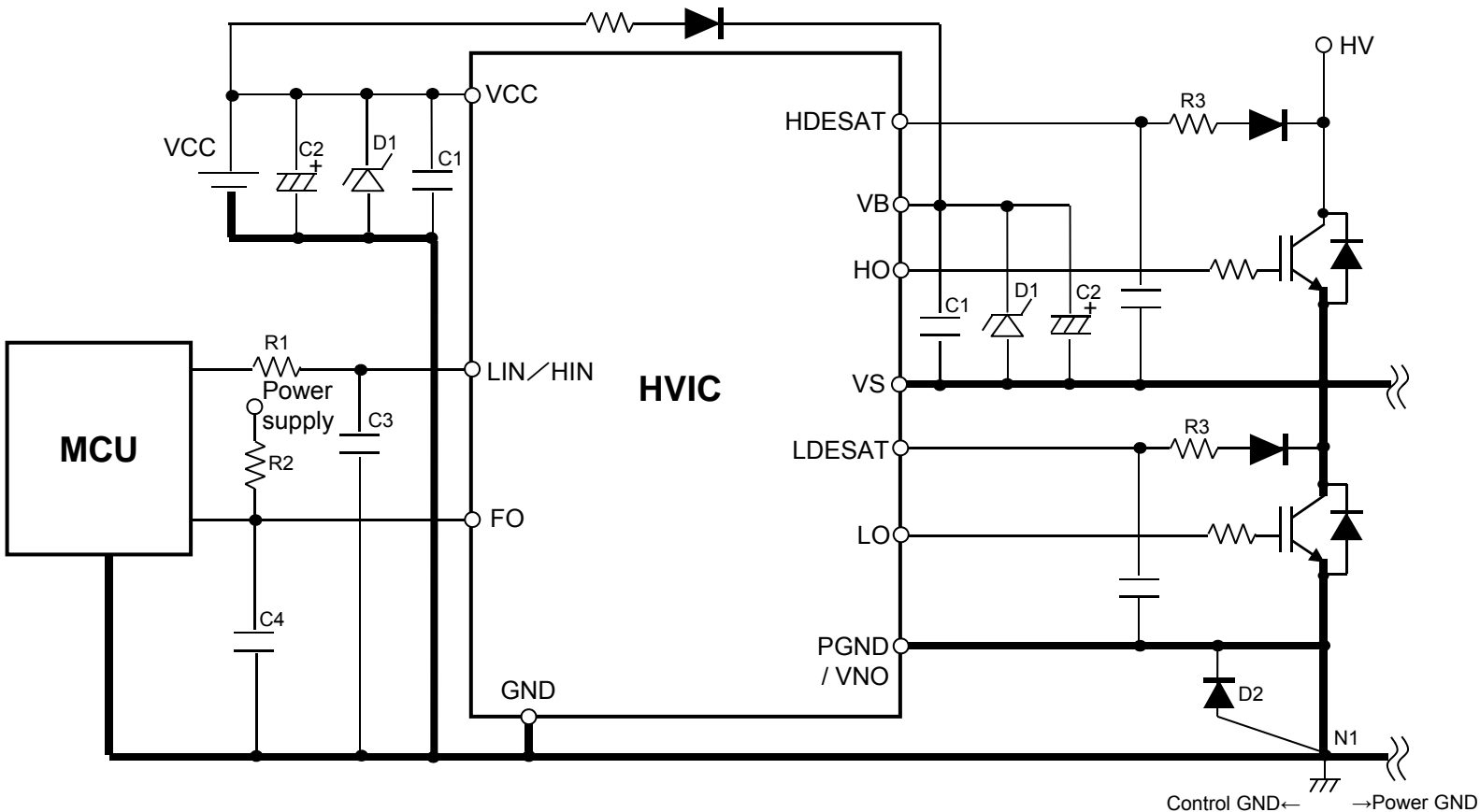


Fig.24 Attention points of circuit board using desaturation method

- More moderate power supply noise than $\pm 1V/\mu s$ and smaller ripple voltage than 2V are recommended to prevent a malfunction. Even when the ripple voltage is less than 2V, recommended operating conditions have to be satisfied.
- Film or ceramic capacitor(C1:0.22~2 μF) in parallel with electrolytic capacitor(C2)is recommended as power supply noise filter.
- Zener diode(D1) is recommended to absorb power supply surge. The zener voltage has to be less than the absolute maximum ratings of power supply terminal of HVIC.
- MCU is brought close to HVIC to decrease a line impedance.
- RC filter(R1,C3) is recommended in high noise condition.
- FO is connected to a pull-up resistor(R2) which makes a sink current less than 1mA. (Ex.10k Ω @5V)
- Film capacitor(C4:1nF) is recommended in high noise condition.
- The bold line in Fig.23 has a large effect on the operation of HVIC and power semiconductor. Shorten and widen the bold line in Fig.23 to decrease a line impedance.
- It is recommended to connect control GND and power GND at only a point N1.
- Diode(D2) between PGND/VNO and N1 is recommended in high noise condition.
- Resistor(R3) is recommended to restrict recovery current. DESAT terminal has to be less than the absolute maximum ratings.
- The high-speed recovery and high voltage diode(D3) is recommended.

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3. Notes in handing

■ To use HVIC safely

The production activity is done to reliability and quality especially in the development of the HVIC unit (Hereafter, it is called an unit) and production with the best of care. However, the reliability of the unit is greatly influenced by not only a factor peculiar to the unit but also use conditions. Please often read notes shown next when you handle our unit and use it correctly.



Cautions

Packaging	The packing box and the interior material of the unit shipped by our company come to be able to endure a constant environment and the condition. However when the packing box is exposed to the outside impact, rain water and pollution, the packing box and the interior material might break and the unit is exposed. Please note handling enough.
Carry	<ul style="list-style-type: none"> • Please put the packing box on the correct direction while transporting it. It keeps inverted, and it leans it. And then unnatural power might join, and it breaks. (This side up) • If it throw out or it drop, the unit might break. (Fragile attention) • It is necessary not to get wet by the water. Please note that it is wetting for the transportation at the rainfall snow. (Water wet attention) • When another of the above-mentioned point is transported, a mechanical vibration and the impact are reduced as much as possible. Please note the way. The unit might break.
Keeping	<ul style="list-style-type: none"> • The temperature and the humidity of the place where the unit is kept as a standard with 5-30°C and about 40-60% Normal temperature is preferable, and avoid each of the temperature and humidity too far apart, please. Moreover, keep it in the place where the temperature changes drastically, the dew of moisture happens in the surface of the unit and the lead part. Thus keep it in the place where the temperature change is a little as much as possible, please. • Keeping by the place where causticity gas generates, an organic solvent or explosiveness dust, etc. exists causes corrosion, the malfunction, and destruction of the units. Thus avoid these places. • You must do not pile up the packing box high, and put the heavy one on the packing box. As a result, the packing box breaks, the cargo collapses, and it is dangerous.
Long storage	If you need long storage, you must do not open the wrapping box. Moreover, if you use the units kept at putting on a very bad environment and a long term is passed, you must confirm it without the wound, dirt or rust.
Ratings characteristics	Absolute maximum ratings defines that our company guarantees maximum ratings. If you use unit beyond this ratings, it brings its reliability, damage or destroy. To avoid these phenomena and realized on the interfacial devices high reliably, we recommend that unit is operated within the ratings and the regulations. And then it makes unit operate effectively for the characteristic and economical point views.
Ambient temperature	Temperature ratings have two ratings. One is operation temperature rating. Another is storage temperature rating. Please use within range of the temperature decided respectively. If it used the exceeding ratings of the operation and storage temperature, it becomes deterioration or destruction of the unit.
Noise	This device is composed of junction isolation structure. Therefore when I/O potential of the unit is less than -0.5V by external noise etc, a parasitic unit operates. Therefore, adjacent transistors inside of the unit cannot isolate, and becoming causes of the decrease in the circuit malfunction and no output and the destruction of the device, etc.
Flame resisting	It is not nonflammability though 94-V0 recognition goods of the UL standard are used for the epoxy molding resin material of this unit.
Electrostatic protection	It is necessary to note static electricity especially in the semiconductor unit. It is preferable to suppress the static electricity level of the working environment to 100V or less, and the mind for which do not use insulation thing (especially, artificial fiber and plastics product) it that humidifies at a dry period, avoids the state of low humidity, and uses the one of electro conductive (electro conductive mat, electrostatic work wear, and Mitibidencts) is injuring necessary for that.

Main Revision for this Edition

No.	Date	Revision	
		Pages	Points
A	Mar 2009	-	New making
B	Jul 2015	-	Review table of contents and enhance contents.

Keep safety first in your circuit designs!

Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

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