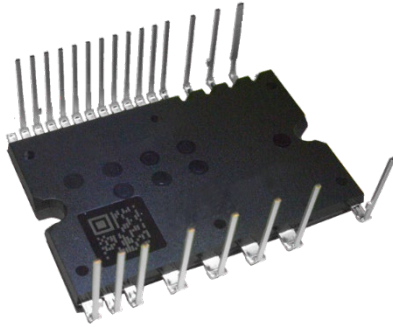


< DIPFC >

PSF30L92A6-A

TRANSFER MOLDING TYPE
INSULATED TYPE

OUTLINE



[-A : Long terminal]

MAIN FUNCTION

- Interleaved PFC (SiC MOSFET / SiC SBD)
- DC-DC converter

* SBD: Schottky Barrier Diode

RATING

- 30Arms/220Vrms input

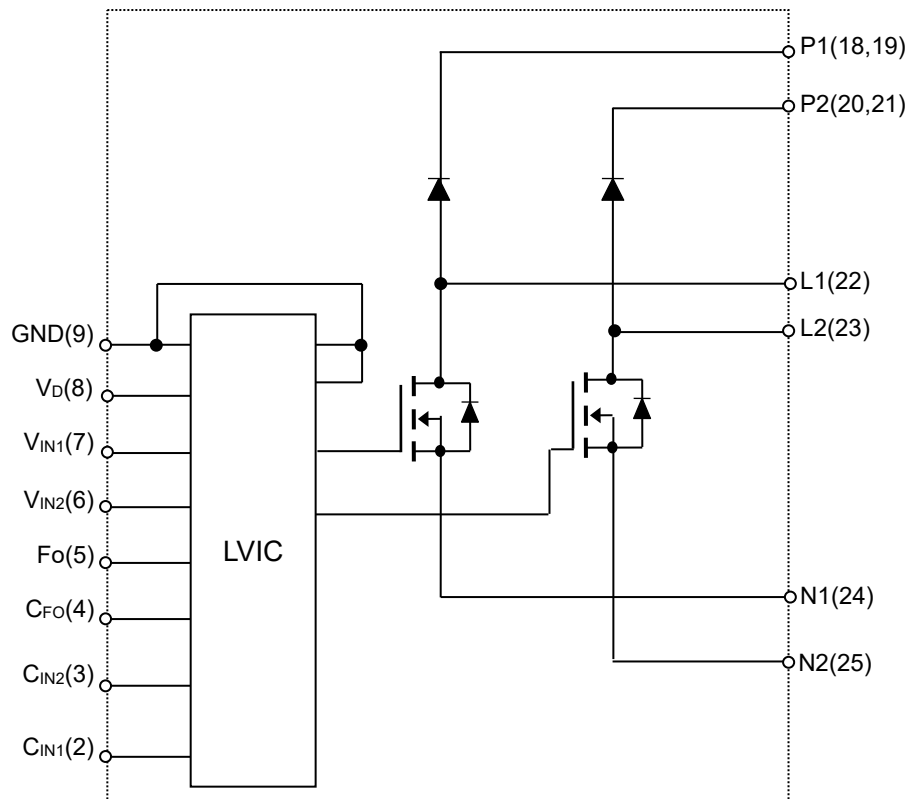
APPLICATION

- AC100-240V active converter for air conditioner and motor inverter drive

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- Drive circuit, Protection circuit (Control supply under-voltage :UV, Over current :OC)
- Fault signaling : Corresponding to OC fault and UV fault
- Input interface : 3~5V high active logic
- UL Recognized : UL1557 File E323585

INTERNAL CIRCUIT



Pin No.1 and 10~17 should leave no connection(NC).

PSF30L92A6-A**TRANSFER MOLDING TYPE
INSULATED TYPE****MAXIMUM RATINGS** ($T_{ch}=25^{\circ}\text{C}$ (MOSFET) / $T_j=25^{\circ}\text{C}$ (SBD), unless otherwise noted)**CONVERTER PART**

Symbol	Parameter	Condition	Ratings	Unit
V_i	Input supply voltage	Between L1-N1, L2-N2 terminals	276	V_{rms}
$V_{i(surge)}$	Input supply voltage (surge)	Between L1-N1, L2-N2 terminals	500	V
V_{CC}	Output Voltage	Between P1-N1, P2-N2 terminals	450	V
$V_{CC(surge)}$	Output Voltage (surge)	Between P1-N1, P2-N2 terminals	500	V
V_{DSS}	Drain-source voltage	Between L1-N1, L2-N2 terminals	600	V
V_{RRM}	Repetitive peak reverse voltage	Between P1-L1, P2-L2 terminals	600	V
I_i	Input current(100% Load)	$T_c \leq 100^{\circ}\text{C}$, $V_i = 220V_{rms}$, $V_{CC} = 370V$, $f_{PWM} \leq 30\text{kHz}$, Inductance of input = 0.2mH	30	A_{rms}
I^2t	I^2t for fusing	Value at 1cycle of surge current, Non-repetition, $t_w \geq 8.3\text{ms}$, Between L1-P1, L2-P2 terminals	100	A^2s
T_{ch}, T_j	Channel / Junction temperature	(Note1)	-30~+150	$^{\circ}\text{C}$

Note1: The maximum junction temperature rating of the power chips integrated within the DIPFC is 150°C ($@T_c \leq 100^{\circ}\text{C}$); however, the average junction temperature should be limited to $T_{ch}, T_j \leq 125^{\circ}\text{C}$ ($@T_c \leq 100^{\circ}\text{C}$) to ensure safe operation of the DIPFC.

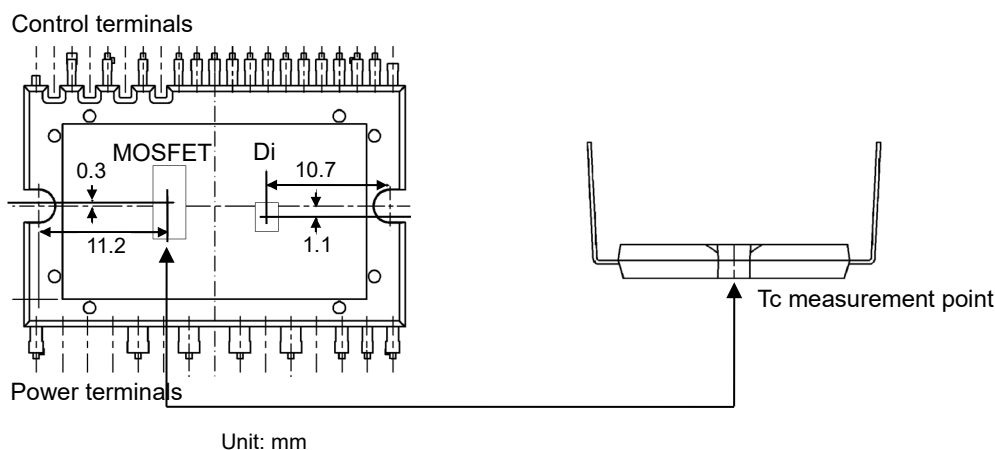
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Between V_D -GND terminals	24	V
V_{IN}	Input voltage	Between V_{IN1} , V_{IN2} -GND terminals	-0.5~ $V_D+0.5$	V
V_{FO}	Fault output supply voltage	Between F_O -GND terminals	-0.5~ $V_D+0.5$	V
I_{FO}	Fault output current	Sink current to F_O terminal	1	mA
V_{OC}	Current sensing input voltage	Between C_{IN1} , C_{IN2} -GND terminals	-0.5~ $V_D+0.5$	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(prot)}$	Self-protection supply voltage limit (Over current protection capability)	$V_D = 17\sim 19V$, Converter Part, $T_{ch} = 125^{\circ}\text{C}$ start, Less than 8 μs , Input inductance= 0.2mH, Non-repetitive,	400	V
T_c	Module case operation temperature	(Note 2)	-30~+100	$^{\circ}\text{C}$
T_{stg}	Storage temperature		-40~+125	$^{\circ}\text{C}$
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between all connected pins and heat sink plate	1500	V_{rms}

Note2: Measurement point of T_c is described in Fig.1.

Fig. 1 Measurement point of T_c 

PSF30L92A6-A**TRANSFER MOLDING TYPE
INSULATED TYPE****THERMAL RESISTANCE**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(ch-c)Q}$	Channel / Junction to case thermal resistance (Note 3)	MOSFET (per chip)	-	-	1.8	K/W
$R_{th(j-c)F}$		Di (per chip)	-	-	1.8	

Note 3: Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100 μ m~+200 μ m on the contacting surface of DIPFC and heat sink. The contacting thermal resistance between DIPFC case and heat sink $R_{th(c-f)}$ is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ is about 0.30K/W (per 1chip, grease thickness: 20 μ m, thermal conductivity: 1.0W/m $\cdot$ K).

ELECTRICAL CHARACTERISTICS ($T_{ch}=25^{\circ}\text{C}$ (MOSFET) / $T_j=25^{\circ}\text{C}$ (SBD), unless otherwise noted)**CONVERTER PART**

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{DS(on)}$	Drain-source on-state voltage	$V_D = 18\text{V}$, $V_{IN} = 5\text{V}$	$I_D = 30\text{A}$, $T_{ch}=25^{\circ}\text{C}$ $I_D = 30\text{A}$, $T_{ch}=125^{\circ}\text{C}$	-	1.40 1.35	2.30 1.65	V
V_F	Forward voltage	$I_F=30\text{A}$, $V_{IN}=0\text{V}$, $T_j=25^{\circ}\text{C}$		-	1.50	2.20	V
t_{on}	Switching time	$V_{CC}=370\text{V}$, $V_D=18\text{V}$, $I_D=30\text{A}$, $T_{ch}=125^{\circ}\text{C}$, Inductive load $V_{IN}=0\leftrightarrow 5\text{V}$		-	0.20	0.43	μs
t_{rr}				-	0.05	-	
$t_{C(on)}$				-	0.13	0.23	
t_{off}				-	0.28	0.47	
$t_{C(off)}$				-	0.08	0.20	
I_{rr}	Di recovery current	$V_{CC}=370\text{V}$, $V_D=18\text{V}$, $I_F=30\text{A}$, Inductive load, $V_{IN}=0\leftrightarrow 5\text{V}$, $T_j=25^{\circ}\text{C}$		-	2.0	-	A
I_{DSS}	Drain-source cut-off current	$V_{DS}=V_{DSS}$	$T_{ch}=25^{\circ}\text{C}$	-	-	1	mA
			$T_{ch}=125^{\circ}\text{C}$	-	-	10	
I_R	Reverse current	$V_R=V_{RRM}$	$T_j=25^{\circ}\text{C}$	-	-	1.5	mA
			$T_j=125^{\circ}\text{C}$	-	-	15	

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
I_{DL}	Circuit current	$V_D = 18\text{V}$	$V_{IN}=0\text{V}$	-	-	2.2	mA
			$V_{IN}=5\text{V}$	-	-	2.2	
I_{IN}	Input current	$V_D = 18\text{V}$, $V_{IN} = 5\text{V}$		-	0.30	0.45	mA
$V_{th(on)}$	ON threshold voltage	Between V_{IN} -GND terminals		-	2.10	2.60	V
$V_{th(off)}$	OFF threshold voltage			0.80	1.30	-	
$V_{th(hys)}$	ON/OFF threshold Hysteresis voltage			0.35	0.80	-	V
UV_{Dt}	Control supply under-voltage protection	Trip level		10.3	-	12.5	V
UV_{Dr}		Reset level		10.8	-	13.0	
V_{FOH}	Fault output voltage	$V_{OC}=0\text{V}$, F_O terminal pulled up to 5V by 10k Ω		4.9	-	-	V
V_{FOL}		$V_{OC}=1\text{V}$, $I_{FO}=1\text{mA}$		-	-	0.95	
$V_{OC(ref)}$	Over Current trip level	$V_D = 18\text{V}$	(Note 4)	0.43	0.48	0.53	V
t_{FO}	Fault output pulse width	$C_{FO}=22\text{nF}$	(Note 5)	1.6	2.4	-	ms

Note 4 : Over current protection works for MOSFET only. Please select the external shunt resistance such that the OC trip level is 30A or less per each phase.

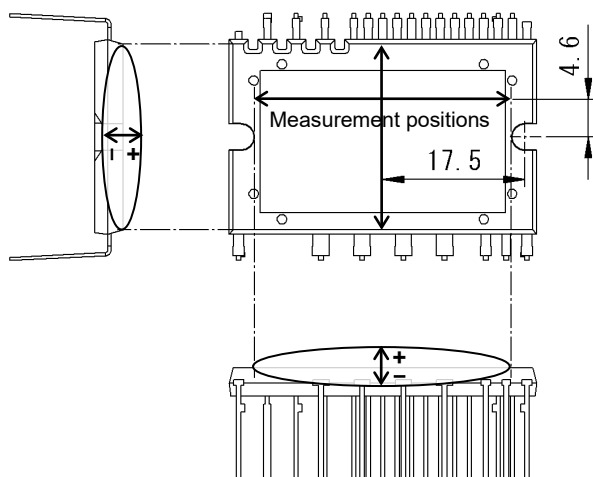
5 : Fault signal F_O outputs when OC or UV protection works, and F_O pulse width is different for each protection mode. In case of OC failure, F_O pulse width is a fixed width which is set by external capacitor C_{FO} (=min. 1.6ms @ $C_{FO}=22\text{nF}$). In case of UV failure, F_O outputs continuously until recovering from UV state. however it continues at minimum for the period which is set by external capacitor C_{FO} . The relationship of t_{FO} and C_{FO} is as following formula. $t_{FO} = C_{FO}/(9.1 \times 10^{-6})[\text{s}]$

PSF30L92A6-A**TRANSFER MOLDING TYPE
INSULATED TYPE****MECHANICAL CHARACTERISTICS AND RATINGS**

Parameter	Condition		Reference	Limits			Unit
				Min.	Typ.	Max.	
Mounting torque	Mounting screw: M3 (Note6)	Recommended: 0.69N·m	JEITA- ED-4701 402 Method II	0.59	-	0.78	N·m
Terminal strength pull	Control terminal: Weight 5N Power terminal: Weight 10N		JEITA- ED-4701 401 Method I	10	-	-	s
Terminal strength bending	Control terminal: Weight 2.5N Power terminal: Weight 5N Bending 90degree		JEITA- ED-4701 401 Method III	2	-	-	times
Weight			-	-	8.5	-	g
Heat radiation part flatness		(Note7)	-	-50	-	+100	μm

Note 6: Applying flat washer (ISO 7089~7094) is recommended.

7: Measurement position of heat radiation part flatness is as below.



Unit: mm

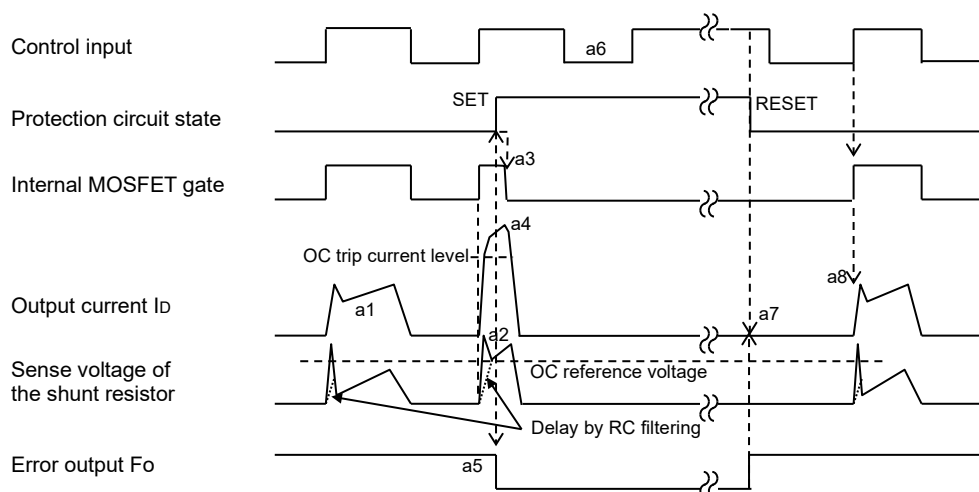
RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V_I	Input supply voltage	Between P_1 - N_1 , P_2 - N_2 terminals	85	-	276	V_{rms}
V_D	Control supply voltage	Between V_D -GND terminals	17	18	19	V
f_{PWM}	PWM input frequency	$T_c \leq 100^\circ\text{C}$, $T_{ch} \leq 125^\circ\text{C}$, $I_L \leq 20A_{rms}$	-	-	40	kHz
T_{ch} , T_j	Channel / Junction temperature		-30	-	125	$^\circ\text{C}$

Fig. 2 Timing Charts of DIPFC Protective Functions

[A] Over Current protection (with the external shunt resistor and RC filter)

- a1. Normal operation: MOSFET ON and outputs current.
- a2. Over current detection (OC trigger)
(It is necessary to set a time constant of RC filter so that MOSFET shuts down within 8.0 μ s.)
- a3. All N-side MOSFET's gates are hard interrupted.
- a4. All N-side MOSFETs turn OFF.
- a5. LVIC starts outputting fault signal (fault signal output time can be set by external capacitor C_{FO})
- a6. Input = "L": MOSFET OFF
- a7. Fo finishes output, but MOSFETs don't turn on until inputting next ON signal (L $\rightarrow$ H).
- (MOSFET of each phase can return to normal state by inputting ON signal to each phase.)
- a8. Normal operation: MOSFET ON and outputs current.

**[B] Under-Voltage Protection (UV_D)**

- b1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but MOSFET turns ON by next ON signal (L $\rightarrow$ H).
(MOSFET of each phase can return to normal state by inputting ON signal to each phase.)
- b2. Normal operation: MOSFET ON and outputs current.
- b3. V_D level drops to under voltage trip level. (UV_{Dt}).
- b4. All N-side MOSFETs turn OFF in spite of control input condition.
- b5. Fo outputs for the period set by external capacitor C_{FO} , but output is extended during V_D keeps below UV_{Dr} .
- b6. V_D level reaches UV_{Dr} .
- b7. Normal operation: MOSFET ON and outputs current.

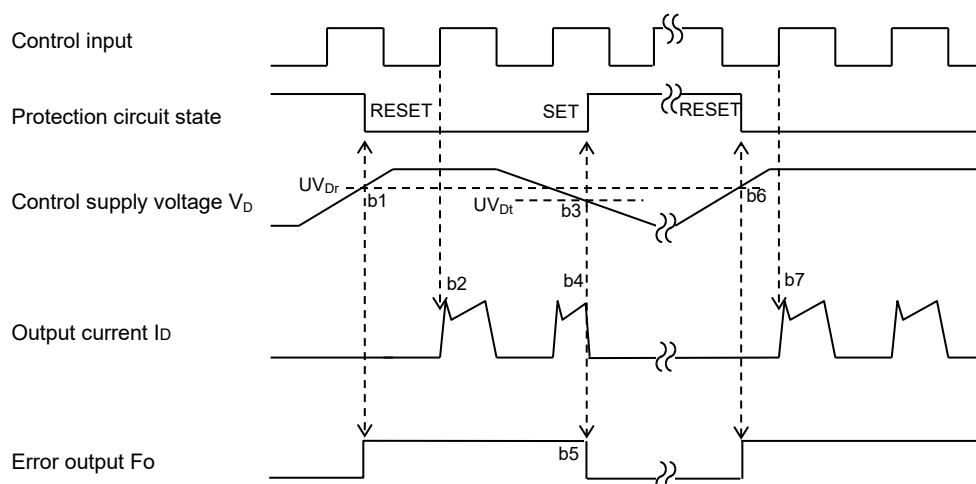
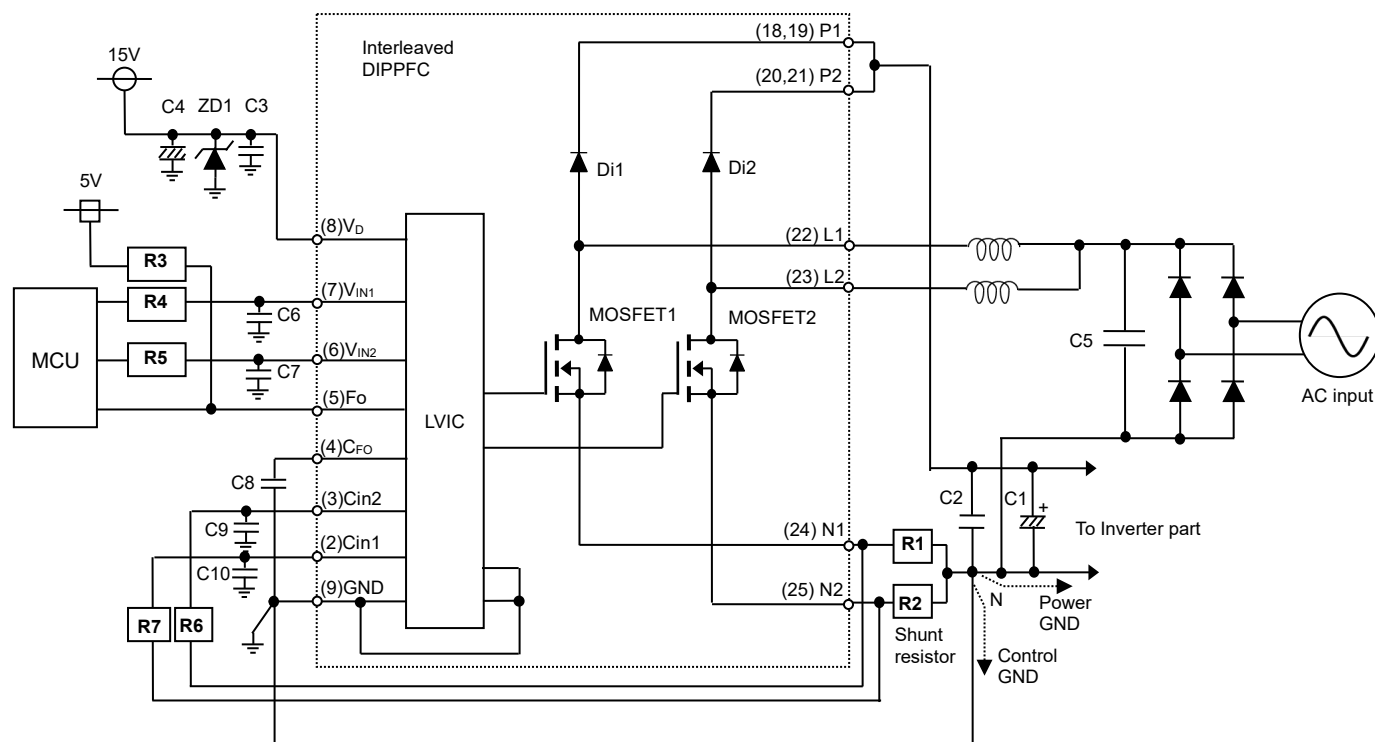


Fig.3 Example of Application Circuit

The notes on using Interleaved PFC

The following notes are minded about the wire connection on the printed circuit board of the interleaved PFC.

1. DIPFC integrates fast switching semiconductor chips, therefore it is easy to generate surge voltage between P-N. It is necessary to apply an electrolytic capacitor for adopting high frequency operation to the capacitor C1, and such a polypropylene film capacitor, which has good high frequency characteristics, to the capacitor C2. Those capacitors should be connected to nearby P-N terminal and it is necessary to make area made by the wirings of P-C2-N as small as possible.
2. Power GND and Control GND should not make common GND wiring and be connected only at the N point for prohibiting control GND potential fluctuation by discontinuous large current flow into power GND. And if control GND of DIPFC and MCU GND fluctuate respectively, it becomes impossible for the control signal to transmit each other normally. So both GND of DIPFC and MCU should be connected as nearby and steadily as possible.
3. The capacitors C3 and C4 for the control supply should be connected to nearby V_D-GND terminal. An electrolytic capacitor which has good temperature and frequency characteristics is recommended as C3 and a ceramic capacitor which has good temperature, frequency characteristics is recommended as C4 for noise reduction. (Also refer to fig.5)
4. It is recommended to connect ZD1 (the Zener voltage 24V and allowable loss 1W) to nearby the control supply terminal for the surge voltage absorption. (Also refer to fig.5)
5. NC terminal (from 10pin to 16pin) should leave no connection (floating state).
6. PWM input logic is High-active type. There is a 11kΩ (Min.) pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meets the turn-on and turn-off threshold voltage.
7. It is necessary to design the wiring inductance between control GND and N point to 40nH or less and the wiring inductance between N1 or N2 and N point to 10nH or less including stray inductance of shunt resistor. Also, the time constant R6C9 and R7C10 should be set so that OC current is shut down within 8μs. OC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is necessary.

1. The setting of RC coupling at each input (parts shown dotted) depends on the PWM control scheme and the wiring impedance of the printed circuit board.
2. The DIPFC input section integrates a 11 k Ω (min) pull-down resistor. Therefore, when using an external filtering resistor, pay attention to the turn-on threshold voltage.

Equivalent to the inductance of a copper pattern with length=17mm, width=3mm

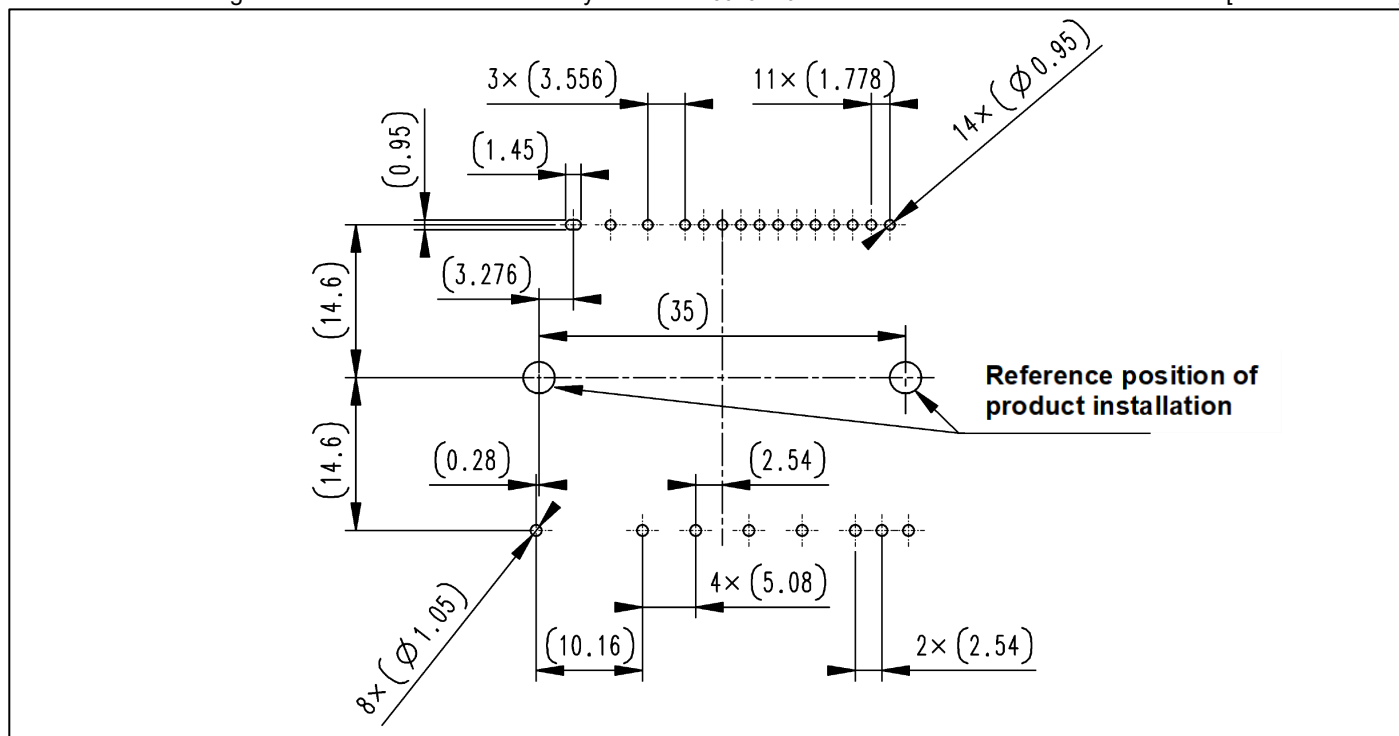
Equivalent to the inductance of a copper pattern with length=40mm, width=1mm

PSF30L92A6-ATRANSFER MOLDING TYPE
INSULATED TYPE

Fig. 6 (Reference Figure) PCB Through-hole Pattern

Recommended through-hole locations and diameter layout for PSF30L92A6-A

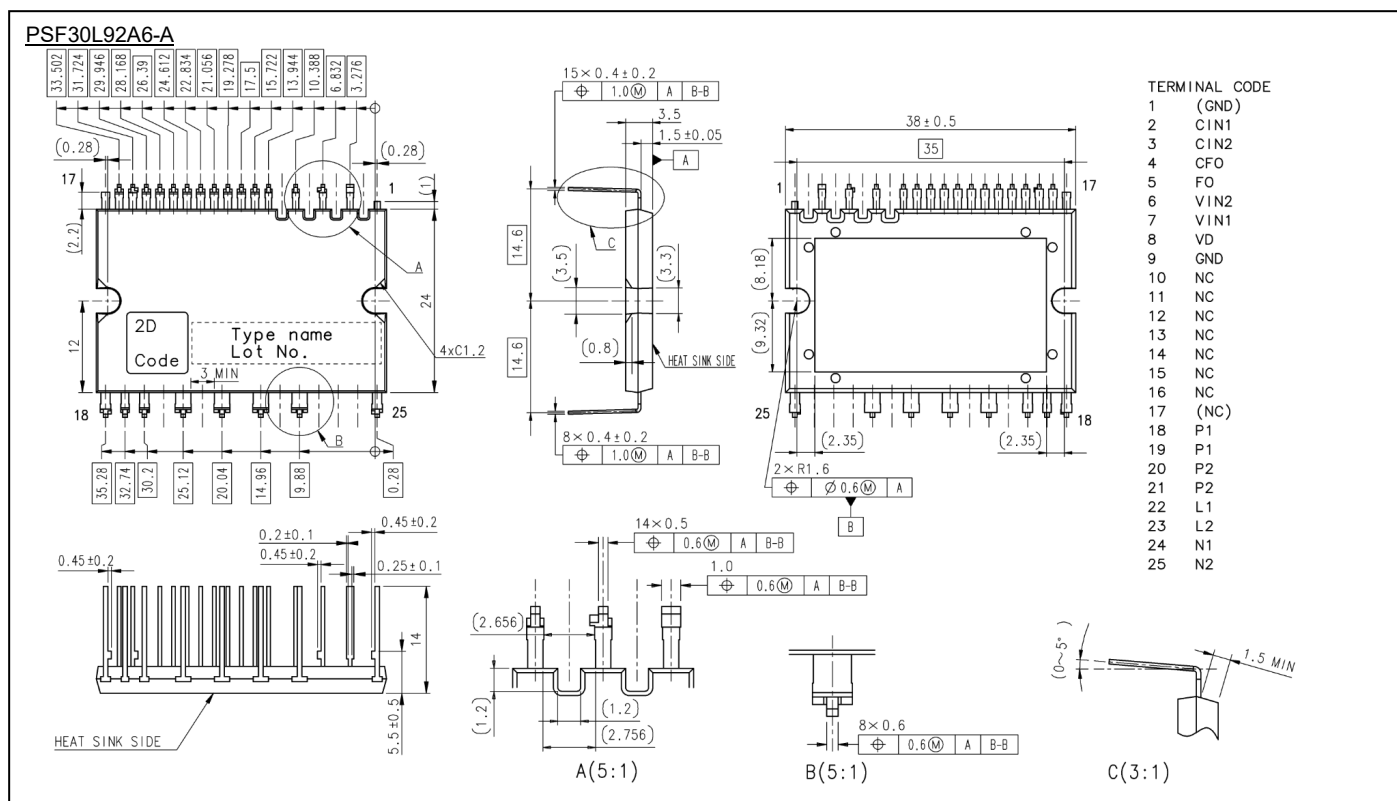
[Dimension: mm]



PSF30L92A6-A**TRANSFER MOLDING TYPE
INSULATED TYPE**

Fig. 7 Package Outlines

[Dimension: mm]



1) 9 & 16 pins (V_{NC}) are connected inside DIPIM, please connect either one to the control power supply GND outside and leave another one open.

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