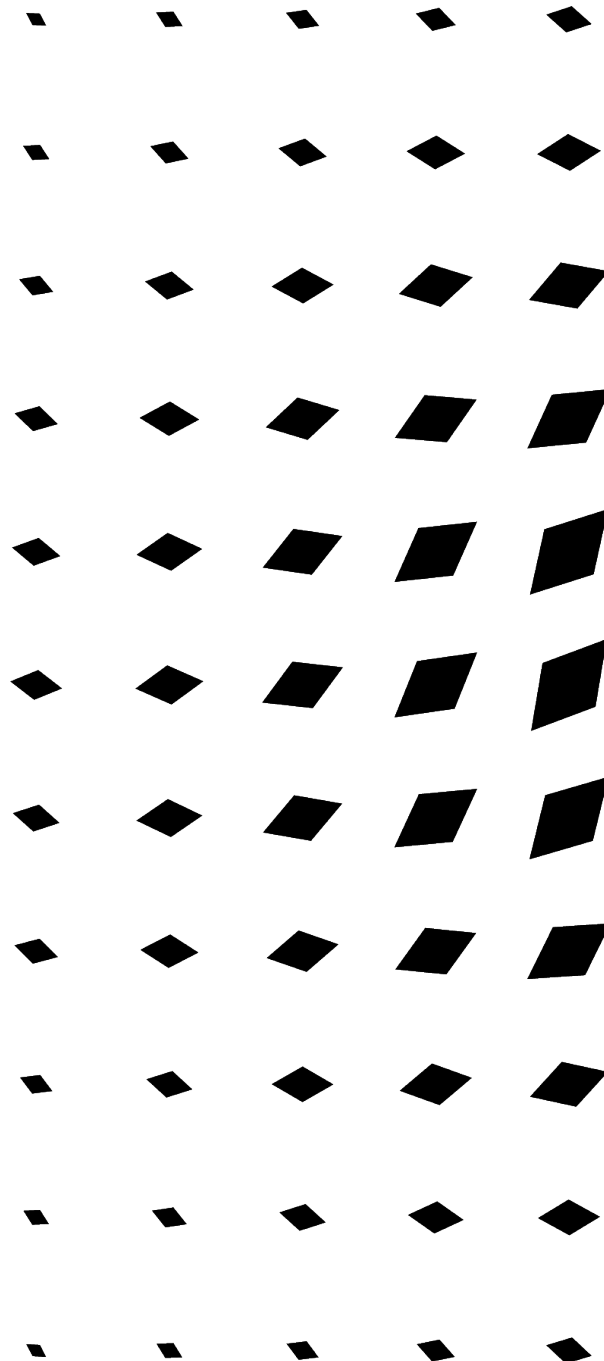


Key technical advantage of trench gate SiC MOSFET chip



Key technical advantage of trench gate SiC MOSFET chip

- Trench-Gate SiC MOSFETs incorporating our proprietary technologies achieve industry-leading low on-resistance and low switching losses.

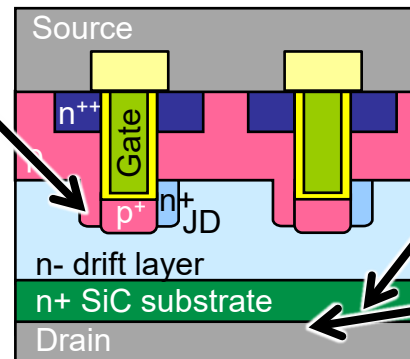
- Furthermore, with respect to gate reliability—a key challenge of trench-gate structures—they achieve a gate oxide lifetime comparable to that of our planar-gate structure devices.

(1) Proprietary high-concentration JFET doping technology enables a high cell density structure, resulting in exceptionally low ON-resistance

(2) The unique Side P-Well (SPW) structure on the trench sidewall suppresses feedback capacitance (C_{gd}), enabling low switching-loss operation.

(3) The Bottom P-Well (BPW) structure mitigates the high electric field at the trench bottom, enhancing gate oxide lifetime and ensuring high gate reliability.

(1) SPW*1 → *Low switching loss*



(2) JFET doping → *Low on-state resistance*

(3) BPW*2 → *High reliable Gate characteristics*

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