MITSUBISHI ELECTRIC

# SiC Lecture Series

## 9. SiC Process Technology (1) Ion Implantation

# SiC Process Technology (1) Ion Implantation

SiC has a very low diffusion coefficient for impurity atoms, making it impossible to form device structures (such as pn junctions) using thermal diffusion processes for doping atoms like donors and acceptors. Therefore, ion implantation doping technology is used in the fabrication of SiC devices. For ion implantation into SiC, donor elements such as nitrogen (N) and phosphorus (P) are commonly used for n-type regions, as they easily achieve low resistivity, while aluminum (Al) is typically used as an acceptor element for p-type regions. The source material for Al ion implantation is usually solid, and a great deal of expertise is required to stably perform high-concentration Al implantation. SiC can achieve high-concentration crystals for both n-type and p-type through ion implantation, which is a significant advantage in device fabrication.

The acceleration voltage for ion implantation into SiC is generally on the order of several hundred kV, and the corresponding depth of the ion implantation region is on the order of several hundred nm, which is relatively shallow. In SiC, the depth distribution of the doping element concentration after implantation is almost retained in its original form even after high-temperature processes. Considering these factors, the ion implantation process is designed to achieve the required device characteristics. Additionally, special considerations are necessary when performing high-concentration ion implantation. If the implantation dose is large, the SiC crystal may suffer damage to the extent that it cannot maintain its original crystal structure, which can cause issues such as accelerated oxidation or excessive sublimation in subsequent processes. When high-concentration Al implantation is required, such as in the formation of electrically low-resistance p-type contact regions, raising the wafer temperature during ion implantation can significantly suppress the polycrystallization or amorphization of the SiC crystal due to implantation damage. It is also known that the suppression of damage to the crystal caused by high-concentration ion implantation can be effectively achieved by using hot implantation at relatively low temperatures.

Immediately after ion implantation, many micro-defects are formed in the crystal due to the high-energy implanted ions, and the implanted atoms do not occupy the appropriate lattice positions, resulting in high electrical resistance in the implanted region. By performing high-temperature activation annealing (usually above 1700°C) in an inert gas atmosphere on the SiC wafer that has undergone ion implantation, low-resistance p-type or n-type regions can be formed. In the device fabrication process using SiC wafers, activation annealing requires the highest temperature, so ion implantation and activation annealing are performed at an early stage of the wafer process.

Since activation annealing of SiC is performed at high temperatures, the surface flatness deteriorates if no measures are taken. Because the device structure is formed in the shallow region of the SiC epitaxial substrate surface, it is necessary to perform activation annealing without compromising the surface flatness. Films containing carbon are generally used as a surface protection film to maintain the flatness of the SiC surface during activation annealing. Various processes for forming carbon protection films have been reported, such as applying resin to the surface and solidifying it at high temperatures, or depositing carbon films by sputtering. However,

Mitsubishi Electric has developed its own CVD method to form carbon protection films that are uniform and of high purity, suitable for high-temperature annealing.

As a reference, here are several examples of the surface morphology of SiC after ion implantation and activation annealing.

Figure 1 shows the surface morphology of SiC after high-concentration Al implantation and activation annealing. Figures 1(A) and 1(B) represent the cases where Al implantation was performed at SiC substrate temperatures of 150°C and 200°C, respectively. At 150°C, the surface becomes polycrystalline, whereas at 200°C, the SiC crystal is preserved, and steps are formed. This indicates that implanting at 200°C allows the crystal structure to partially recover during the ion implantation process.

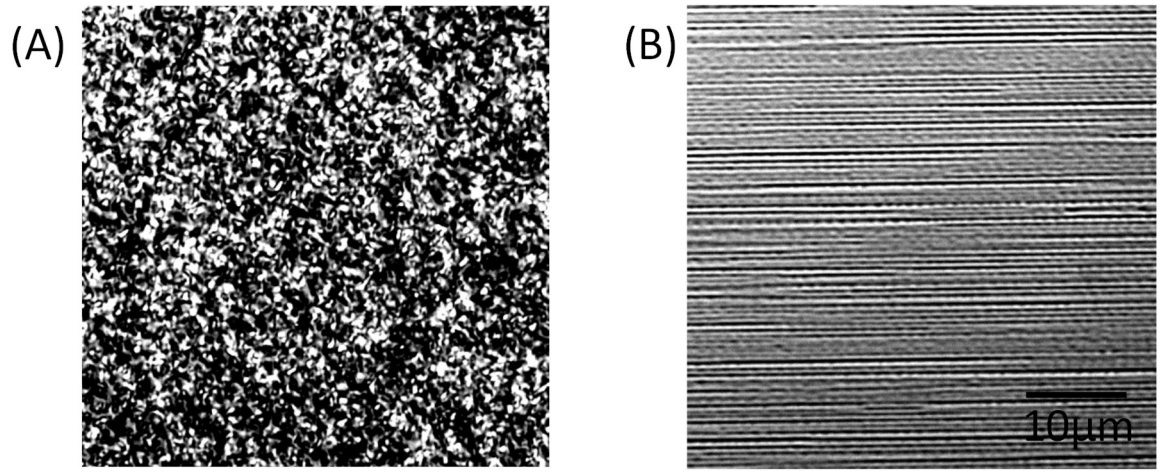


Figure 1 Photographs of the SiC surface after high-concentration Al ion implantation and activation annealing: (A) implantation temperature of 150°C and (B) implantation temperature of 200°C.

Figure 2 shows AFM (Atomic Force Microscope) images of the SiC surface after activation annealing, with and without a carbon protection film formed by the CVD method. Without the protection film, giant steps with heights of 20-50 nm are formed on the SiC surface, resulting in degraded flatness. Surface irregularities can affect device characteristics and, for example, can cause fatal current leakage in the gate oxide film of MOSFETs. On the other hand, when activation annealing is performed with a deposited protection film, a flat surface with an RMS (Root Mean Square) value of 0.3 nm is obtained. The CVD protection film has almost no macro defects such as pinholes, resulting in an extremely good surface. Additionally, the carbon protection film can be easily removed by thermal oxidation or oxygen plasma irradiation.

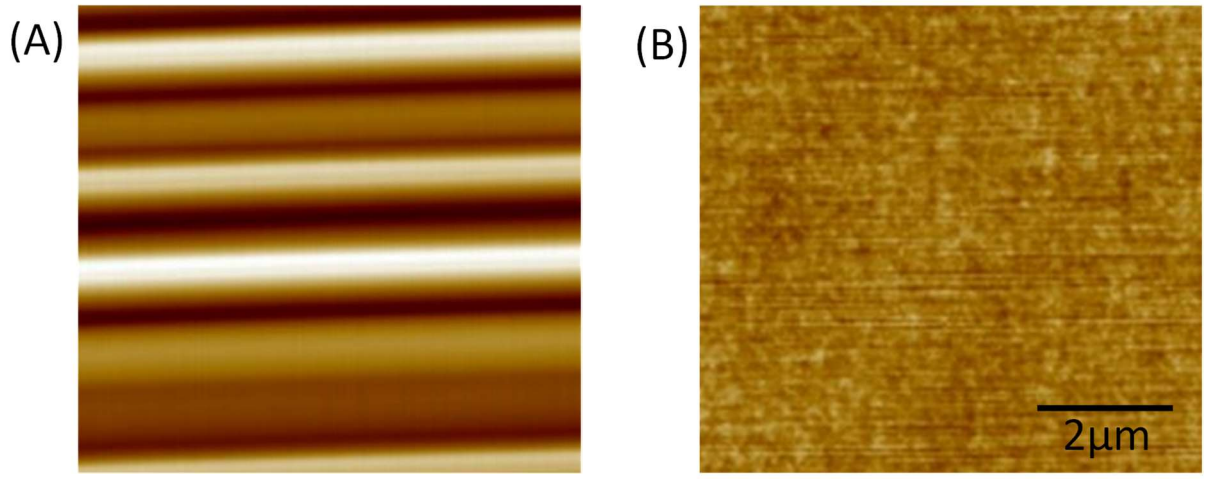


Figure 2 AFM images of the SiC surface after activation annealing:
(A) without carbon protection film and (B) with carbon protection film.

Since crystals have atoms arranged in a regular pattern, ion implantation along the crystal axis allows ions to be implanted deeply (channeling implantation). Utilizing this phenomenon, attempts are being made to form pillar structures of pn junctions deep within the material and to fabricate SJ MOSFETs (Super Junction MOSFETs) using SiC. SJ MOSFETs have already been commercialized in silicon, demonstrating a significant reduction in on-resistance, but they are still in the research and development stage for SiC. Channeling implantation requires the ion beam direction to be precisely aligned with the crystal axis, among other technical challenges. However, if SJ MOSFETs using SiC can be realized, they are expected to significantly improve performance, especially in high-voltage MOSFETs, and thus development progress is highly anticipated.

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