MITSUBISHI ELECTRIC

SiC Lecture Series

10. SiC Process Technology (2) Gate insulation film

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SiC can form high-quality SiO_2 insulating films on the wafer surface through a thermal oxidation process similar to that of Si. This is a significant advantage in the fabrication of SiC devices. In planar-type SiC MOSFETs, this thermally oxidized SiO_2 is typically used as the gate insulating film and has been commercialized. However, there are several differences in the thermal oxidation of SiC compared to Si, and these differences must be taken into account when applying thermal oxidation to the SiC device process.

First, the thermal oxidation rate of SiC is slower compared to Si. As a result, the process takes a long time and requires high temperatures. Consideration of the load on the equipment due to the high-temperature process is essential in the thermal oxidation of SiC. Additionally, the thermal oxidation rate of SiC exhibits significant anisotropy depending on the crystal plane. The oxidation rate is typically slowest on the (0001) Si face, where devices are usually fabricated, and fastest on the (000-1) C face. For example, when fabricating trench-type SiC MOSFETs, measures such as using CVD oxide films are necessary because the gate oxide film is formed on planes orthogonal to the Si and C faces. Regarding the oxidation atmosphere, both steam and dry oxygen atmospheres are used. When comparing the two, the oxidation rate is higher in a steam atmosphere, similar to Si. Since the atmosphere gas affects the formation of electron and hole traps at the SiC/SiO_2 interface, careful selection of the atmosphere gas is required. The carbon in SiC detaches from SiO_2 in the form of CO or CO_2 during thermal oxidation. It has been found that the SiO_2 formed by the thermal oxidation of SiC contains very little residual carbon, except near the SiC/SiO_2 interface. The dielectric breakdown field strength of thermally oxidized SiO_2 formed under appropriate conditions for SiC is comparable to or better than that of SiO_2 formed by the thermal oxidation of Si, indicating no fundamental issues with electrical insulation performance.

A significant difference between the thermal oxide films of SiC and Si is that many electron and hole traps are formed at the SiC/SiO_2 interface in SiC. These traps at the SiC/SiO_2 interface increase the resistance when the MOSFET is on and cause changes in characteristics over time, negatively impacting device performance. Therefore, many attempts have been made to reduce the density of interface traps. Among these, annealing the SiC/SiO_2 interface in a nitriding gas atmosphere such as NO or N_2O is a widely used method and can significantly improve the effective electron mobility at the SiC/SiO_2 interface of MOSFETs. The temperature required for this nitridation annealing process is similar to or higher than that of the thermal oxidation process, necessitating annealing process equipment capable of handling high temperatures. The origin of the electron and hole traps is thought to involve complex defects associated with residual carbon, but this is still under debate. Additionally, research and development to further reduce trap density are ongoing at many institutions.

Regarding the impact of SiC/SiO_2 interface traps on MOSFETs, Figure 1 shows the results of a gate voltage stress test (HTGB test) conducted on planar-type SiC MOSFETs manufactured by Mitsubishi Electric. The test temperature was set at 150°C, and the changes in threshold voltage when 20V or -20V was continuously applied between the gate and source are shown. For both MOSFETs, the variation in threshold voltage was small regardless of the positive or negative gate voltage, indicating very good stability. Additionally, Table 1 summarizes the changes in on-resistance and threshold voltage after 1000 hours of gate voltage application. Similar to the threshold voltage, the variation in on-resistance was also small and not at a problematic level.

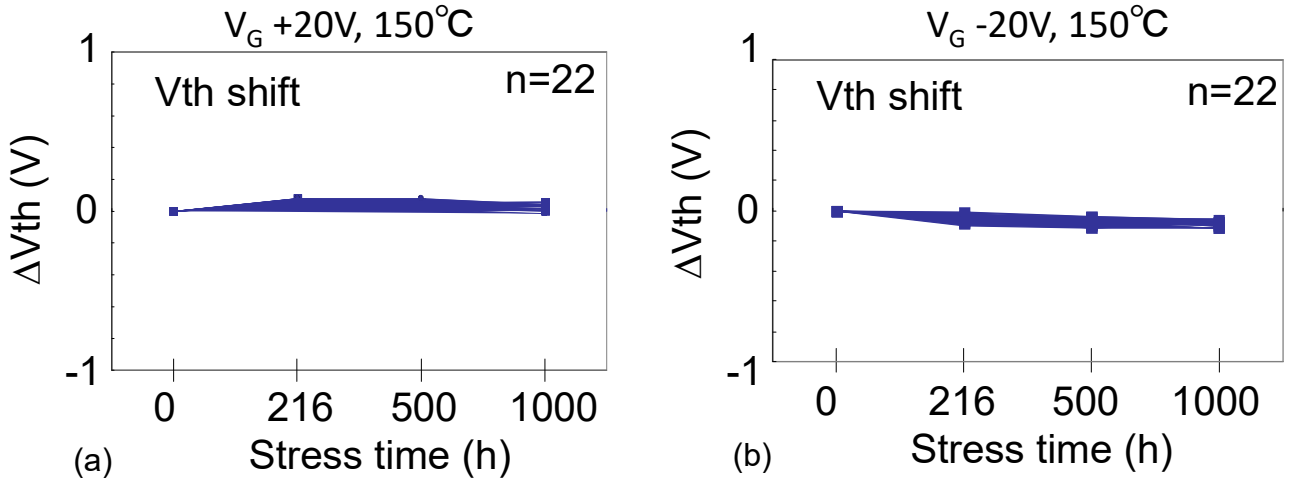

Figure 1 Time-dependent changes in the threshold voltage during a high-temperature (150°C) gate bias test (HTGB test) on SiC MOSFETs: (a) with gate voltage of 20V (b) with gate voltage of -20V.

Table 1 Changes in on-resistance and threshold voltage after HTGB test on SiC MOSFETs

Gate stress condition	Electrical characteristics	Deviation
V_G +20V 150℃ 1000h 22pcs	Ron	< 3%
	Vth	< 0.1V
V_G -20V 150℃ 1000h 22pcs	Ron	< 4%
	Vth	< 0.06V

In recent years, the time-dependent shift in electrical characteristics such as threshold voltage when high-frequency AC voltage is applied to the gate of SiC MOSFETs has garnered attention. This phenomenon involves the capture and release of charges by traps present at the SiC/SiO_2 interface and is different from the hysteresis often observed in voltage sweeps, where characteristics gradually drift over time. If the drift amount is significant, it could pose practical issues, leading to concerns about long-term reliability from the application side. Figure 2 shows the time-dependent changes in the threshold voltage when high-frequency AC bias is applied to the gate of SiC MOSFETs. Mitsubishi Electric's MOSFETs exhibit a small drift in threshold voltage, indicating good stability, and show a significant difference when compared to products from another company (Company A).

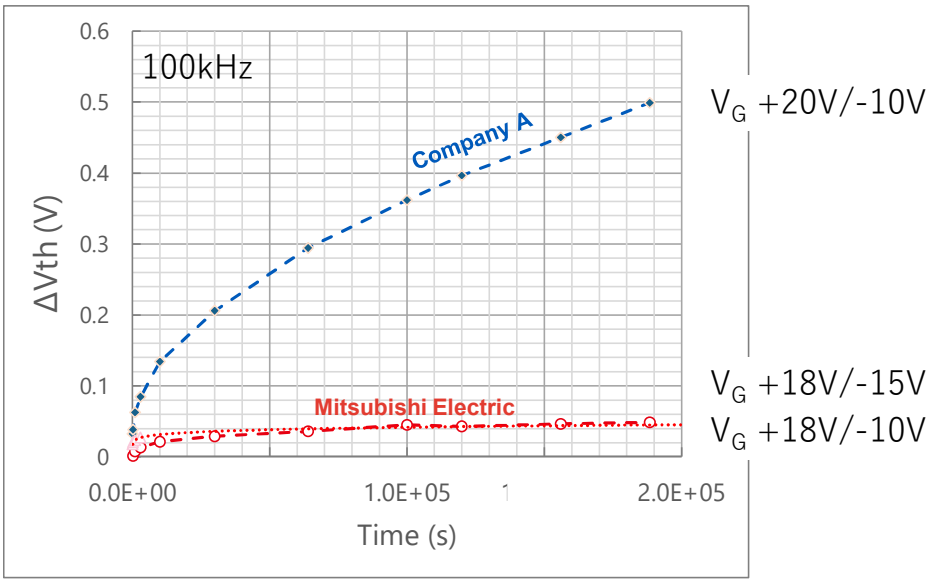

Figure 2 Changes in the threshold voltage
when high-frequency AC stress is applied to the gate of SiC MOSFETs

The unstable behavior of electrical characteristics when a bias voltage is applied to the gate of SiC MOSFETs has been reported in various studies, leading to a somewhat chaotic situation and causing concerns. The stability of characteristics involving the MOSFET gate strongly depends on the fabrication method of the gate insulating film, device structure, and driving conditions. Additionally, reducing on-resistance and achieving stable characteristics do not necessarily go hand in hand. To obtain SiC MOSFETs with low resistance and stable characteristics, it is essential to optimize processes and structures based on extensive experience and data. Mitsubishi Electric's SiC MOSFET gate characteristics have been evaluated in various application systems, demonstrating excellent stability, which is one of its significant advantages.

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